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RFSoC on MTCA

MTCA Workshop 2023

December 2023

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What is a RFSoC?

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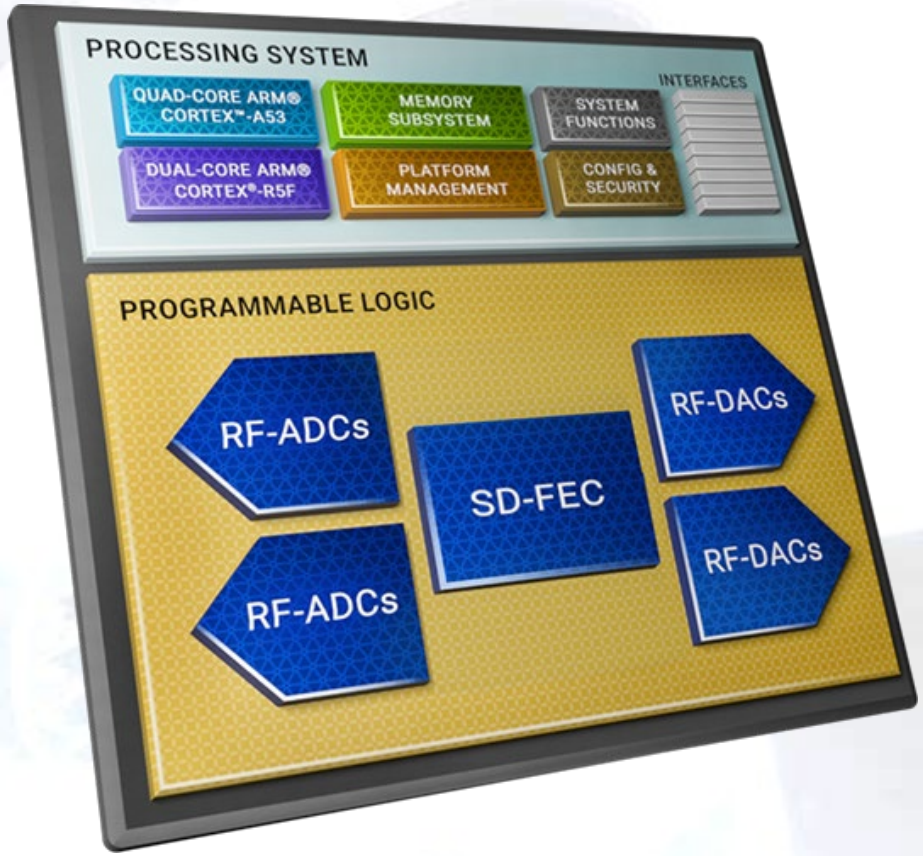
What is RFSoC?

- **R**adio **F**requency **S**ystem **o**n a **C**hip
- Combination of analog I/Os and a FPGA on one chip
- Perfect for RF signal generation



https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html

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Advantages

- All in one chip
- Monolithic design of the FPGA and the ADCs/DACs
  - No need for additional converter chips, e.g. ADC
  - No power hungry external JESD204 interface needed
  - Low latency

Created by parkjisun
from Noun Project

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Advantages

- 6x ARM processors on board
  - Quadcore Arm A53
  - Dualcore Arm R5F
  - Wide range of computing possibilities

ARM®

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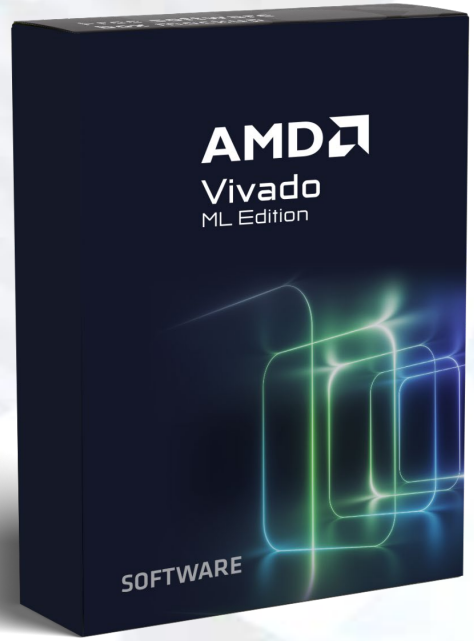
Advantages

- Good software programming
  - Working only on the FPGA, no other drivers for ADC and DAC required
  - No need for an additional device driver for external analog chips
  - Easy configuration with AMD Vivado



https://www.xilinx.com/products/design-tools/vivado.html#advantages

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Applications

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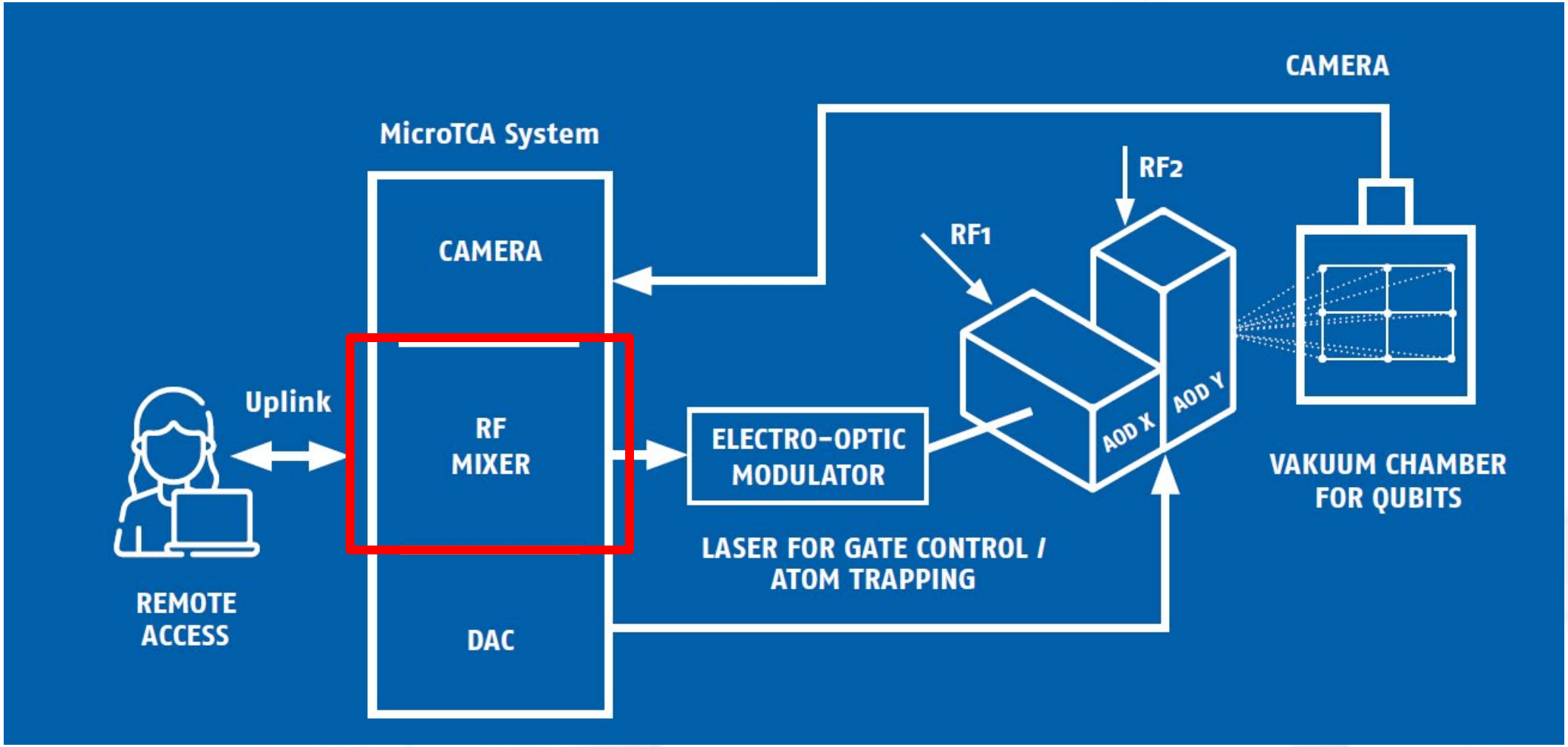
MTCA for Quantumcomputing



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Quantumcomputing

- RFSoC‘s used for signal generation and analog readout
- High bandwidth and frequency accuracy are required

Photo by Timothy Paule

Source:
Presentation on MTCA Workshop 2022 from Atom Computing / Jan Marjanovic: Modular and scalable control systems for atomic array quantum computers

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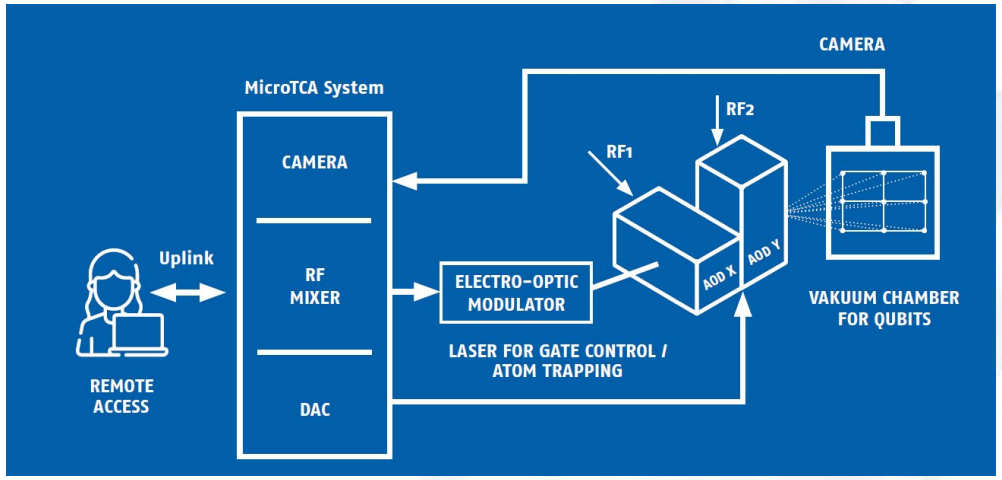
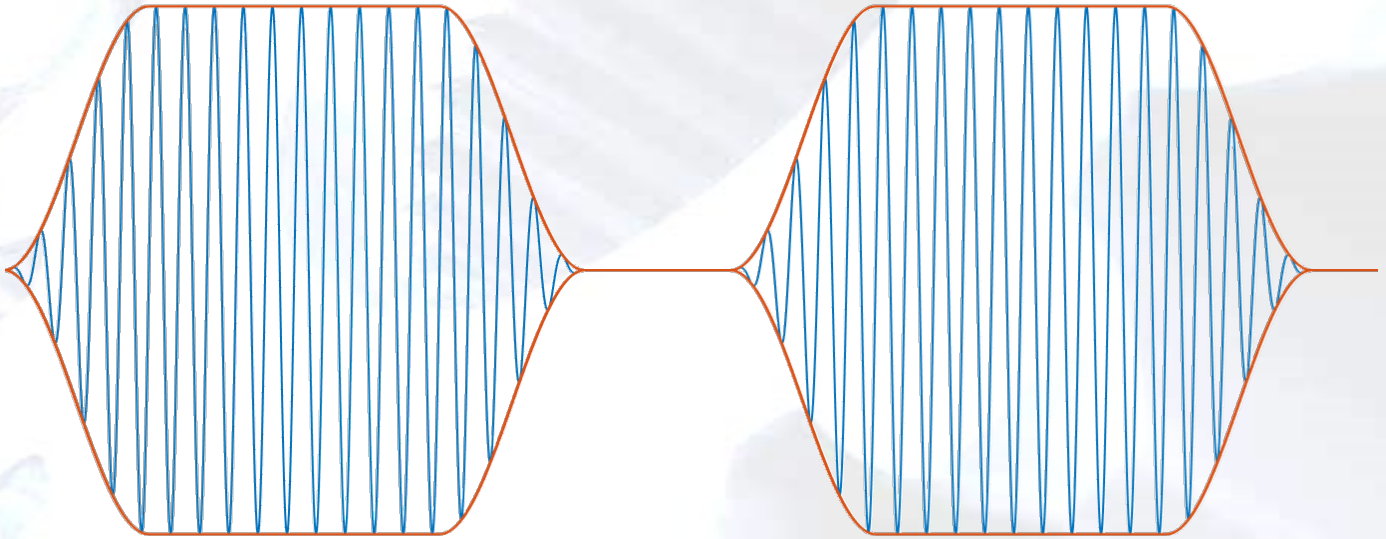
HF Control

- Controlling systems with RF signals like AODs
- High frequency signals can enveloped in pulses
- Several envelope functional edges are possible, e.g. $f(t)=A*\sin^2(t)$





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Hyperloop

- Controlling trains in high vacuum pipes
- High reliable

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SDR /Communication

- Wireless communication
- Development 5G/6G mobile communication systems
- Joined communication and sensing
  - Parallel radar and communication
- Waveforming
- Cellfree massive MiMo
  - High data bandwith

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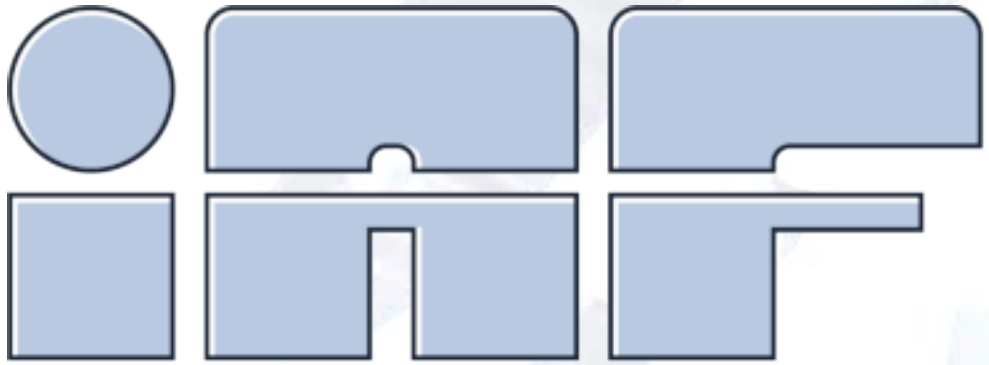
Who is our Partner IAF?



Future Radio Technology

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IAF

Future Radio Technology

IAF GmbH:	System solutions for digital data transmission and communication systems
Headquarters:	Braunschweig
Founded:	1992
Competence:	Eight employees in research, development and production
Focus:	Design and development of hardware and software digital data transmission and communication systems. FPGA hardware design and programming

Cooperation of pBC and IAF

Future Radio Technology

Development, VHDL programming and design

Sales, product management and integration

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The Journey

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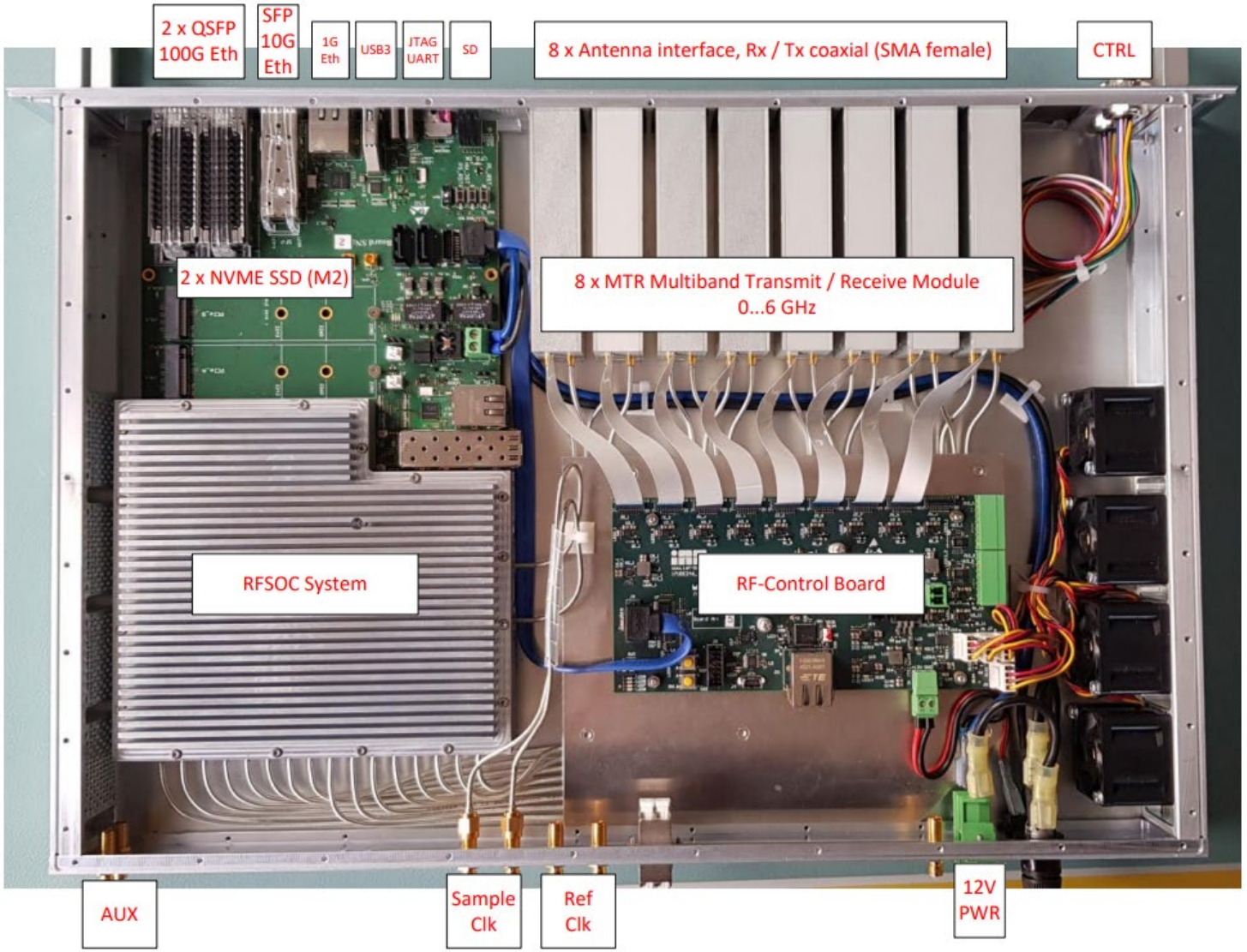
Existing System from IAF



Future Radio Technology

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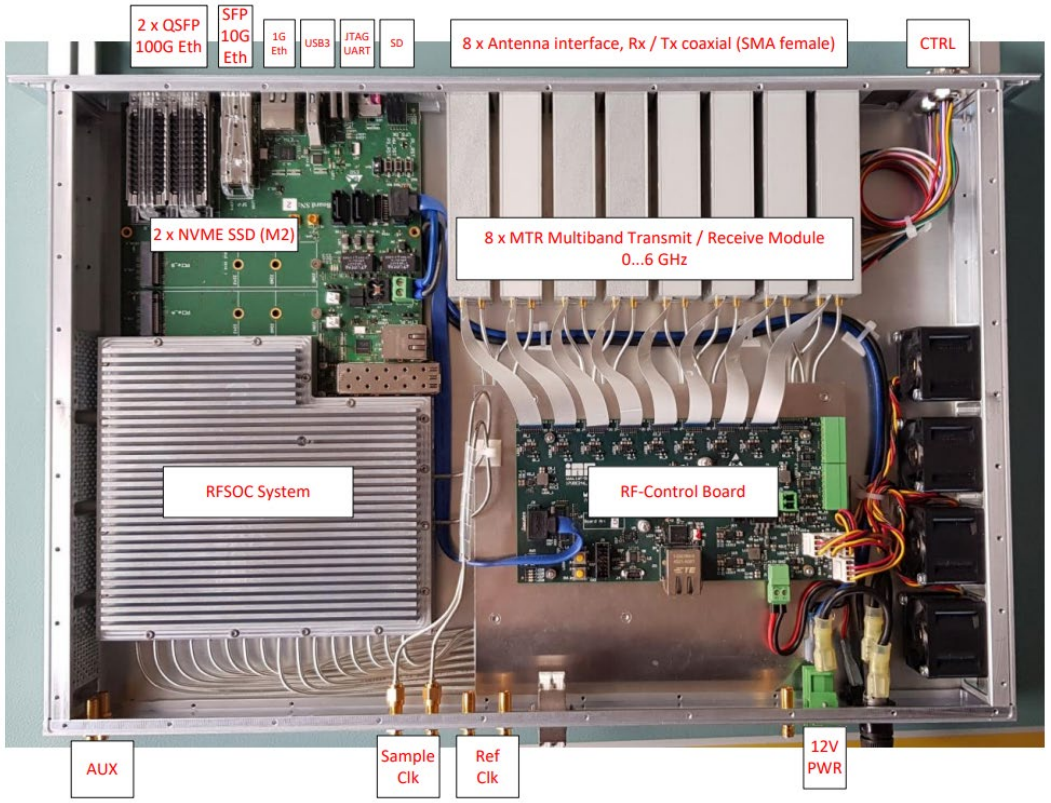
Details

Future Radio Technology

- 19“ / 1 U chassis
- HF- shielded housing
- Integrated active fans
- Interfaces:
  - RF in/out
  - Sampling clock in/out
  - Reference clock in/out
  - Trigger, synchronization
  - 2 x 100GbE
  - SFP/10GbE, 1GbE, USB, JTAG, SD



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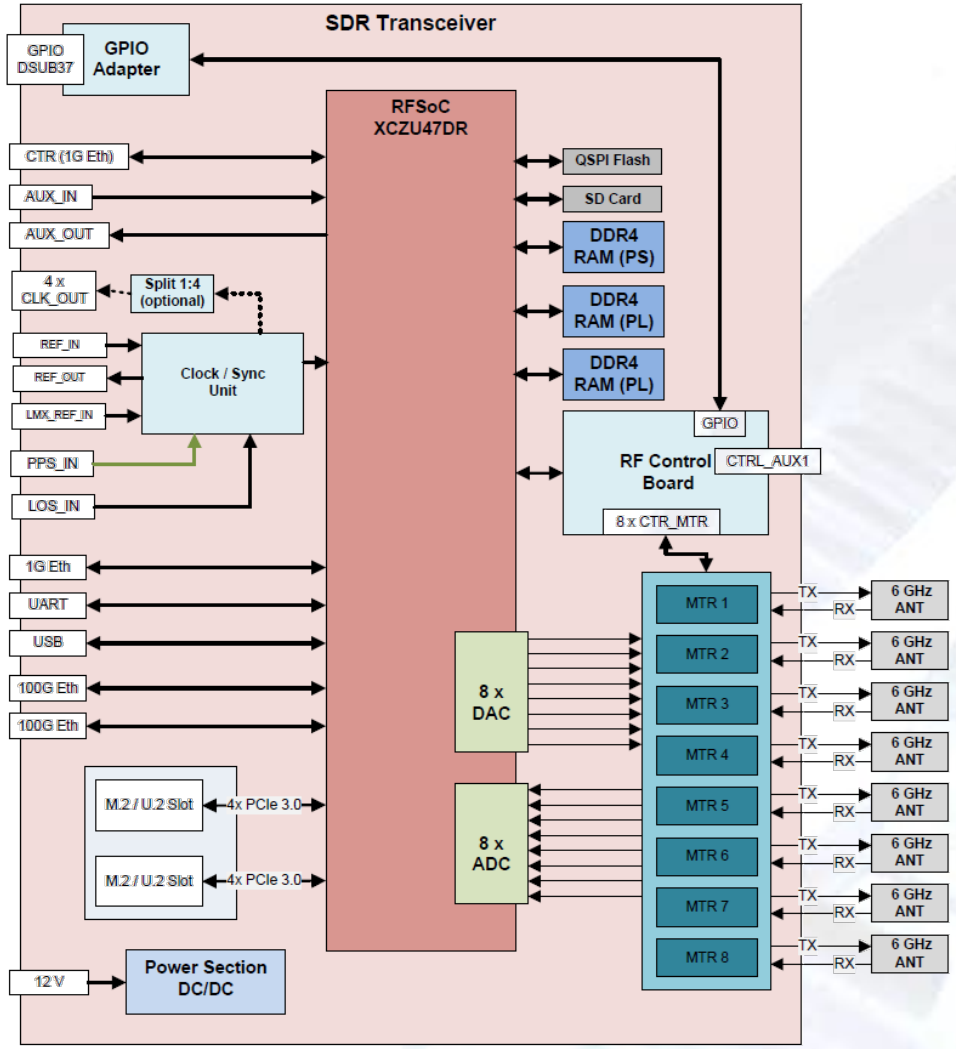
Facts



- **5 Gsps ADC**
- **10 Gsps DAC**
- **14 bit resolution**

- Based on the Xilinx RFSoC Gen. 3 –
- 8 antennas per device
- Integrated clock generation
- Integrated NVME SSD for offline data storage
- Integrated RF frontend up to 6 GHz
- Connection of external RF frontends possible
- Scalable number of antennas n x 8

- Engineered by IAF Braunschweig

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RFSoC with Custom Extentions

- 8x **5 Gsps** ADC
- 8x **9,85 Gsps** DAC
- 930k logic cells
- 4200 DSP slices

Table 1: **RF Data Converter Subsystem Features**

		ZU21DR	ZU25DR ZU27DR ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR ZU48DR	ZU49DR
		Gen 1			Gen 2	Gen 3				
12-bit RF-ADC w/ DDC	# of ADCs	0	8	16	16	–	–	–	–	–
	Max Rate (GSPS)	0	4.096	2.058	2.220	–	–	–	–	–
14-bit RF-ADC w/ DDC	# of ADCs	–	–	–	–	8 2	4	8 4	8	16
	Max Rate (GSPS)	–	–	–	–	2.5 5.0	5.0	2.5 5.0	5.0	2.5
14-bit RF-DAC w/ DUC	# of DACs	0	8	16	16	8	4	12	8	16
	Max Rate (GSPS)	0	6.554	6.554	6.554	9.85(2)	9.85(2)	9.85(2)	9.85(2)	9.85(2)
Number of DDCs per RF-ADC(1)		0	1	1	1	1	2	1	1	1
RF Input Freq. Max (GHz)		4			5	6				
Decimation/ Interpolation		1x, 2x, 4x, 8x			1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x				

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From a 1U Crate to MTCA

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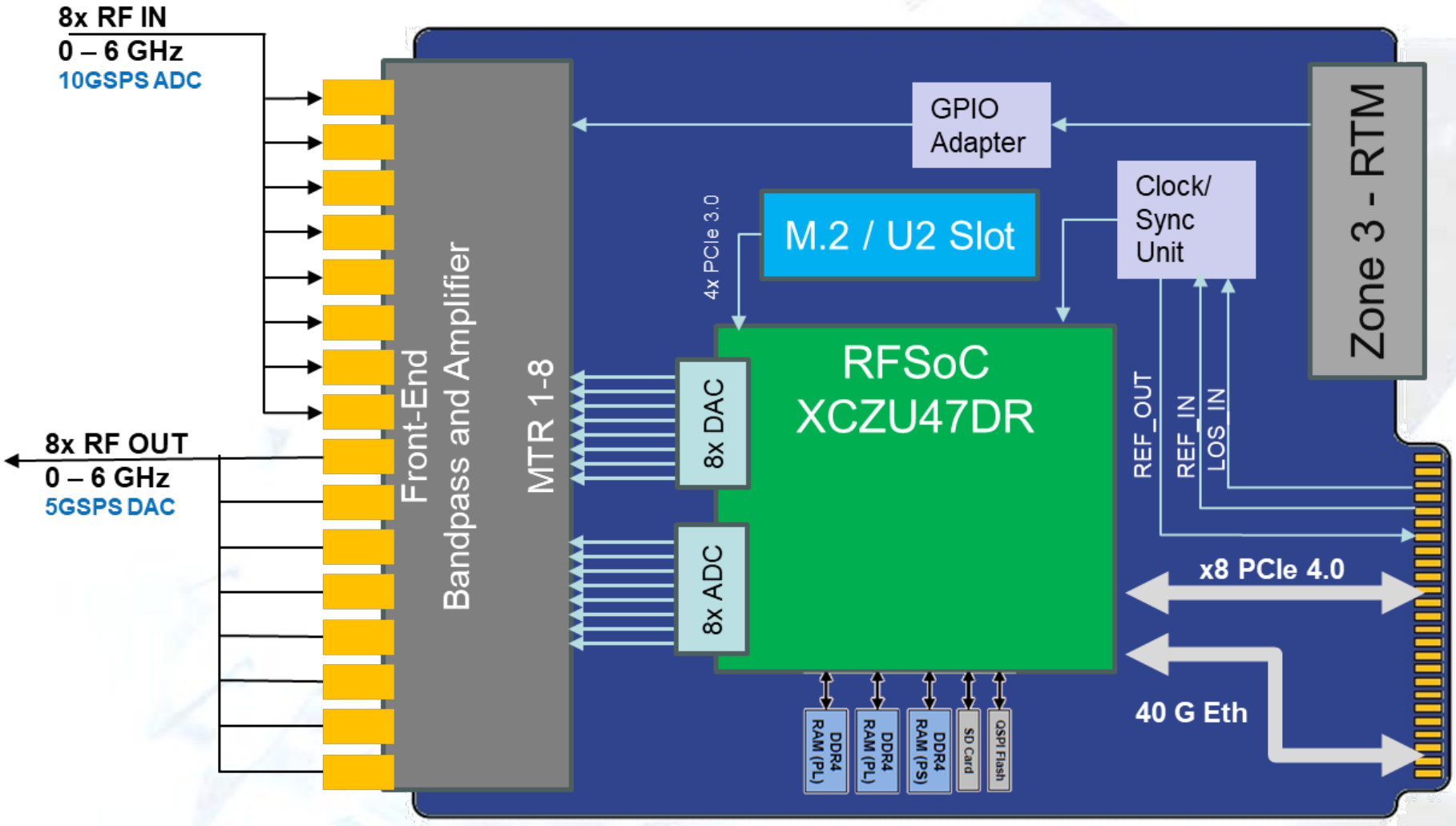
MTCA – Variant 1



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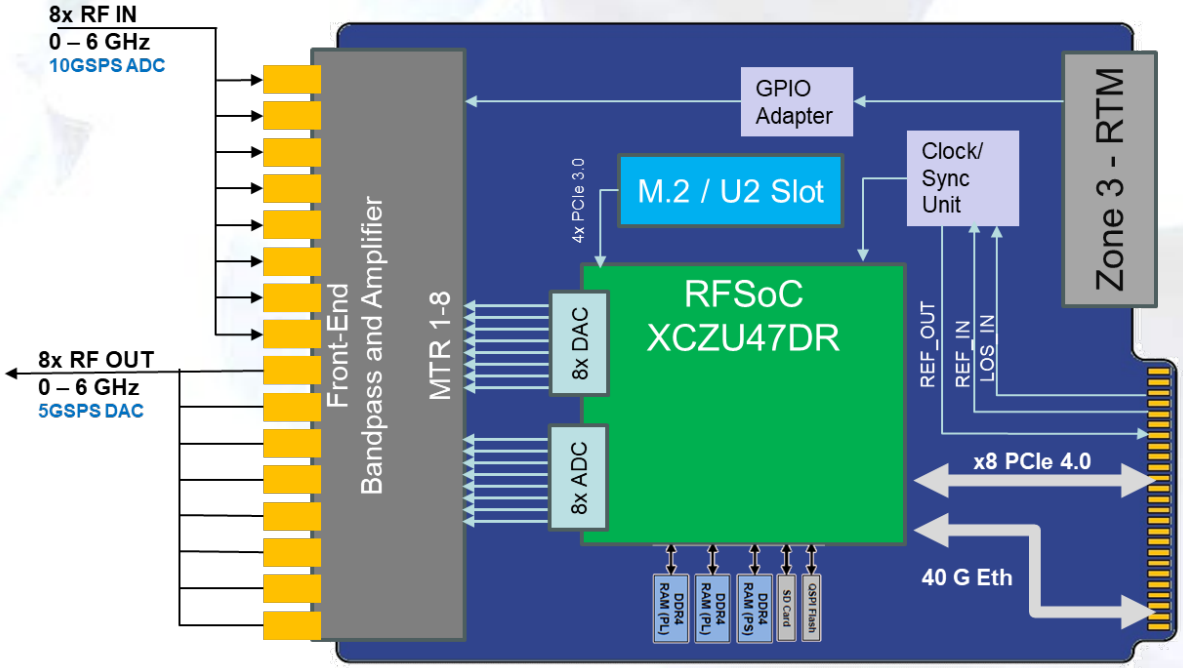
MTCA – Variant 1

- Base RFSoC AMC
- Frontends on the AMC
- Mid-size double AMC
- Flexible design
- Commercial of-the-shelf
- No FMC, all on AMC
- 40 GbE
- PCIe Gen4



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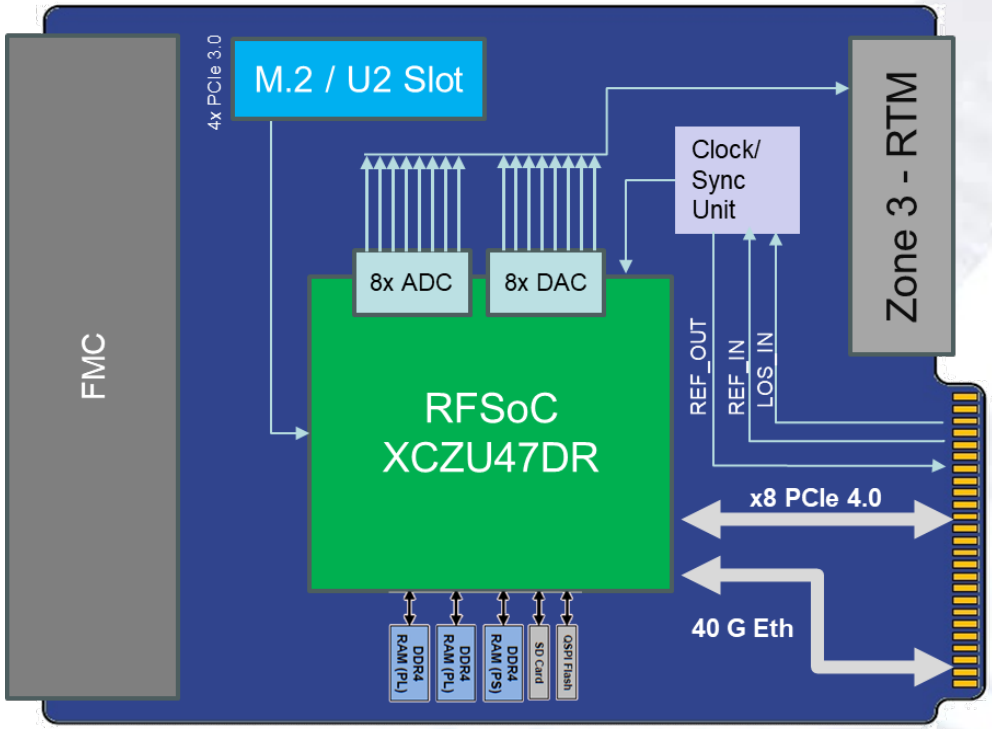
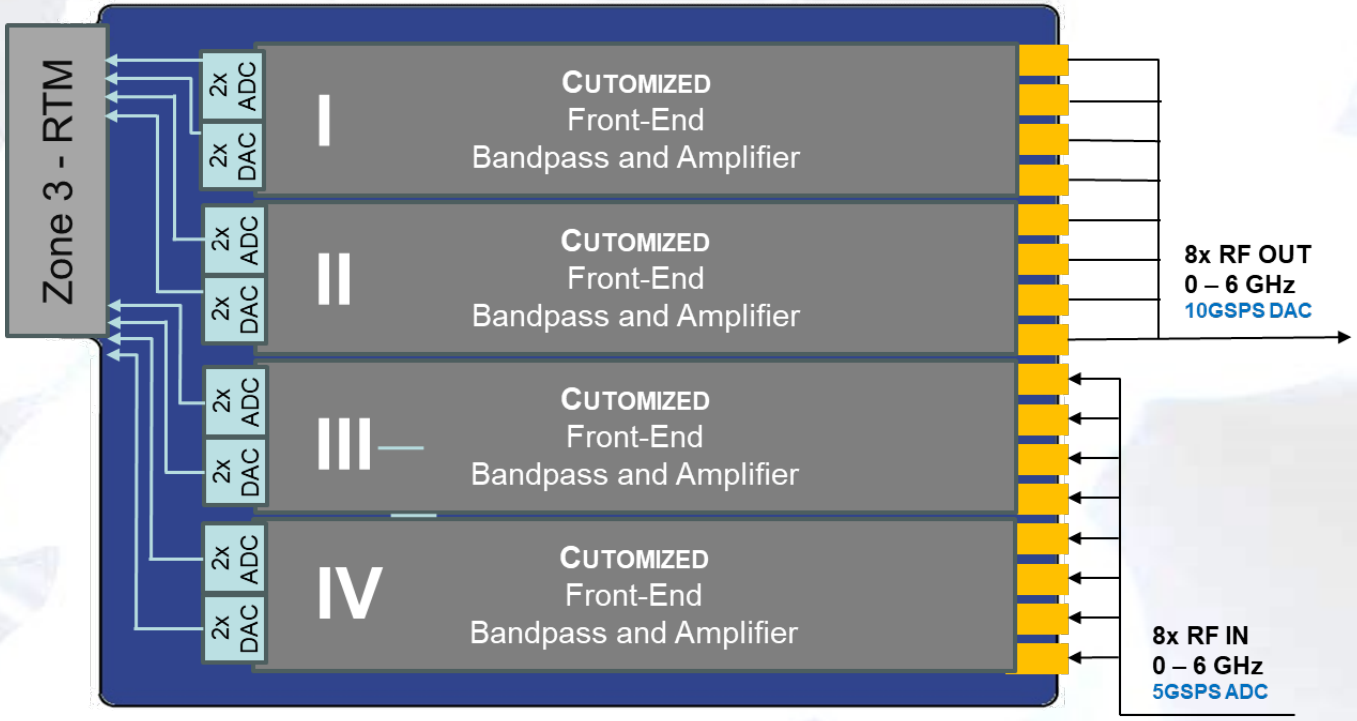
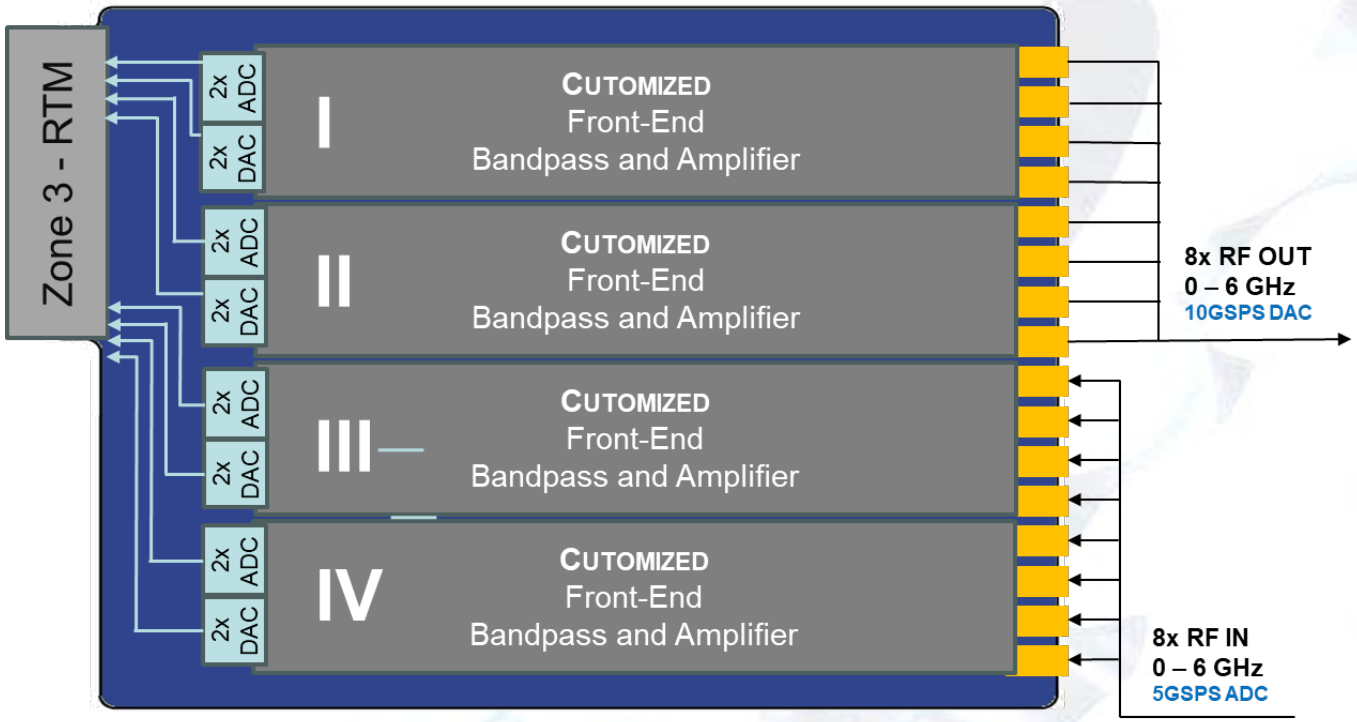
MTCA – Variant 2





MTCA – Variant 2



Customized Frontends:

E.g:

- 10...6000 MHz
  - no filter, no amplifier, P_{out} = -10 dBm
- 2400...2700 MHz
  - P_{out} = 20 dBm sample rate 3,6 GHz
- 3400...3800 MHz
  - P_{out} = 20 dBm, sample rate 4,8 GHz
- 5150...5900 MHz
  - P_{out} = 20 dBm, sample rate 4,8 GHz

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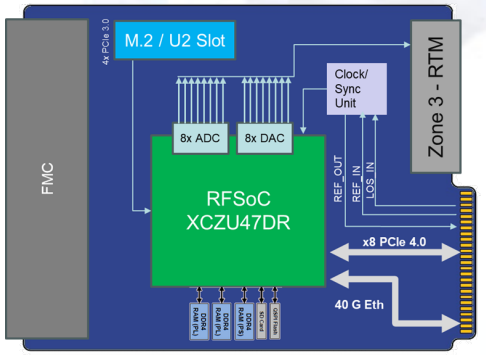
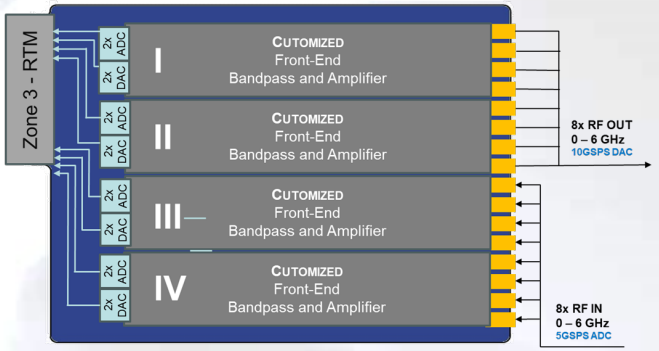
MTCA – Variant 2

- COTS AMC with RFSoC
- Custom RF front end on RTM
  - Bandfilter
  - Amplifier
  - Feedback Loops
- Low effort to individualize your system with custom RTMs
- Exchangeable RTMs





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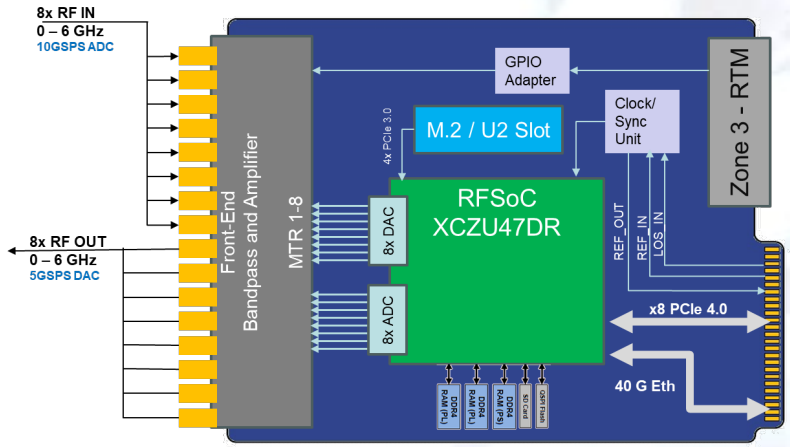
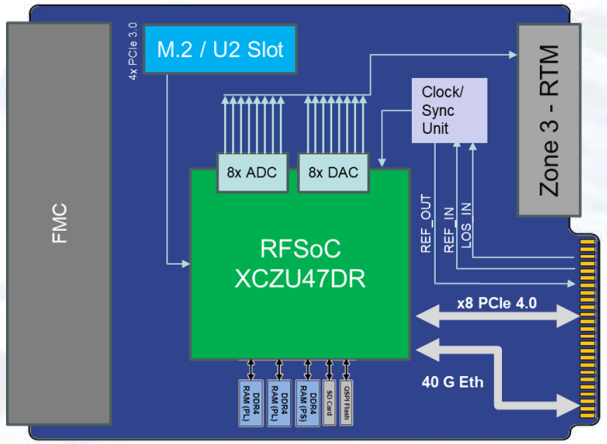
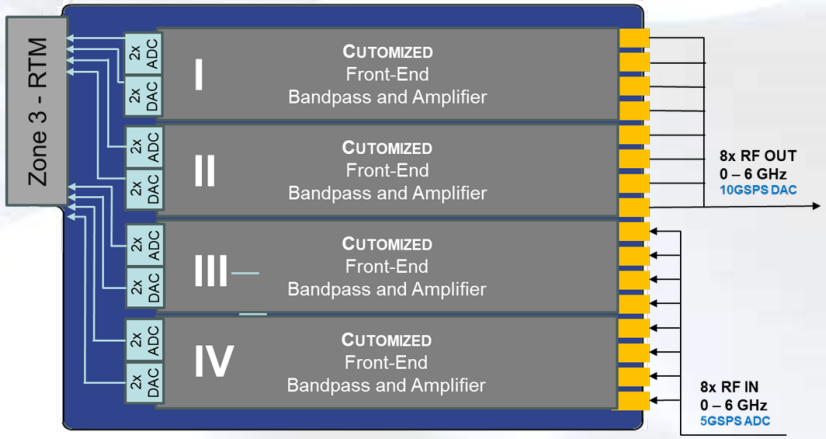
Summary

- Flexible design
  - RF on RTM or AMC
- **C**ommercial **o**f-**t**he-**s**helf







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Conclusion for Trapped-Ion QC

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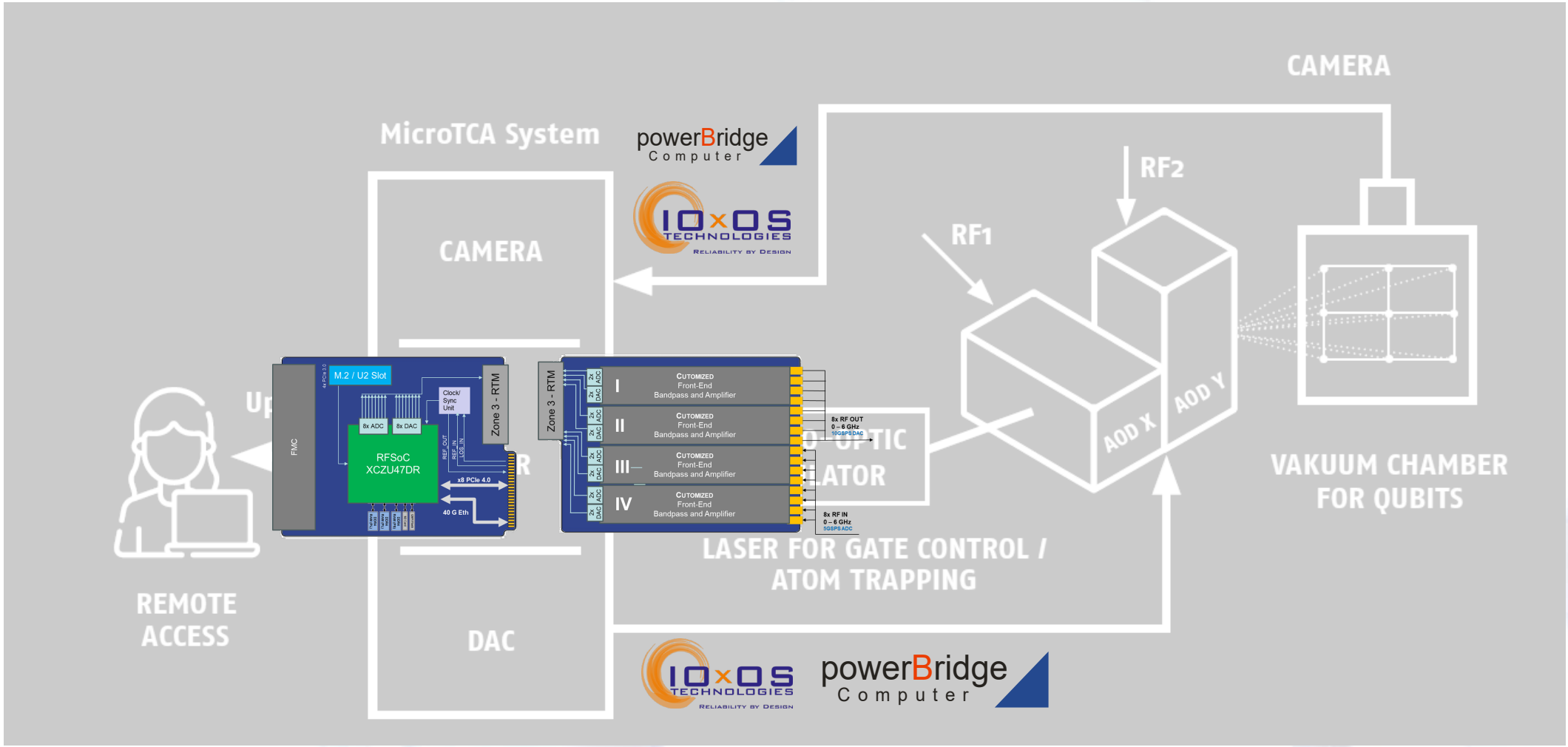
MTCA for Quantumcomputing



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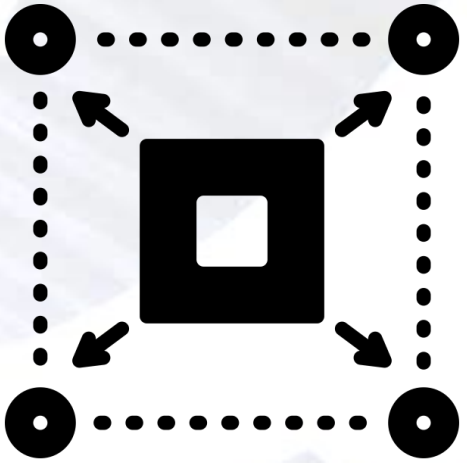
DDS Expandable

- Customizable for multiple applications
- Customizable with exchangeable RTM modules
- Expandable with FMC modules

IOxOS TECHNOLOGIES
RELIABILITY BY DESIGN



Created by WEBTECHOPS LLP
from Noun Project

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Questions to the Community

- Specification of the required RF signals: bandwidth, center frequency, modulation, signal level
- Specification of the RF interface, e.g. single ended, coaxial, 50 Ohm, SMA sockets only the Tx direction required or also Rx?
- How many parallel channels should be supported?
- Specification of the baseband signal to be transmitted: continuous streaming or periodically repeated sequence?
- Required memory depth for transmit/receive signals on board connection to computers / computer clusters for signal provision / evaluation: 100GbE or other?
- System controller for configuration and control / our current architecture: Linux on ARM processor is available on every SDR system, higher-level controller (PC) communicates with all SDR units via 1GbE

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Let‘s talk on our pBC Booth