



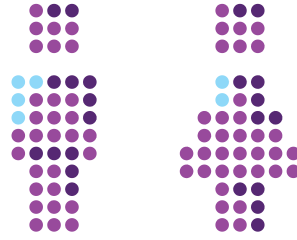
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Belgian Nuclear Research Centre

**TEST CAMPAIGN AT 2K OF THE BETA
0.35 SPOKE CRYOMODULE PROTOTYPE
WITH A MTCA.4-BASED LOW LEVEL RF
SYSTEM PROTOTYPE WITHIN THE
MYRRHA/MINERVA R&D**

W. De Cock - 06/12/2023

**12th MicroTCA Workshop for Industry and
Research**



CNRS/IN2P3, IJCLab, Université Paris-Saclay, Orsay, France

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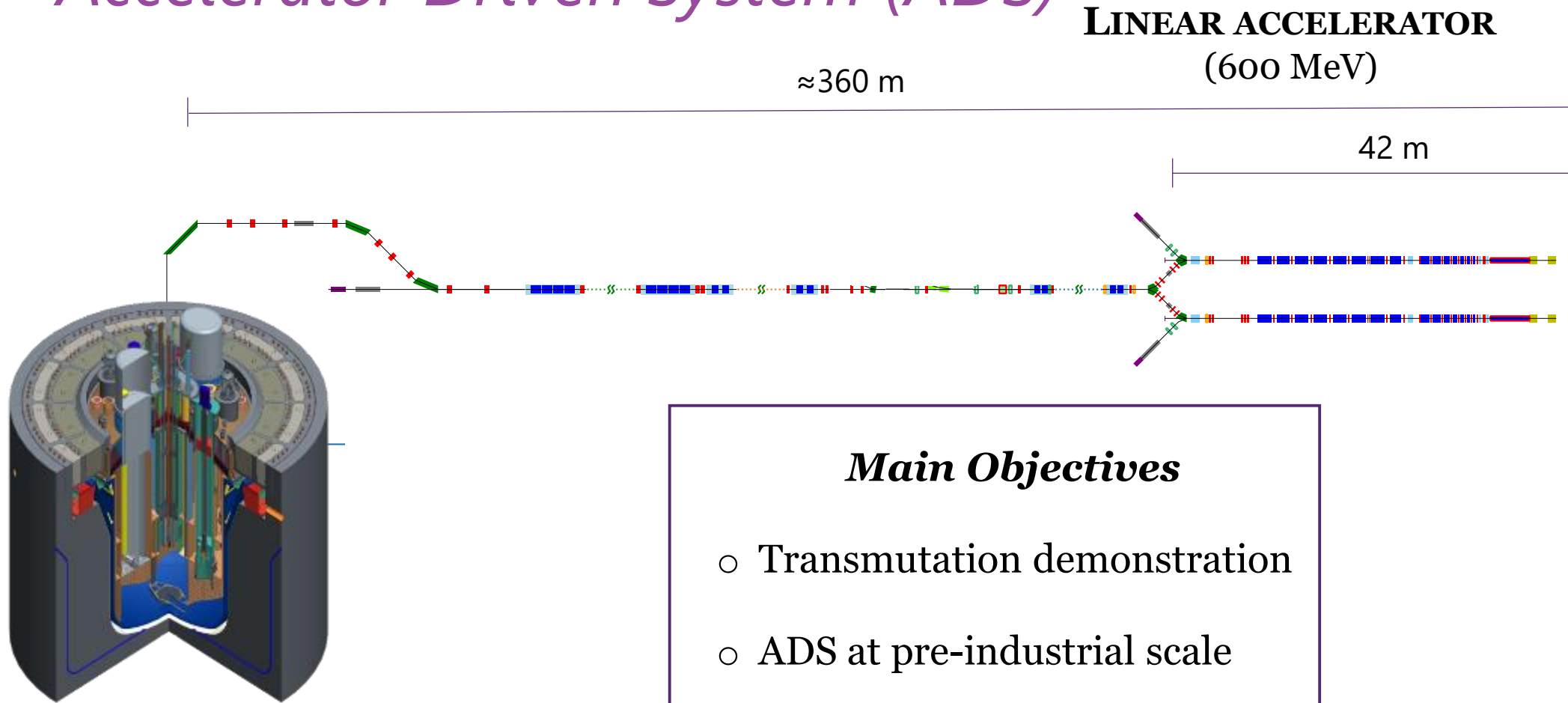
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Context

MYRRHA

Accelerator Driven System (ADS)



Main Objectives

- Transmutation demonstration
- ADS at pre-industrial scale
- Flexible irradiation facility

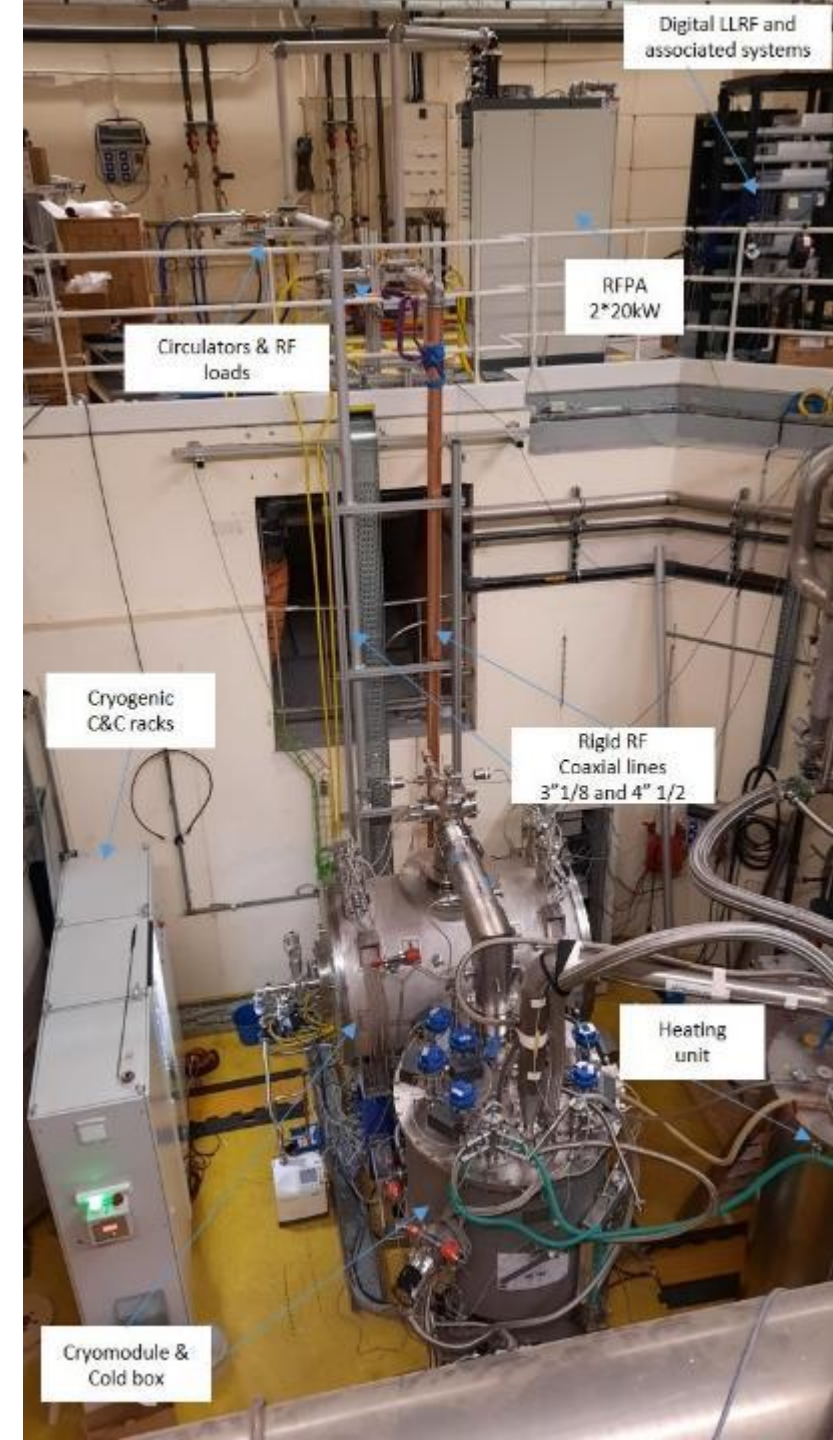
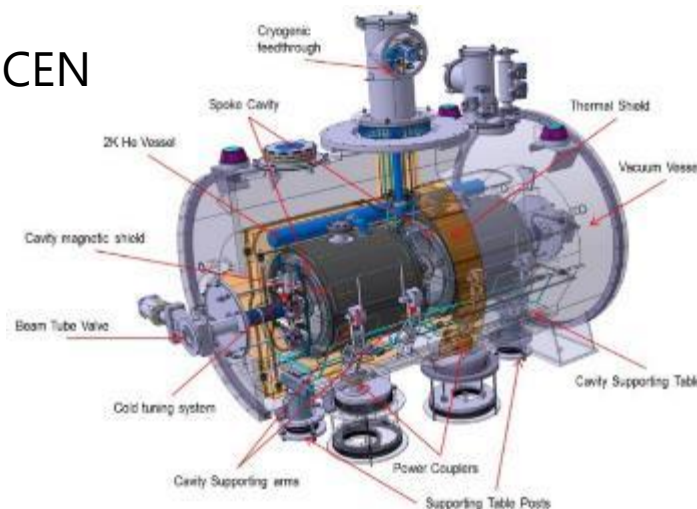
MINERVA ACCELERATOR MAIN SPECIFICATIONS

- Protons
- 4 mA
- CW operation with pulses to adapt beam power on targets & 250Hz target switching
- 176.1 MHz normal conducting injector up to 17MeV
- 352.2 MHz super conducting linac up to 100 MeV
- Possibility to later extend to 600 MeV (704 MHz)
- 3s fast fault compensation coordinated by central system
 - <10 beam trips of >3s per 90 day run (Beam trips must be resolved within 3 seconds to be transparent to the reactor)

Cryomodule Test Area at Orsay

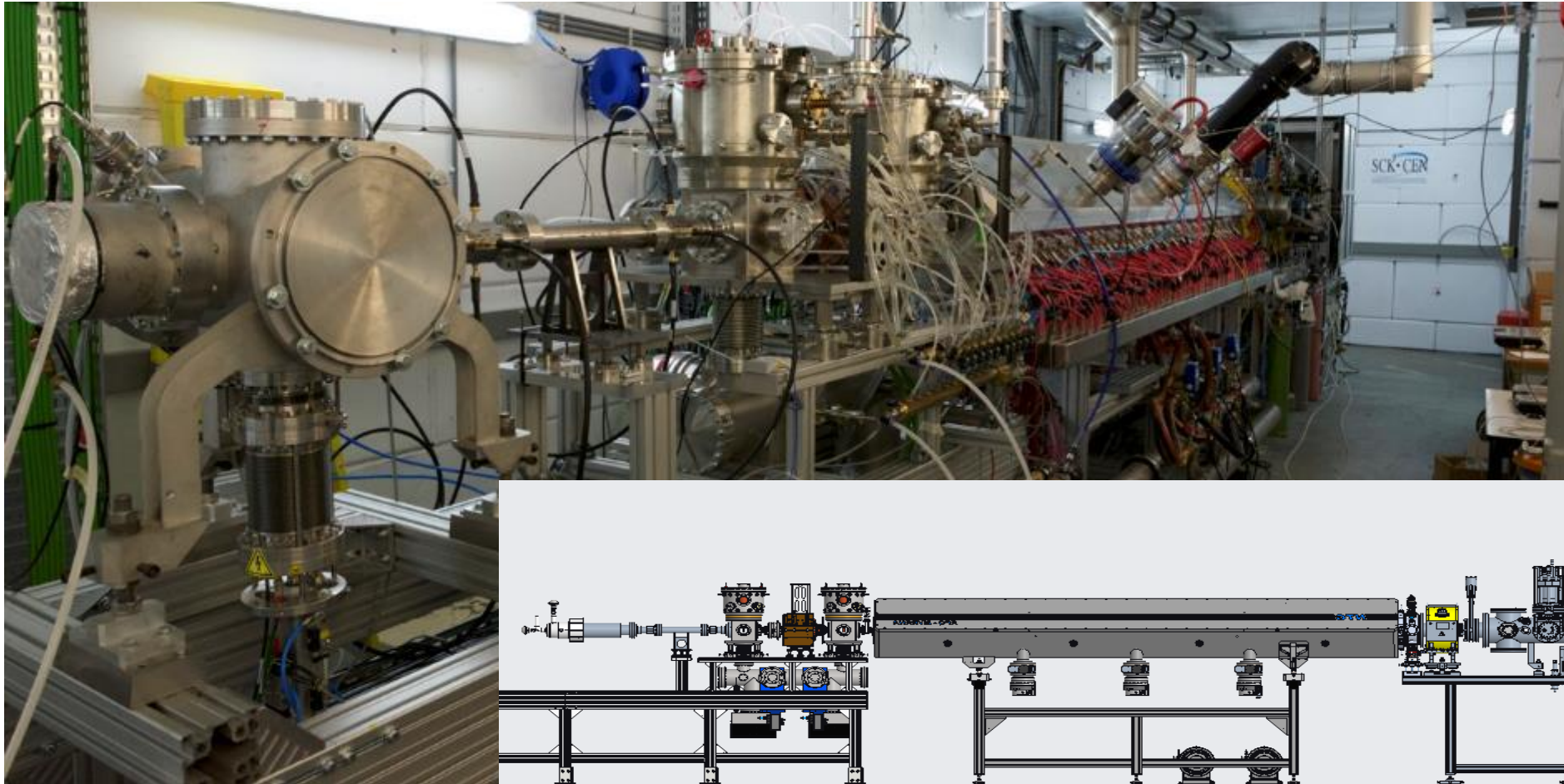
SupraTech platform, IJCLab

- R&D on the design, construction and test of a fully equipped cryomodule prototype for 352.2MHz LINAC section using single spoke cavities
- IJCLab: cryomodule, cavity tuner and LLRF control developed by IJCLab
- RF power couplers and C&C board for the Cold Tuning System (CTS) by LPSC
- EPICS based control system by SCK CEN



Injector Test Area at Louvain-La-Neuve

ITS, SCK CEN



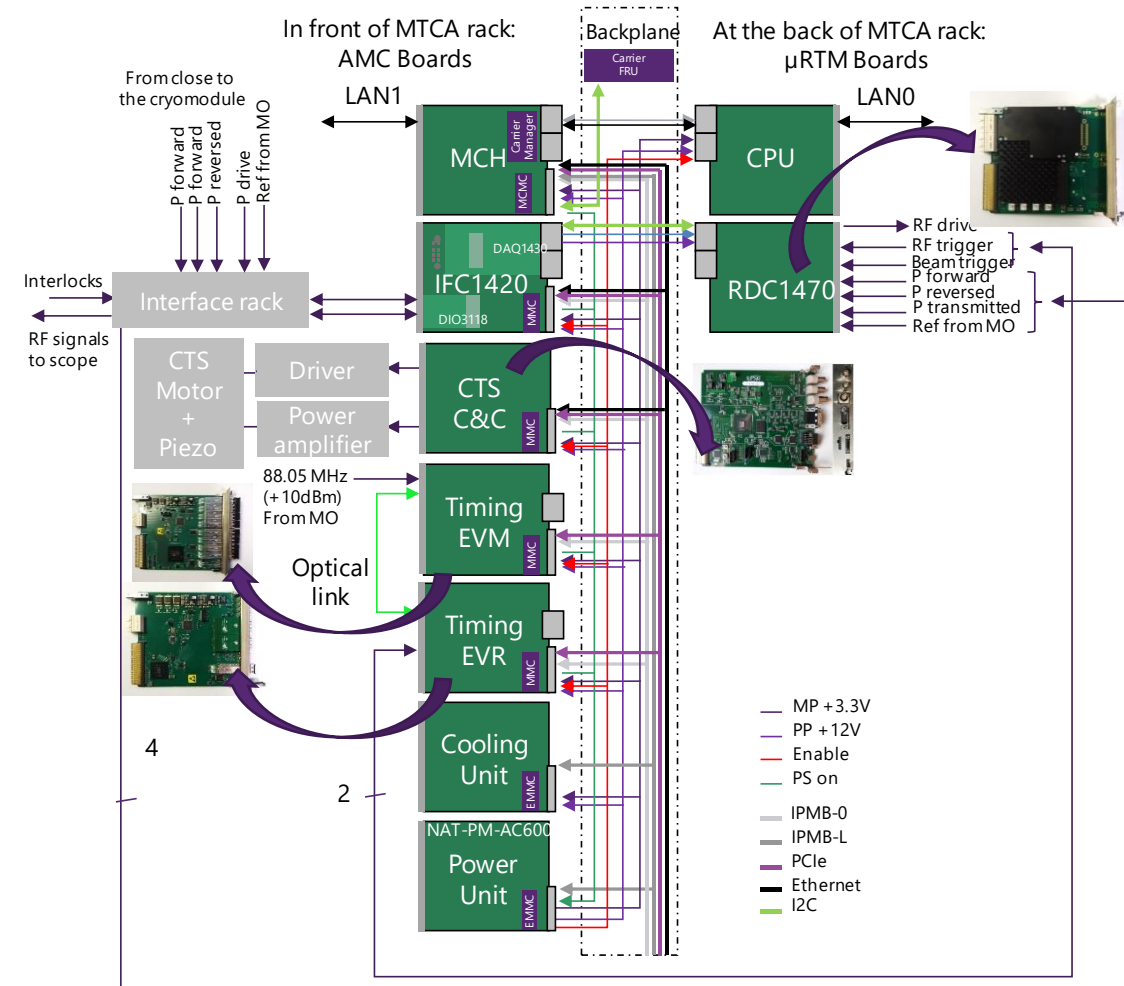


LLRF System

Low Level RF System

Hardware Architecture

- amplitude and phase stabilities of the accelerating field: $\pm 0.2\%$ and $\pm 0.1^\circ$ respectively.
- MTCA.4-based:
 - 2 crates (1 per cavity): NATIVE-R5
 - main board: IFC1420
 - μ RTM prototype board: RDC1470 developed in collaboration with IOXOS Technologies.
 - C&C CTS board developed by LPSC
 - Timing: MRF EVM/EVR distributed via backplane
- Operation:
 - QWRB cavity field regulation at 176.1MHz, with beam.
 - Two single SPOKE cavities at 352.2MHz during Cryomodule tests



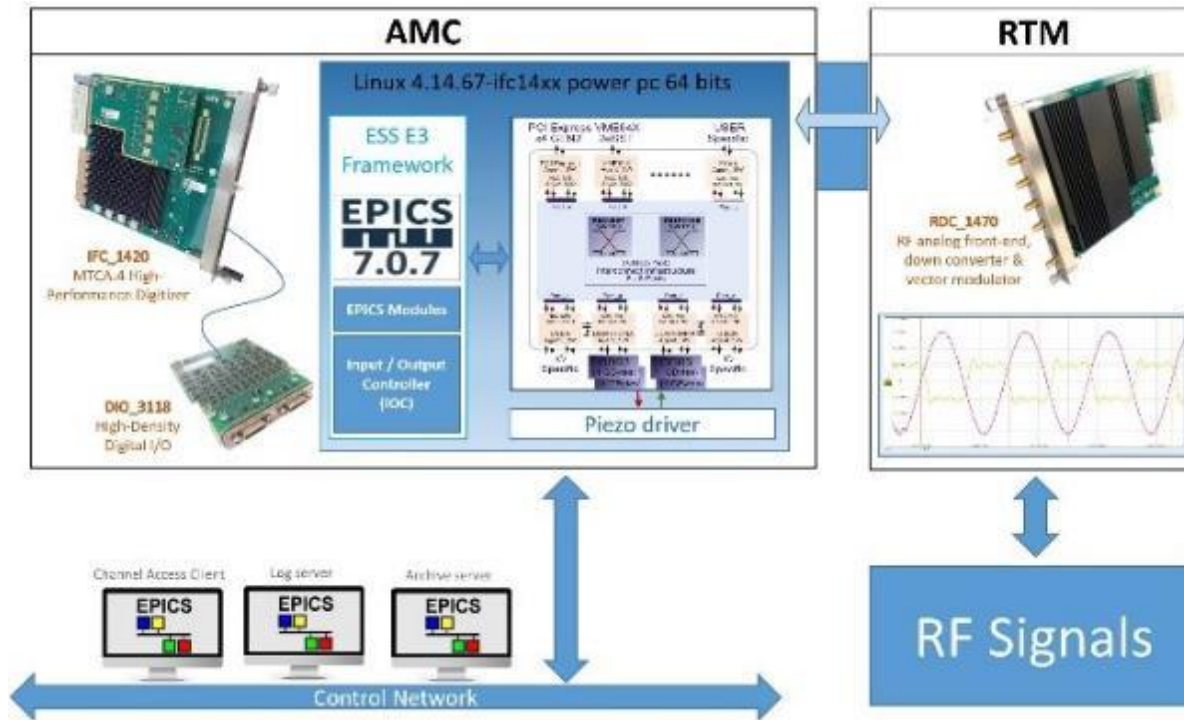
Firmware Architecture

-
- The diagram illustrates the SPOKE control system architecture, categorized into Hardware (blue), VHDL/Firmware (green), and Planned/in going (dashed green).
- Legend:**
- HARDWARE
 - VHDL/Firmware
 - Planned/in going
- System Components and Interactions:**
- Inputs:**
 - RF:** Input to the top demodulation stage.
 - Ref:** Reference input to the second demodulation stage.
 - LO (Local Oscillator):** Provided to all four demodulation stages.
 - IVol:** Input to the bottom demodulation stage.
 - Beam trigger:** Input to the I&Q FeedForward block.
 - Look-up tables:** Input to the I&Q setpoints block.
 - Search ramp modes:** Input to the I&Q setpoints block.
 - Debug mode:** Input to the I&Q setpoints block.
 - Quench detection, limiting power, Pattern or Cut modes:** Inputs to the Base Band signal processing block.
 - T⁺ & Water flows, Arc detectors, Multipactor e⁻, RF authorization, RF trigger, MPS interlock, PSS interlock:** Inputs to the MPS logic/HW block.
 - Processing Blocks:**
 - I&Q setpoints:** Receives search ramp modes, debug mode, and look-up tables. Outputs $E^*(Q)$ and $I^*(Q)$ to the PI/SEL/VAL controllers.
 - PI/SEL/VAL controllers:** Receives $E^*(Q)$ and $I^*(Q)$. Outputs I_{cmd} and Q_{cmd} to the I&Q FeedForward block and the Base Band signal processing block.
 - I&Q FeedForward:** Receives beam trigger and I_{cmd} , Q_{cmd} . Outputs I_{feed} and Q_{feed} to the Base Band signal processing block.
 - Base Band signal processing:** Receives I_{cmd} , Q_{cmd} , I_{feed} , and Q_{feed} . Outputs to the Dual DAC.
 - Dual DAC:** Outputs to the RF Mod.
 - RF Mod:** Receives LO and outputs RF to the RF Switch.
 - RF Switch:** Routes RF signal to the SSPA or back to the RF Mod.
 - SSPA (Solid State Power Amplifier):** Receives RF signal and outputs to the SPOKE Cavity.
 - MPS logic/HW:** Receives various interlocks and triggers. Outputs Fast detuning interlock to the Driver.
 - Phase shift calculations, Automatic mode authorization and Phase registers writing:** Receives valid measurements from the demodulation stages. Outputs to the Driver and Phase shift signal processing.
 - Dead Zone range:** Receives RS-232 input and outputs to the Driver.
 - motor Control with Dead Zone:** Receives RS-232 input and outputs to the Driver.
 - Automatic mode:** Receives RS-232 input and outputs to the Driver.
 - Driver:** Receives RS-232 input and outputs to the motor.
 - motor:** Receives RS-232 input and outputs Slow CTS to the SPOKE Cavity.
 - Piezo actuator Control μ C:** Receives RS-232 input and outputs Fast CTS to the SPOKE Cavity.
 - Piezo Amplifier:** Receives RS-232 input and outputs Fast CTS to the SPOKE Cavity.
 - RF pick up:** Receives RF signal and outputs to the SPOKE Cavity.
 - Demodulation Stages:** Four stages of "IF to Base-Band IQ or Non IQ Demodulation" blocks. Each stage receives LO and outputs I and Q signals to CORDIC blocks. The top stage also receives RF. The bottom stage also receives IVol. The CORDIC blocks output A and ϕ signals, which are used for valid measurements.



EPICS Development

Control System Architecture

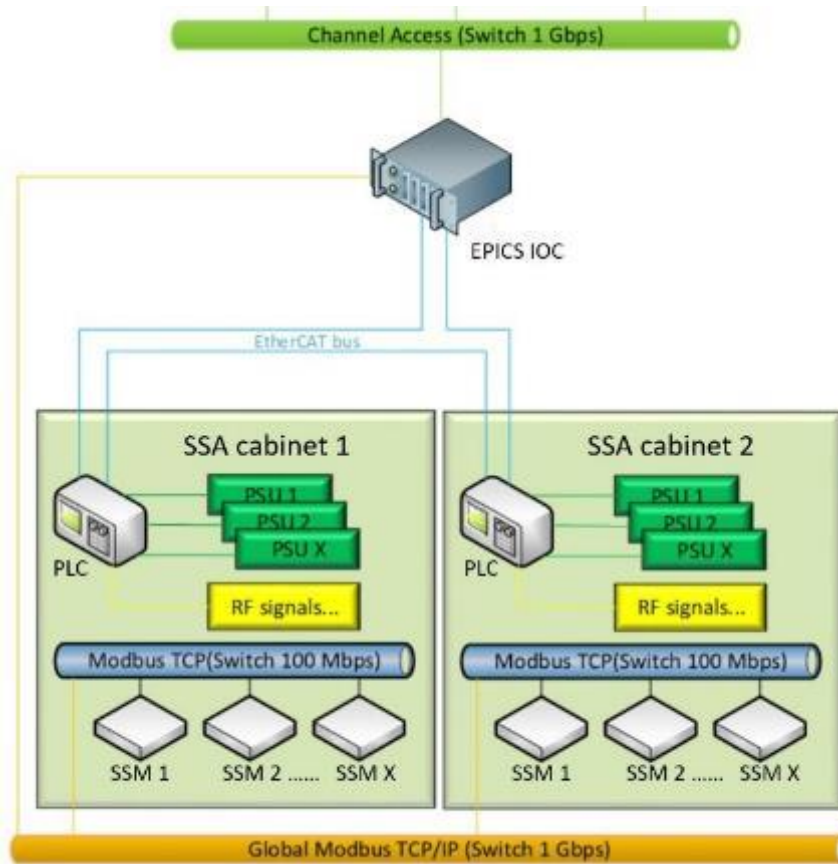


LLRF

- EPICS Input-Output Controller (IOC) implemented on a IOxOS IFC 1420 board, using ESS E3 framework
- Collaborative work with the IOXOS Technologies team in order to control the RF front-end board and to adapt the TOSCA libraries .
- Multifunctional IOC associated to the FPGA firmware.
 - LLRF regulation on the cavity
 - Real oscilloscope which returns data in the form of triggered buffers with a precision of +/- 12 ns between each measurement.
 - Buffers are archived via EPICS channel access (CA) for retrospective analysis.

- Piezo driver installed on the IOxOS OS communicating with the CTS C&C card.
 - C++ Hardware Access Library (uHAL) which provides an API for IPbus reads, writes, and transactions.
 - Compiled for 64-bit Power PC architecture
 - Runs independent of the EPICS layer and realizes the data exchange with an update rate which can be chosen by configuration.
 - Registers exchange can also be configured using an xml file.

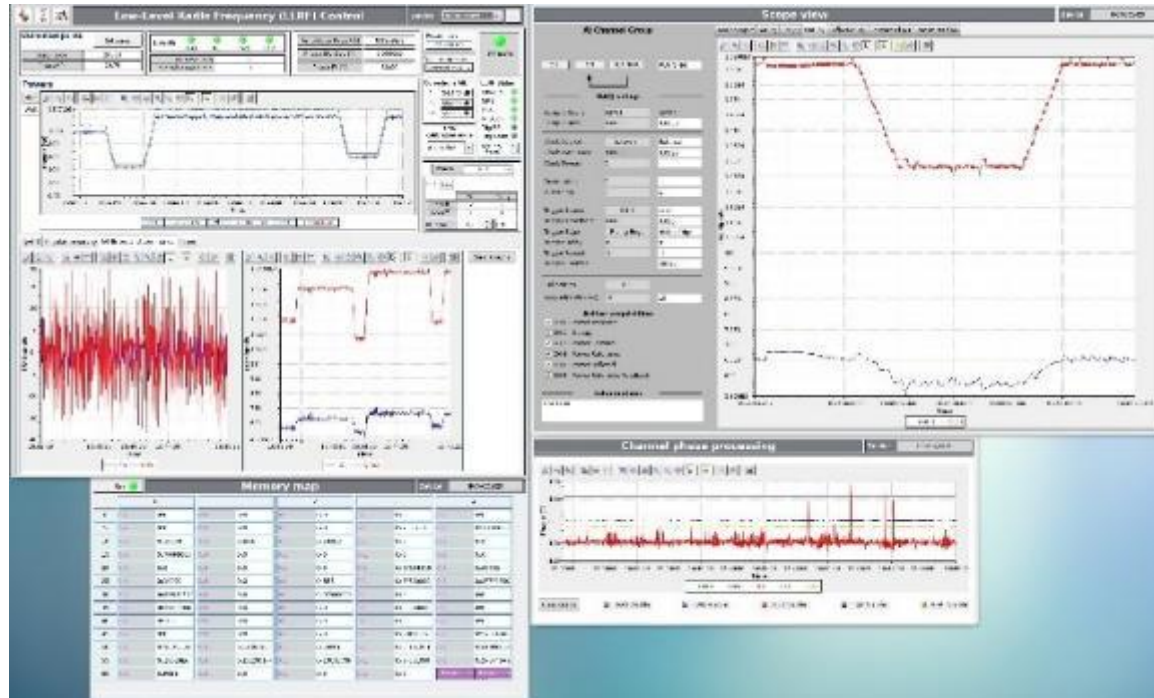
Control System Architecture



Solid-State Amplifiers

- Driven by the LLRF boards (μ RTM) and synchronized via PTP protocol.
- Data can be recovered in the form of triggered buffers sent to the archivers via EPICS.
- One SSA cabinet holds:
 - 1-to-n Solid State Module(s) (SSM)
 - 8 power supply units (PSU).
 - 1 PLC
- SSM data is directly pulled through Modbus communication by the IOC, remaining data is pulled from the amplifier PLC through Ethercat bus communication.
- Post-processing function is supported with circular buffers as in the LLRF system.
- EPICS IOCs running on PC with CentOS .

Control System Architecture



Graphical User Interface

- Realized with Control System Studio 4.6.1.25 (CSS)
- Configuration files to start the LLRF system easily and to manage several similar hardware boards in parallel.
- Possible to change the configuration on-line for specific functions.
- automatic high-level functions (e.g. frequency tuning) are implemented using the EPICS sequencer
- Main EPICS modules: archiver, sequencer, pvAccess/CA

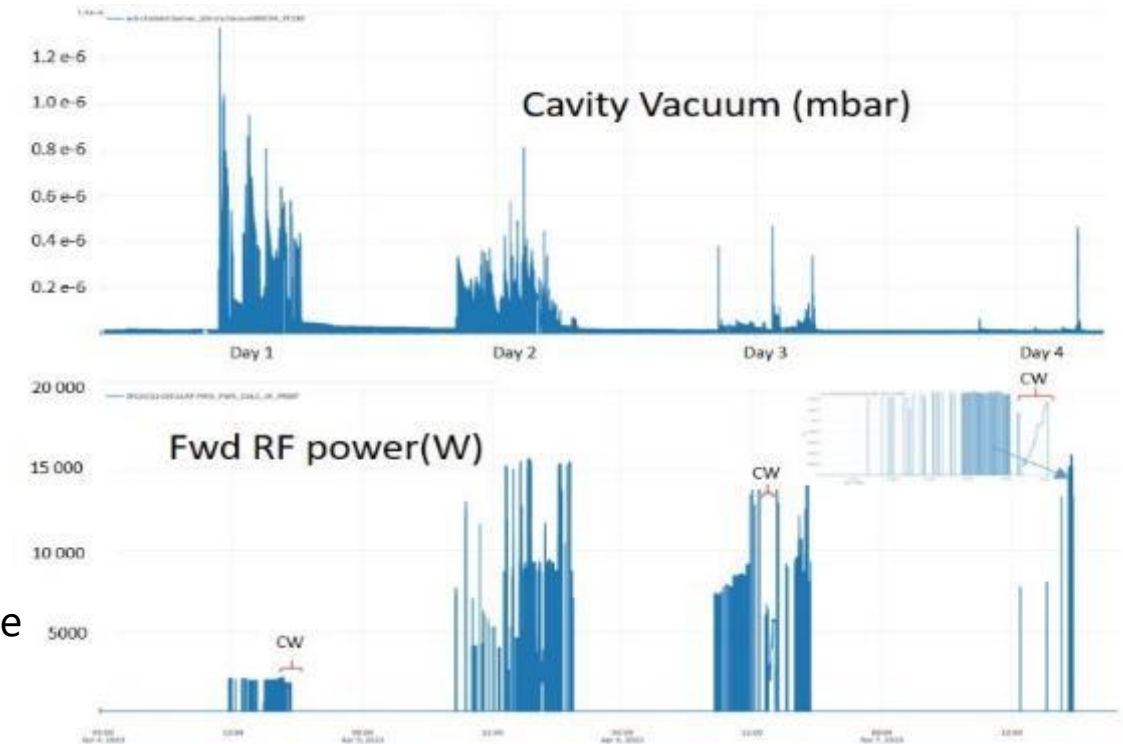


Results of the test campaign

Test Campaign

RF Power Couplers at 300K and 4K

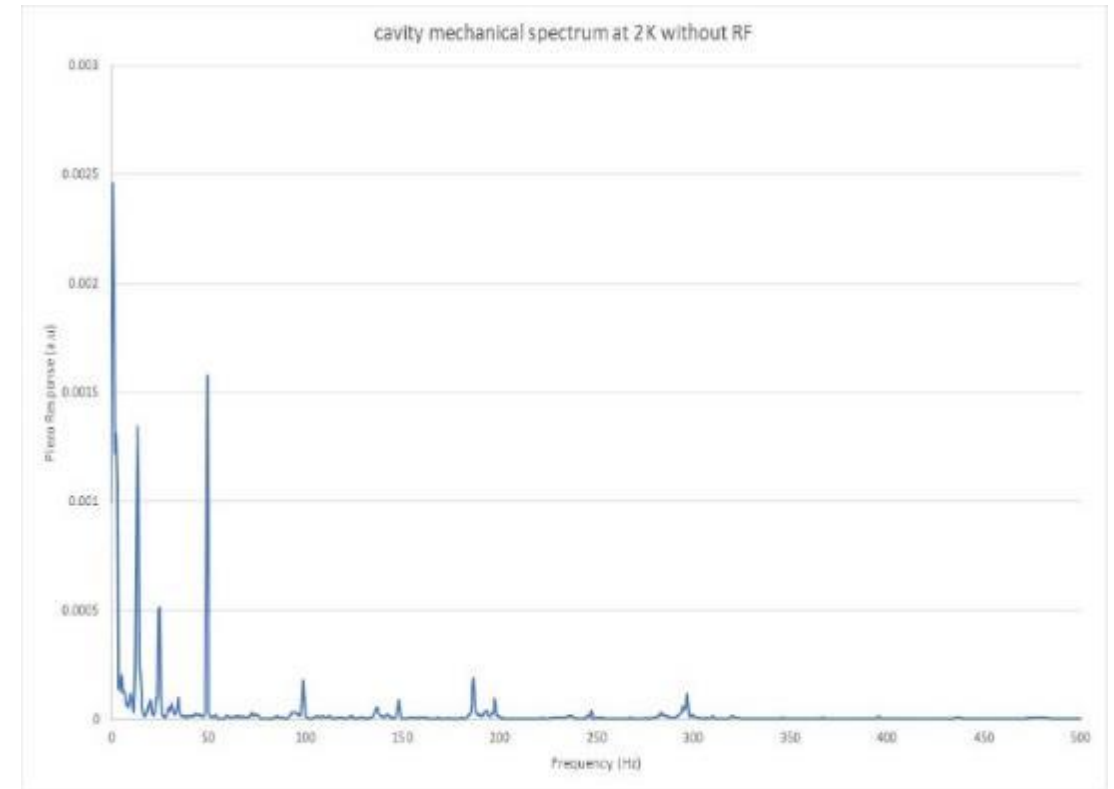
- RF power conditioning at 14kW CW
 - 2 Couplers
 - LLRF system in GDR and Pulsed mode using the MRF timing system.
 - RF pulses ranging from $10\mu\text{s}$ @ 16Hz to 99.9ms @ 1Hz.
 - Conditioning out of the bandwidth with first step below the multipacting level
- First RF power coupler, 4 days at 300K to reduce the e- pick up current due to the multipacting effect.
- Second RF power coupler, just one day of conditioning has canceled the e- pick up current.
- At 4K, the cryogenic pumping effect made conditioning easier.



Test Campaign

CTS at 2K

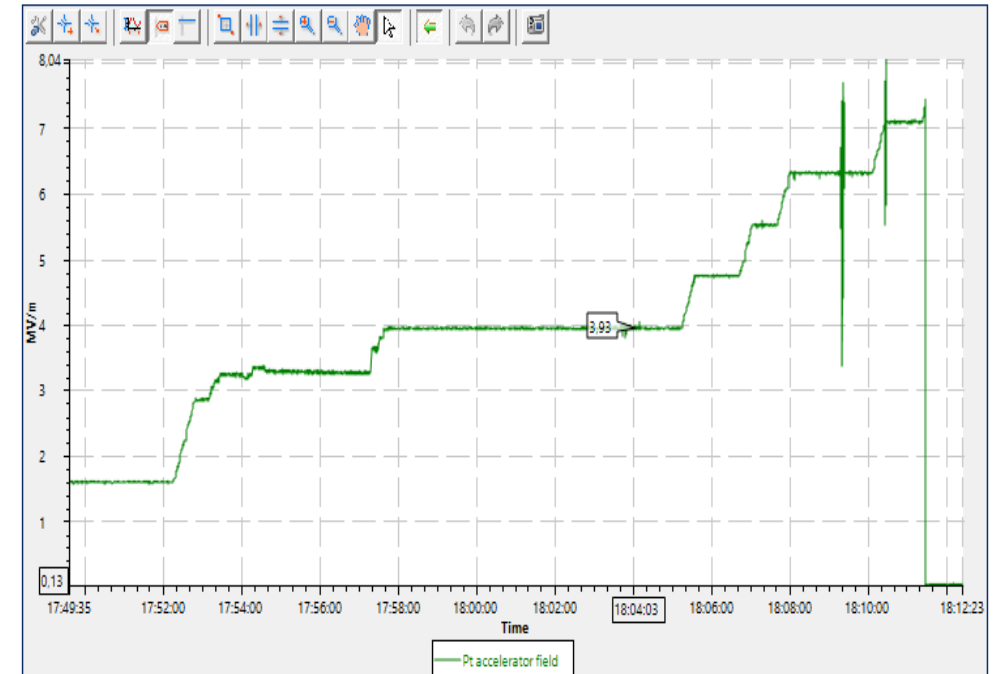
- LLRF system in GDR mode for tuning the cavity at the accelerator reference frequency = 352.2MHz.
- SEL loop tested in IQ demodulation mode.



Test Campaign

Spoke Cavities

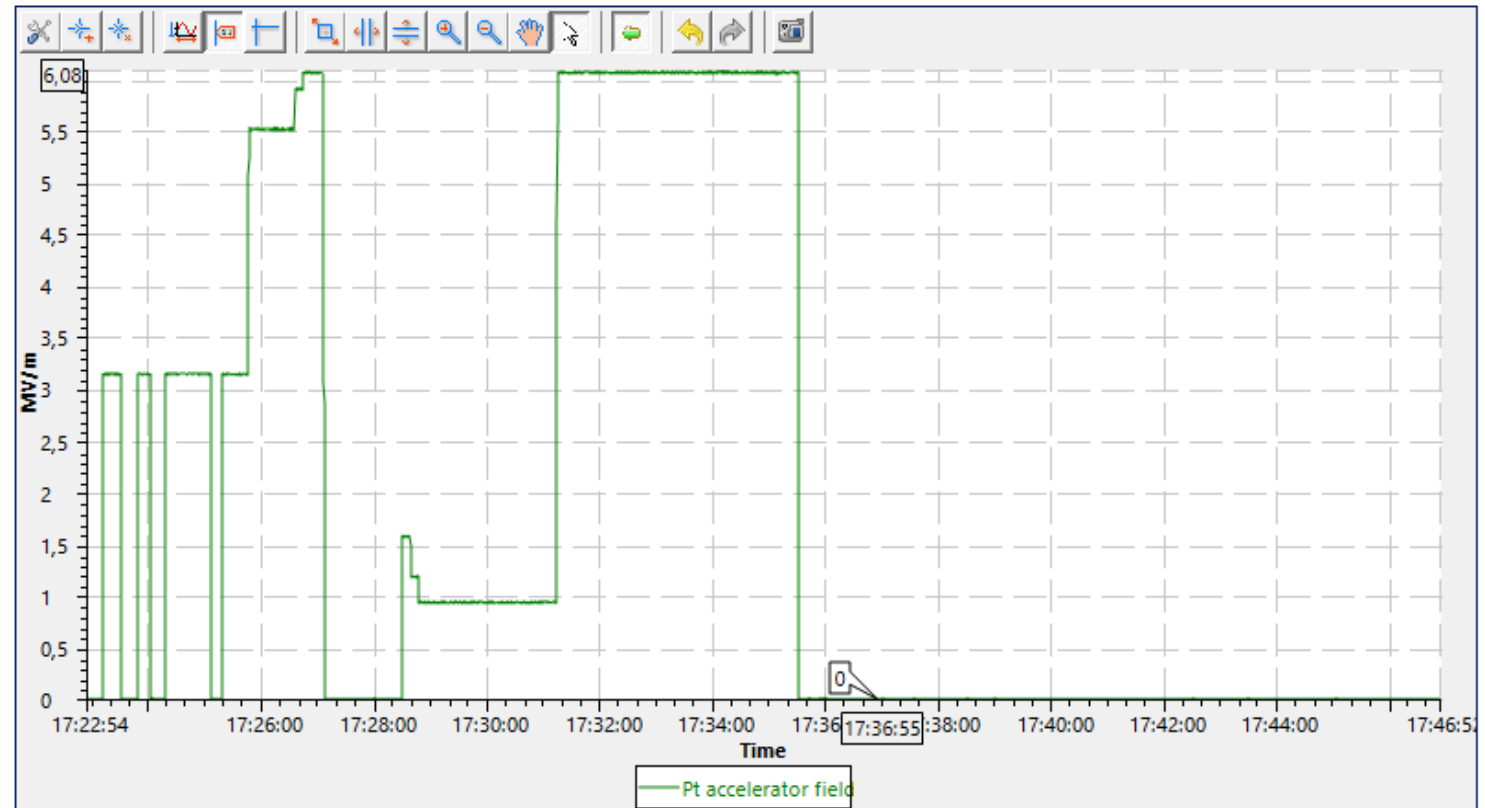
- Increase of the accelerator field without a frequency regulation (OL)
- Slow RF power increase using a ramp and a manual tuning to compensate for Lorentz forces.
- Manual tuning using the mechanical cavity spectrum transformed to a “little music”
- Phase shift between the forward and transmitted signals calculated with FPGA. Communicated via supervision and IPBUS to the CTS C&C board.
- Stepper motor position changes can be observed as well as Quench and the RF OFF interlock.



Test Campaign

Spoke Cavities – Fault Tolerance Test

- First cavity field changing from 1MV/m to 6MV/m with the second cavity detuned out of band
- Switch within 1 second with field and frequency regulation on the first cavity.
- Compliant with the fault tolerance strategy



Conclusions

- MTCA4 based LLRF system validated successfully at 176MHz on the injector prototype (two QWRB cavities) with beam.
- Currently being validated at 352.2MHz with superconducting cavities at 2K
- Planned improvements (firmware and software):
 - Second version of the RF AFE μ RTM board prototype (IOxOS RDC1470)
→ more flexibility and functionality.
 - R&D on integrating White Rabbit (WR) for timing and accelerator reference signals.
- “Lessons learned” are incorporated in the final design of the accelerator

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