First Light of the New Modular Controller for Astronomical Detectors (NGCII) and Further Developments

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ELT Construction Progress

https://www.youtube.com/watch?v=QqRREz0iBes

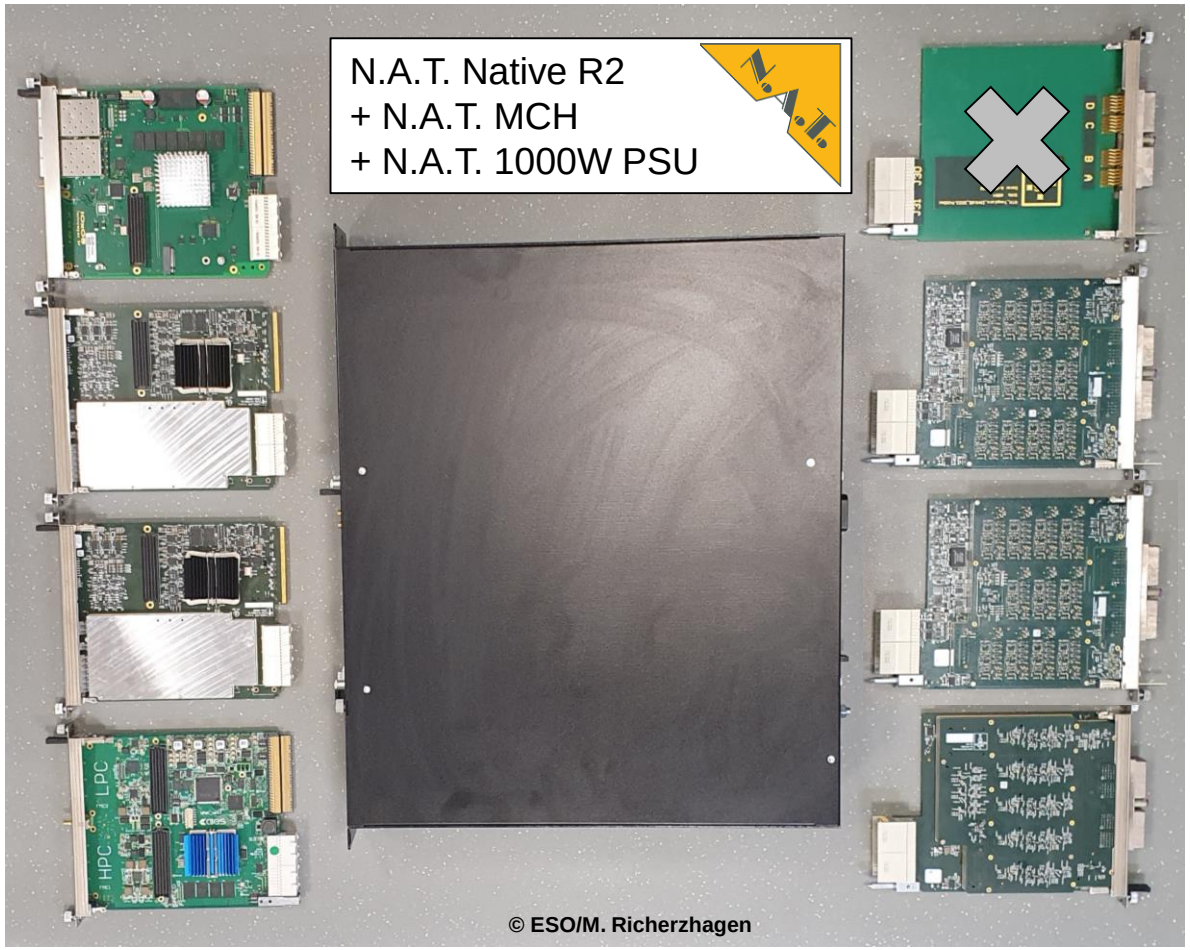
NGCII – MTCA.4-based General Detector Controller

Modular controller. Configured for CMOS detectors here.

IOXOS IFC1414
New Board for ESO
Zynq US+ FPGA
PROTOTYPE

2x AQ22 AMC
ADC Module
Artix FPGA
In-house Dev.

AIES MFMC
Artix FPGA



APD Bias RTM
Negative APD Bias
In development
Not needed for first light

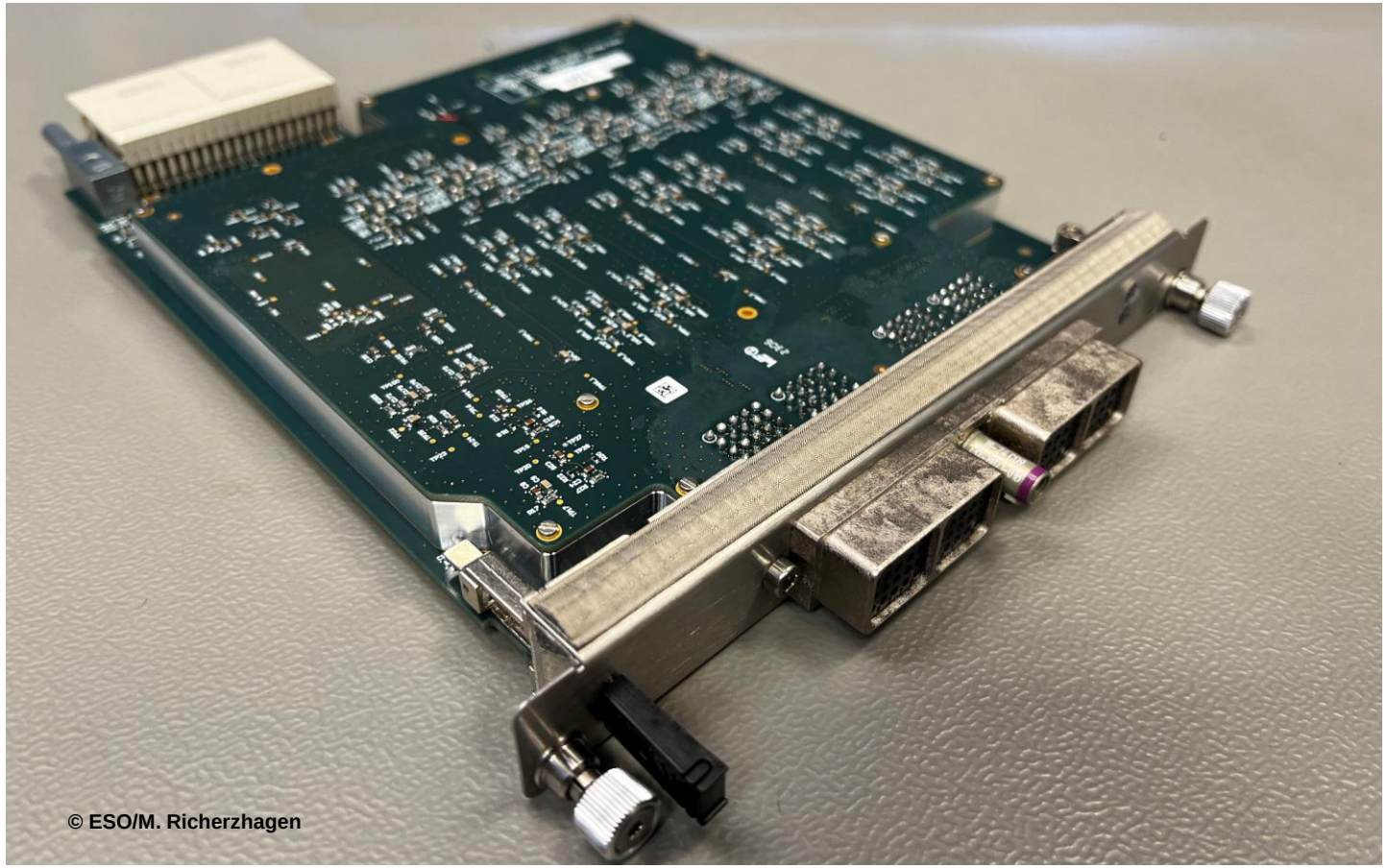
2x CMOS AQ22 RTM
Signal Conditioning
In-house Development

CMOS C20B20 RTM
Clock + DC Bias
In-house Development

In-House Developed Modules

Modular controller. Significant in-house development.

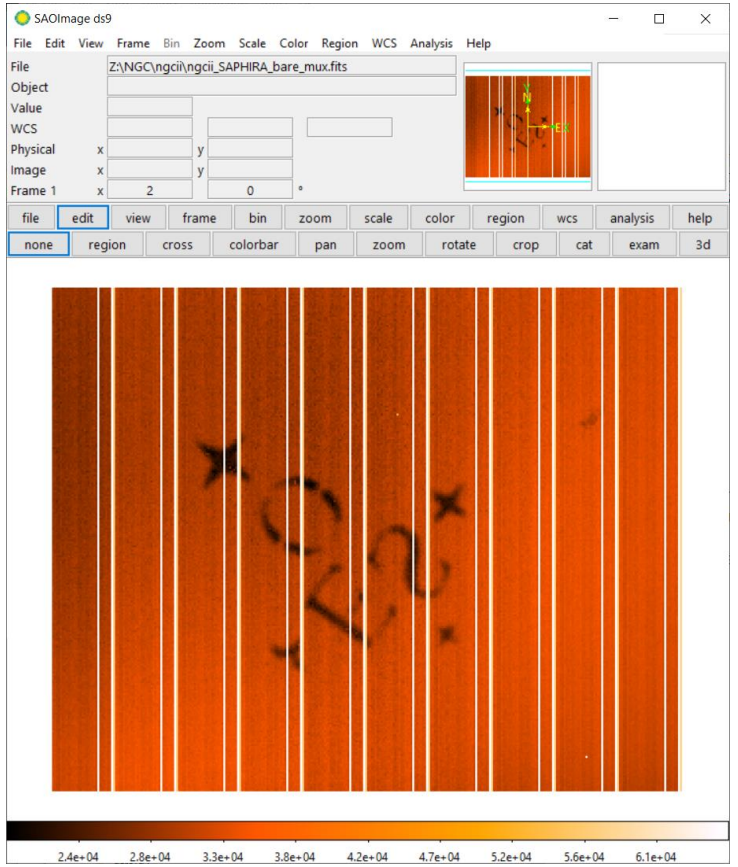
- Developed up to now:
  - 1 type of analog AMC
  - 2 types of analog RTM
  - 6 types of digital RTM
- “Double decker” double mid-size modules.
- EN4165 military interface connectors.



First Light SAPHIRA

First light in the laboratory was achieved shortly after MTCAWS 2023

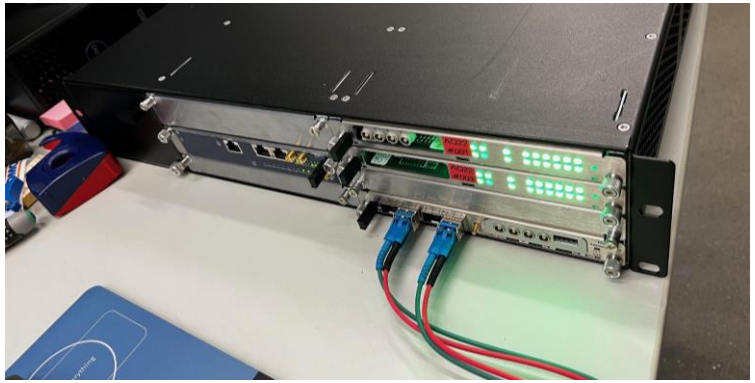
- SAPHIRA Detector
  - Infrared CMOS APD
  - 500fps
  - 256x320px
  - CMOS APD
- Tested with bare ROIC and cold detector.

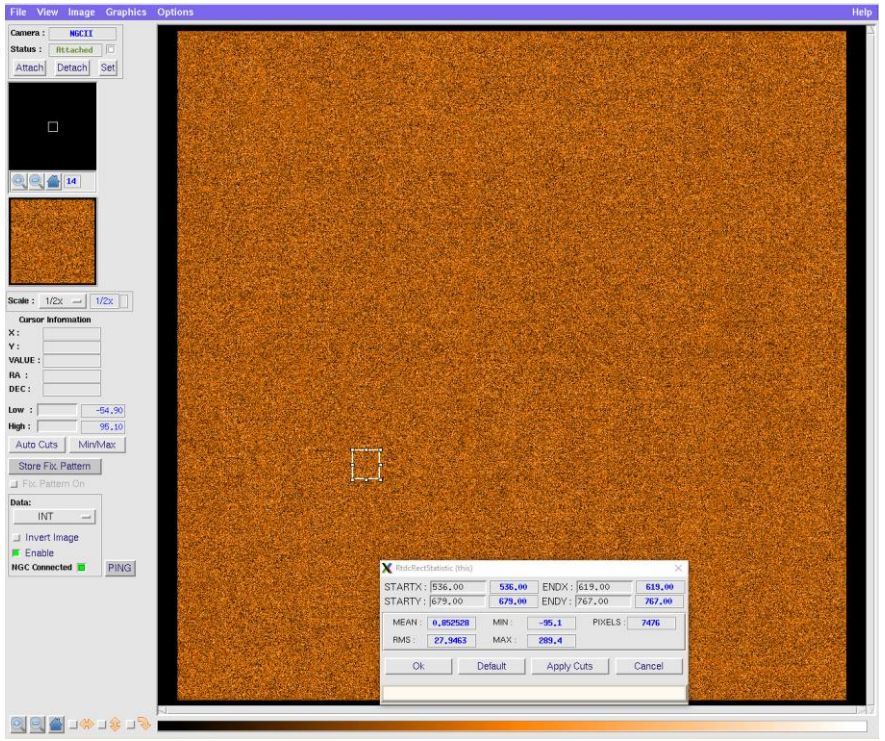


First Light HAWAII2-RG

First light with another CMOS detector achieved summer 2023

- HAWAII2/RG Detector
  - Infrared CMOS
  - Slow mode: ~0.33fps
  - Fast mode: ~33fps
  - 2048x2048px
- Workhorse of the ELT
  - ~20 detectors in first generation instruments
- Tested with bare ROIC





Further Development – CMOS System Refinement

All first light tests performed with Rev. 1 hardware

- Developing Rev. 2 Hardware
- Some iterations but no conceptual changes yet.
- No design regression yet.
- Example: CMOS AQ22 RTM
  - Video channels showed spurious noise.
- In Rev. 2:
  - RMS Noise ≤ 0.1LSB$_{16}$
  - All peaks from known source

Further Development – CCD System Development

CCD detector control in 2024

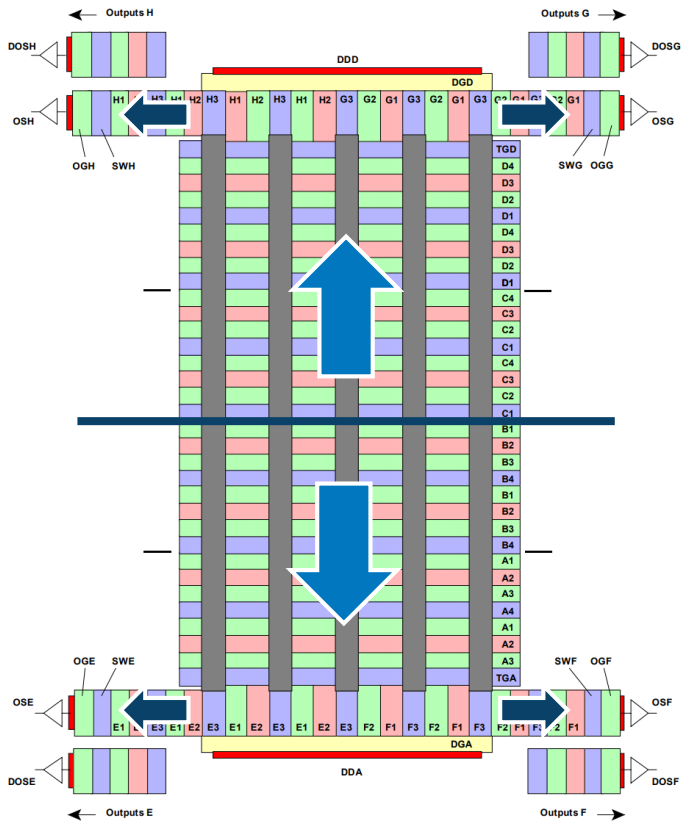
- CCD Detectors
  - Operate at higher voltages
  - Require more “analog” waveforms
- A set of 3 RTMs is developed

Module	Functions
CCD B24 RTM	24x DC voltage bias for CCDs • 0V to 34V range • ~50µV/K drift • ~12μV_{RMS} noise
CCD C24 RTM	12x “fast” clock for CCD 8x “slow” clock for CCD • See following slide
CCD AQ8 RTM	8x CCD video channel • Analog clamp and sample • Switchable gain (x1 / x2) • Switchable low pass filter

Further Development – CCD Clock Module

CCD detector control in 2024

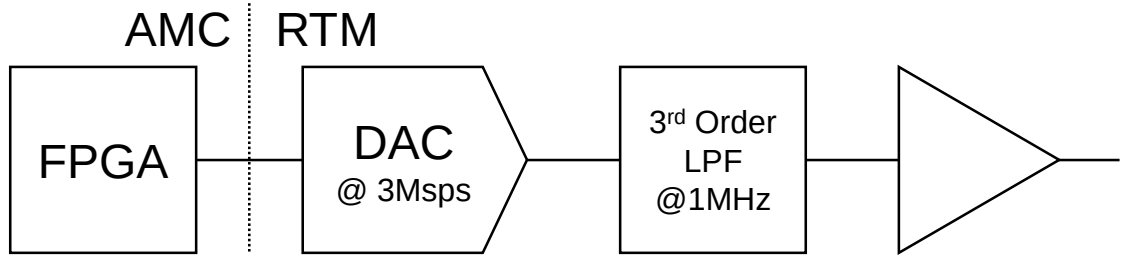
- CCD clock module directly controls charge shifting on detector.
- 4096x4112 pixel array
- “Slow” clocks shift rows of pixels up or down into the serial registers (up to 50kHz)
  - High capacitive load (up to 120nF)
  - Careful waveform shape control
- “Fast” clocks shift the serial registers into the analog outputs (up to 2MHz)

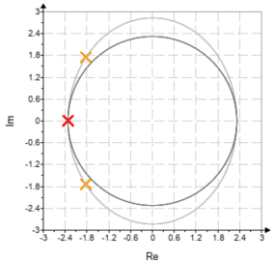


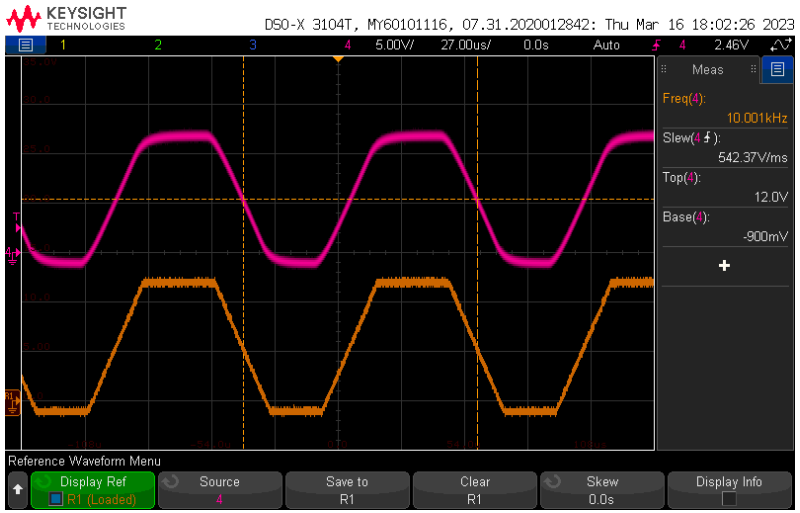
Further Development – CCD Slow Clock DDS

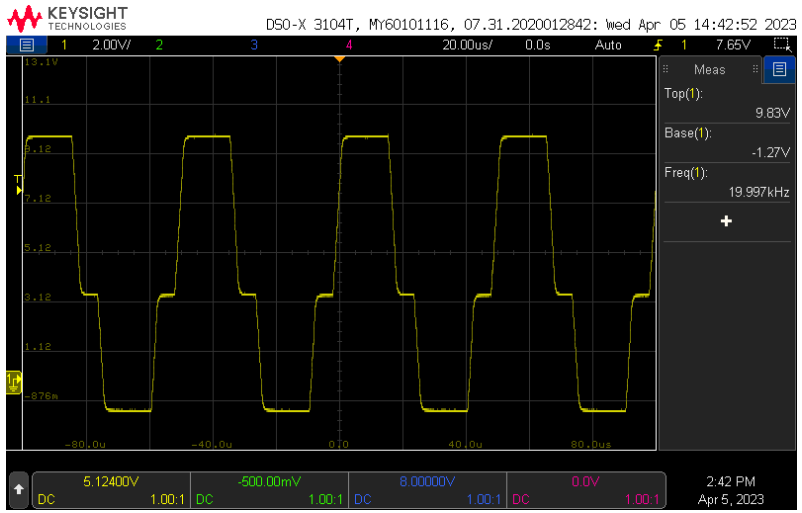
CCD detector control in 2024

- Parallel clocks for CCDs
- Voltage swing:
  - 0V to ~10V
- Extended control over clock waveform is desirable.
  - Clean trapezoid ramp
  - Tri-level clocking
- Solution: Direct Digital Synthesis









Orange: Generated Waveform

Pink: Waveform with cable and 100nF load

Yellow: Tri-Level Clock

Yes, it can play the imperial march!