

Application of MicroTCA in the Hybrid Pixel Detector for the High Energy Photon Source

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Outline

- Background & Requirements
- Hybrid Module
 - ASIC Upgrade
 - Front-end Module Upgrade
 - Single Module Test
- New Electronics System based on MicroTCA.4
 - FPGA Readout Board (AMC)
 - Clocking
- Summary

High Energy Photon Source (HEPS)





- Fourth-generation synchrotron light source
- Under construction in Huairou District, Beijing
 - Start the user operation in 2026
- Key-parameters for beam

Parameters	Nominal
Beam energy	6.0 GeV
Emittance	better than 0.06nm×rad
Beam	Higher than 1×1022 phs/s/mm2/mrad2/0.1%BW
Spatial resolution	10 nm
Energy resolution	1 meV
Photon energy	Up to 300keV



- HEPS Phase I plans 14 beamlines with the area array pixel detector in 2025
 - Detectable energy range: 8-20 keV
 - Spatial resolution: 140 µm
 - Total pixels: 6M, 2M, 1M, & 150K
 - Frame rate: Up to 2 kHz

Ref: http://english.ihep.cas.cn/heps/index.html

Hybrid Pixel Detector









Dynamic image



- Image recorder
 - Assembled from multiple front-end modules
- Front-end modules
- Sensor
 - An array of individual pixels arranged in a grid pattern
 - Convert the incident radiation into electrical signals
- Readout ASIC
 - An array of individual pixels match with sensor
 - Amplify electrical signals and process to generate a digital image or data
- Module hybridization
 - One sensor bump-bonded with multiple readout AISCs

Single Module Test





- Single module passed the preliminary tests
 - All functions are as expected
 - Reliability tests in progress



Threshold scan before calibration



Threshold scan after calibration



PCB for bPOL12v in ATLAS HGTD





Preliminary X-ray image (uncalibrated) A leaf exposed by an Au X-ray tube with 15 kV and 200 μA current for 0.3s

Prototype Systems Evolution



	1 st BPIX (2015-2016)	2 nd BPIX (2017-2018)	3 rd BPIX (2019-2021)	4 th BPIX (2022-now)
Modules	6	16	24	40
Pixels	360K	~1M	1.4M	6M
Assembly Scheme	Wire bonding & Rigid-flex PCB	Wire bonding & Rigid-flex PCB	Through Silicon Via (TSV) & Rigid-flex PCB with low CTE (coefficient of thermal expansion)	Advanced wire bonding & HTCC (High Temperature Co-Fired Ceramic)
Dead Area Occupancy	26.3%	26.3%	11.8%	~9.3%
FPGA Board	Spartan6 + SFP	Kintex7 + DDR3 + Molex Nano-Pitch I/O [™] Cable	Kintex7 + DDR3 + Molex Nano-Pitch I/O [™] Cable	UltraScale Kintex Plus + DDR4 + <mark>MicroTCA.4</mark>
DAQ Interface	1G Ethernet x12	1/10 G Ethernet x4	10G Ethernet x4	100G Ethernet x2
Power	100W	370W	500W	<2500W









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Electronics System Architecture (Baseline)



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Data sorting

Data compression

Real-time algorithm



On-detector

- **FPGA AMC board** •
 - **Front-end Electronics Control**
 - **Clock Synchronization**
 - Monitoring —
 - **Data Acquisition** _

Electronics System Architecture (Alternative)





Control & monitor

Use the MCH with 40/100GbE switch to replace the commercial network switch

• More compact

Options:

- NAT, NAT-HUB-E
- Vadatech, UTC056-500-212-110

FPGA Board (AMC + RTM)







uRTM-v2



u4FCP & uRTM:

FPGA-based MicroTCA compatible AMC board

- For generic system control and data acquisition in HEP/HEPS experiments
- Conceived to serve a mid-sized system residing either
 - inside a MicroTCA crate or
 - **stand-alone** on desktop with high-speed optical links or Ethernet to PC
- HPC FMC sockets
 - Provide additional clock signals, user-specific I/O and high-speed transceivers that can be used to extend the connectivity as well as the I/O bandwidth
- The red lines are high-speed serial links connected to the <u>gigabyte transceivers</u> (<u>GTY/GTH/GTX</u>) of the FPGA. The blue lines are the general input/ outputs connected to the High Performance (HP), High Range (HR) or High Density (HD) banks of the FPGA.
- More details:
 - https://github.com/palzhj/u4FCPv2

Clock Redundancy Consideration

- Due to the life limit of fiber optic transceivers, we plan to use a redundant WR clock
- Each uTCA crate has two WR slave nodes Clock source selection WR node report the loss of lock Ref clock DCS get the report, and configure the hardware to switch to the redundant node The White Rabbit Project CERN switch 18-port WR switch slave slave slave slave slave slave FPGA **FPGA FPGA** uTCA crate uTCA crate uTCA crate



Clock Distribution in MicroTCA





Two clock allocation schemes inside the crate

- Port 17 ?
 - Native R9 crate with WR Support
 - MLVDS multi-drop connection



- TCLK ?
 - TCLKB (slot12)-> MCH (NAT-MCH-PHYS80) -> TCLKA (slot1-11)



Mini-WR FMC for System-level clock synchronization

Clock Distribution in MicroTCA





AMC with mini-WR fixed in slot 12, move AMC receiver





Receiver is fixed at slot 2, add more adjacent AMC boards





- TCLK scheme has deterministic skew, but more jitter
- Port17 scheme has smaller jitter, but the skew is related to the location and receiver quantity



Summary

HEPS-BPIX40

- An new hybrid pixel detector for the High Energy Photon Source
- Front-end module
 - Complete small batch assembly, pass the preliminary tests, under reliability tests
- 6M prototype system based on MicroTCA.4
 - Complete hardware design and production
 - Firmware and software development in progress

More Applications – SHINE STARTLIGHT Detector





- Shanghai HIgh repetitioN rate xfel and Extreme light facility (SHINE)
- Under construction in Zhangjiang, Shanghai
 - Start the user operation in 2026
- 3 beamlines and 10 end-stations
- One end-station for area array detector with silicon pixels
 - Detector: STARTLIGHT (SemiconducTor Array detectoR with Large dynamic ranGe and cHarge inTegrating readout
 - ASIC: HYLITE (High dYnamic range free electron Laser Imaging deTEctor)

Specs	STARLIGHT
Pixel size	100 μm X 100 μm
ASIC Pixel Array	128 X 128
Gain	Self-adaptive 3 gains
Dynamic range	1 ~ 10000 photons/pulse @12 keV
Frame rate	12 kHz (continuous readout)
Detector	A 4.2M pixel detector in vacuum, quadrant movable



Challenge: Continuously data stream up to 654.3 Gbps

More Applications – JUNO TAO Experiment





- The Taishan Antineutrino Observatory (TAO) is a satellite experiment of the Jiangmen Underground Neutrino Observatory (JUNO), located in the southern China, expected to start collecting data in 2024.
- TAO consists of a spherical ton-level Gadolinium-doped Liquid Scintillator (Gd-LS) detector (1.8 m diameter) at \sim 30 m from a reactor core of the Taishan Nuclear Power Plant (4.6 GW) in Guangdong.
- By means of 10 m² SiPM covering the spherical LS, the **reactor antineutrino spectrum** will be measured with a sub-percent energy resolution ($\leq 2\%$ / \sqrt{E} MeV).







- **Electronics**
 - **In-detector**
 - > Discrete readout (ROMA TRE): 2 channels/SiPM tile
 - **Off-detector**
 - ➢ 6 uTCA.4 crates
 - Each crate has 12 slots and will be mounted with 11 Front-end **Electronics Controller (FEC) boards**
 - 9 FEC boards with 4 ADC FMC cards
 - » Each ADC FMC card supports 32 channels (ROMA TRE)
 - 2 FEC board with 3 ADC FMC cards and 1 WR FMC card
 - 1 spare slot is reserved for veto/ redundancy/backup/debugging

Total: up to 8064 ADC channels

- Each crate supports up to 1344 ADC channels _
 - $= 6 \times (9 \times 4 \times 32 + 2 \times 3 \times 32) = 6 \times 1344 = 8064$
- Note: project requirement is 8048 ADC channels



THANKS TO YOUR ATTENTION

Photon Counting Readout ASIC: BPIX





Chip architecture

- Pixel cells organized in array, connected in series, read out by shift chains
- Peripheral part
 - Config, control, data packaging & monitoring

Photon Counting Readout ASIC: BPIX





- Pixel cell:
 - Electrical signal amplified with a low noise amplifier, shaped through a shaper and then discriminated with an adjustable threshold
- Threshold setting:
 - Global DAC for the coarse threshold
 - In each pixel cell, local DAC for the fine threshold
- Once the amplified signal exceeds the threshold, the counter adds 1.

Photon Counting Readout ASIC: BPIX





Specs	BPIX-20	BPIX-40
Pixel size	150 µm X 150 µm	140 µm X 140 µm
Pixel Array	104 X 72	128 X 96
Thresholds	1	<mark>2</mark>
Gain	Fixed	2 bits tunable
Counting rate	> 2 Mcps	> 2 Mcps @ Med gain
Frame rate	1.2 kHz continuous	2 kHz continuous
Counting Depth	20 bit	14 bit



BPIX photon counting chips

• CMOS 130nm, 1P8M



Module Assembly Evolution



Module assembly was evolved in four generation of prototype systems:

- Indium bump used for the 1st, nice yield but low productivity
 - Low temperature in the full product flow was an issue
- CuSn bump for the 2nd, high productivity for mass production, and high temperature compatible
- TSV (Through Silicon Via) features added in the 3rd to eliminate the wire bonding for ASIC (not for sensor), for smaller module assembly gaps
 - But found long-term stability problem
- Back to CuSn bump for 4th, but with ASIC pin map optimization and advanced wire-bonding, the non-detectable area is even better than the TSV version



Advanced wire-bonding



Indium bump bonding module for the 1st prototype

CuSn bump bonding module for the 2th prototype



Bump bonding + TSV module for the 3rd prototype

J. Zhang et al 2020 NIMA 980 164425



CuSn bump bonding module for the 4th prototype after ASIC pin map optimization

<u>J. Zhang et al 2019 NIMA **958** 162488</u>

Bump Bonding & TSV Features





Cross-section view of a Bump Bonding +TSV 3D stack

ASIC Pin Map Optimization



- ASIC pin pitch: 100 um
- PCB pin pitch: 200 um
- ASIC pin map optimization
 - need to consider the fan-out limitation of the PCB
 - ➢ PCB via diameter: 200 um (8 mil)
 - ➢ Via gap: 400 um (16 mil)
 - Test pins and readout pins are interleaved
 - The test pin will not be used in the final product.



uFC Series Board



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uFC v2

- Xilinx Kintex-7 28nm 7K325T
 - 0.32 Million System Logic
 - 840 DSP
- PCle2.0 x4
- 8GB DDR3 800MHz SDRAM ECC
- (8+2)*10G High-Speed Serial Links



u4FC&P v1

- Kintex Ultrascale+ 16nm KU11P
 - 0.65 Million System Logic
 - 2928 DSP
- 4*PCIe4.0 x4 + PCIe4.0 x8
- 2*16GB DDR4 1200MHz SDRAM ECC
- 4*40G/100G High-Speed Serial Links



u4FC&P v2

- Kintex Ultrascale+ 16nm KU15P
 - 1.14 Million System Logic
 - 1968 DSP
- SAMTEC Firefly x3 + PCIe4.0 x8
- 2* 16GB DDR4 1200MHz SDRAM ECC
- 8*40G/100G High-Speed Serial Links

Name	Instance Specs					
	Status	FPGA	Memory	NVMe	PCIe BW	Network
uFC v2	Ready	7K325T	8GB	-	2 GB/s	10GbE
uFC&P v1	Ready	KU11P	2*16GB	4*(up to 4TB)	8 GB/s	40/100GbE
uFC&P v2	R&D	KU15P	2*16GB	-	8 GB/s	40/100GbE

FMC Cards

FPGA node

- **AMC+RTM boards** •
 - With various FMC cards node





FPGA node



Mini-WR FMC





QSFP28 x2

QSFP28 x2

ADC FMC board

- 16 single-end channels
- 125 MHz analog bandwidth •
- DC coupled analog input •
- 12/16-bit Σ - Δ ADC •
- Raw sample rate up to 2 GSps .



FPGA Firmware





- Config & monitor via UDP/IP
- Readout via TCP/IP

Key Parameters of the Pixel Detectors for HEPS and SHINES

	HEPS BPIX-6M	SHINE STARLIGHT
Mode	Photon counting readout	Charge-integration
Pixel size	140 µm x 140 µm	100 µm x 100 µm
Total pixel	5.9M	4.2M
Modules	40	16
ASICs per module	6 x 2	8 x 2
ASIC Pixel Array	128 x 96	128 x 128
Data length per pixel	28 bit	13 bit
Total detectable area	403.2 mm x 286.72 mm	204.8 mm x 204.8 mm
Frame rate (Max.)	1 kHz	12 kHz
Peak data rate from electronics to DAQ	165.2 Gbps	654.3 Gbps