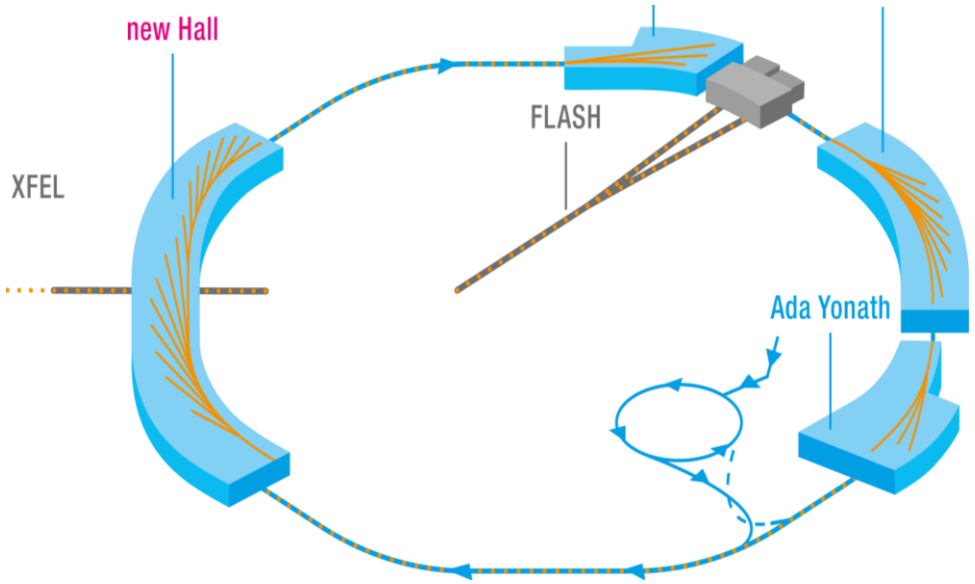
PETRA IV.
NEW DIMENSIONS

DAMC-X3TIMER

Update of the development

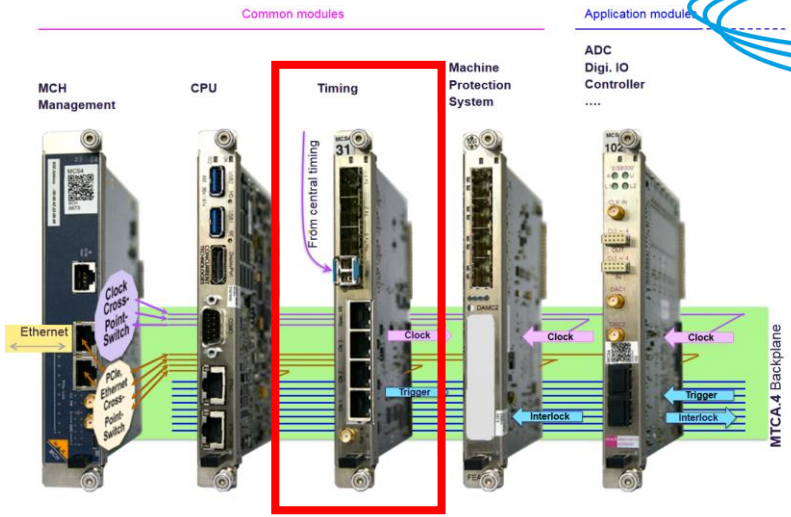
Hendrik Lippek *in behalf of the PETRA IV Timing & synchronisation project team (WP2.09)*
Hamburg 07.12.2023

PETRA IV Overview



PETRA IV Highlights

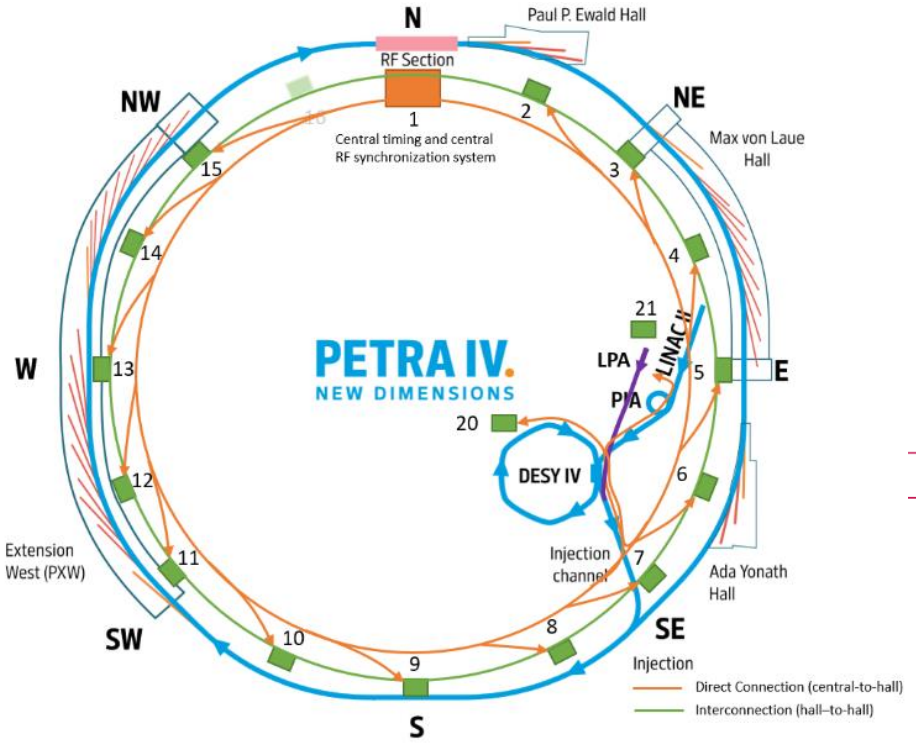
- 4th Generation Light source
- low emittance: hor. 10-30 pm rad, vert. < 10 pm rad
- 500 MHz + 1.5 GHz RF
- timing / brightness mode: 80 / 1600 Bunches
- Injector chain with
  - LINAC II, PIA + (new) DESY IV booster synchrotron
  - LPA for 6 GeV “Moonshot“ into PETRA IV option
- 30 Beamlines in 4 Experimental Halls

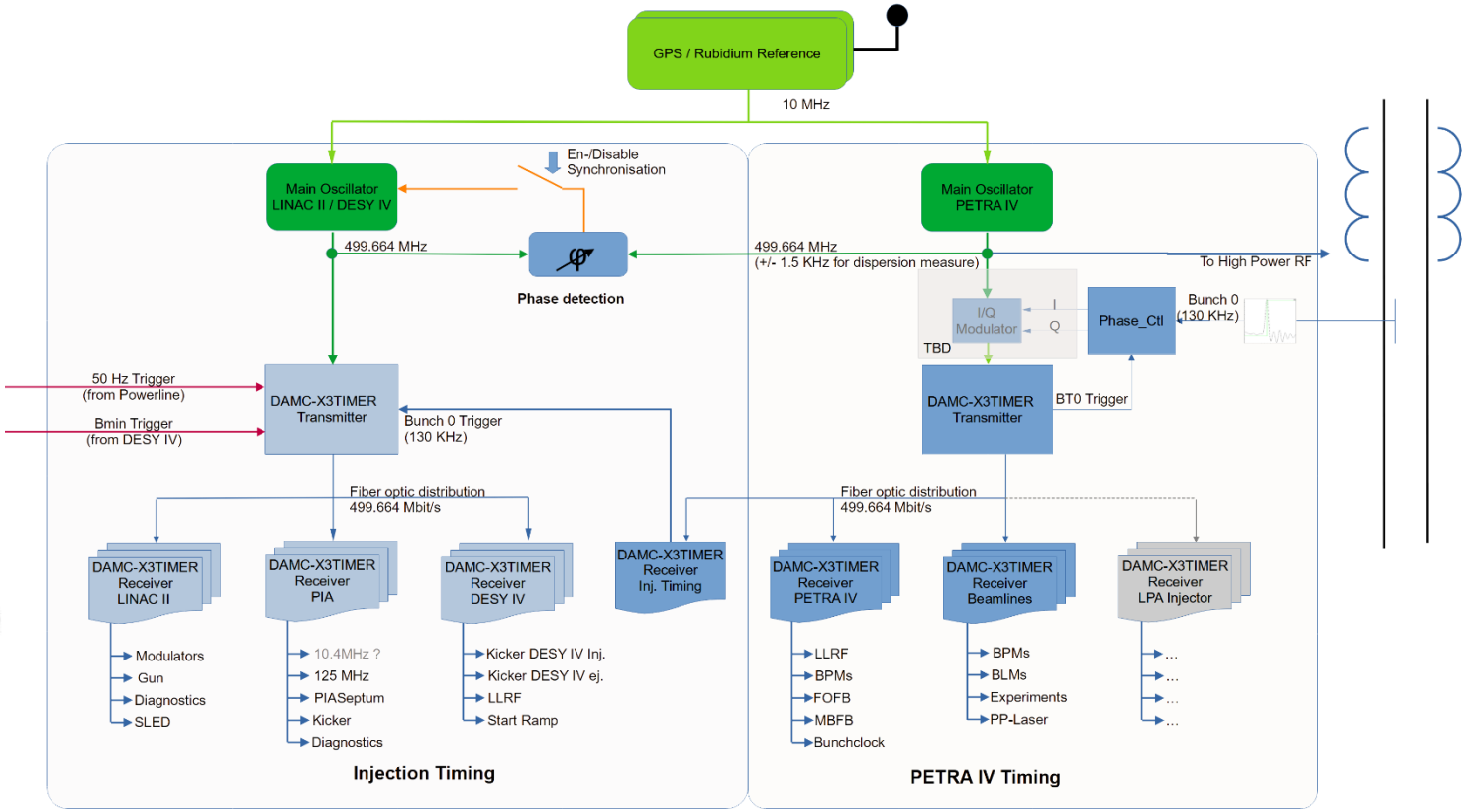


Timing System development for PETRA IV

- **MicroTCA.4 components will replace existing PETRA III hardware** for controls and diagnostics
- A **new MTCA based timing distribution** hardware replaces the old system based on VME, SEDAC, 19” standards
- **Make use of experience from well-established Timing System concepts** as utilized at the FLASH and European XFEL facility
- **Keep the design flexible** to enhance functionality during life-cycle of PETRA IV

Timing and Synchronization System Design





Key Requirements

- Distributing a continuous RF reference signal
- Provide low jitter clocks (e.g. for ADC sampling)
- Provide continuous timing signals & trigger events
- Provide beam-synchronous data as:
  - Timestamp / revolution counter
  - Beam mode / bunch pattern
  - bunch currents

- Common hardware for timing transmitter and receiver
- Dedicated fiber optic distribution with drift compensation
- Common timing system for accelerator and beamlines

DAMC-X3TIMER Block Design

Front Panel

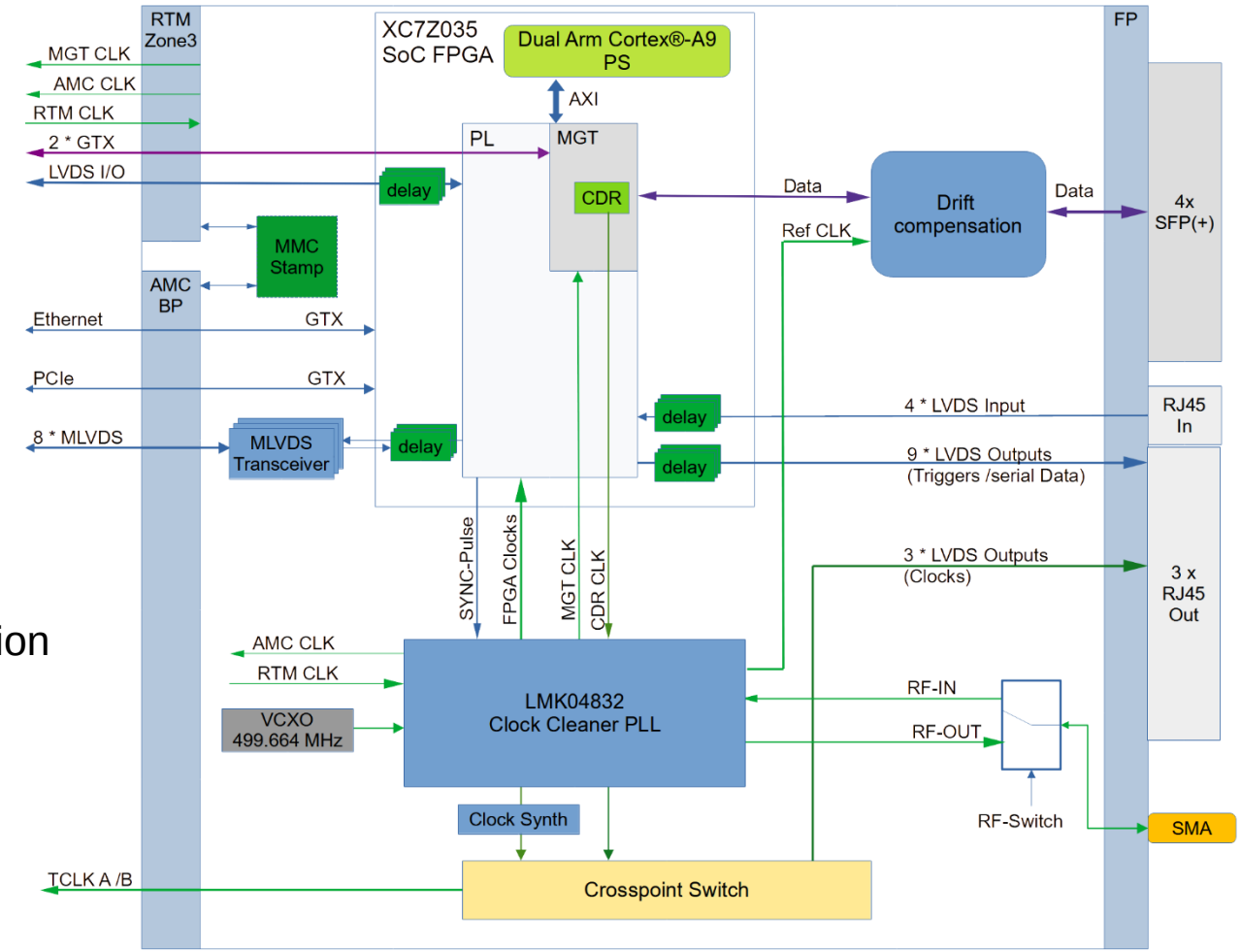
- SFP - timing signal distribution
- SMA - RF-Input / RF-Output
- RJ45 - LVDS Out (Triggers, CLK, Data)
- RJ45 - LVDS In (Sync signal, Trigger)
- USB - Debug/JTAG

AMC - Backplane

- PCIe - Communication to MTCA-CPU
- Ethernet - For Zynq SoC PS
- TCLK A/B - clock distribution
- Port 17-20 - M-LVDS - Trigger/Clock/ Data distribution
- IPMI to MMC - Management, Firmware update

RTM Zone 3 (Class D1.1)

- MGT lanes - timing signal distribution
- LVDS - Trigger / Clocks / Data
- SPI / I2C - for peripherals configuration



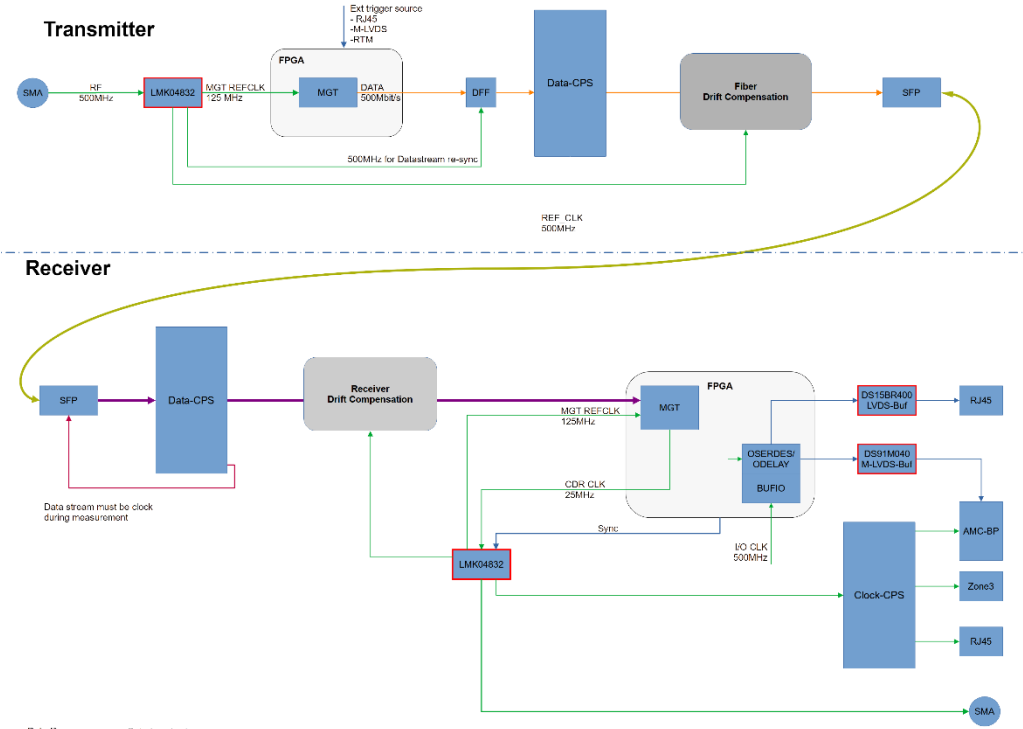
Transmitter – Receiver concept

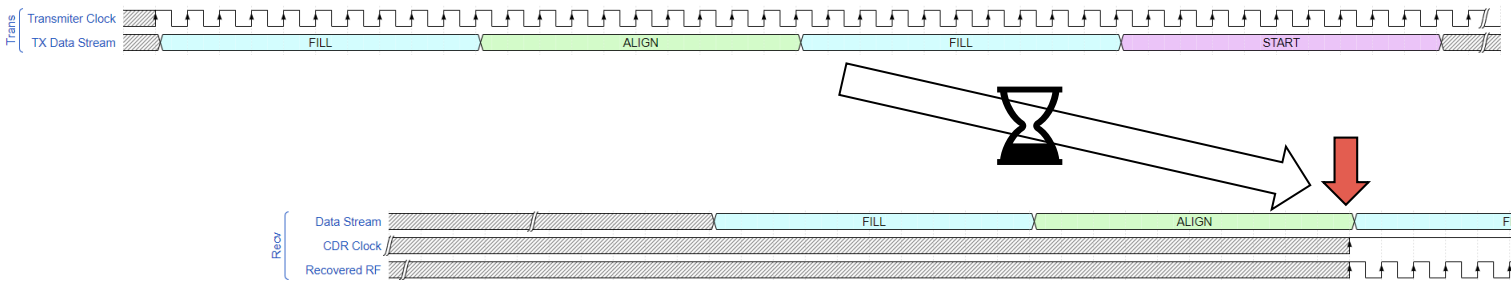
Transmitter

- Generates RF synchronous Datastream
- Encodes timing information into data frame
- Aligns Datastream (K28.5) to the beam (Bunch 0 marker)
- 8B/10B extended transmission over MGT transceivers
- Active drift compensated distribution path

Receiver

- Recovers Clock from Datastream in MGT
- Jitter Cleans CDR Clock with dual loop PLL
- Alignment:
  - Decodes Alignment characters (K28.5) in the data
  - Align LMK04832 output Clock phases
- Distributes RF derived divider clocks
- Delivers decoded Trigger signals





Timing Data Frame @~500 MHz (3840 bits x ~130.1 kHz)

	Bit Number 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	REV. NUM. [7:0]								K28.5								Channel A
1	REVOLUTION NUMBER [23:8]																
2	REVOLUTION NUMBER [39:24]																
3	GLOBAL COMMANDS [7:0]								REV. NUM. [47:40]								
4	MACHINE STATUS [7:0]								MPS DATA [7:0]								
5	BEAM CRT. MPS [7:0]								BEAM MODE [7:0]								
6	BEAM CRT. LIFETIME [6:0]								BEAM CURRENT MPS [16:8]								
7	BEAM CURRENT LIFETIME [22:7]																
8	SPARE BITS [13:0]															[24:23]	
9	K28.0 (SOB)								DATA BLOCK ID [7:0]								Channel B
10	DATA BLOCK LENGTH [15:0]																
11	TIMING DATA [15:0]																
...	. . .																

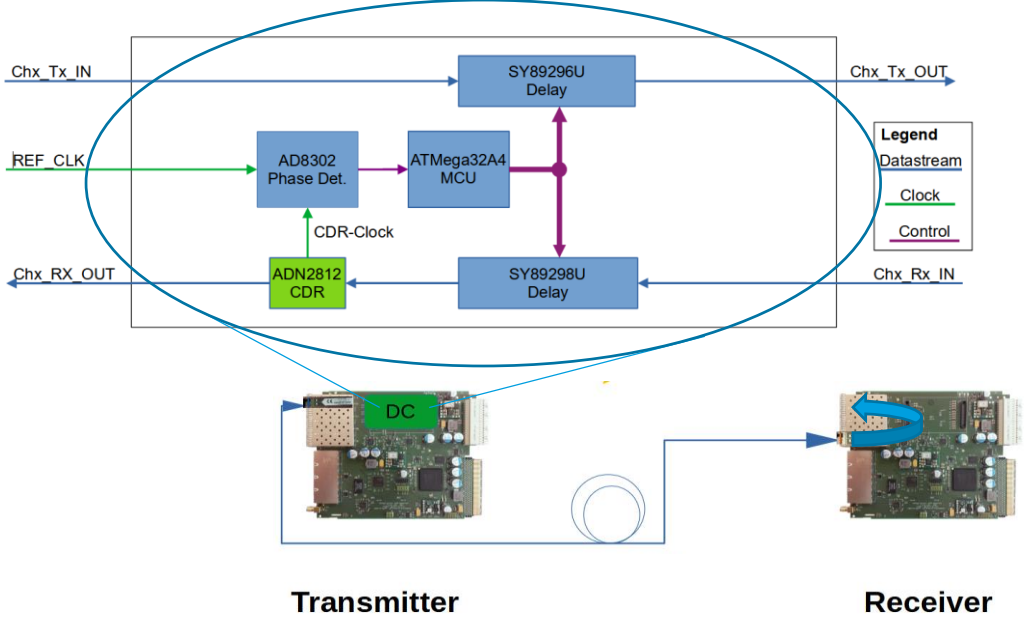
16-bit Word Number

Courtesy of V. Andrei

Transmitter: Fiber Drift Compensation

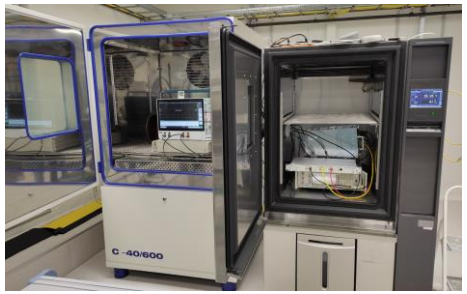
Active drift compensation on Transmitter side

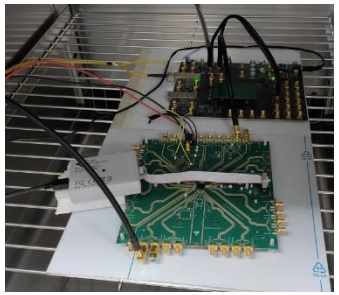
- Detect phase differences between local reference and recovered clock from looped back data stream
- Sets delays to keep the phase relation constant
- separate module option to keep Receiver BoM cost low
  - receivers or applications with no critical drift requirements



Drift stability tests with x2timer hardware

Environmental chamber tests were used to investigate clock and trigger signal drifts over variation on temperature and humidity. Two aspects were investigated:





Drifts on optical fiber and active drift compensation

- Test setup
  - 2 x2timer Transmitter & Receiver
  - 1 km of optical fiber as signal path
  - Standard SFP Transceiver
  - vs. wavelength multiplexing BiDi SFP Transceiver

Tests	Drift (over 1 km)
No compensation	250 ps/°K
Standard SFP (2 fibers) 1310 nm	15 ps/°K (due to not identical fiber lengths)
BiDi SFP (one fiber) Tx 1310 nm, Rx 1490 nm	5 ps uncertainty (no drift over temperature)

Receiver: Active Drift Stabilization

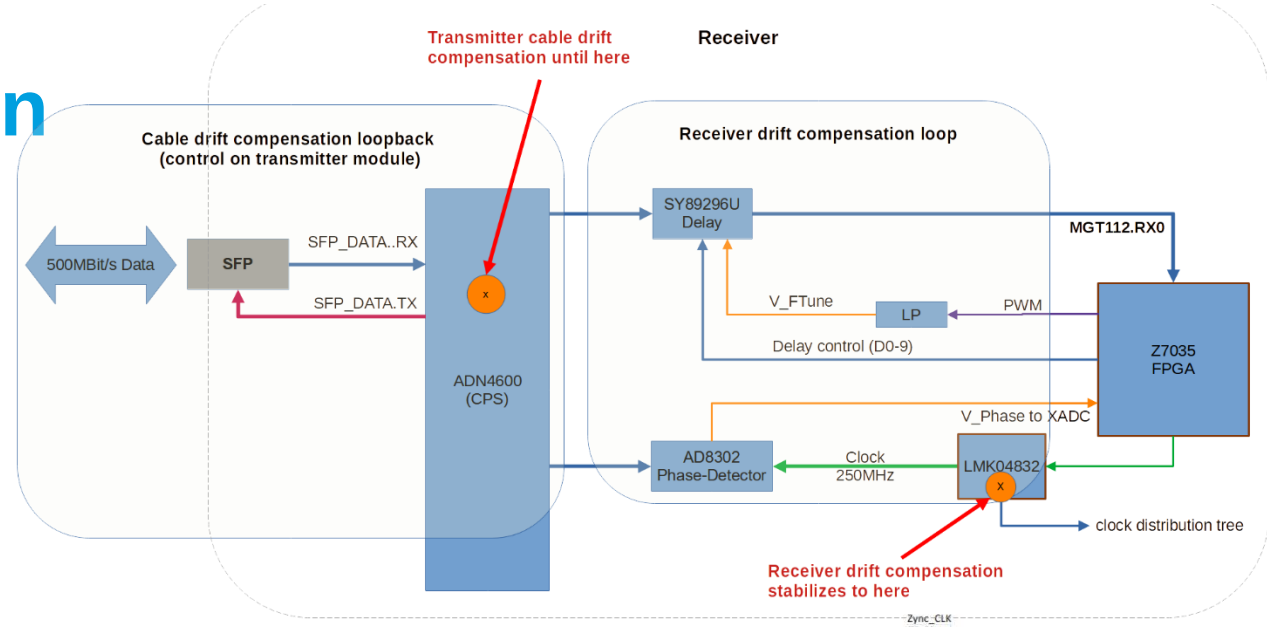
Why do we need more stabilisation?

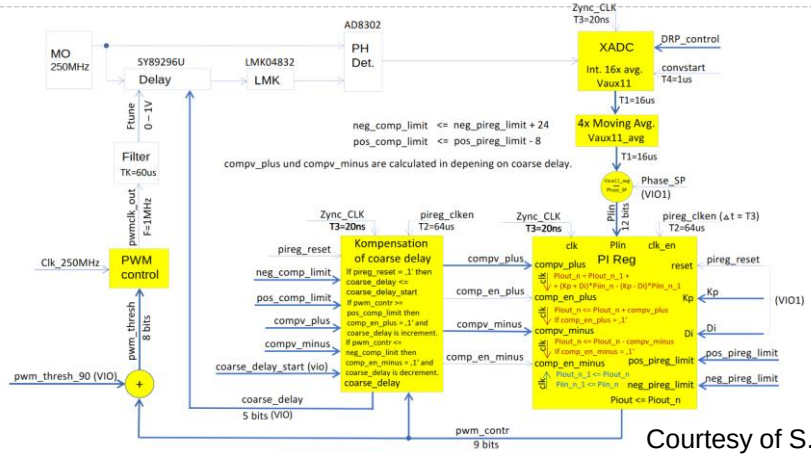
- Thermal drifts in the compensation loop are compensated well
- There is still **drift in the out of loop components**
  - Dividers /Crosspoint-Switches /FPGA
- Temperature changes by MTCA **Fan activities** have a big influence on AMC temperature and component drifts

What can we do?

- Room / Rack / Crate level
  - temperature & humidity controlled electronics room
  - Use (water)-cooled Racks
  - Set Crate to **steady air stream** configuration

- PCB level
  - Reduce amount of critical components
    - LMK04832 contains also divider, delay and multiplexer
    - Cleaned up clock and data distribution path
  - **Receiver drift compensation**
    - Compensates drift in FPGA CDR and clock cleaner
  - Optional on board temperature regulation
    - Control temperature of critical IC components
    - Local FET based heating loop





Courtesy of S. Ruzin

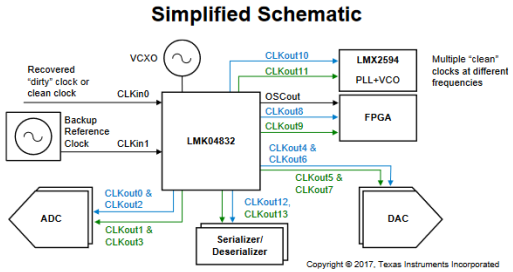
Clock jitter cleanup

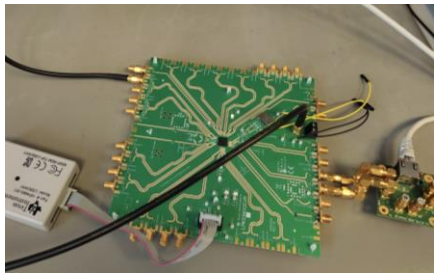
Clock Cleaner (TI LMK04832)

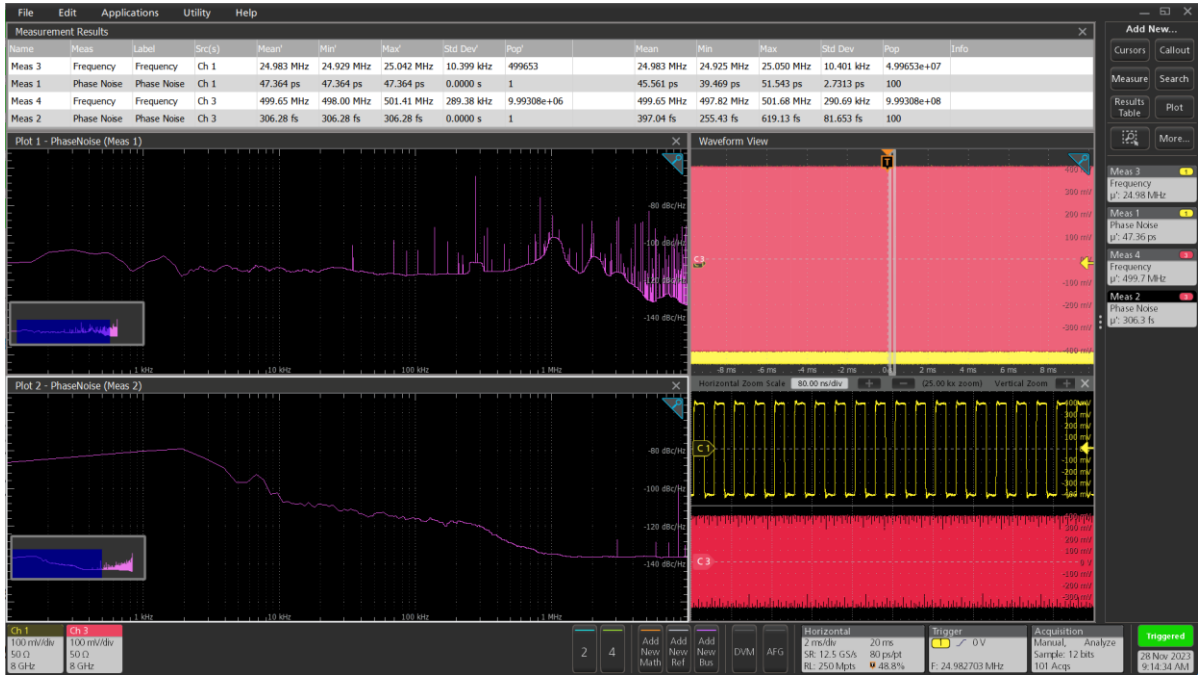
- Dual loop PLL
  - PLL1: custom VCXO (KVG V7221-EP-LF)
    - PETRA: 499.6643 MHz +/-100 ppm
    - Can be customized to Acc Frequencies
  - PLL2: internal VCO
- 3 Clock inputs (RF, CDR, Aux)
- internal output dividers
- Digital output delays
- programmable output levels (LVDS, LVPECS, CMOS,..)

Test Setup

- RF-Generator (R&S SMA100A)
- Transmitter: DAMC-FMC1Z7IO (With SFP-FMC)
- Receiver: Trenz TE0745 Evaluation board
- Fiber connection:
  - 1 KM single mode
  - BiDi SFP Modules Tx 1310 / Rx 1490 nm
- 50 GS/s Oscilloscope with Jitter & phase noise analyzer







Option	Description	Phase noise*
No jitter cleaner	Clock from CDR	45 ps
Single loop	LMK04832 internal VCO only	1-3 ps
Dual loop	custom VCXO and internal VCO	397 fs

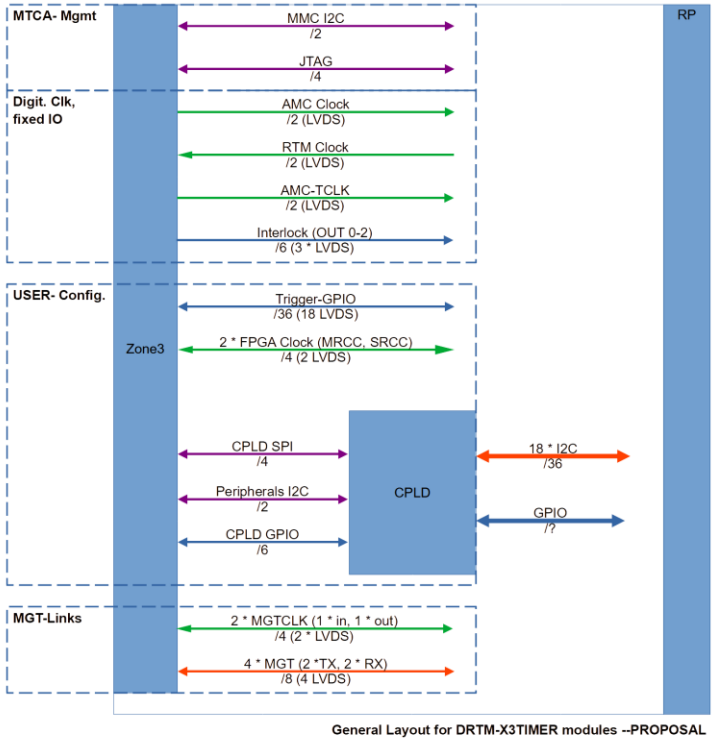
*100 Hz – 10 MHz

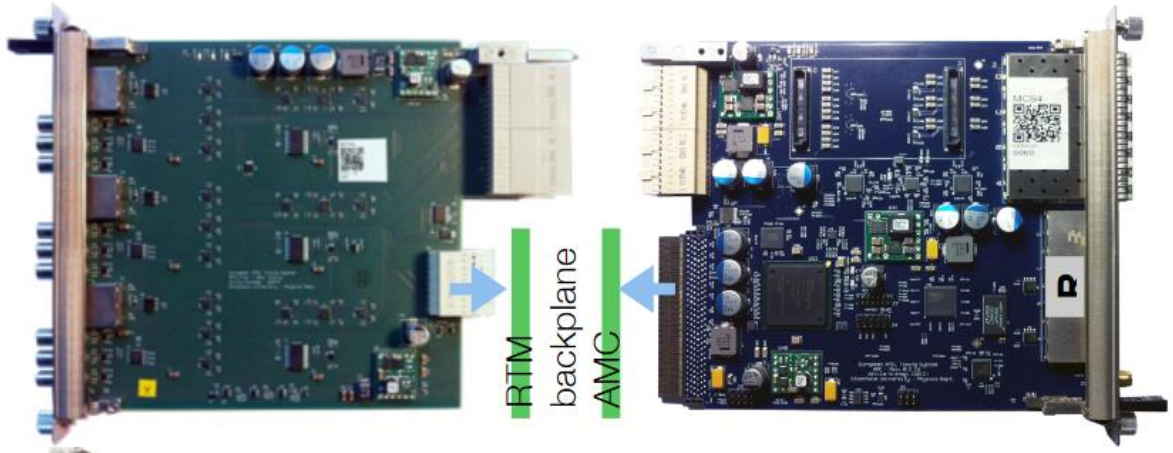
RTM Interface

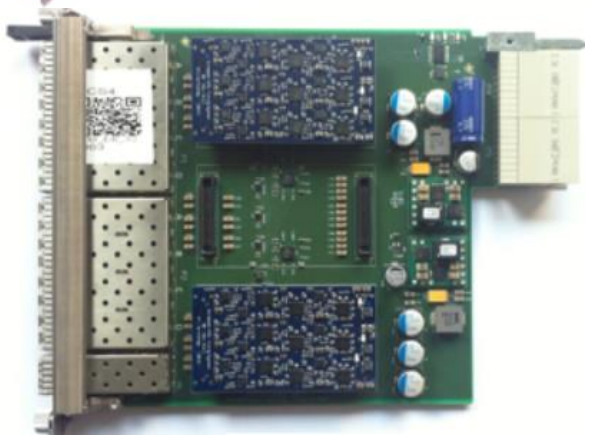
Zone 3 (RTM-Connector)

RTM Class D1.1

- 3 Clocks (AMC- /TCLK out, RTMCLK in)
- 18 Trigger outputs
- 2 FPGA Clocks (Clock capable I/O)
- SPI / I2I / GPIO / JTAG
- 2 MGT (TX, RX, REFCLK)







RTM types

- Rear panel interfaces
  - LEMO
  - SMA Clock output (with LNA)
  - LVDS
  - Optical
  - NIM?
- RF-Backplane interface
  - Clock distribution
- Functional
  - Programmable delay line
  - SFP Fanout module

Pictures from x2timer RTM modules

Summary

Improvements in the DAMC-X3TIMER design:

- **Jitter reduction** by using a clock cleaner
- **Better drift stability**
  - Usage of BiDi SFP/SFP+ transceivers
  - Receiver drift compensation
  - Thermal stabilization of board components

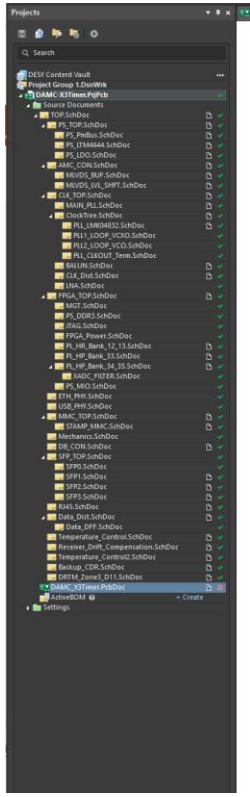
- **Enhanced onboard processing capabilities**
  - Real-time bunch delay calculation
  - Local control servers
  - Flexible configuration of peripherals

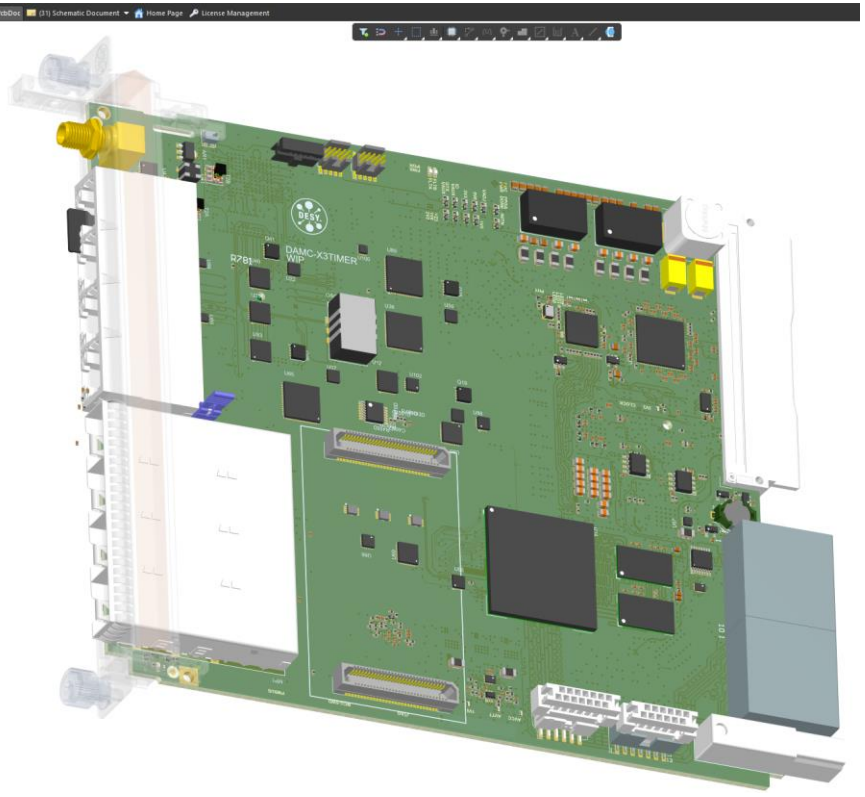
- More flexibility by the use of in-house s**oftware & firmware framework solutions**
  - Interfacing to various **control systems**
  - **Modular firmware** for easy portability

DOOCS.

ChimeraTK

FWK FPGA firmware framework





Schematics

- 48 Pages of schematics compete

PCB

- Board shape designed
- Connectors placed
- Main components placed
- FPGA SoC and peripherals routed
- Power supplies placed and routed

Production

- Components checked for availability
- Main components ordered & stocked
- In contact with assembly companies
- First Prototype production planned in early 2024

PETRA IV.
NEW DIMENSIONS

Thank you for your attention!

Contact

DESY. Deutsches Elektronen-Synchrotron

www.desy.de

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MSK

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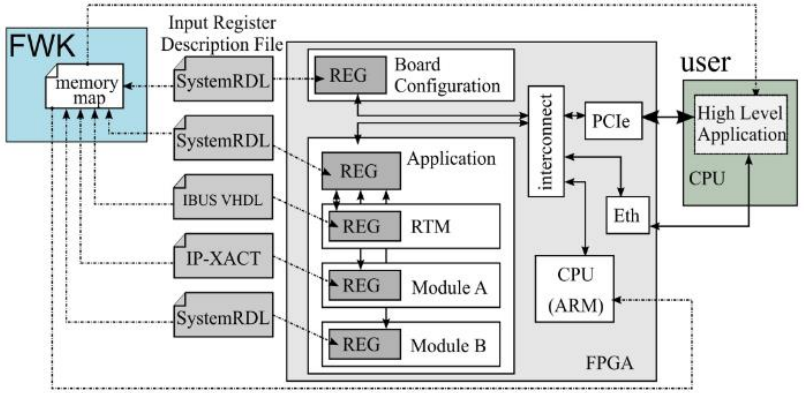
Backup

Firmware Framework & software interface

MSK firmware framework

- Generic framework for various (Xilinx) FPGAs
- Maintained by MSK firmware group
- Register maps for software interface
- Supports also ARM core interface for SoC devices

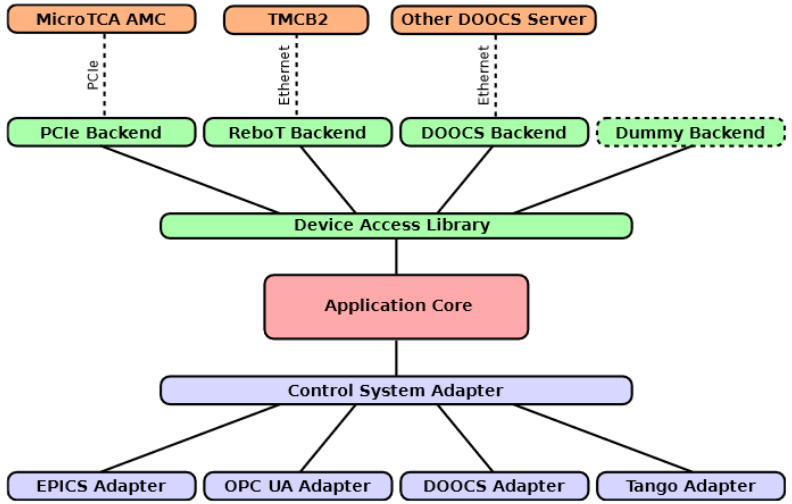


REDMINE
MSK project management tool

MSK GitLab

Application Core / ChimeraTK software layer

- Middle layer to abstract hardware and control system
- Supports multiple controls systems
- Uses Xilinx xdma driver to access FPGA via PCIe
- Support to run on (Zynq) ARM cores in preparation
- Public available: https://github.com/ChimeraTK



Tutorial: from Martin Killenberg
From Tuesday!

Jenkins