MicroTCA Module Management with DMMC-STAMP

Overview & recent developments

Patrick Huesmann (DESY) 2023-12-07



12th MicroTCA Workshop for Industry and Research, Hamburg

DMMC-STAMP overview

DESY - MSK | MicroTCA Module Management with DMMC-STAMP| 2023-12-07

Overview MicroTCA MMC

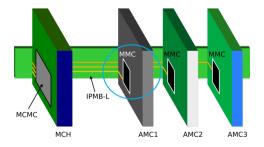
Management in MicroTCA

 On MCH side: MicroTCA Carrier Management Controller (MCMC)

 On AMC side: Module Management Controller (MMC)

Responsibilities of MMC

- IPMI protocol handling
- FRU information (AMC, RTM, FMCs)
- AMC payload management (FPGAs/SoCs)
- RTM control (hot-plug)
- Monitoring (temperatures, voltages, currents) Event handling (thresholds, alerts)



Overview DMMC-STAMP

- DESY's drop-in solution for AMC MMC
- Used at DESY for internally developed AMCs
 - hin production:

DAMC-FMC2ZUP DAMC-FMC1Z7IO DAMC-DS812ZUP DAMC-MOTCTRL



DAMC-UNIZUP DAMC-DS5014DR DAMC-X3TIMER

- Used by several customers in research and industry
- Interoperability tested with various MCHs (NAT, Vadatech)

MMC MMC MCMC мсн AMC1 AMC2 АМСЗ

DMMC-STAMP System on a Module

DMMC-STAMP ecosystem

System on Module (SoM)

- 25.5 x 29.5 x 2.3 mm
- Pre-programmed firmware
- Evaluation board available (BoB)

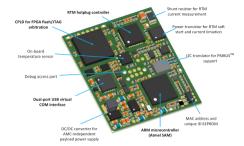
Software Development Kit (SDK)

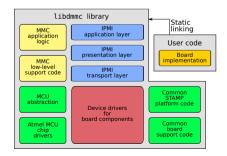
MMC firmware customization

- DESY MMC Software Library (libdmmc)
- Example implementations (BoB, DAMC-FMC2ZUP)

Open Source Tools and Templates

- AMC and RTM Altium Designer Templates
- mmcterm: serial over IPMB
- bin2hpm: create HPM files for IPMI upgrade
- frugy: read and write FRUs
- cpld-img-tools: bitstream conversion for Lattice CPLDs





Recent developments & special features

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FMC sensor integration

- Some FMCs dissipate lots of heat, requiring extra cooling
- To monitor their temperature and control cooling on demand, local temperature sensors are needed → FMC-local temperature sensors need to be integrated into IPMI monitoring
- But we don't want to change the MMC for every new FMC module

FMC sensor integration

- Some FMCs dissipate lots of heat, requiring extra cooling
- To monitor their temperature and control cooling on demand, local temperature sensors are needed → FMC-local temperature sensors need to be integrated into IPMI monitoring
- But we don't want to change the MMC for every new FMC module
- Solution: ANSI/VITA 57.1
 I2C Device Definition FRU record
- FRU record encodes a "device name" and a I2C address
 - MMC implements a lookup table from device name to sensor driver
 - MMC parses device name and address, then reads the sensor and exposes its reading to IPMI

 \rightarrow MMC only needs to know the particular sensor, not the particular FMC

Field	Byte Offset	Bit Location	Length	Description
Subtype	0	7:4	4 bits	1 for I2C device definition subtype
Version	0	3:0	4 bits	0 for current version
Device String	1N/8		N bits	Device address / name strings, see below

Table 9. Subtype 1: I2C Device Definition (variable length and optional)

The device string portion of this MultiRecord subtype consists of 6-bit ASCII text as defined in the ISD. The string is divided into one or more 12C device records. Each device record consists of one or more address characters followed by one or more bytes of device name.

From FMC standard (ANSI/VITA 57.1)

Example: Atom Computing DAC FMC

AMC-FMC2ZUP@0x7E_MMC>fru_ RU #0:		show_sens r Informa					n MCH ca	insole
roduct info: DESY/CAEN ELS DAMC-FMC2ZUP-11EG								
S/N 22Y23W0632 P/N DAMCFMC2ZUP1	#	SDRType	Sensor	Entity	Inst	Value	State	Name
Version revB								
Board info: DESY/CAEN ELS DAMC-FMC2ZUP-11EG	-	MDevLoc		0xc1	0x67			DAMC-FMC2ZUP-11E
S/N 22Y23W0632 P/N DAMCFMC2ZUP1	Θ	Full	0xf2	0xc1	0x67	0x01		AMC Hot Swap
Mfg.Date 2022-09-27 10:17:00	1	Compact	0x0b	0xc1	0x67	0x00		0x00 682719B5F5E3
dule current requirements: 6.5A	2	Full	Temp	0xc1	0x67	30.0 C	ok	STAMP Temp
ne3 interface compat: Class D1.1	3	Full	Voltage	0xc1	0x67	3.360 V	ok	AMC MP 3V3
	4	Full				12.32 V		AMC PP 12V
U #1:	5	Full	Current	0xc1	0x67	0.000 A	ok	I_RTM MP 3V3
t present	6	Full	Current	0xc1	0x67	0.00 A	ok	I_RTM PP 12V
	7	Compact	0x14	0xc1	0x67	0x01		0x00 CPLD Done
U #2: This is FMC1 on the FMC carrier	8	Compact	0x14	0xc1	0x67	0x00		0x00 RTM MP 3V3 PG
oduct info: N/A	9	Compact	0x14	0xc1	0x67	0x00		0x00 RTM PP 12V PG
Board info: Atom Computing, Inc. Opus DAC	10	Compact	0x14	0xc1	0x67	0x00		0x00 RTM Fault
S/N 2 P/N Opus-DAC-revA	11	Compact	0x14	0xc1	0x67	0x01		0x00 PGood_A
Mfg.Date 2022-05-18 18:02:00	12	Compact	0x14	0xc1	0x67	0x01		0x00 PGood_B
Load P1_12P0V: 12V (min 11.4, max 12.6) ~0mV, min 0mA / max 1000mA	13	Compact	0x14	0xc1	0x67	0x01		0x00 FPGA1 Init
Load P1_3P3V: 3.3V (min 3.12, max 3.46) ~0mV, min 0mA / max 100mA	14	Compact	0x14	0xc1	0x67	0x01		0x00 FPGA1 Done
Load P1_VADJ: 2.5V (min 1.8, max 3.3) ~0mV, min 0mA / max 100mA	15	Compact	0x14	0xc1	0x67	0x01		0x00 FPGA2 Init
Output P1_VREF_B_M2C: 0 -0+0V ~0mV, min 0mA / max 0mA	16	Compact	0x14	0xc1	0x67	0x01		0x00 FPGA2 Done
Output P1_VREF_A_M2C: 0 -0+0V ~0mV, min 0mA / max 0mA	17	Full	Temp	0xc1	0x67	37.5 C	ok	Inlet Temp
Output P1_VIO_B_M2C: 0 -0+0V ~0mV, min 0mA / max 0mA	18	Full	Temp	0xc1	0x67	37.5 C	ok	Outlet Temp
C size: single, clock dir: m2c, TCK max clock: 64	19	Full	Temp	0xc1	0x67	37.0 C	ok	LTM4630 Temp
P1: lpc, num signals: A 68, B 0, num Gbt trcv: 0	20	Full	Temp	0xc1	0x67	39.0 C	ok	LTM4650 Temp
P2: lpc, num signals: A 0, B 0, num Gbt trcv: 0	21	Full	Temp	0xc1	0x67	41.0 C	ok	LTM4633_F Temp
C I2C device definition:								
AT30TS75A, addrs: 9 (0x48) FMC1 has an AT30TS75A sensor at PC address 0x48	30	Full	Voltage	0xc1	0x67	1.7856	V ok	VCC_Vadj
	31	Full	Voltage	0xc1	0x67	1.1904	V ok	VCC_1V2
J #3:	32	Compact	0x14	0xc1	0x67	0x01		0x00 Opus DAC PG_M2
oduct info: N/A		Full	Temp	0xc1	0x67	35.0 C	ok	Opus DAC AT30TS7
Board info: CAENELS FMC-4SFP+	34	Compact	0x14	0xc1	0x67	0x01		0x00 FMC-4SFP+ PG_M
S/N 17006 P/N F	35	Compact	0xf0	0xc1	0x67	0x10		HS 011 AMC7
Mfg.Date 2015-06-10 00:00:00								

The FMC temperature is fully integrated into MTCA management

PMBUS multi-chip configuration

- On complex boards with lots of power rails, a lot of power management logic is required
- Example DAMC-MOTCTRL:
 - 2x LTC2979 (PMBUS manager for ext. DC/DCs)
 - 1x TPS40425 (PMBUS controller for ext. MOSFETs)
 - 2x TPS65400 (PMBUS PMU with int. MOSFETs)
- 3 different Windows applications and 3 different programming adapters needed, just to configure the PMBUS chips...
 - Analog Devices LTpowerPlay & DC1613A
 - Texas Instruments Fusion Digital Power Designer & USB2ANY
 - Texas Instruments PI-Commander & USB-TO-GPIO2



Programming adapters needed for power managers on the DAMC-MOTCTRI

Conversion script for PMBUS project files

nl version="1.0" encoding="utf-8"?> "LTpowerplay" Project File	
chip addr7bit="0x5C" modelnum="LTC2979" moduleIndex="0" subModuleIndex="0"	_
<global> <reg cmd="8x8010" hex="0x00" len="1"></reg></global>	
<reg cmd="0x0035" hex="0xD280" len="2"></reg>	/
<pre>step cnd= <?xnl version="1.0" encoding="UTF-6"?></pre>	
<reg crd="<P1-Convander" tp505408="" version='1.0"'></reg>	
<pre>«Reg cnd=</pre>	
<pre>rda crda (register code="D1">0000(/register)</pre>	
energy cregister code cregister keg credister credister credister keg credister credister credister	
<pre><reg cmd="</pre"></reg></pre>	
<reg 1<="" <="" <registern="" cwda="" regions="" resions="" td=""><td></td></reg>	
<pre>chas crediter viewstampzozziniaaminingia, appendater index intercampzozziniaamini company intercompany index index intercompany index intercompany index intercompany index intercompany intercompa</pre>	
ang cod «register» devices/seas instruments roston vigitat romer besigner viriato [2021-10-0]/vireator/	
and segisters approximate and a second and a second and a second as a second a	
<pre>kmg cnds <registers <hdocss="" partup<br=""><reg <hdocss="" <registers="" cnds="" partup<br=""><reg <li="" <registers="" cnds="">didress/partup <lidocs <="" li="" solutions=""></lidocs></reg></reg></registers></pre>	
Reg cruis <registers <i.s.urritheeratser="" is_urritheera<="" td=""><td></td></registers>	
<reg <register#="" <saved="" cmd#="" in="" mode="" offline="">false</reg>	
<registerk saved_white_www.write_rendingsrates="" saved_white_www_write_rendings<="" td=""><td></td></registerk>	
<register* <package="">6</register*>	
<registers a="" an="" an<="" and="" enditional="" second="" td=""><td></td></registers>	
eregisters endowerers the	
<t09v0ut_m00e< t0=""> </t09v0ut_m00e<>	
<idandcode>VOUT_MODE [0x20]</idandcode>	
<pre><valuetextbexp =9<="" valuetext=""> </valuetextbexp></pre>	
<pre><parametertype>Custom</parametertype></pre>	
<parametercategory>Configuration</parametercategory>	

\$ hexdump	-C	pri	ous.	_C0	nf.l	otn											
0303030303	60	4e	85	۶c	4c		43	32	39	37	39	60	08	60	68	60	.N.\LTC2979
								39		39	00	60	00			03	^LTC2979
80808020		09					30				08	60					TPS40425
														60			1TPS65400L1
80808040							30	30	08	60	08		08			80	TPS65400
80808050	61		10	12	10	68			d2	80		36	d2	40		4f	a\56.@.0
00080608	eb	48		50	80				30			80	08				I.H.PO.O.RS.
80808070	80						d3								88		j
08080808														60			
00000000	60	68		b 4	60	08				4b			08			dS	
	0f	12	d6	68	12	d7	0f		d8	60	12	d9	88	12	da	60	
808080b0		db										20			80	60	
808080c0			80	68									88		68		
00000000				02													ls3.\$y%x
808080e0					78		48					80			7b	d7	&mp.g~AB{.
				8f						45			5e	6e	97		.CjDgEG.^n
80808180					60	ba	60			db					88		10
80808110	63	88			0a			b1	88	66		b 3	88	60		de	[cd

/libdnnc/tools/pmbus conv.pv motctrl power manager all ok r2.proj \ tos48425 A9h AV8Strimmed rc1 xml \ tos65480 device1 69h, xml 0x69 \ tps65480 device2 6Ch.xml.0x6c \ -o pmbus_conf.bin Parsing motctl power_manager_all_ok_r2.proj... Converting a LTC29xx configuration file ound LTC2979 at 0x5c Writing page section 0x00 Writing page section 0x01 Writing page section 0x02 Writing page section 0x03 Writing page section 0x04 Writing page section 0x05 riting page section 0x06 riting page section 0x07 und LTC2979 at 6x5e vriting page section 0x00 writing page section 0x01 vriting page section 0x02 Writing page section 0x03 Writing page section 0x04 Writing page section 0x05 writing page section 0x06 Writing page section 0x07 Parsing tps40425 09h 0v85trimmed rc1.xml... onverting a TPS40425 configuration file TI file detected: Texas Instruments Fusion Digital Power Designer v7.7.1.0 [2021-10-01] found TOCARATE at ByRG Writing page section 0xff Writing page section 0x00 Writing page section 0x01 Parsing tos65480 device1 69h.xml... onverting a TPS65400 configuration file for device at 0x69 writing page section 0x03 Writing page section 0x02 writing page section 0x01 writing page section 0x00 Parsing tos65480 device2 6Ch.xml... onverting a TPS65400 configuration file for device at 0x6c Writing page section 0x03 Writing page section 0x02 Writing page section 0x01 vriting page section.0x08

Writes binary blob containing device list & register contents, to be linked into DMMC-STAMP firmware

PMBUS configuration from DMMC-STAMP

Now the MMC configures the whole zoo of PMBUS chips with one CLI command

- No more fiddling with 3 different HW / SW tools
- Saves time & effort during production / development
- Less error prone
- Build system can directly read project files of PMBUS config tools
- PMBUS project files become part of the versioned MMC source tree
- PMBUS config is in a known state across all DAMC-MOTCTRL boards and can update with new MMC version

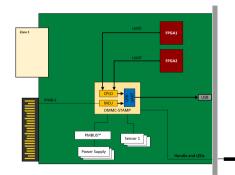
DAMC-MOTETRL@0x7C_MMC>pmc_write aiting for PSM 0x5c shutdown... aiting for PSM Ax5e shutdown.... rite chin at 0x5c TC29xx device detected at 8x5c: 8x8061 rite globals Vrite page 0 rite page 1 rite page 2 Irite page 3 rite page 4 Irite page 5 rite page 6 rite page 7 rite for #0 (LTC2979) successful tore chip at 0x5c TC29xx device detected at 0x5c: 0x8061 tore for #0 (LTC2979) successful cite chin at Av5e TC29xx device detected at 0x5e: 0x8071 write globals rite page 0 rite page 1 rite page 2 rite page 3 rite name / rite page ! Write page 6 rite page 3 rite for #1 (LTC2979) successful TC29xx device detected at 0x5e: 0x8071 tore for #1 (LTC2979) successful rite chin at 0x09 PS40425 device detected at 0x09: 0x00c rite name 255 rite page 0 tite name f rite for #2 (TPS40425) successful tore chip at 0v09 PS40425 device detected at 0x09: 0x00c Store for #2 (TPS40425) successful cite chip at 0x69 PS65400 device detected at 0x69: 0x00f

Remote console with Serial-over-IMPB

For serial console access we have USB-UART on the front panel. But how to access the serial console remotely?

- Serial-over-IMPI would require MMC connected to Ethernet directly
- ► But in MicroTCA, Ethernet is part of payload, not management → DMMC-STAMP has no Ethernet connection, only IPMB(I2C)

- UART implemented on DMMC-STAMP CPLD
- Custom IPMI protocol for serial port forwarding (Serial-over-IPMB)
- Open source tool: mmcterm
- Support for 3 channels (MMC, FPGA1, FPGA2)



Remote console with Serial-over-IMPB (example)

MCH URLIPMB addr

\$ mmcterm mskmchscav2 0x7c - List channels channel 0: WWC Console channel 1: MPSoC Console channel 2: Kintex-7 Console

\$ mmcterm mskmchscav2 0x7c -c 0 Open channel 0 (MMC) Press Ctrl-x to exit DAMC-MOTCTRL@0x7C MMC>v App. version + V2.01 Build host, date: msktechjenkins.desy.de, 2023-03-29T11:15:41Z Compiler version: 10.2.1 20201103 (release) Library version : V2.08 Build host, date: msktechienkins.desv.de, 2023-03-29T11:15:41Z Compiler version: 10.2.1 20201103 (release) IPMI version : 1.5 Vendor ID : 0x053F Product ID : 0x0710 Board DAMC_MOTCTRL STAMP revision : Rev. A STAMP LITD • 801E1234DD71 Copyright (C) 2022 Deutsches Elektronen-Synchrotron (DESY) DAMC-MOTCTRL@0x7C MMC>#

\$ mmcterm mskmchscav2 0x7c -c 1Open channel 1 (MPSoC)
Press Ctrl-x to exit

root@mskdamcmotcft:-# uname -a Linux mskdamcmotcft: 5.4.0-xilinx-v2020.2 #1 SMP Thu Sep 21 13:28:03 UTC 2023 aarch64 aarch64 aarch64 GNU/Linux root@mskdamcmotcft:-# Z

	tps:// github.com /MicroTCA-Tech-Lai: 🖲 🏠 🔤 💈
README.md	
mmcterm	2
Terminal for the custor	n "serial over IPMB" protocol used by DMMC-STAMP.
Installation ${\scriptscriptstyle \mathscr{O}}$	
pip3 install mecter	a Q
Usage 🖉	
mmoterm [-h] [-v] [-0 CHANNEL] [-1 DITERVAL] [-1] [-0] [-1] [-0
DESY MMC Serial ove	r IPMB console
positional argument	*1
mch_addr mnc_addr	IP address or hostname of NCH IPAR-L address of NMC
me_are	THE C BOLLES OF HE
optional arguments:	
-h,help -v,version	show this help message and exit show program's version number and exit
-c CHANNEL, cha	
	console charmel (defmult 9)
-t INTERNAL,10	
	polling interval in ms (default 10)
-1,115t -d,00510	list available channels pylp#1 debug mode
-i,ipmitcol	make pyipmi use inmitool instead of native r
	max-pkt-size MAX_PKT_SIZE
	max IPMB packet size to use (Higher numbers

mmc-mailbox

- Data interface between management (DMMC-STAMP) and payload (primary FPGA)
- Implemented as virtual I2C "EEPROM" for ease of access (U-Boot, etc.)

Use cases

- Ethernet MAC Address from DMMC-STAMP UID (No dedicated EEPROM necessary)
- Orderly shutdown of Payload OS, when handle is pulled
- Propagation of management data (RTM/FMC FRU, sensor values, slot number, ...) to payload side
- AMC Ethernet discovery (mmceth)
 MMC retrieves ethernet address from payload and exposes it over IPMI
- Application specific data transfer from/to MMC

	019 🔽 mmcinfo mmc
MMC information	
· · · · · · · · · · · · · · · · · · ·	
App version	
Lib version	
CPLD board ver	
CPLD lib ver.	
STAMP revision	
AMC slot	: 7
IPMB addr	: 0x7e
Board name	: DAMC-FMC2ZUP
IANA Vendor ID	: 0x053f
IANA Product I	D : 0x200b
Uptime	: 22 days, 16 hours, 57 minutes, 51 seconds
	19 mmcinfo fmc2
FRU 3 descript	
UID	: N/A
Manufacturer	CAENELS
Product name	
Part number	
Serial number	
Version	
VEISLOII	. N/A
FRU 3 status	
Flags	: +Present +Compatible +Powered -Failure
	: Type: FMC, ClkDir: M2C, PG_M2C: asserted
	ryper me, eekser mee, remeer asserted

mmcinfo command on payload Linux

Summary

- DMMC-STAMP is a drop-in solution for management of MicroTCA AMC boards
- ► FMC sensors are supported in compliance with ANSI/VITA 57.1 → FMC temperatures are fully integrated into standard IPMI monitoring (i.e. can be monitored and trigger increase of cooling or AMC shutdown)
- In-system configuration of PMBUS components facilitates development & production Configuration of all PMBUS chips can be bundled with MMC code
- Remote console over Serial-over-IPMB provides useful remote debugging facilities for MMC itself and for payload FPGAs
- MMC mailbox allows data sharing between management (MMC) and payload (FPGA)

Thank you!

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https://innovation.desy.de

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