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Using high-level synthesis languages to accelerate DAQ and processing applications for AMD-XILINX MPSoC-based AMCs

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In recent years, FPGA vendors have integrated high-level synthesis languages (HLS) into their development tools, allowing HDL (Hardware Description Languages) to be set aside in application development.
This contribution presents the development of a Board Support Package (BSP) for the NAT-AMC-ZYNQUP-FMC board based on a Zynq UltraScale+ MPSoC that allows the implementation of data acquisition and processing applications using the HLS and OpenCL tools. The BSP hardware is divided into a static and a dynamic region. The static region provides the PCIe interface to the MicroTCA backplane and the interface with an external FMC module that features JESD204B ADCs and DACs. The JESD204B uses the open-source IPs from Analog Devices. The accelerated functions or kernels written in HLS or OpenCL are implemented in the dynamic region interface with the PCIe and JESD204B through HLS Streams. The SoC's ARM cores run an embedded Petalinux Linux distribution that handles the JESD204B configuration and provides the environment in which the kernels are executed.
Finally, a use case is presented where the BSP implements and verifies a digital pulse shape analysis algorithm of signals acquired at 1GS/s.

Primary authors: Mr PIÑAS, Alejandro (Universidad Politécncia de Madrid); Mr GONZALEZ, Cesar (Universidad Politécncia de Madrid); RUIZ, Mariano (Universidad Politecnica de Madrid); Dr CARPEÑO, Antonio (Universidad Politécncia de Madrid); Prof. BARRERA, Eduardo (Universidad Politécncia de Madrid); Dr NIETO, Julián (Universidad Politécncia de Madrid)

Presenter: Mr PIÑAS, Alejandro (Universidad Politécncia de Madrid)

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