The H2M Test Chip

From Design to Testing

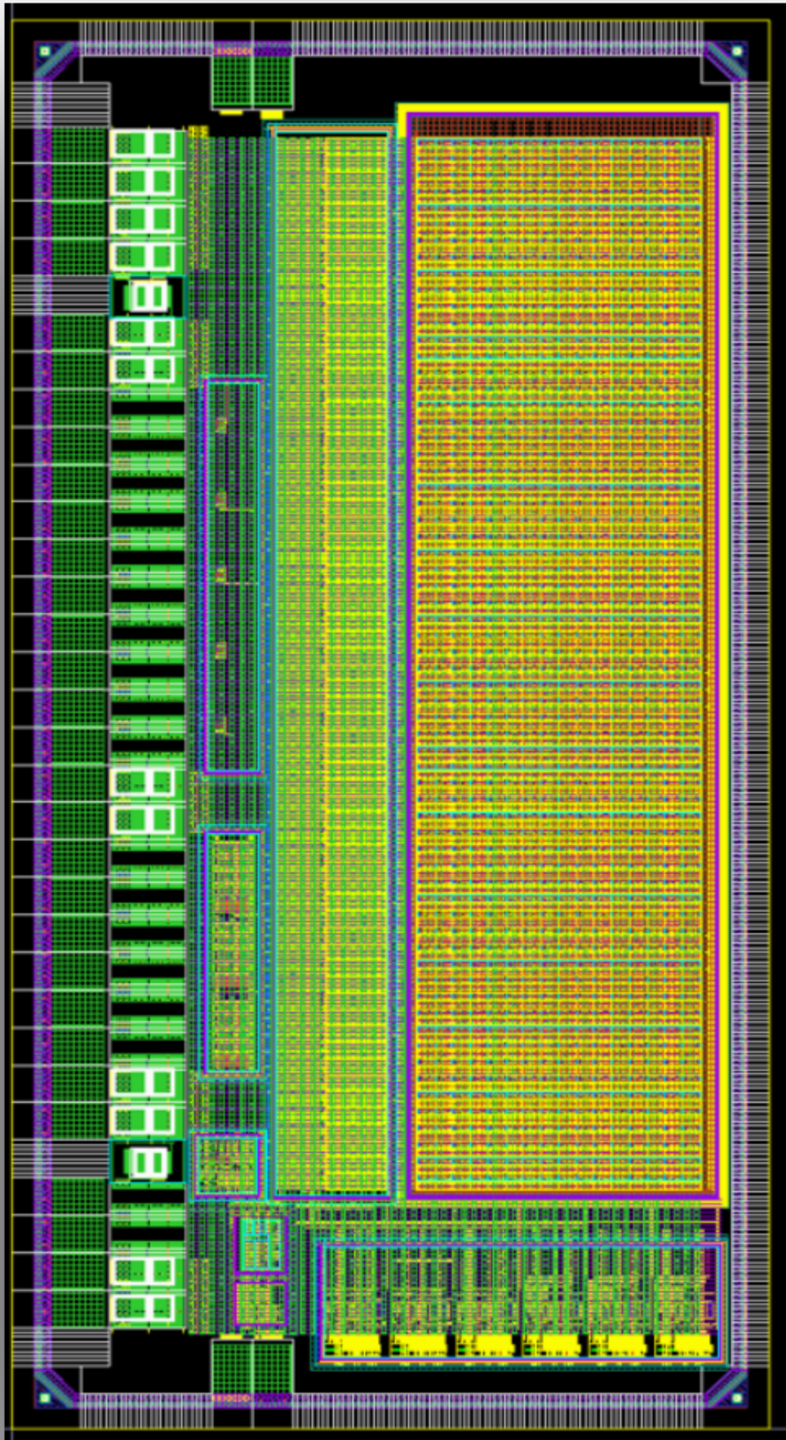
Sara Ruiz Daza on behalf of the Tangerine Collaboration

SiDet Meeting, DESY
24 October 2023

HELMHOLTZ

UNIVERSITÄT BONN

DESY.



The Tangerine Project

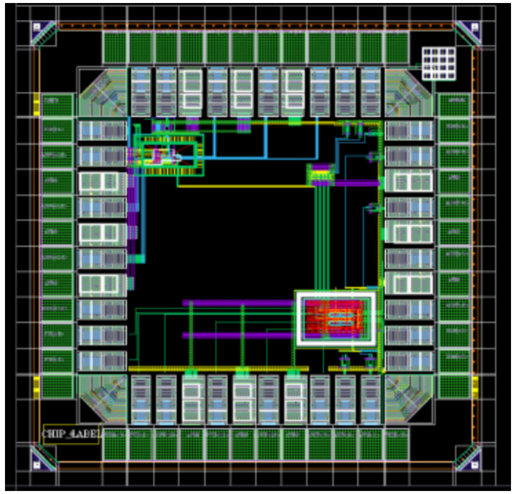
Towards Next Generation Silicon Detectors

- Research and development of **new silicon sensors** for future lepton and electron-ion colliders, and test beam telescopes.

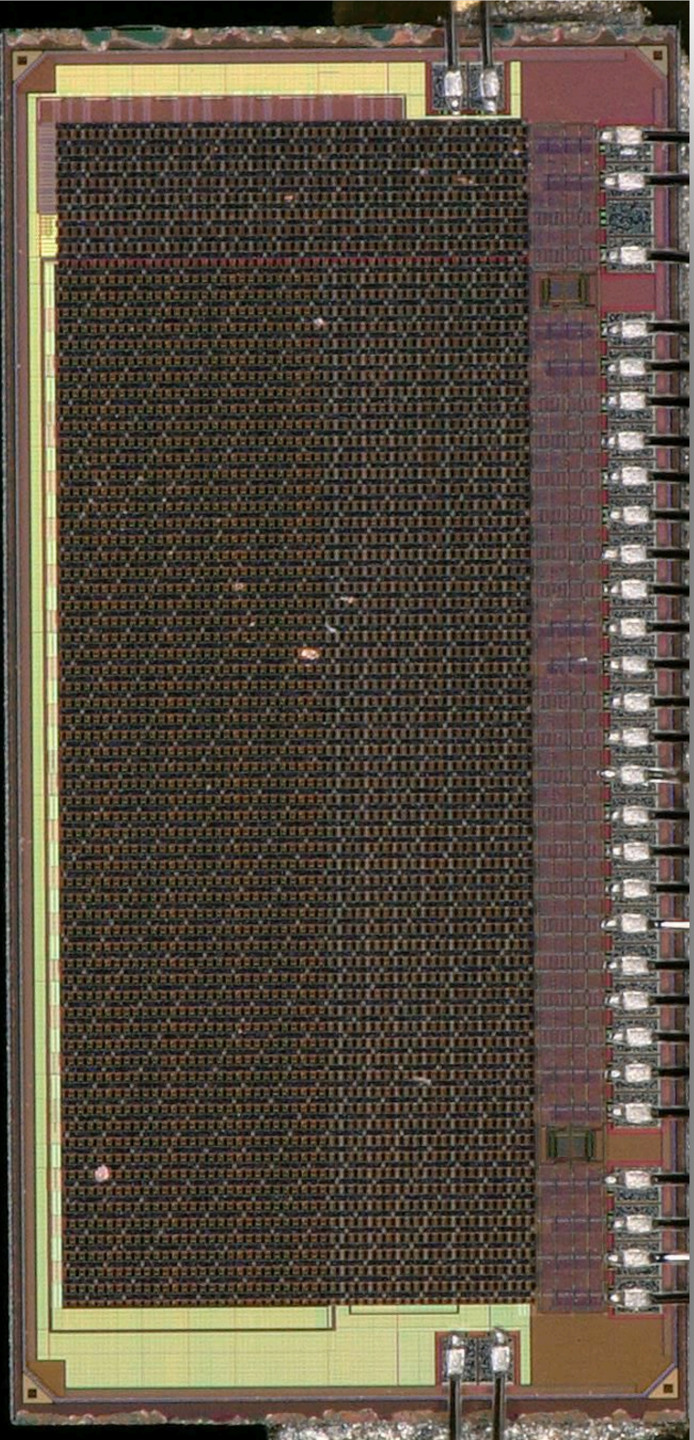
- Project goal: development of a sensor with **high spatial** (~ 3 µm) **and time resolution** (1-10 ns), and a **low material budget** (~ 50 µm Si).

- Exploiting **monolithic sensors** based on a novel **65 nm CMOS imaging technology** with a **small collection electrode**.

- Comprising **all the steps of sensor R&D**: electronics design, sensor design based on simulations, prototype testing.



DESY Chip V2



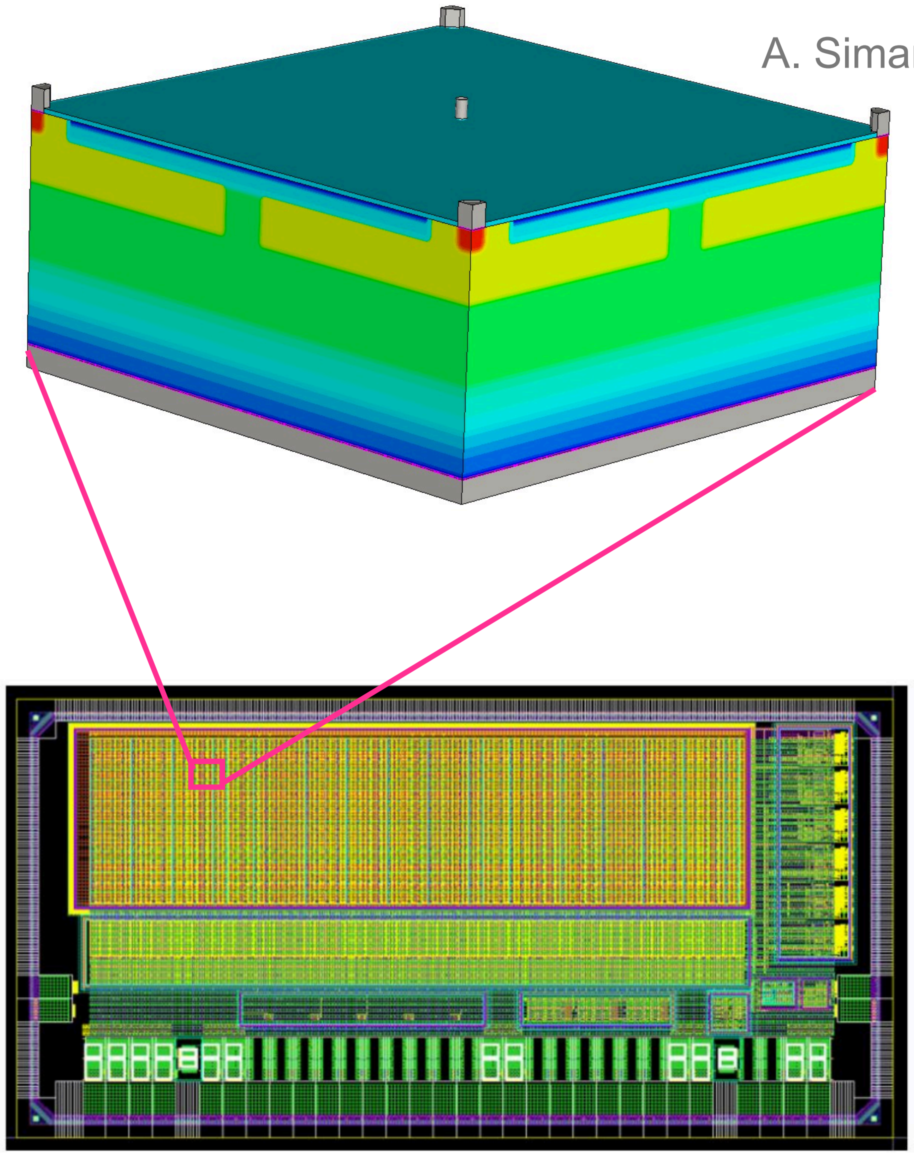
Overview

- ➤ Design
    - ➤ Analog front-end
    - ➤ Digital front-end
    - ➤ Monte Carlo Simulations of the sensor
- ➤ Testing
    - ➤ DAQ System
    - ➤ First lab measurements
    - ➤ First test beam measurements
- ➤ Summary & Outlook

H2M (Hybrid to Monolithic) test chip

- DESY, CERN & IFAE **collaboration**
- **Goal:** Port a known hybrid pixel architecture into a monolithic design + Exercise digital-on-top design.
- Monolithic pixel sensor chip design in a 65 nm CMOS imaging process
  - **Pixel matrix**: 64x16 pixels
  - **Pixel pitch**: 35 µm
  - **Total sensitive area**: 2.24 × 0.56 mm^2
  - **Sensor**: n-gap layout (2.5 µm gap size)
- Each pixel:
  - **analog front-end:** collection electrode, CSA, discriminator.
  - **digital logic:** 8-bit counter, 4 acquisition modes: ToT, ToA, photon counting, triggered binary readout.

A. Simancas



Analog front-end

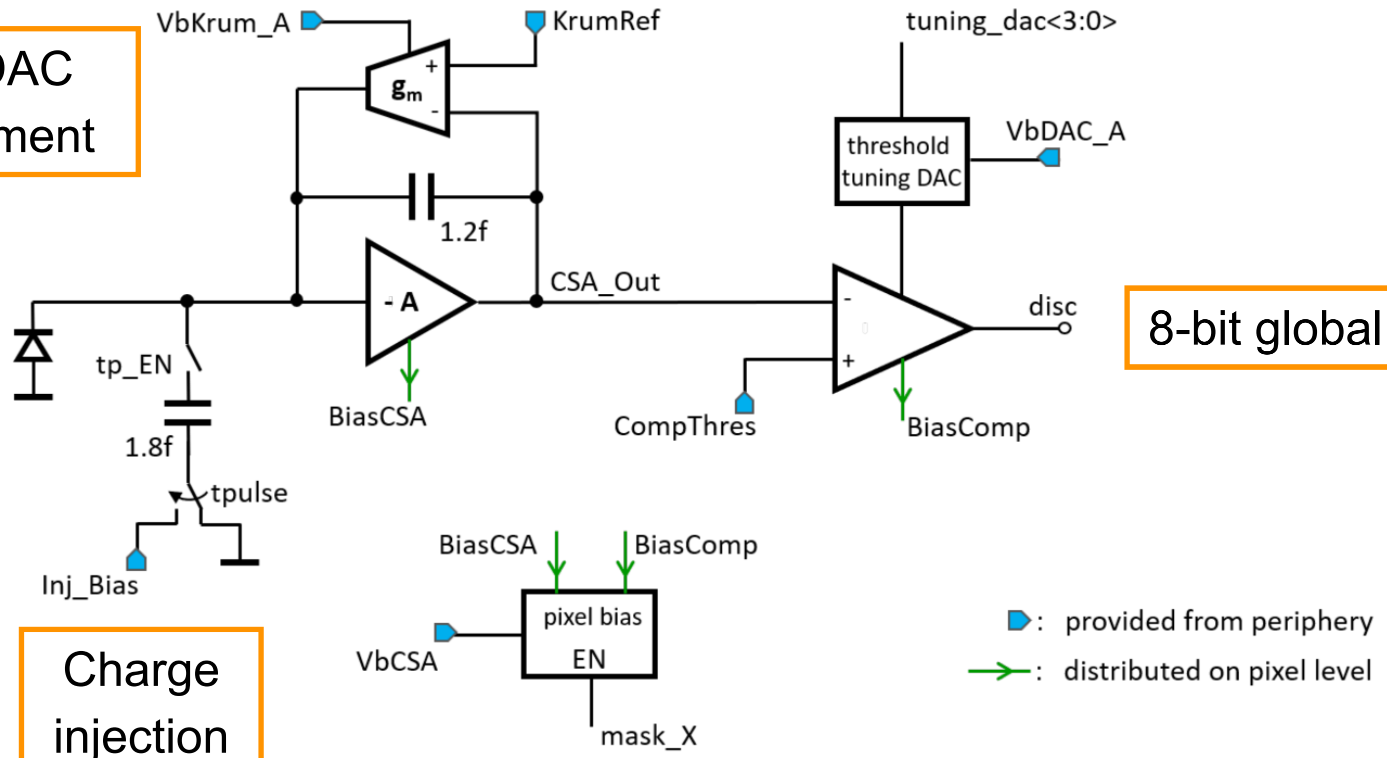
Designed at DESY by Christian Reckleben and his team.

Charge sensitive amplifier with Krummenacher feedback

4-bit in-pixel trimming DAC → threshold mismatch compensation

3-bit in-pixel trimming DAC for feedback bias adjustment

Sensor diode



8-bit global threshold DAC

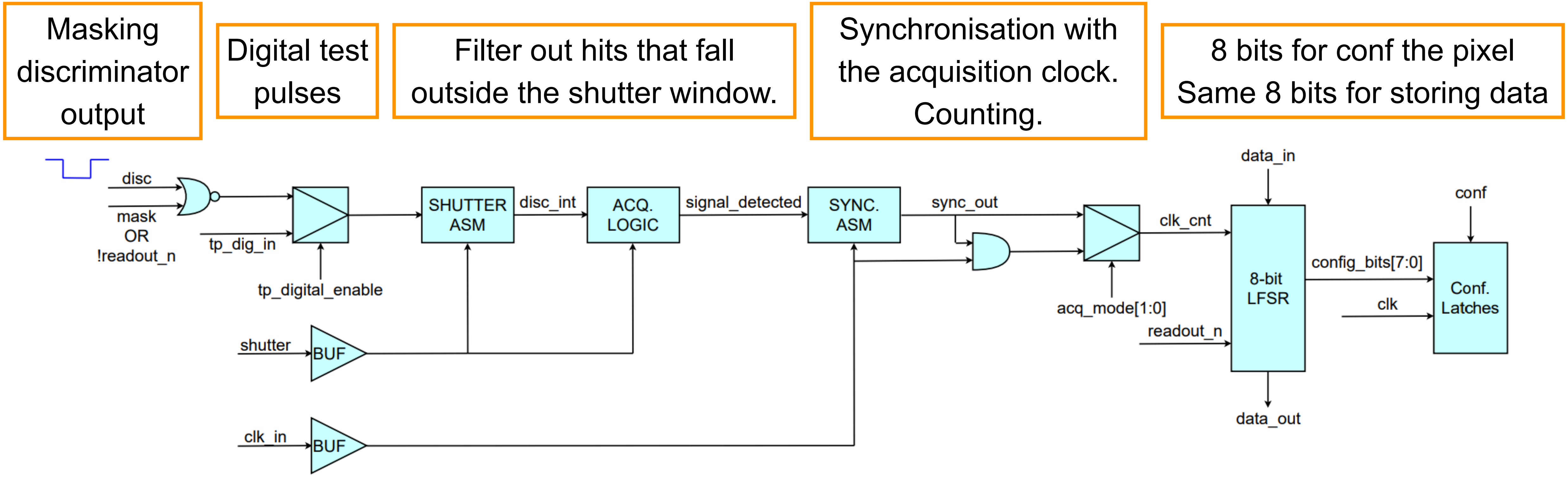
Charge injection

Pixel enable/ disable

The output signal of the comparator is processed by the digital logic.

Digital logic

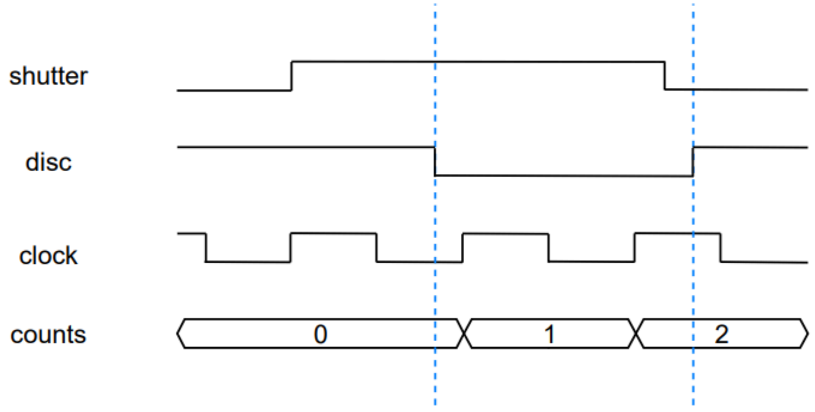
Designed at CERN.



- **Configuration:** 8 bits shifted from bottom to top of the column and latched to the pixels.
- **Readout:** 8 bits are shifted from top to bottom of the column.

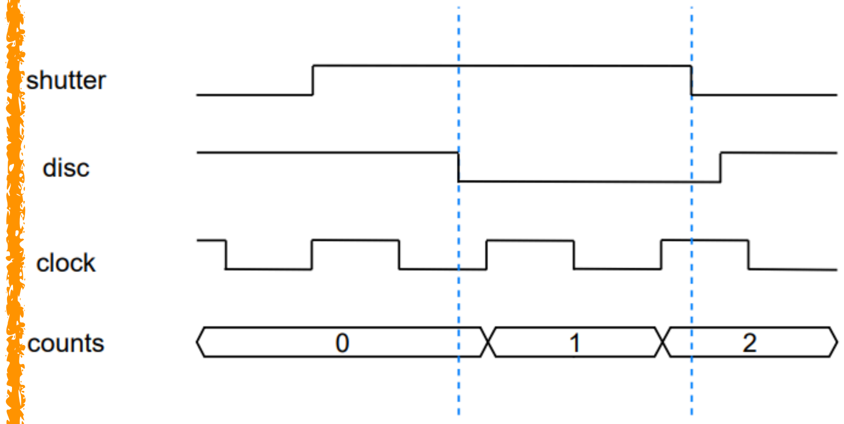
Frame-based modes (Timepix4/Medipix4)

Time-over-Threshold (ToT)



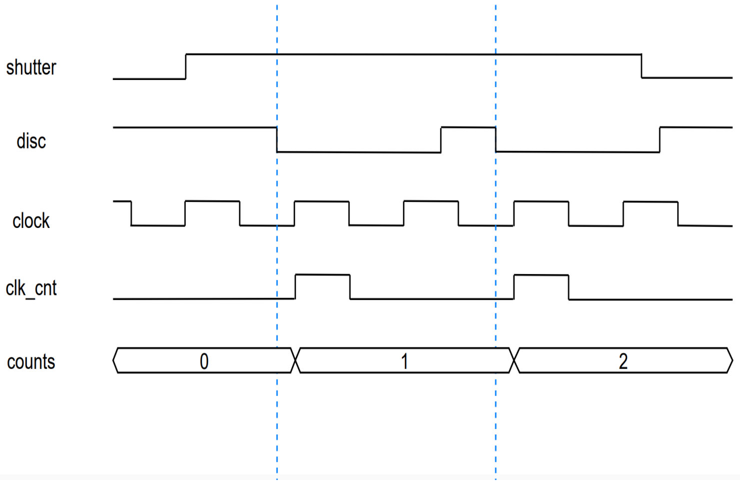
- Number of clock cycles:
  Threshold crossing → threshold crossing
- After calibration ToT ~ collected charge

Time-of-Arrival (ToA)



- Number of clock cycles:
  Threshold crossing → shutter closed

Photon counting

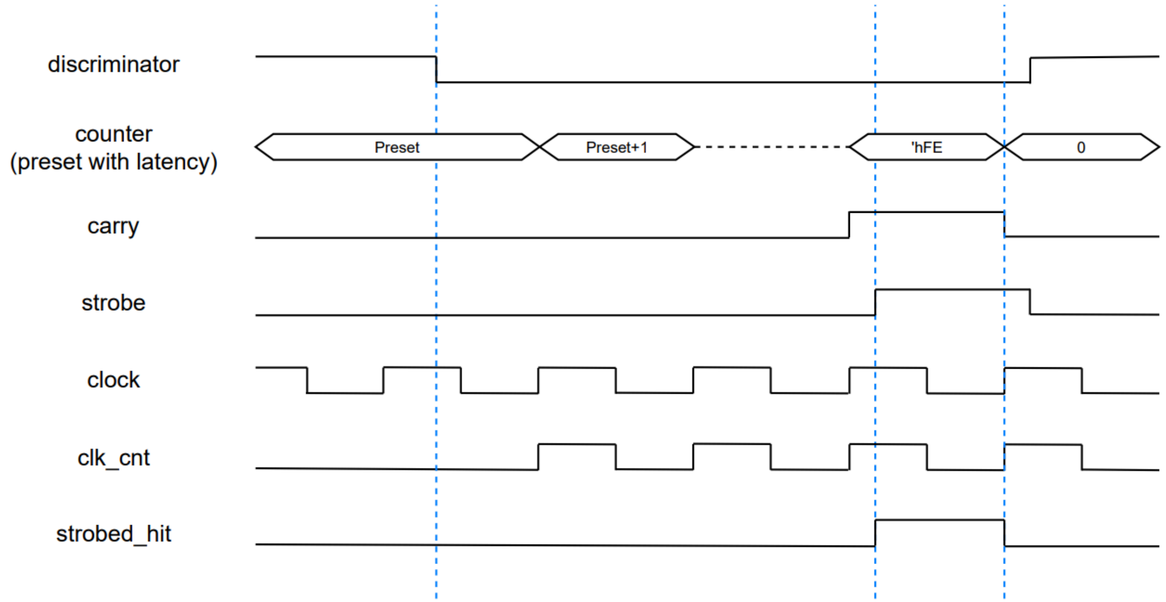


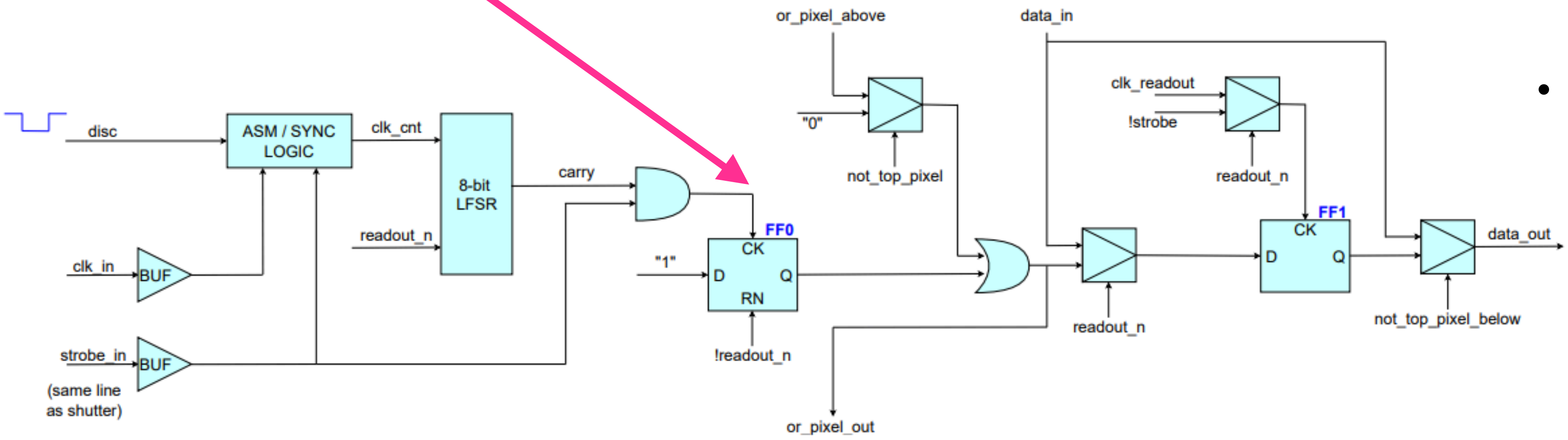
- Number of threshold crossings

- 8-bit counter
- 100 MHz acquisition clock ⇒ 10 ns binning

Triggered acquisition mode

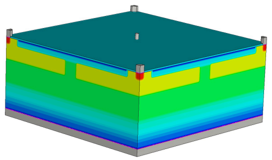
- Counter preset with the trigger latency value.
- Start counting whit the discriminator crossing edge.
- Counting reaches overflow (8 bits = 254 values)
  → **carry signal**
- **External strobe signal** provided, synchronised with the clock period (10 ns)
- If carry signal AND strobe are in coincidence, we have a **hit**.





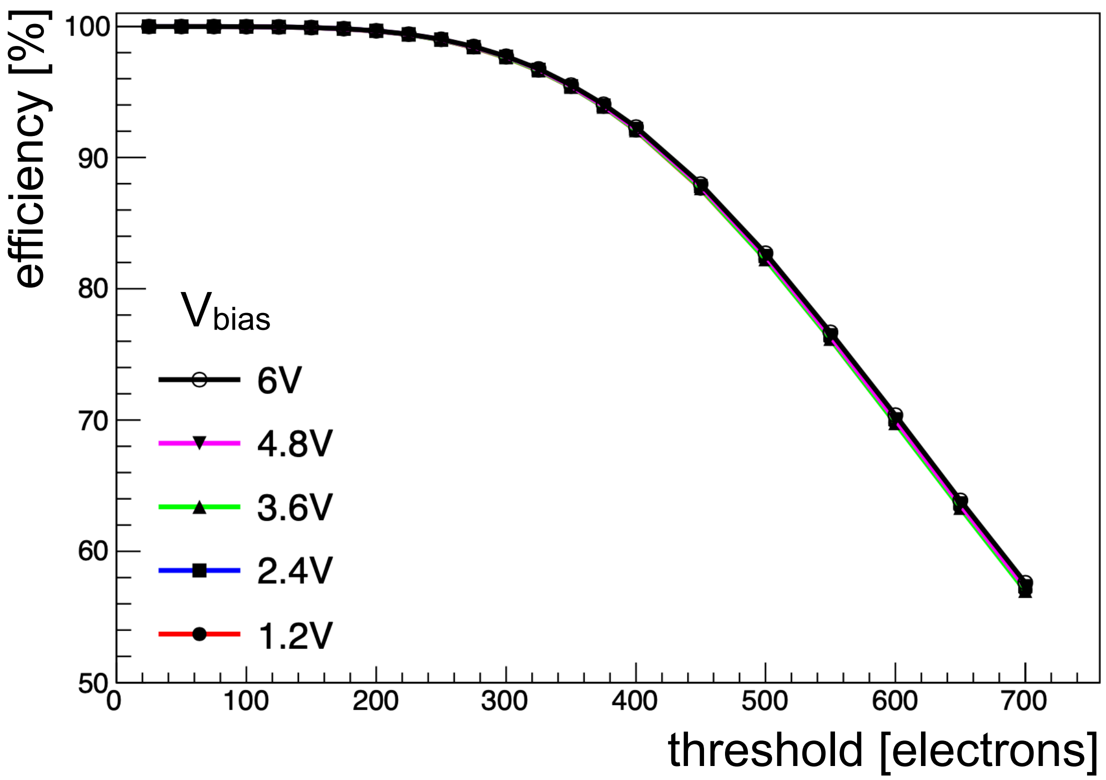
- Depending on the pixel configuration: the pixel stores its own hit or combines data from a group of pixels.

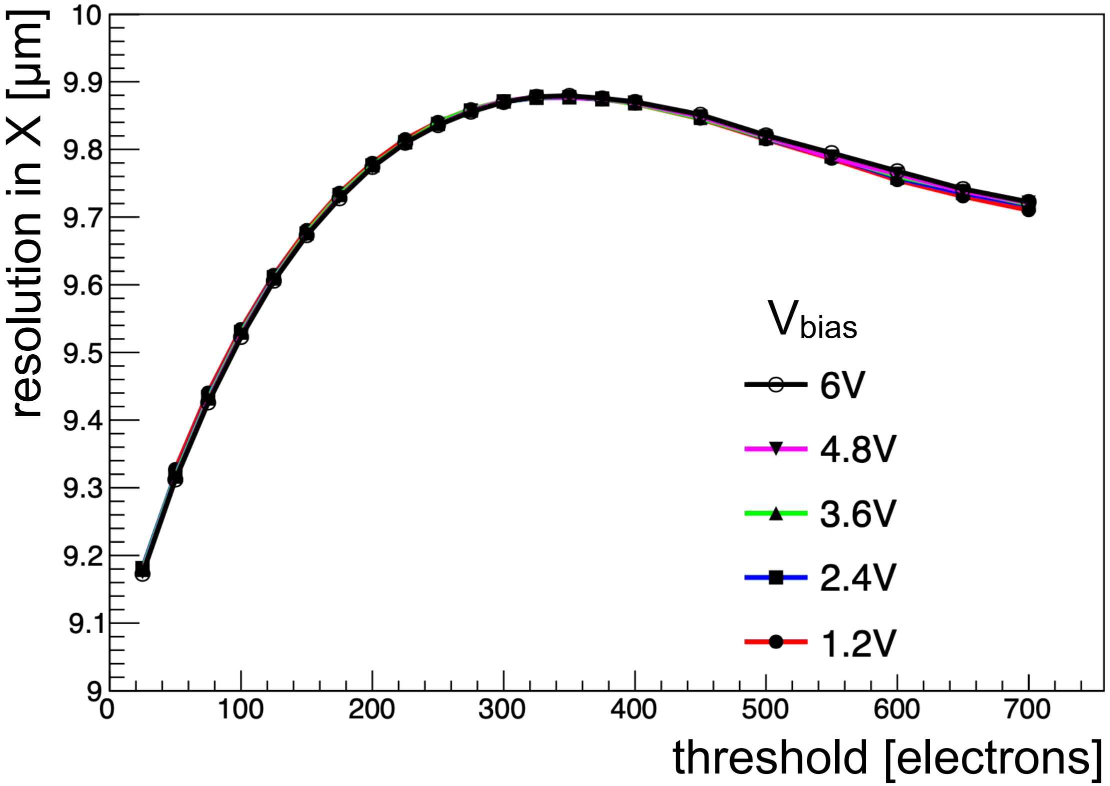
MC Simulations of the sensor



Sentaurus TCAD
SYNOPSYS® Silicon to Software™

ap² allpix squared

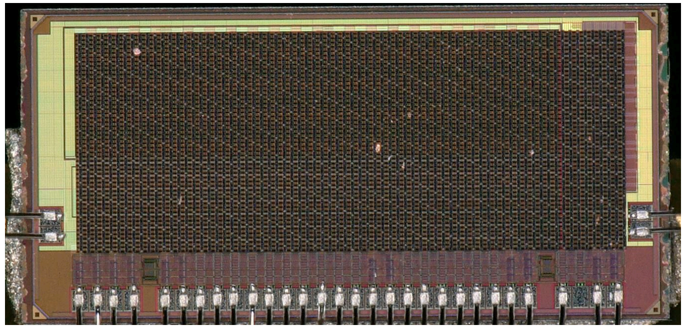


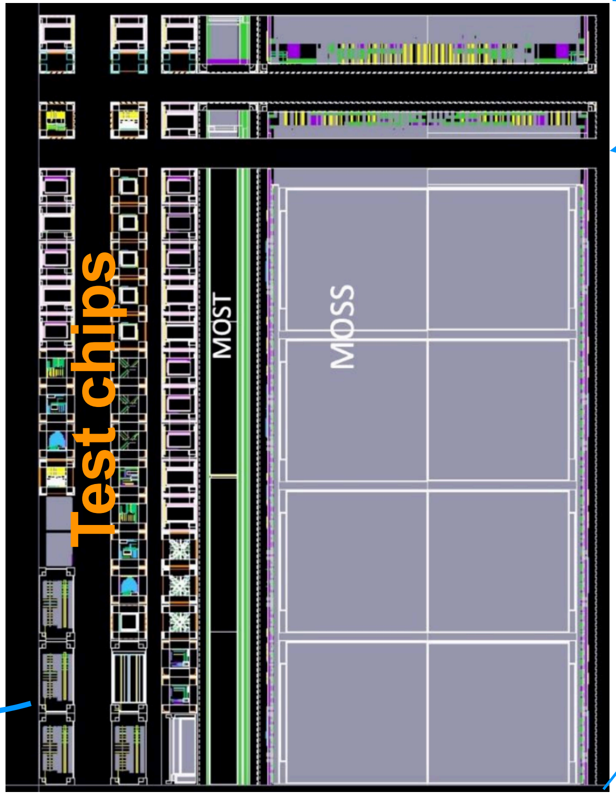


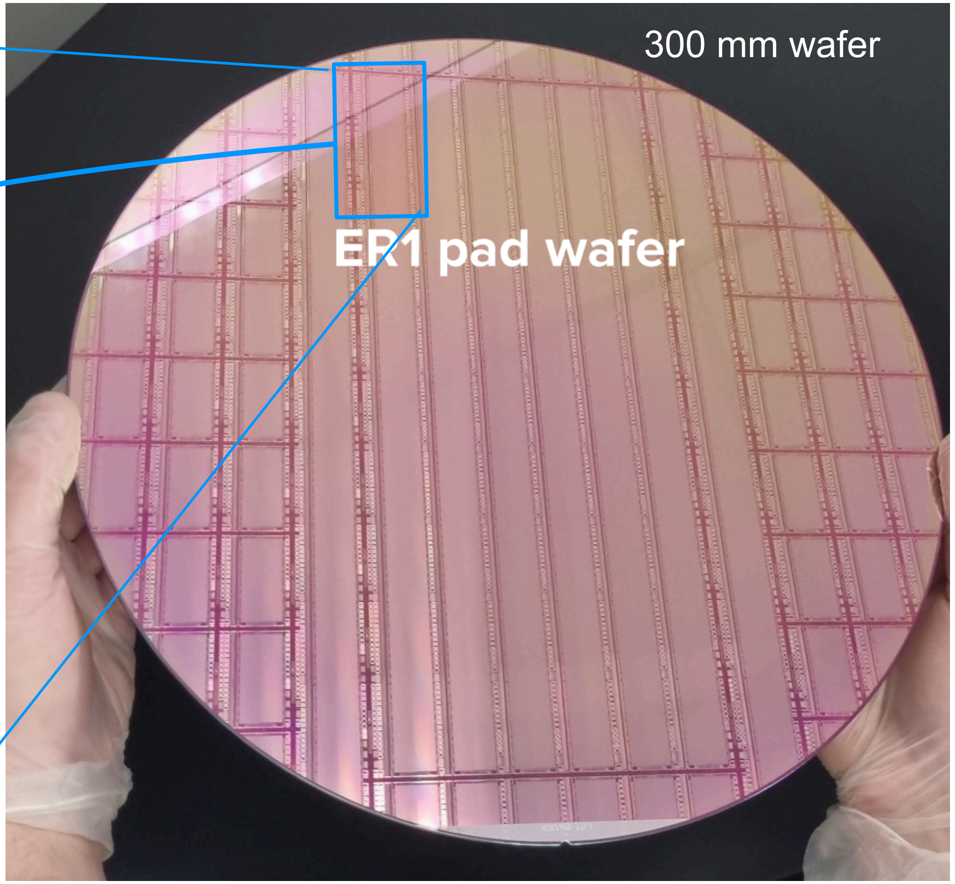
- **For the expected threshold operation** (150-300 electrons):
  - ➤ Efficiency > 97%
  - ➤ Spatial resolution in X: 9.5 - 9.9 µm
- Observed **small differences for the V_{bias} applied** (small undeleted region around the collection electrode for low V_{bias})

ER1 Production

- The design was submitted to the foundry in December 2022.
  → Engineering Run 1 (ER1) submission.







- First chips from wafers **manually diced** at CERN received at the end on July 2023.

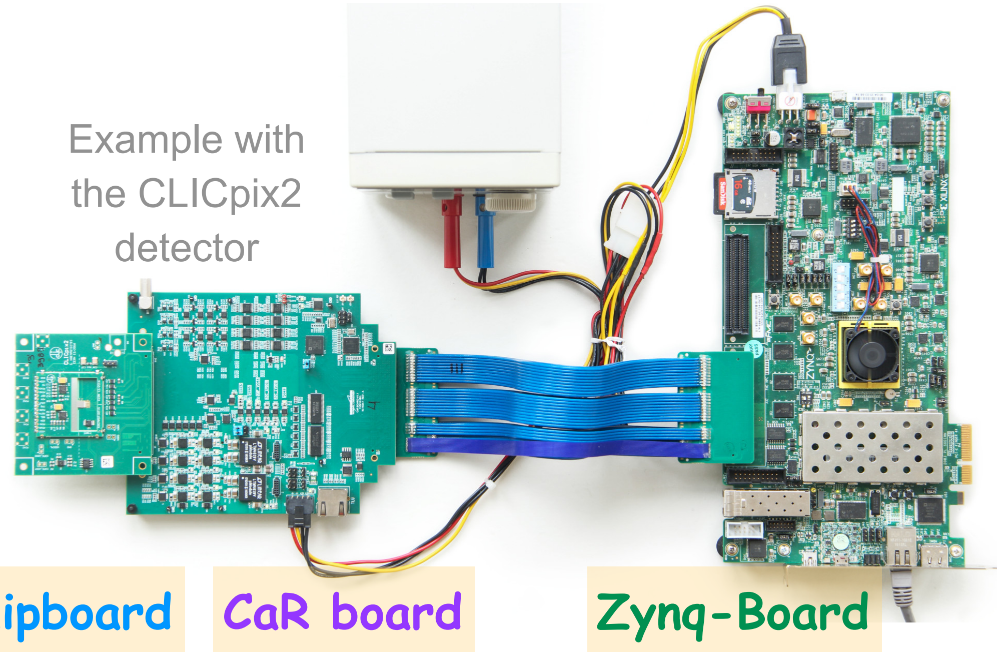
End of design…
… beginning of testing

Preparation for testing

The Caribou Data Acquisition System

T. Vanat doi:10.22323/

Example with the CLICpix2 detector



➢ **Zynq-Board:**

- User connects via ssh/Ethernet
- Runs Linux system with DAQ and control software
- An FPGA runs custom hardware blocks for data processing

➢ **CaR board (Control and Readout Board):**

- Physical interface between Zynq-Board ↔ Chipboard
- Contains all peripherals needed to interface and run the chip (eg. adjustable voltage/current references, pulser control…)

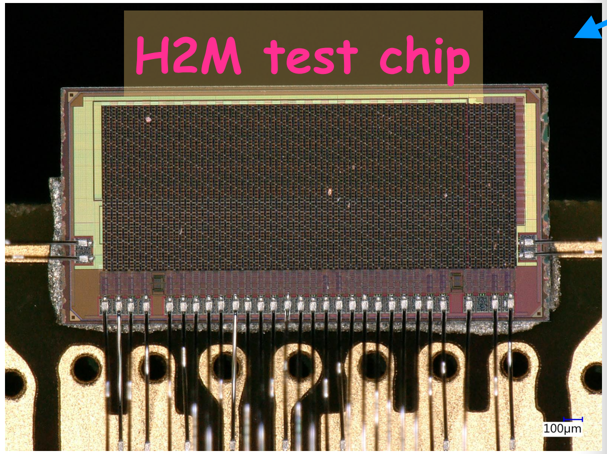
➢ **Chipboard:**

- Application-specific detector carrier board
- Mostly passive components + detector chip

What did we need to prepare to test H2M?

↪ The chipboard, the FPGA firmware and the DAQ software framework.

DAQ System



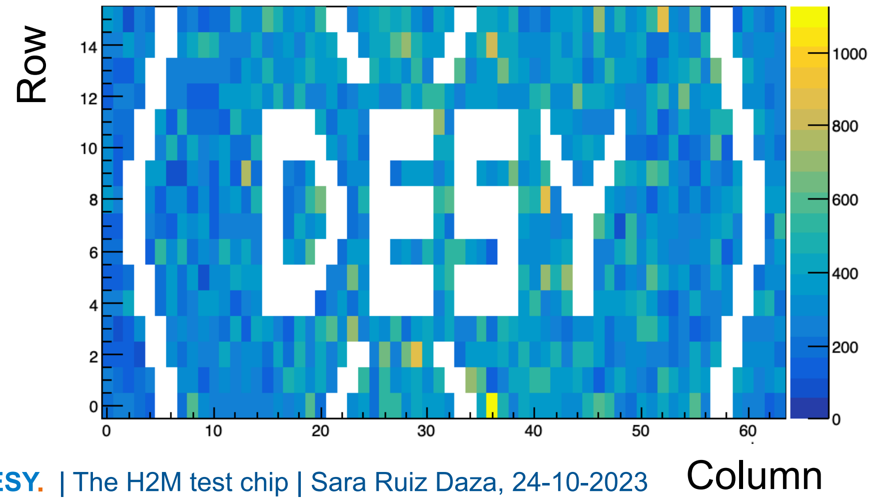
- Sensitive part **outside** of the the chipboard.

→ Reduce material budget.

- **6 test chips on chipboards**

  → 3 of them are being tested without issues.

  → 3 of them show problems related with the circuit start-up. Under investigation

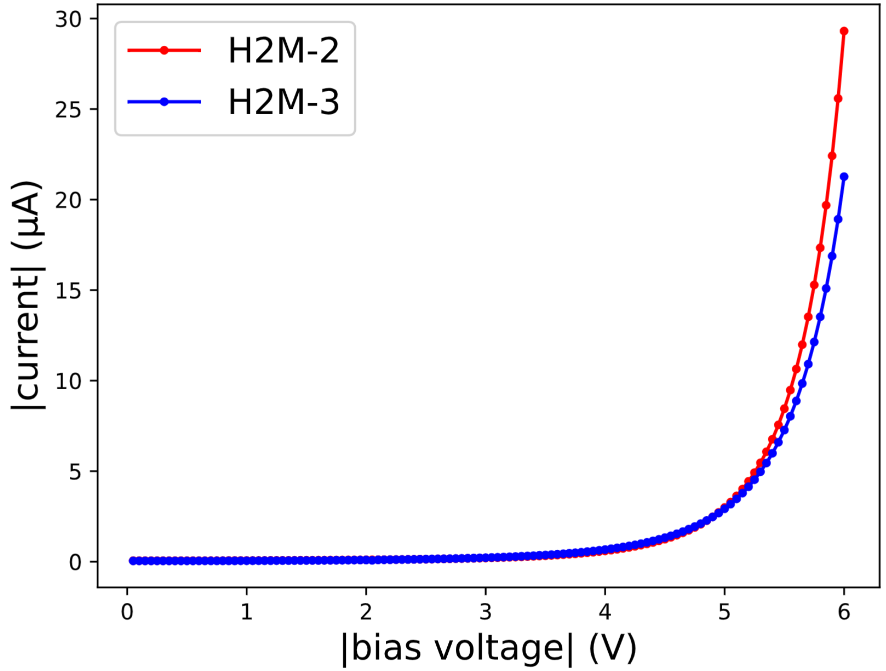


Masking pixels ✓
Writing pixels ✓
Reading pixels ✓

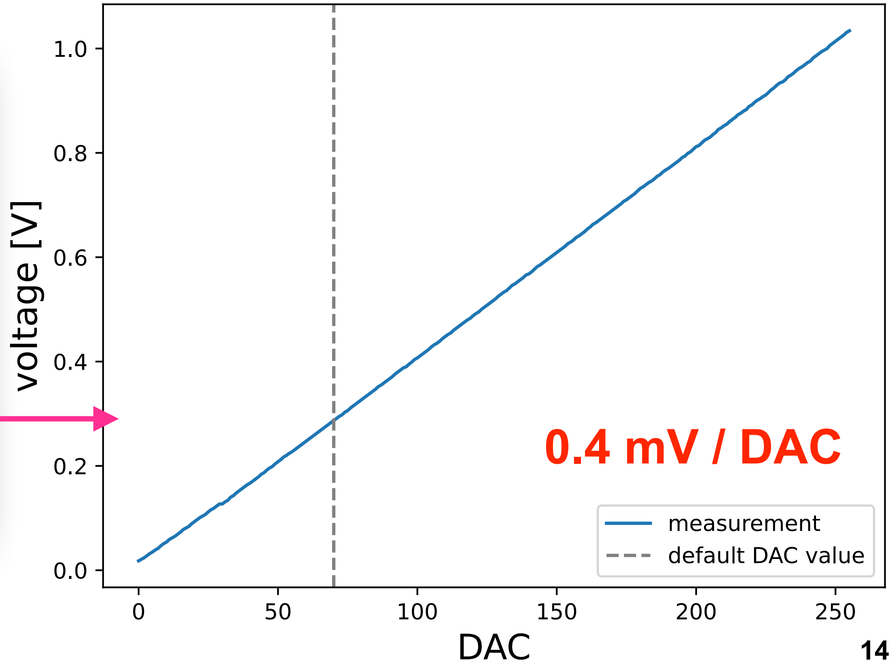
IV measurements and DACs scan

- PWell and Sub biasing at the same values.
  → **Similar behaviour for all the assemblies.**

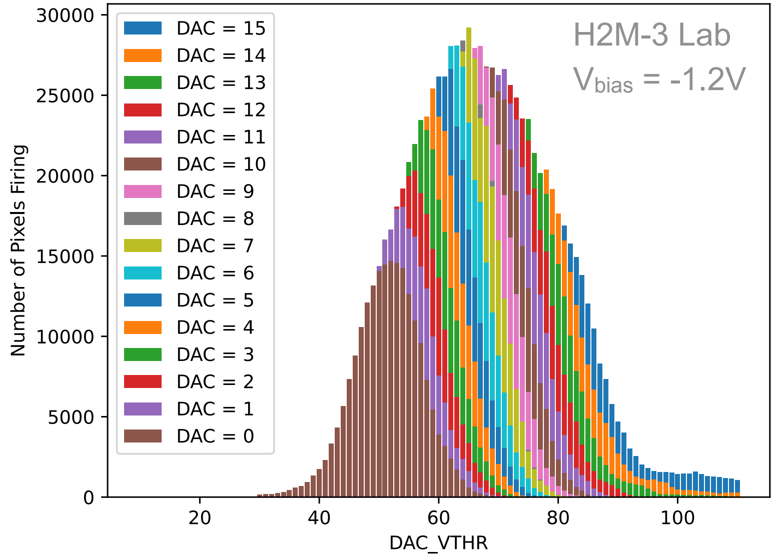
- The **analog periphery** consists of 6 biasing DACs that are used for biasing the front-end to the desired operating point.
  → **Expected behaviour for the three working assemblies.**

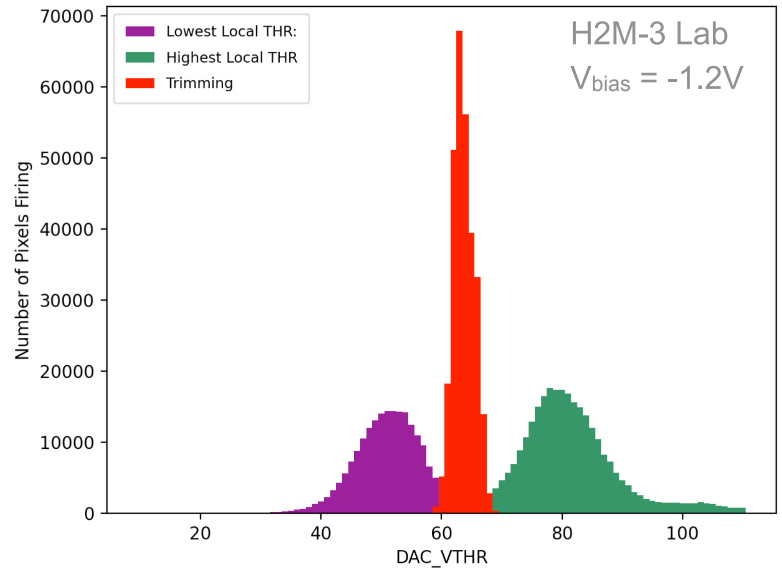


analog_out_ctrl	Monitored DAC	Description
0	-	-
1	IBIAS	CSA and comparator bias current DAC
2	ITRIM	Trim DAC bias current DAC
3	IKRUM	Krummenacher current DAC
4	VTHR	Threshold voltage DAC
5	VREF	Reference voltage DAC
6	VTPULSE	Test pulse voltage DAC



Trimming

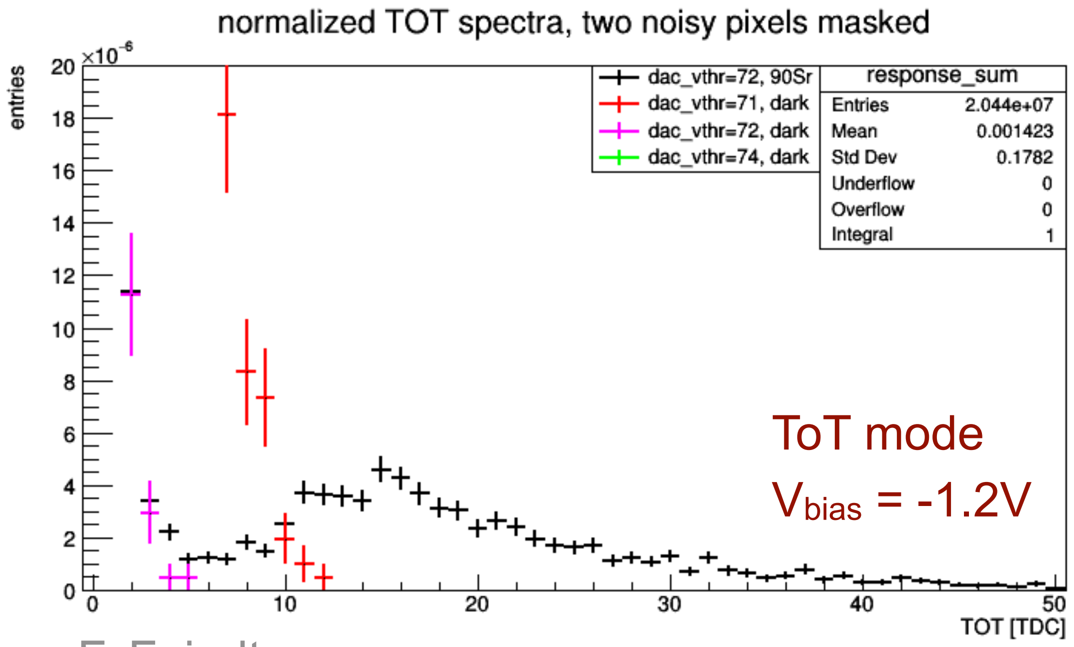




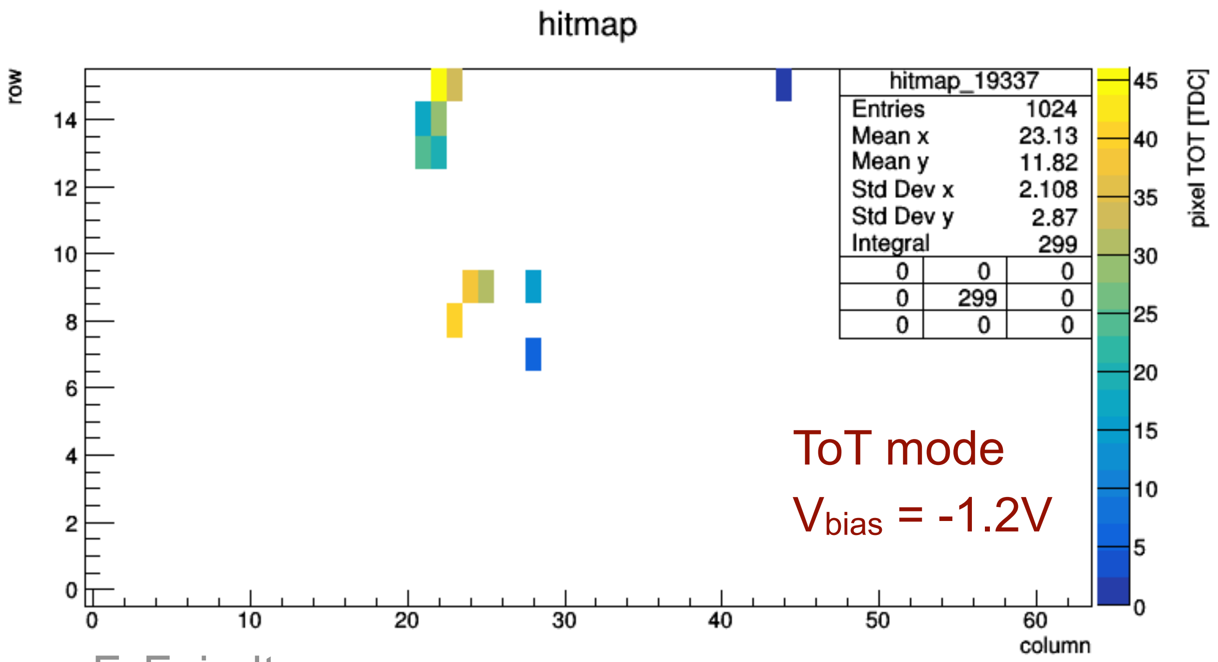
- Based on **noise measurements**.
- Scan of the global threshold for the 16 possible **threshold trimming DACs**.
- The <u>mean</u> of the distributions represents the most common turn-on threshold for the pixels in that conditions.
- The <u>width</u> represents the threshold dispersion between pixels (very broad for the 16 distributions).
- A **target baseline of 65** is selected.
- **For each pixel**, the trimming DAC is adjusted to that one that makes the most common turn-on threshold closest (and higher) to the target baseline.

Currently being improved by Judith

Sr90 source measurements



F. Feindt



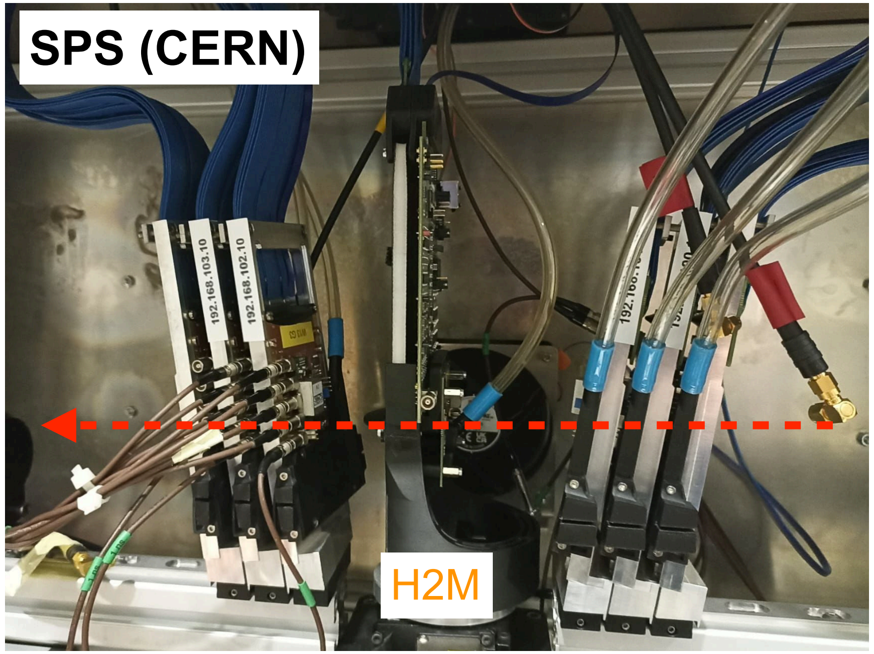
F. Feindt

- Signal distinguished from noise.
- Charge sharing observed (even with a small epitaxial layer).

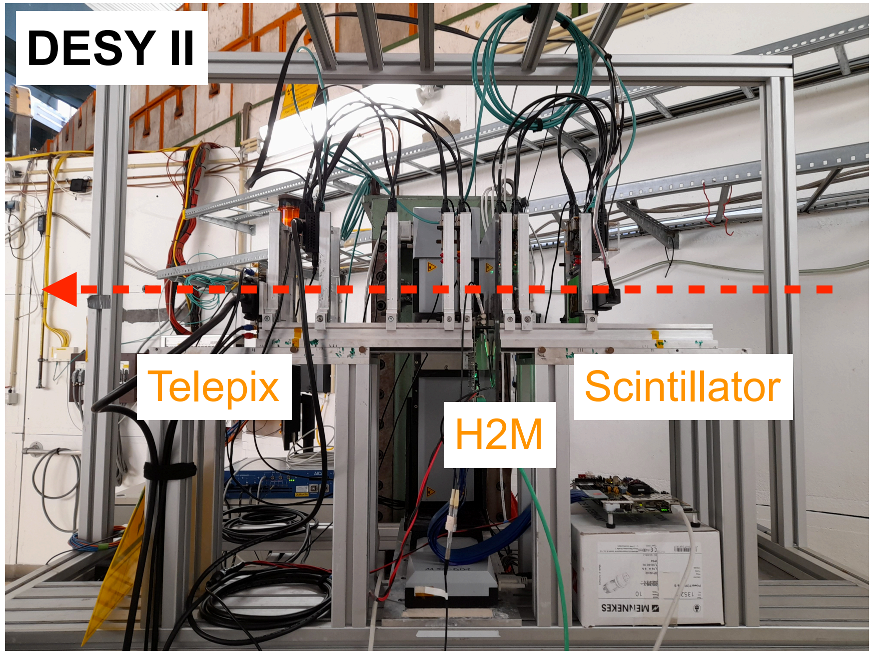
We are ready for test beam measurements!

Test beam measurements

Test beam campaigns

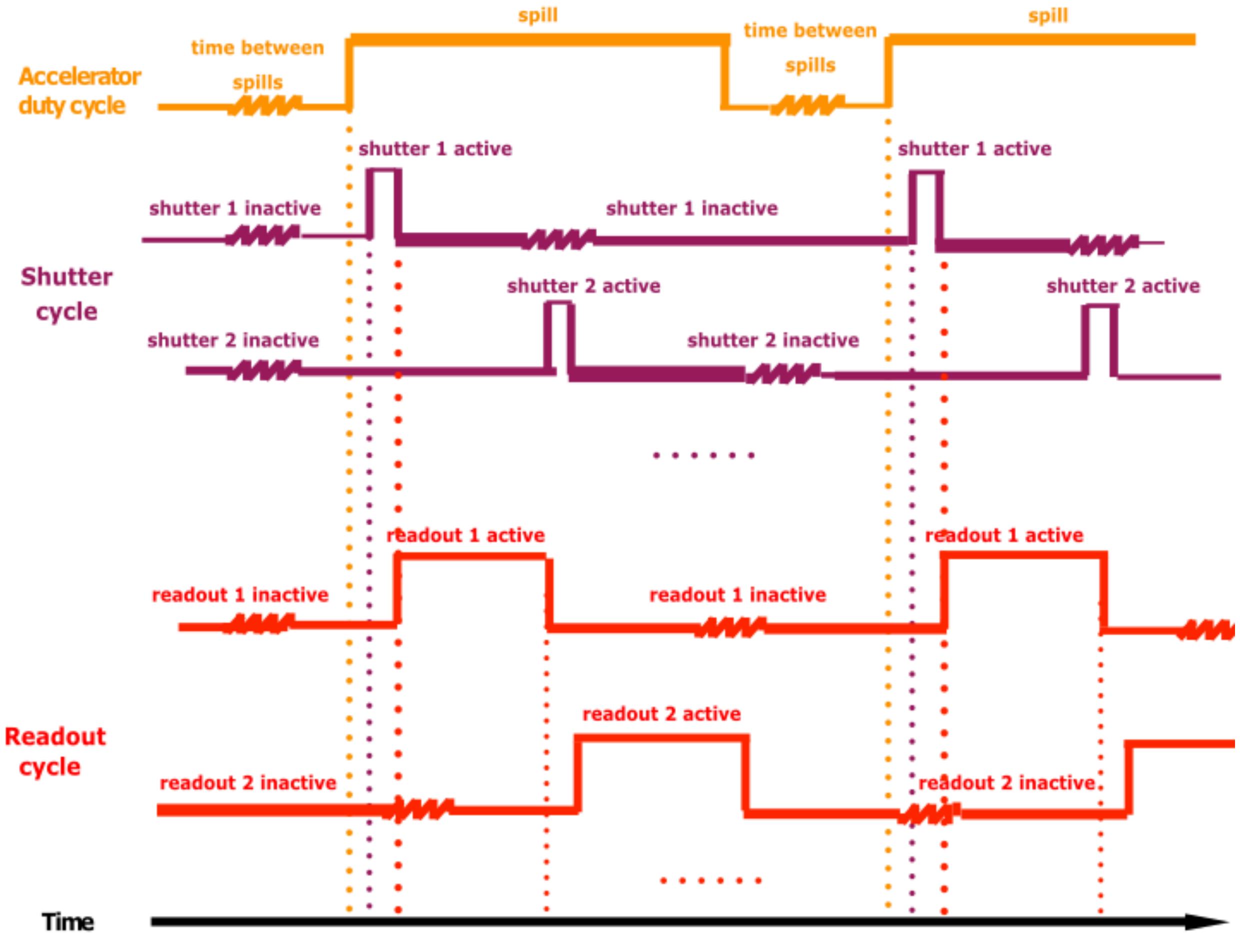


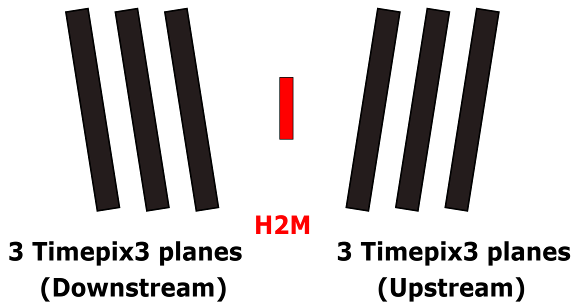
- H6 beam line, 120 GeV/c charged pions.
- **Timepix3 reference telescope.**
  - Pointing resolution ~ 1.8 µm
  - Track time resolution ~ 1 ns



- Beamline 22, electron beam ~4.8 GeV.
- **Alpide reference telescope.**
  - Pointing resolution ~ 3 µm

Test beam measurements @ SPS





- **Trigger Logit Unit (TLU):** provides global clock (40 MHz) and T0 for the telescope and DUT.

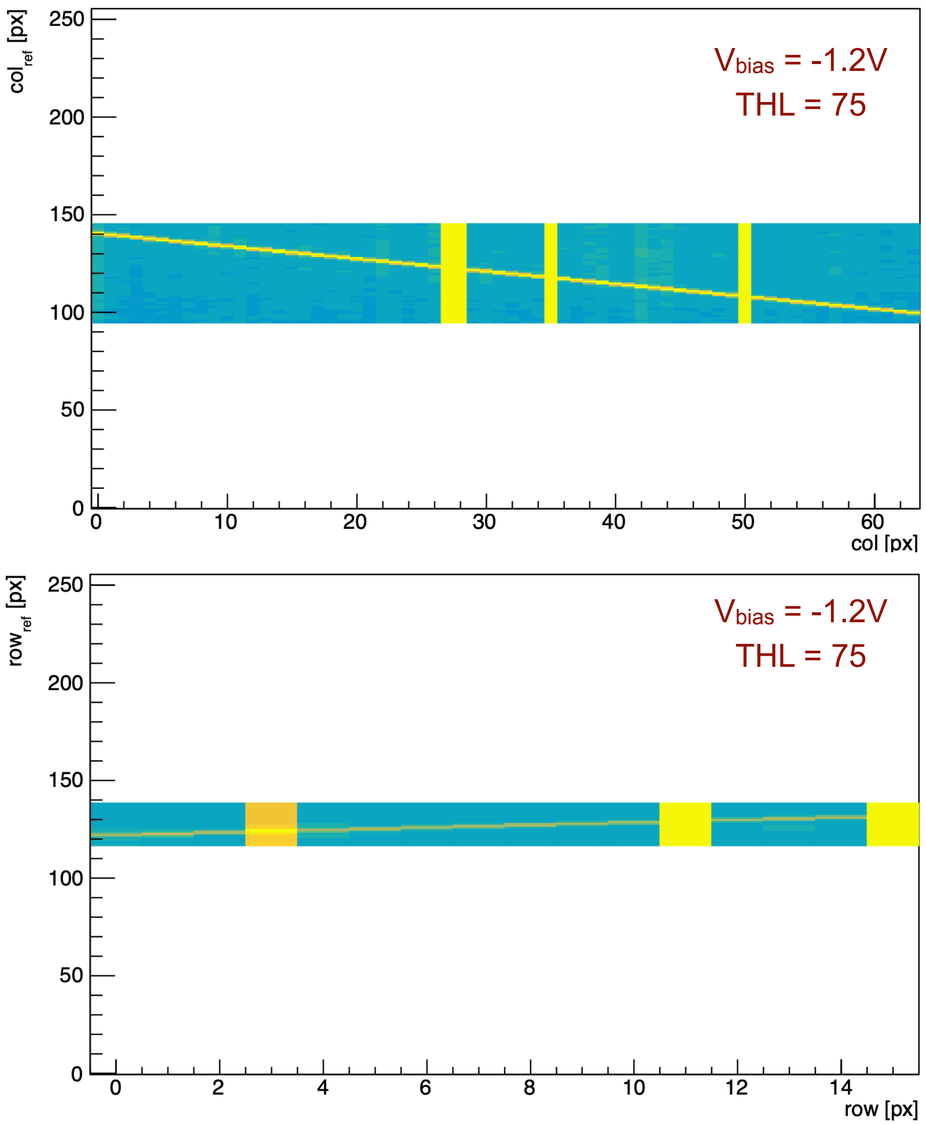
- **H2M**:
  - ToT mode
  - Gated with SPS spill signal
  - Shutter window of 150 μs
  - Readout time ~ 500 μs

- **Timepix3**:
  - In data-driven mode
  - Selecting region of interest (ROI)

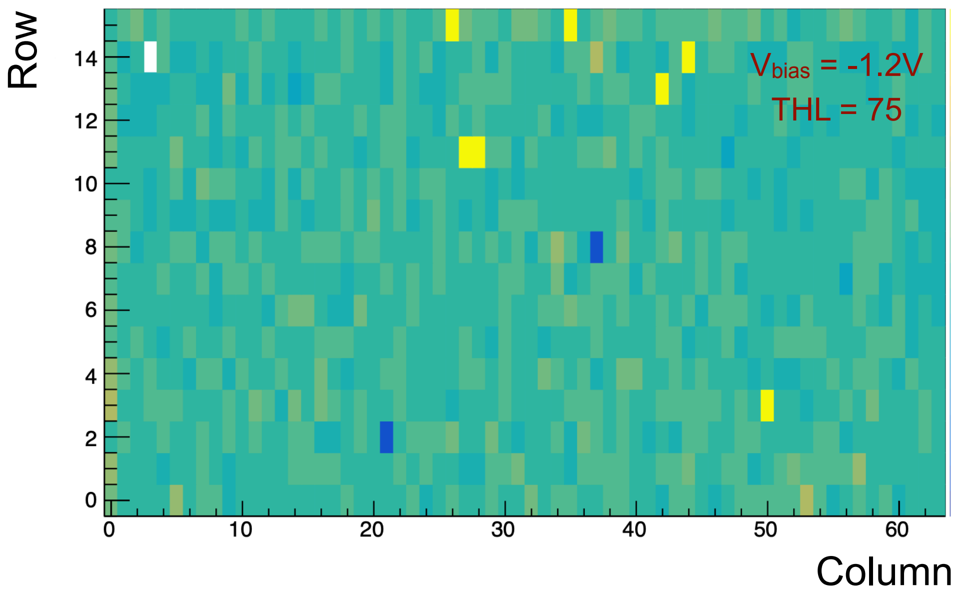
Turning on the beam…

Turning on the beam… hitmap & correlations!

Correlations



Hitmap

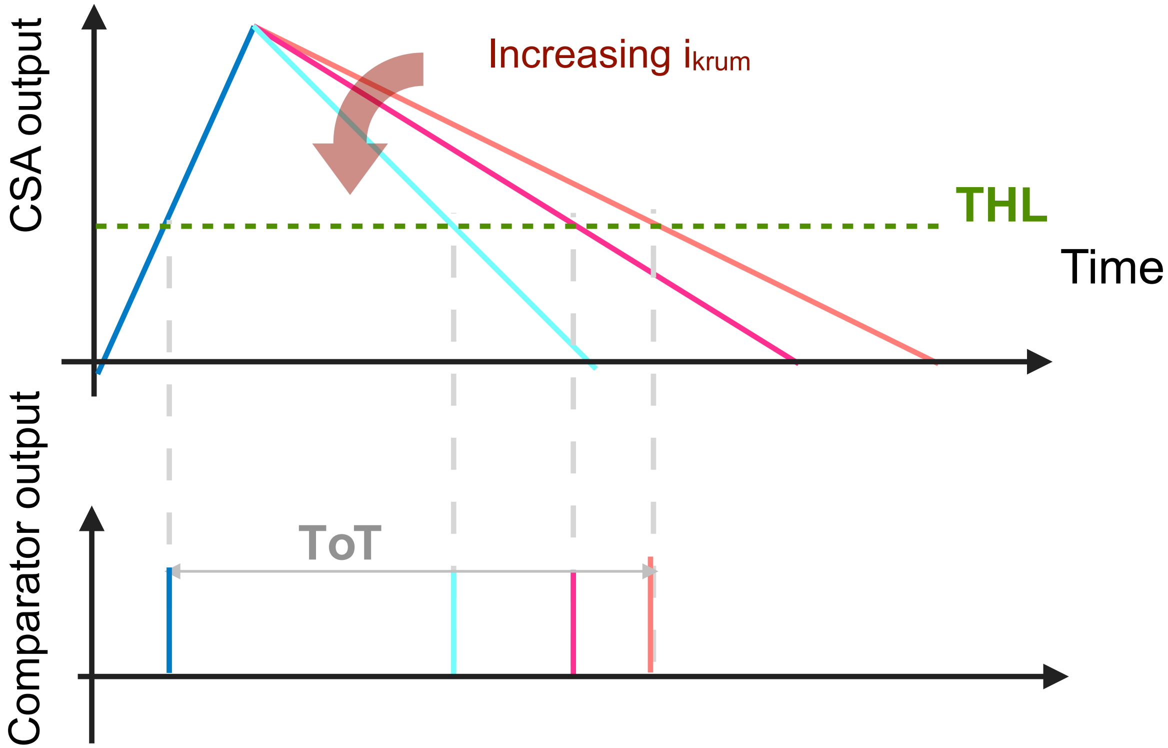


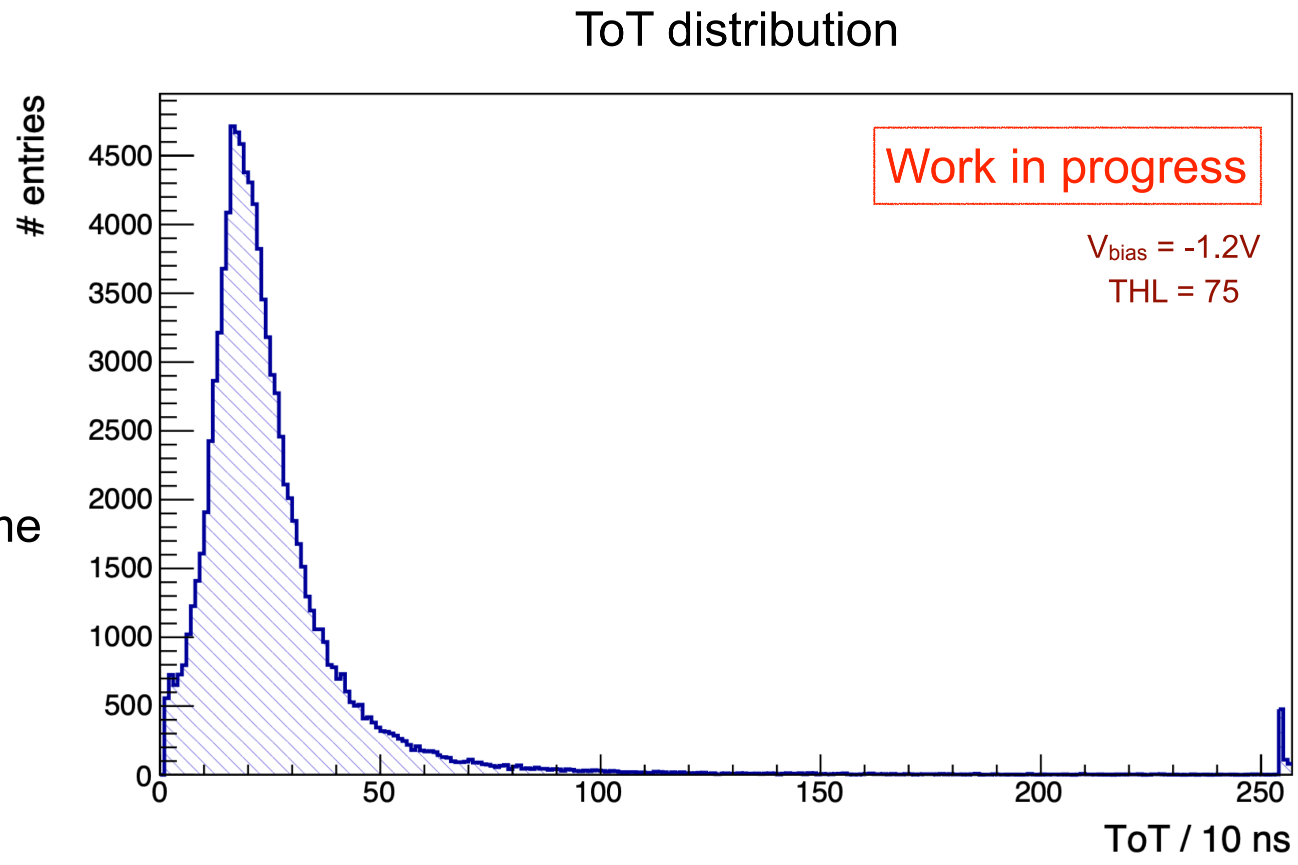
- Analysis with the Corryvreckan Framework.
- **Correlations** with the reference Timepix3 plane (rotated 180° along the row axis).
- **Homogenous hitmap**: few noisy pixels and one unresponsive.

Chip is working!

ToT distribution

- Return to baseline adjusted with the krummenacher current.



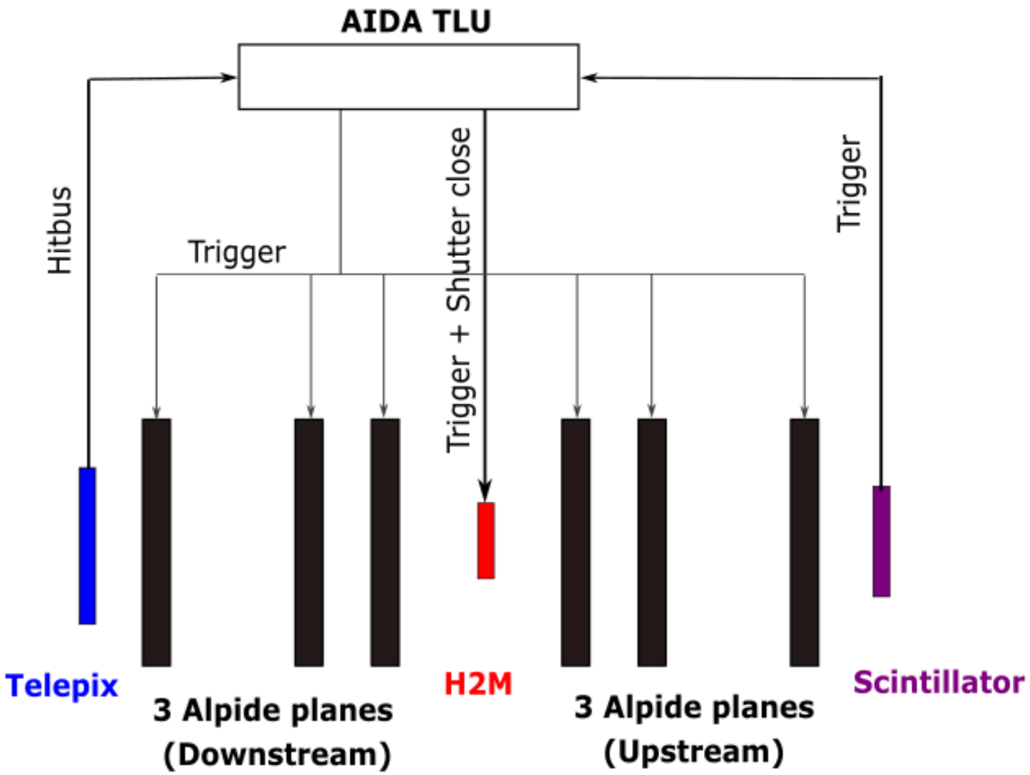


↪ **ToT distribution** used to tune the krummenacher current.

ToT mode works!

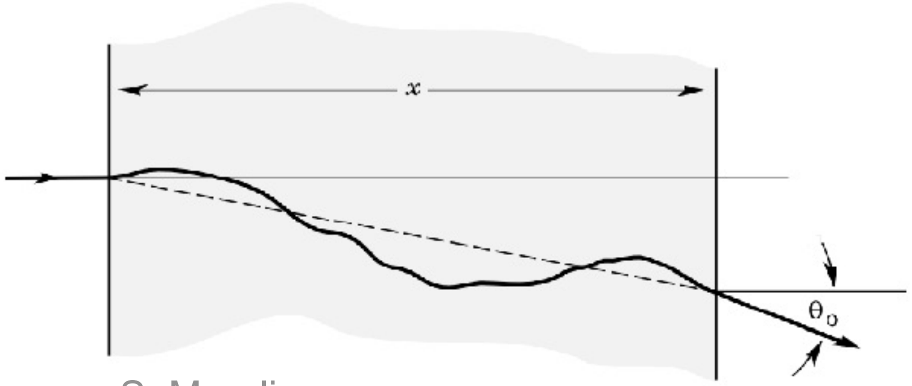
- We also recorded data for different thresholds and bias voltages → analysis is ongoing.

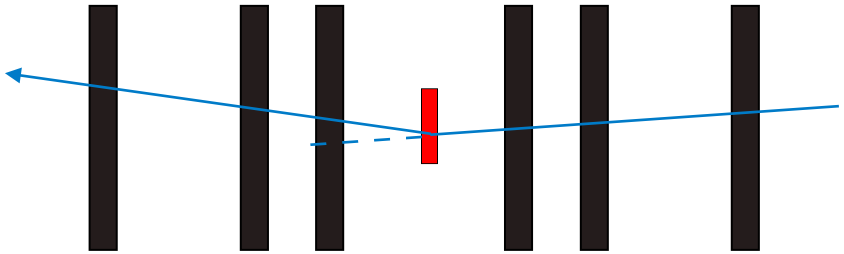
Test Beam Measurement @ DESY

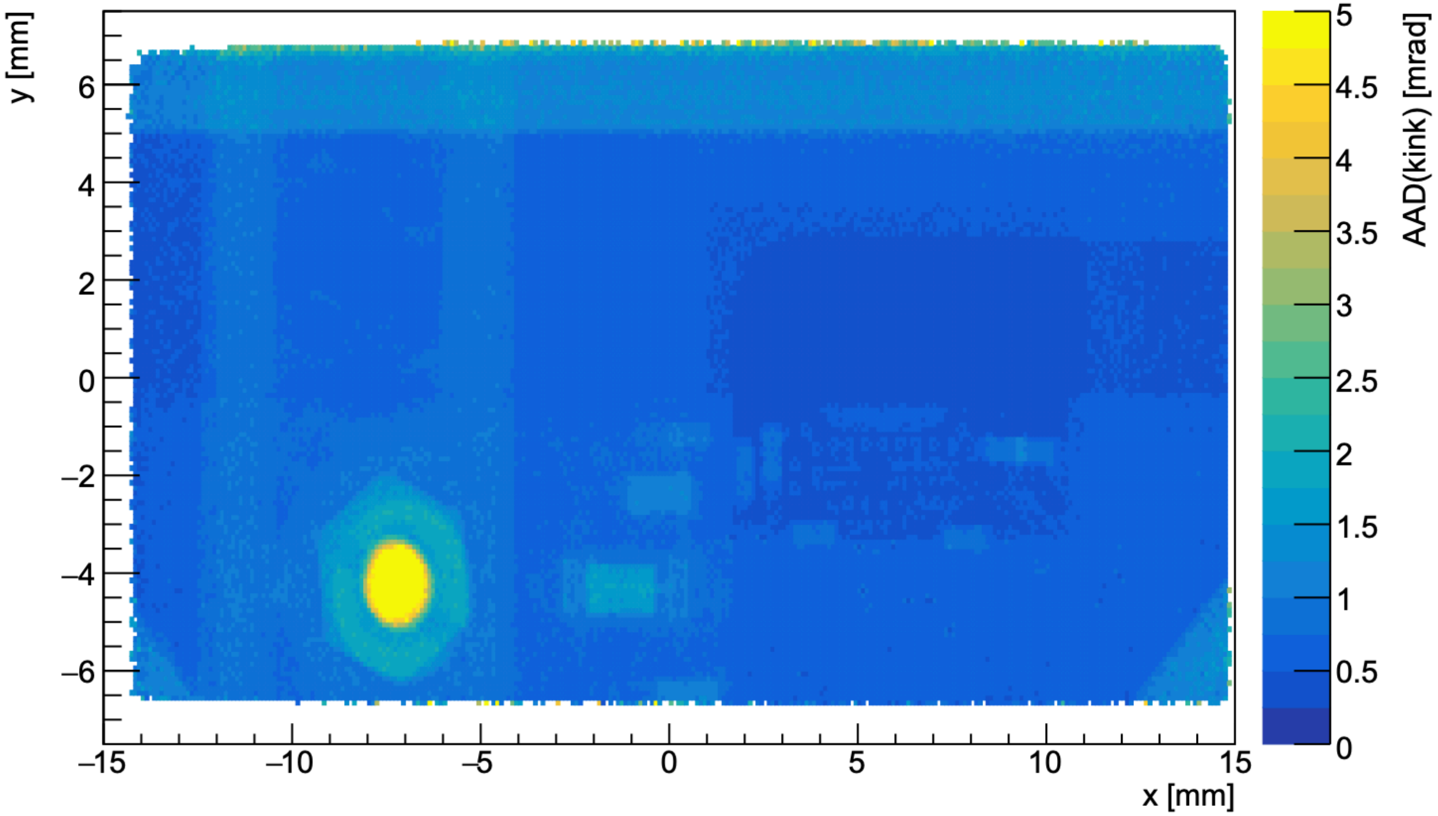


- **Trigger Logit Unit (TLU):** provides global clock (40 MHz) and T0 to all devices.
- **Trigger signal:**
  - Coincidence of Telepix AND scintillator
  - ROI defined on Telepix
- **H2M:**
  - ToA mode
  - Shutter opened after previous readout
  - Shutter closed with trigger signal
  - Readout time ~ 500 μs

Alignment of the DUT

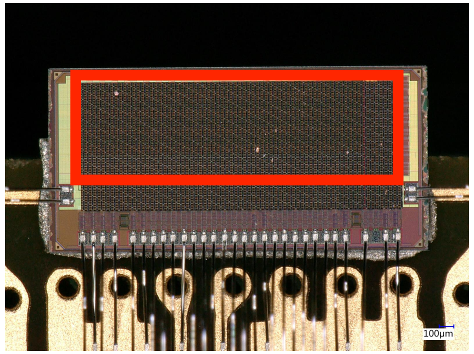




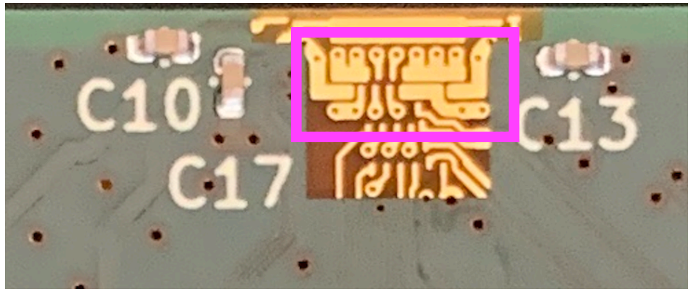


- Relative alignment to triggers using **material budget imaging.**
  → Large kink angles corresponds to regions with high material budget.

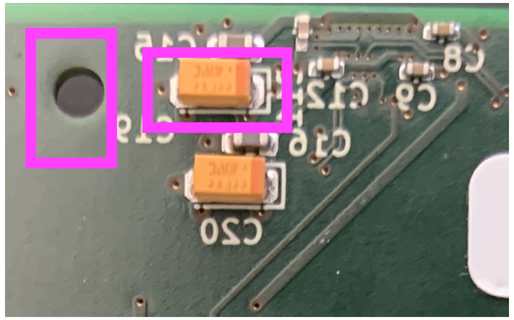
Alignment of the DUT

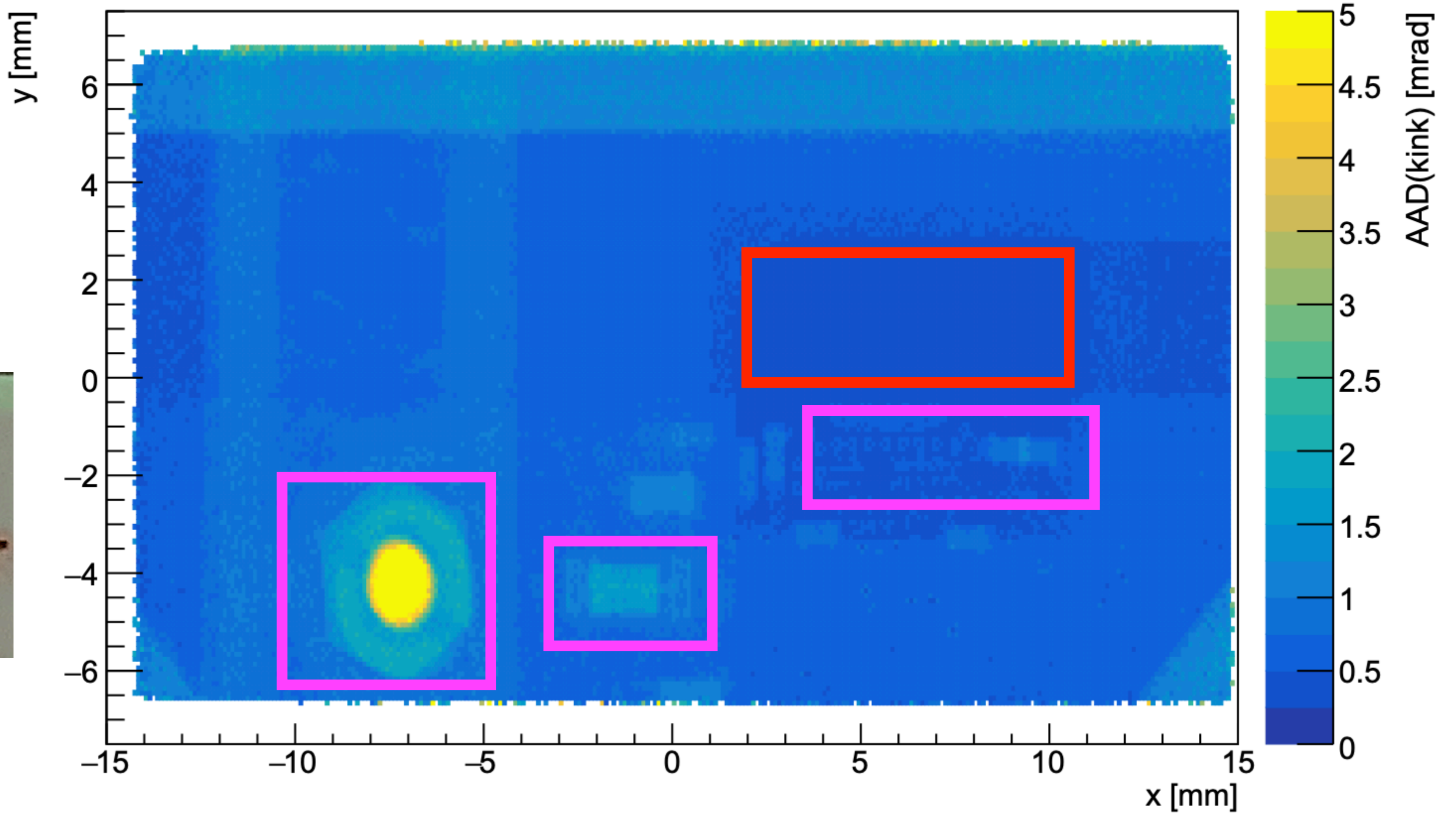


Chipboard front side



Chipboard back side

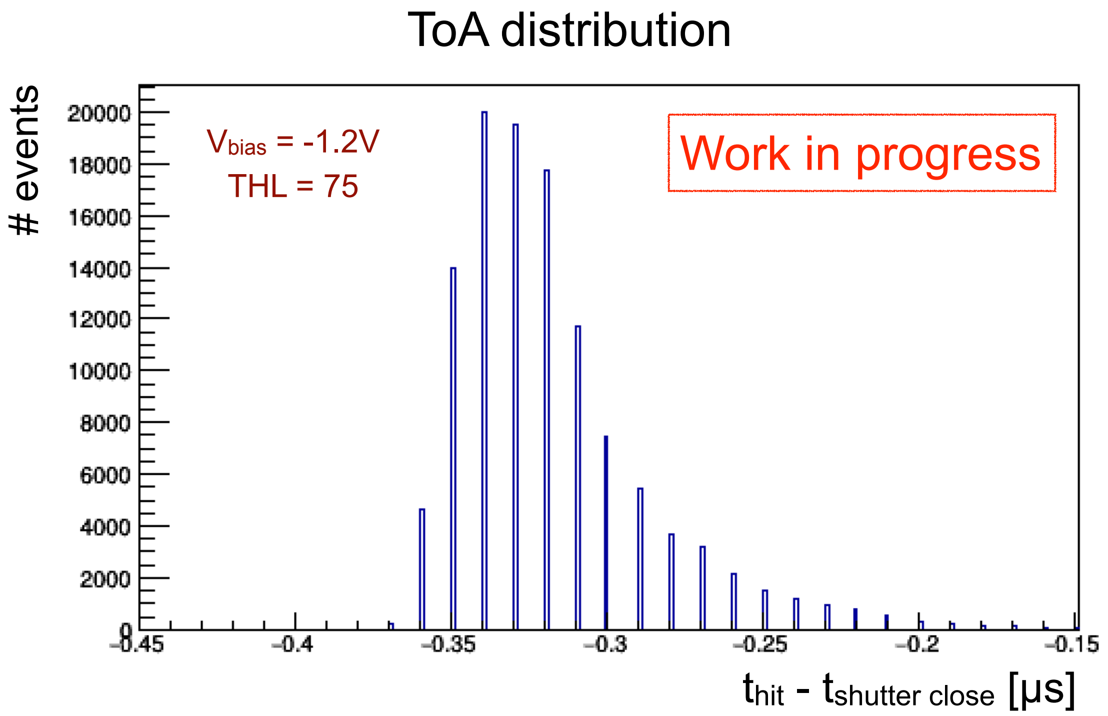


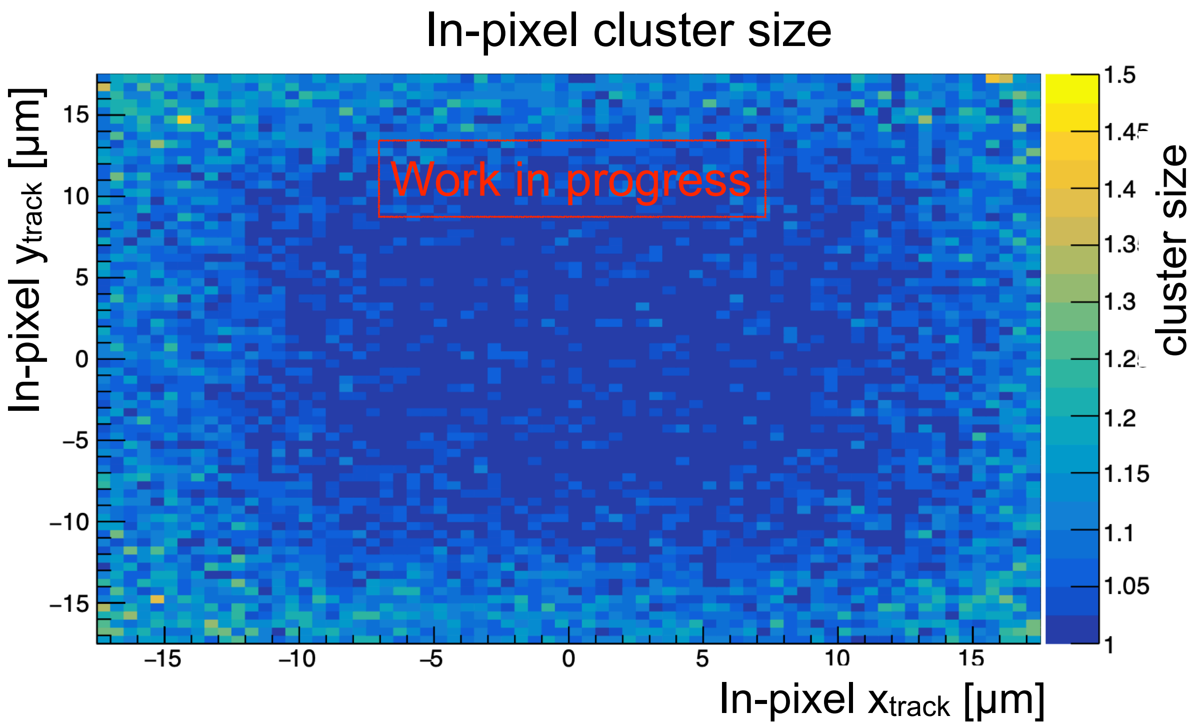


- Identification of elements in the chipboard.

Ready to take data!

ToA and cluster size distribution





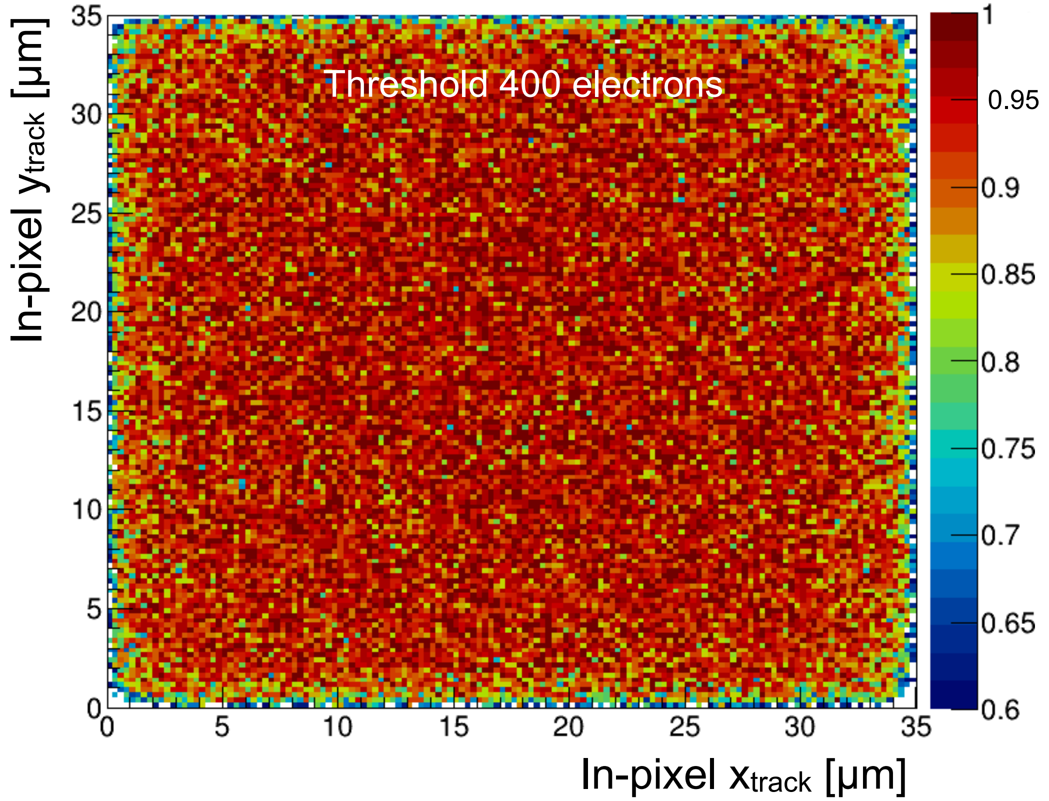
- **Dominated by 25 ns trigger binning** → can be fixed in the analysis with scintillator timestamp.

- Dominated by **cluster size 1.**
- Larger cluster size in the edges and corners due to charge sharing.

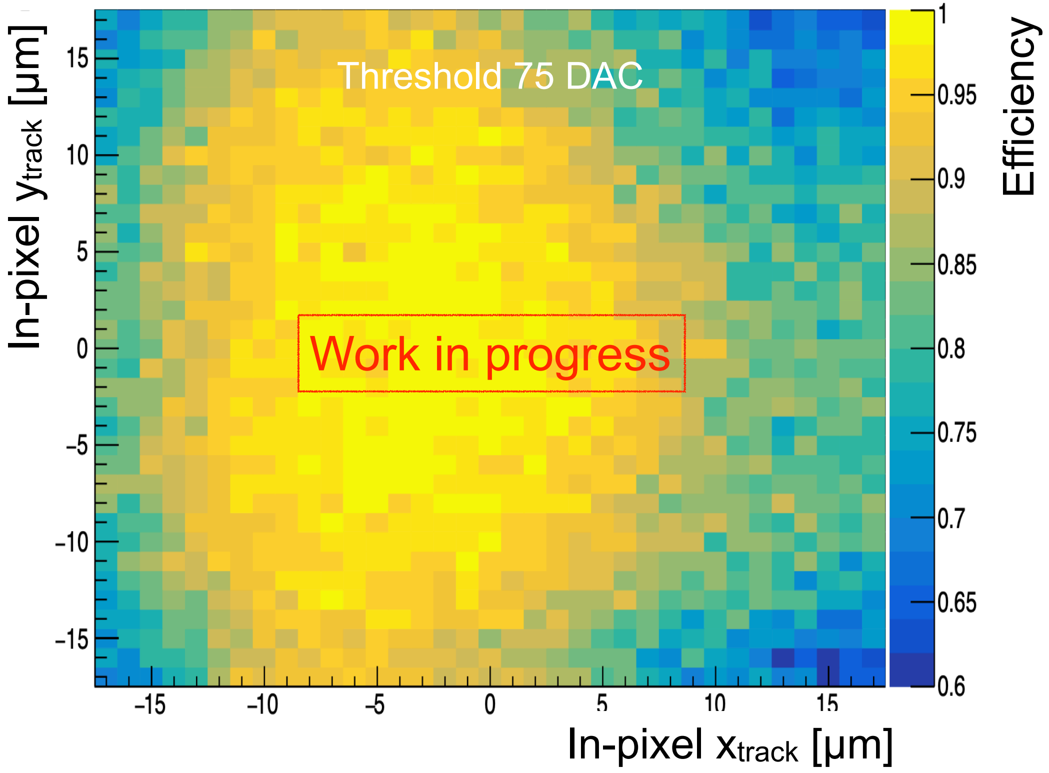
ToA mode works!

In-pixel efficiency map

In-pixel efficiency map (Simulations)

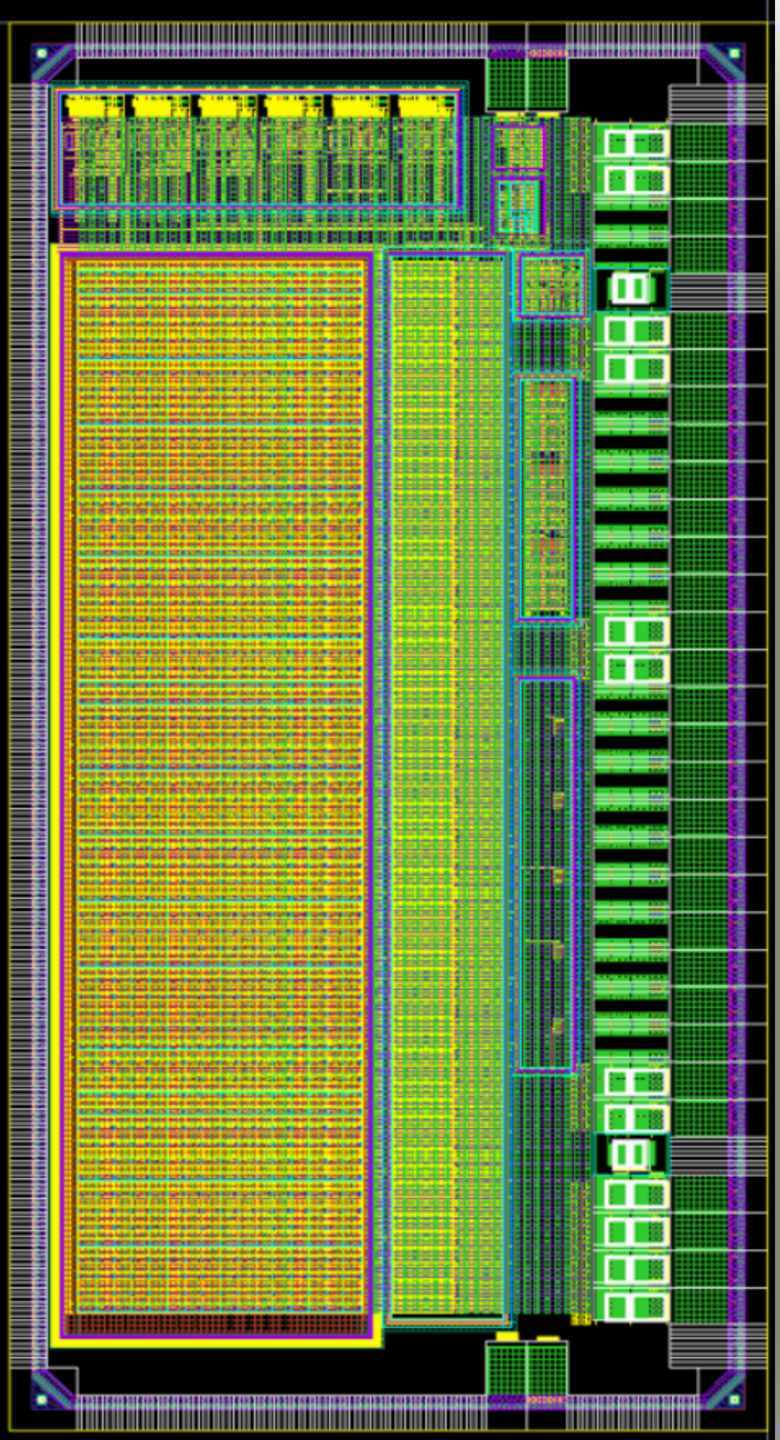


In-pixel efficiency map (Data)



- **Observed an in-pixel efficiency map pattern**

  → Seems related to where the analog and digital front-ends are placed. Work in progress
- Same effect is observed for different bias voltages and hit detection thresholds. Also at the SPS test beam.



Summary & Outlook

Summary

- **Full hybrid design ported to monolithic pixel sensor chip design a 65 nm CMOS imaging process.**
- Successful first **lab measurements**.
- **First test beam campaigns at SPS and DESY.**
  - ✓ **Slow control** (read/write registers).
  - ✓ **ToT and ToA** modes tested.
  - ✓ **Integration** with the reference places and trigger signal.
  - ✓ **Digital and analog circuities** working as expected.

Outlook

- **Understanding of the efficiency patterns.**
- Continuing test beam **analysis.**

- **Four more weeks of test beam** in 2023.
- **Optimisation** of the parameters + calibration.
- Testing the **triggered** and **photon counting modes.**

Thank you!

Contact

Deutsches Elektronen-Synchrotron DESY

www.desy.de

Sara Ruiz Daza

sara.ruiz.daza@desy.de