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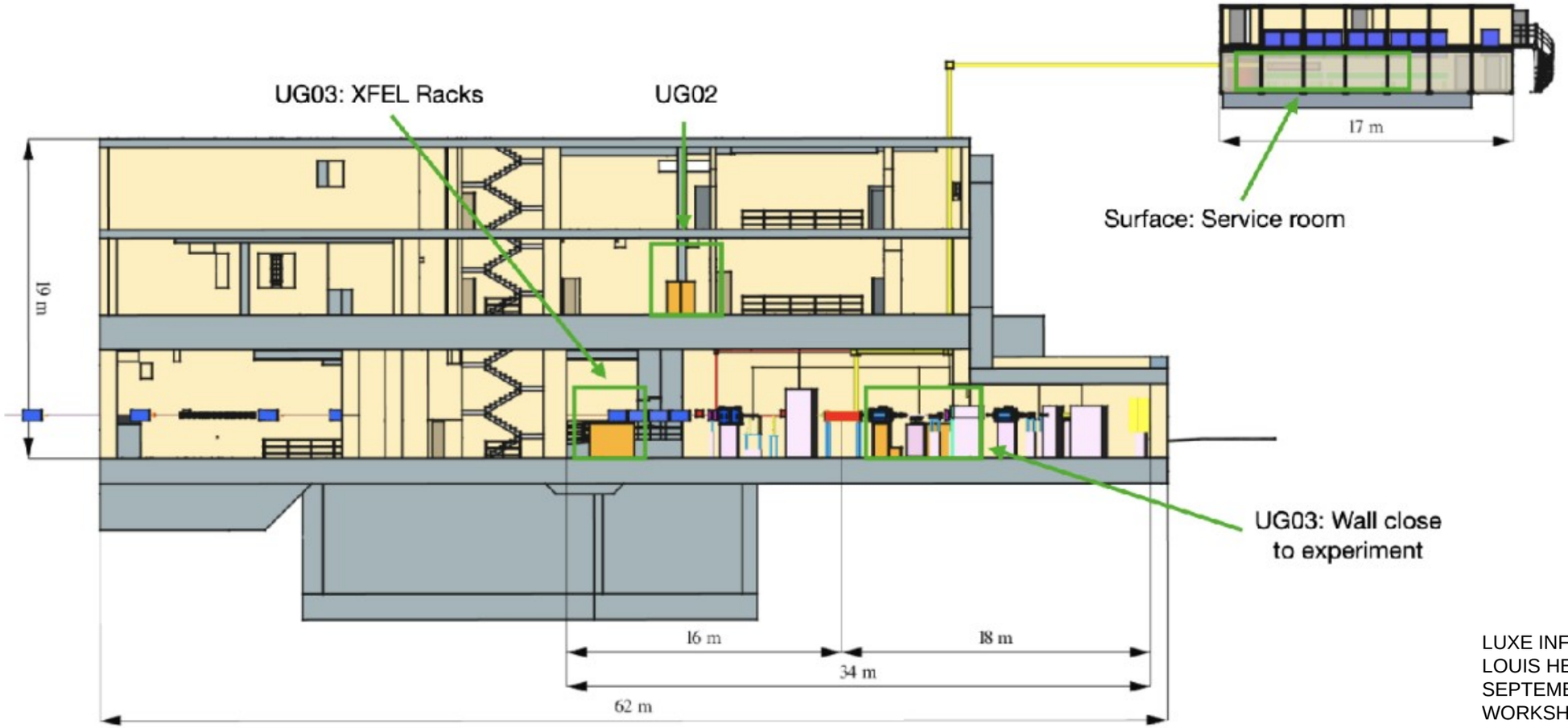
ECAL-P readout status

ECAL working group meeting 2023.10.25

- **<u>FLAXE fabrication just started recently</u>**
  - We do not know the detailed schedule yet
  - We just started discussion with packaging company about details (package pinout)
  - As soon as the package pinout will be finalized we can start FEB design
- I have prepared the backed electronics concept – details in this talk



- **Position foreseen for backend electronics:**
  - In UG03 (not accessible during data-taking).
  - In UG02 (potentially accessible at every time but for short stay and space limited).
  - In surface building (further away), space to be understood.

Area	Length
UG03: Side north wall	7 m
UG03: EuXFEL rack	16 m
UG02	26 m
Surface: service room	≈ 50 m

FLAXE ASIC requires six signals:

- Main clock (20 MHz)
- Acquisition control (aka. pre-trigger)

} Common for all FEBs

- Reset (slow, asynchronous, no timing requirements)
- Data bus:
  - SCK (data clock, independent from main clock)
  - MOSI (data from FPGA to FLAXE)
  - MISO (data from FLAXE to FPGA)

} One bus per FEB
40 buses in parallel

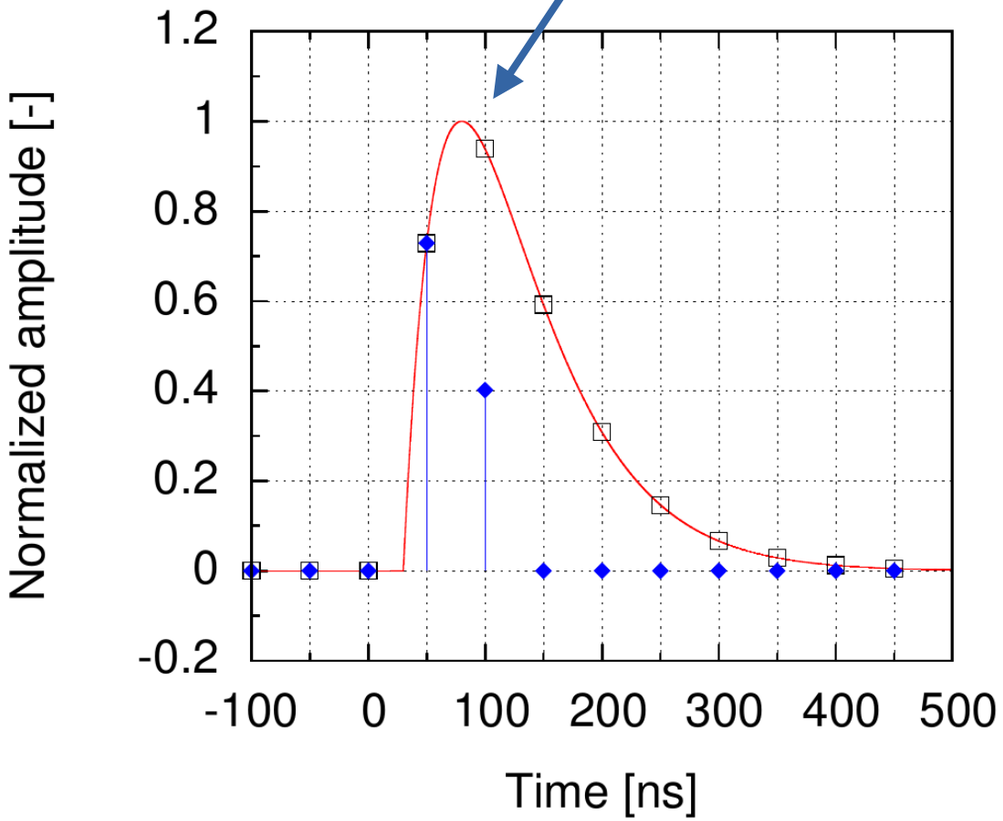
We decided to distribute separate reset lines to each FEB:

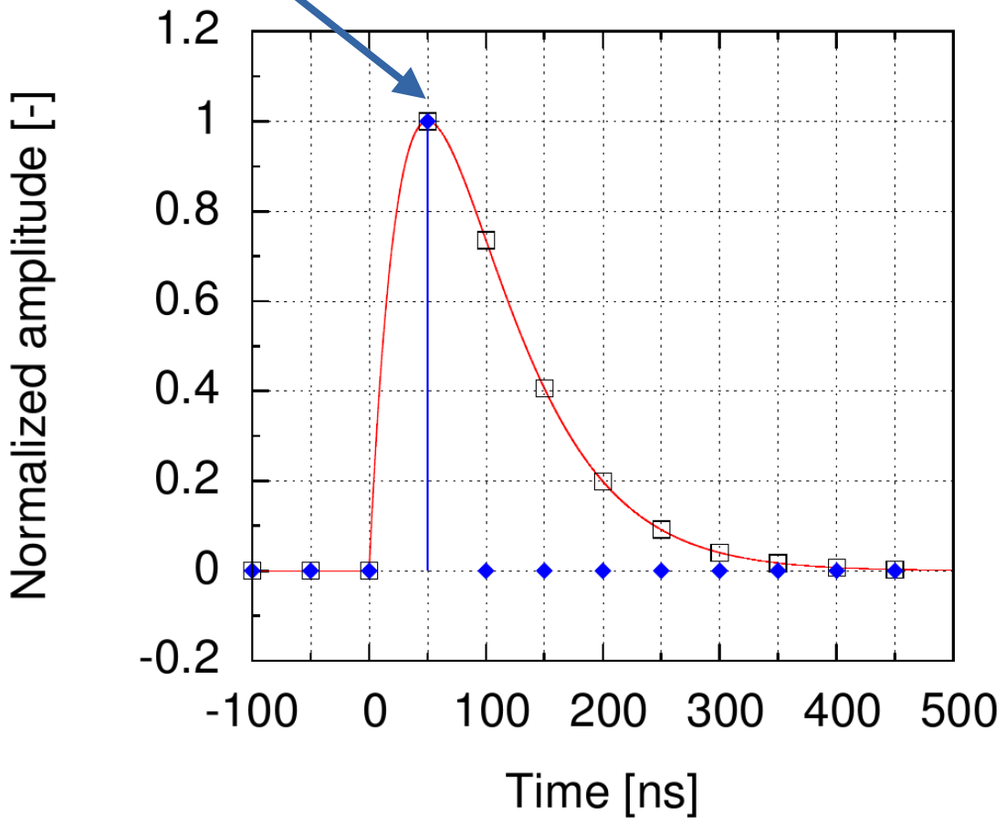
- We can reset only a selected FEB, not the whole ECAL-P
- It will be difficult to achieve higher granularity (like one reset per sensor or ASIC) and we do not think it is necessary

After meeting in Weizmann we now know we can run readout in synchronous mode during the experiment:

- One sample directly at pulse maximum → amplitude from simple pedestal subtraction → better SNR

We still need asynchronous mode (and reconstruction) for testbeam and cosmic muons





For synchronous mode we need precise clock distribution:

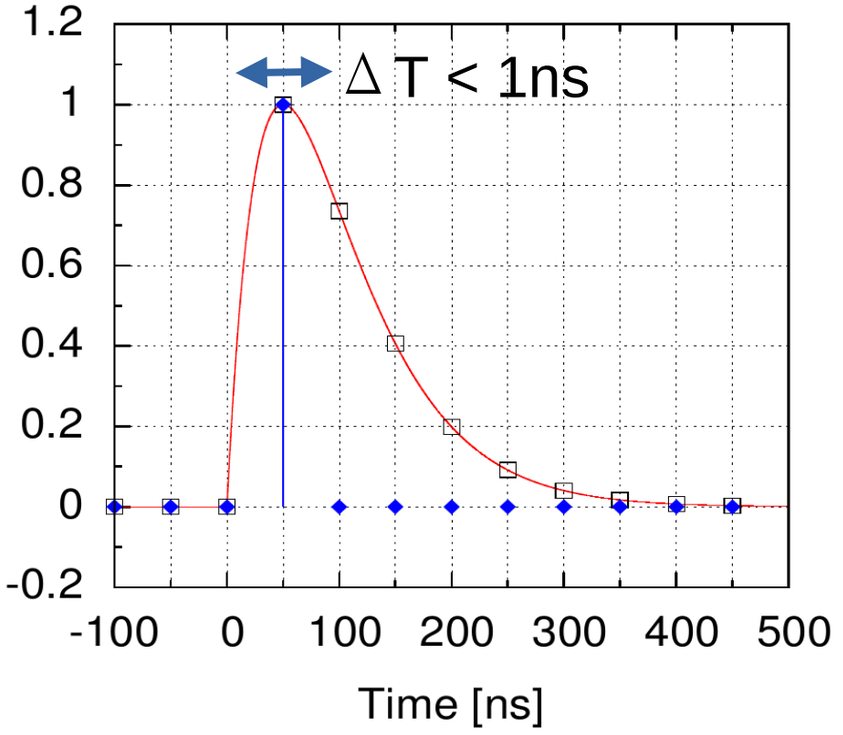
- Skew between all FLAXE ASICs in whole ECAL-P
- Clock phase drift in respect to machine clock

} below 1 ns (±500ps)

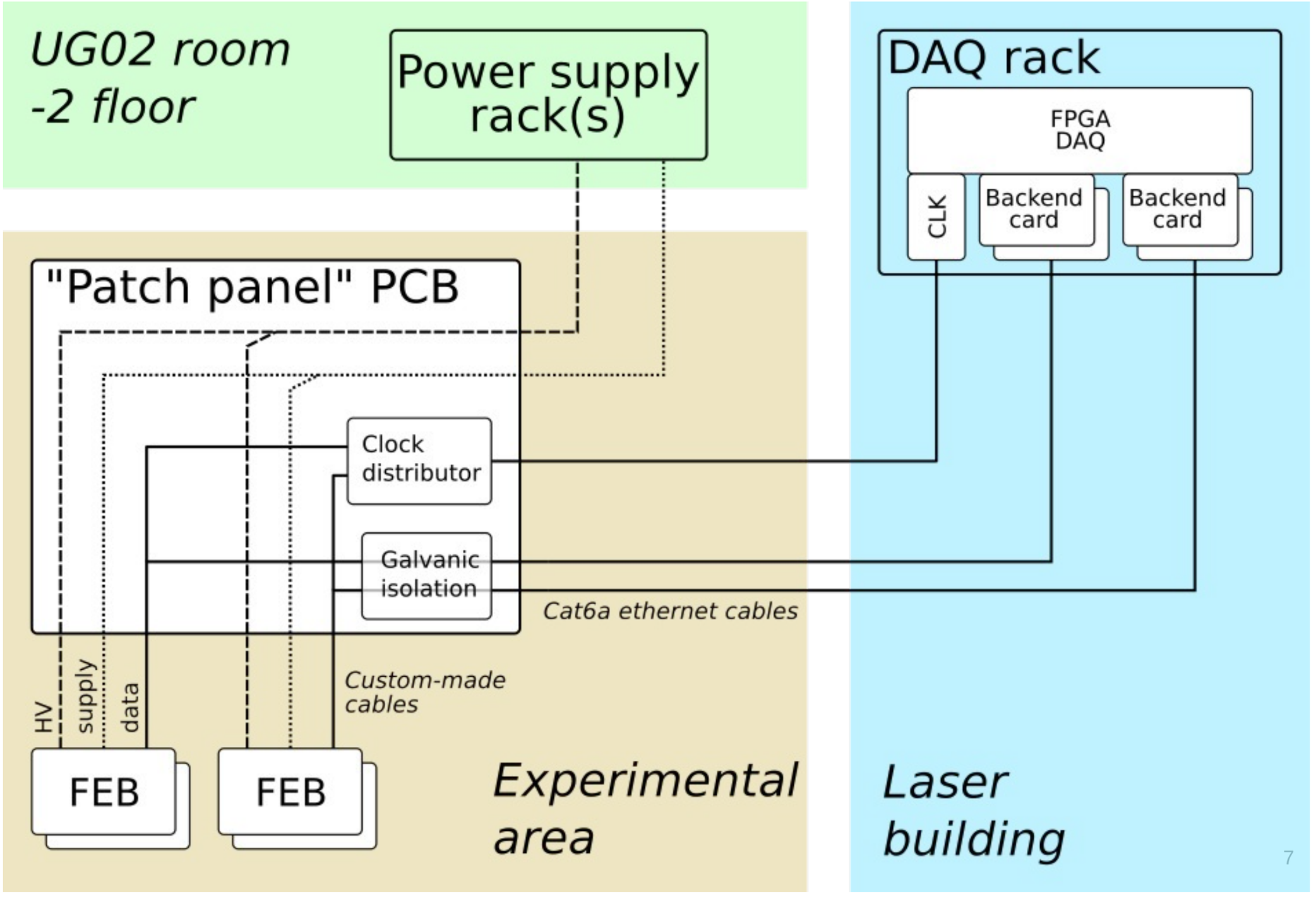
We need to create clock from main 45MHz LCS clock with configurable phase shift

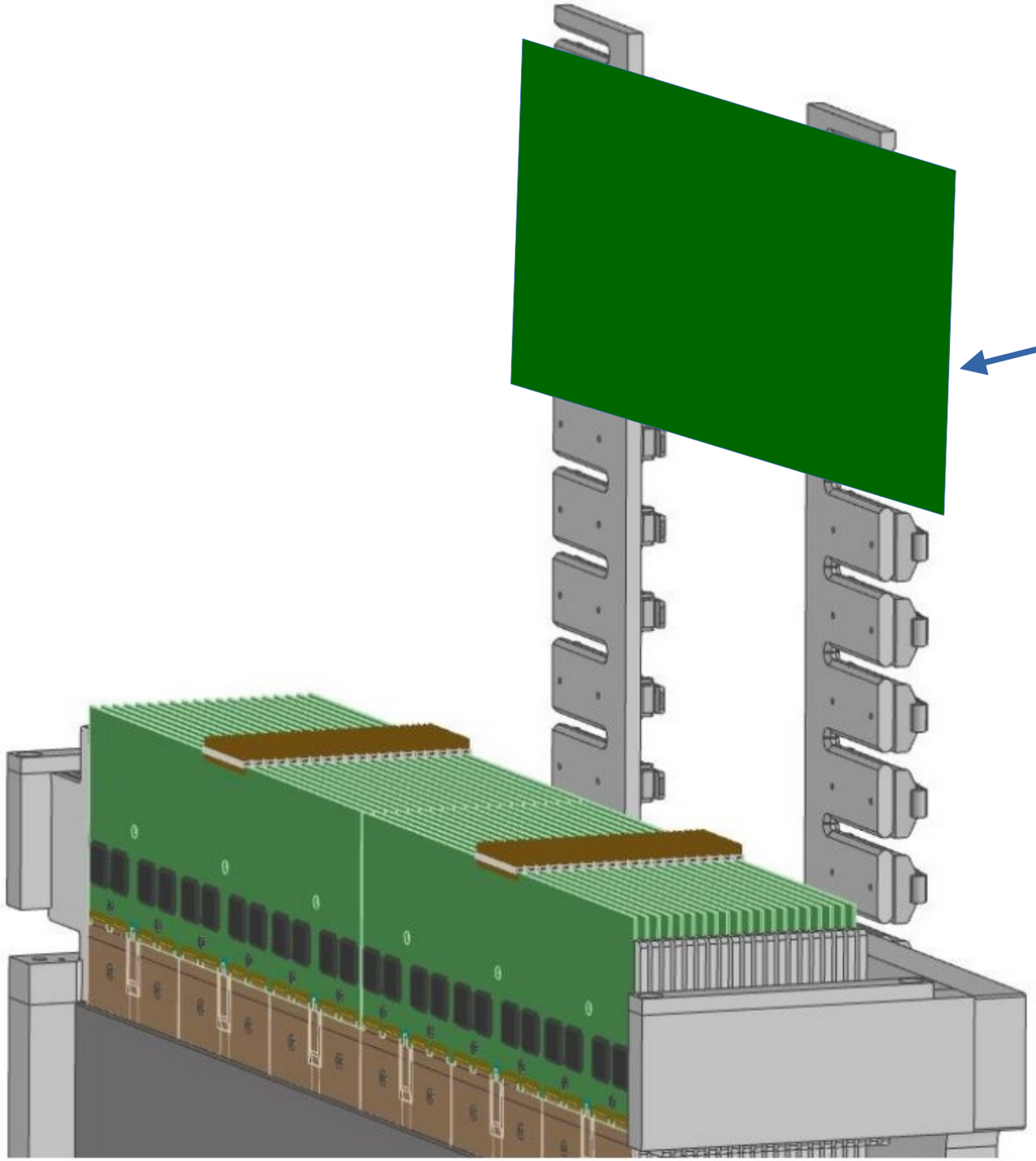
- Sophisticated PLL directly controlled by the FPGA

We need to create 40 copies of the clock → one per each FEB



To keep the skew and drift as low as possible we should keep the length of the parallel clock distribution as short as possible → clock distributor close to the FEBs


UG02 room
-2 floor
Power supply
rack(s)
DAQ rack
FPGA
DAQ
CLK
Backend
card
Backend
card
"Patch panel" PCB
Clock
distributor
Galvanic
isolation
Cat6a ethernet cables
HV
supply
data
Custom-made
cables
FEB
FEB
Experimental
area
Laser
building



Warsaw proposed new hood (top cover) design.
We can put the “patch panel” PCB on the back side, roughly in the orientation presented here.

Custom ribbon cables will be short and contained inside hood.

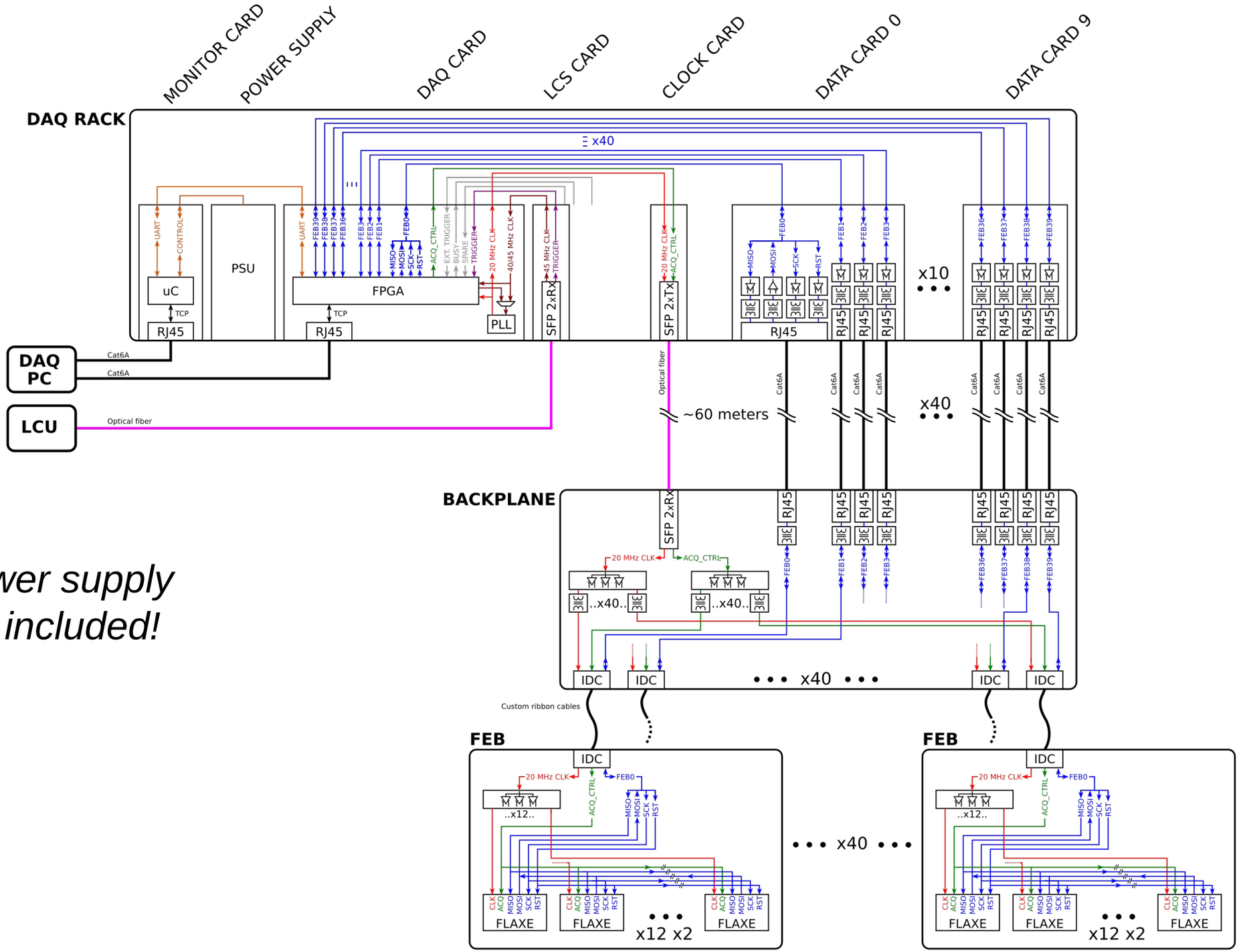
From the patch panel PCB we can use commercial cables:

- To HV/LV rack
- To DAQ backed

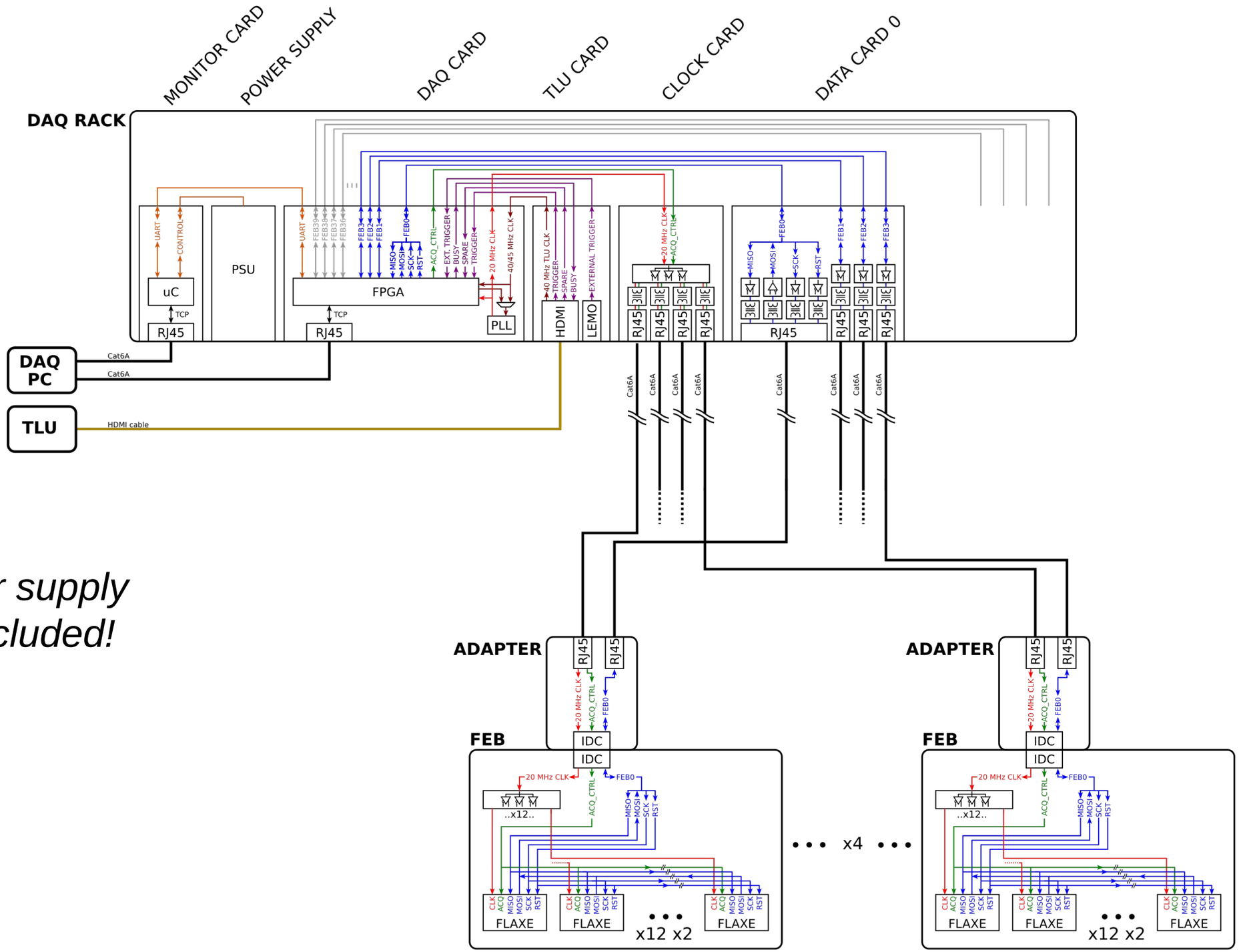
There is one unresolved issue:
How to send main clock for ~60 meters with <1ns drift?

- Optic fiber is difficult for such low frequency (20 MHz)
- Copper coaxial cabel:
  - Typical drift of around 1ps / m K
    For 100m long cable and 10 ^{O}C temperature change – already 1 ns

We are searching for solutions, all inputs well welcome!



Power supply not included!



Power supply not included!

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EXPERIMENT

Remote control

Power supply

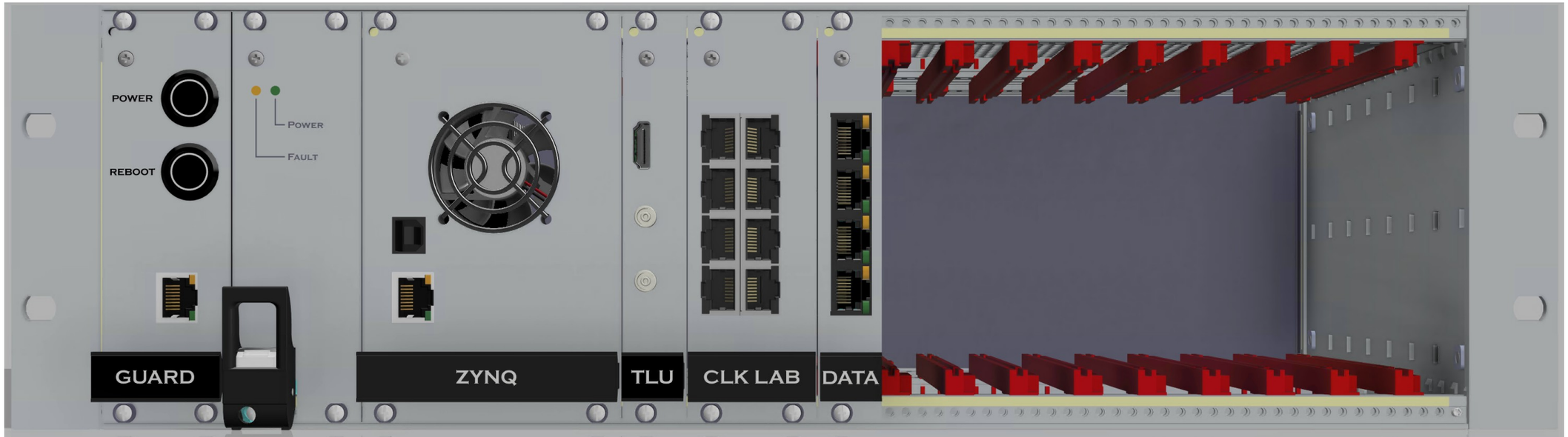
DAQ (FPGA)

LCS or TLU

Clock distrib.

Data and reset cards, one card per 4 FEBs

LAB/TESTBEAM



Currently we want to make one, prototype rack.

Finally:

- Two “experiment” type racks – one working in experiment, one spare
- Three “lab” type racks:
  - 1 for Valencia
  - 1 for Tel-Aviv
  - 1 for Krakow and initial testbeams

Questions:

- Does anyone else need the “lab” type rack?

- The "Lab" type will allow a maximum of **8** FEBs to work in parallel. Is it enough?

- Any input (or contact to expert) about precise clock distribution over long distances well welcome!