Design of a monolithic digital SiPM-IC in 150-nm CMOS technology

In house-design

Presentation for the retreat of the detector platform

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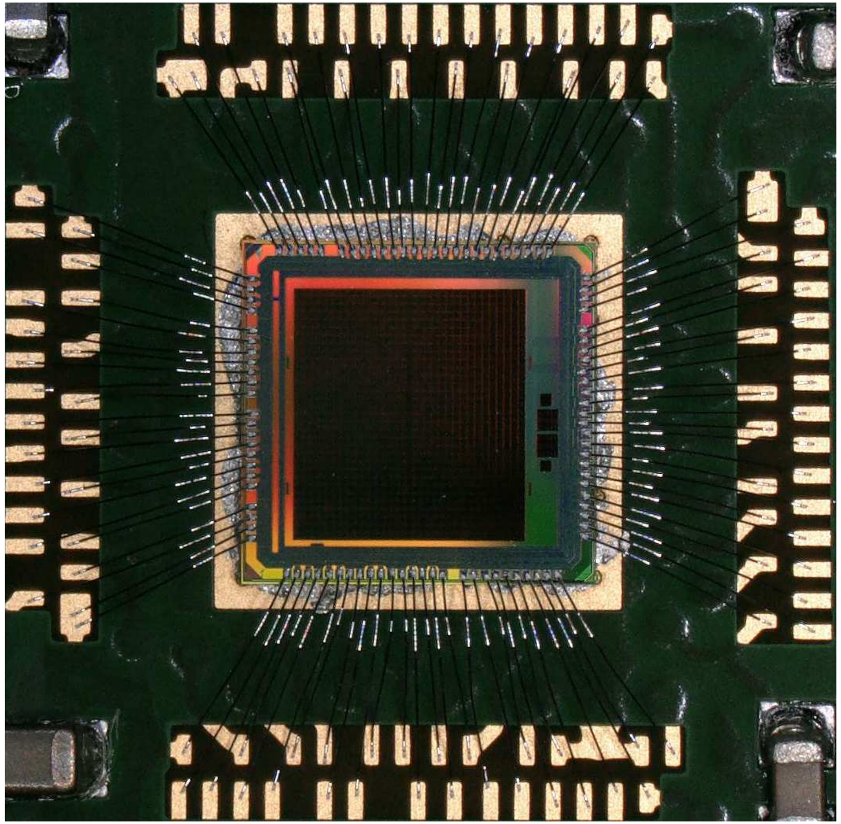
HELMHOLTZ

DESY.

Outline

- Introduction to Silicon photomultipliers
  - What are SiPMs?
  - Why going to „digital“?
- DESY’s 32-by-32-pixel digital SiPM-IC
  - Features
  - Circuit blocks description and characterization
- Lab measurements
  - With Caribou DAQ system
  - With laser source
  - In dark environment
- Conclusion

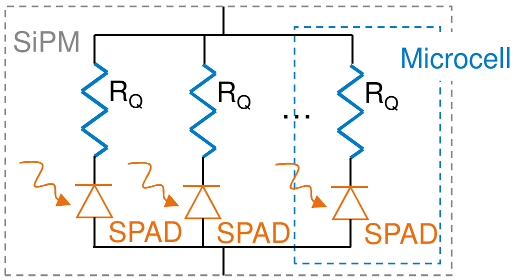


Silicon photomultipliers (SiPM)

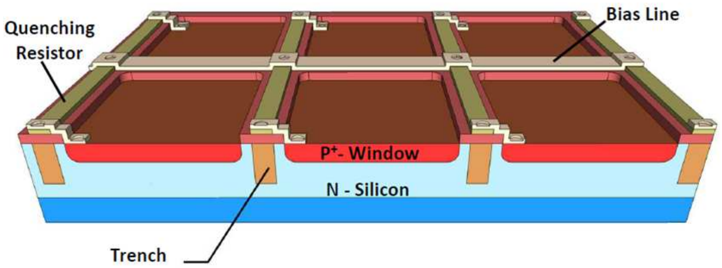
What are SiPMs?

- SiPMs are solid-state single-photon-sensitive devices based on single-photon avalanche diodes (SPADs) implemented on common silicon substrate.
- Each SPAD is biased above breakdown voltage and operates in Geiger mode with typical gain of 10^5 to 10^6.

Analog SiPM



Section of KETEK SiPM Microcell



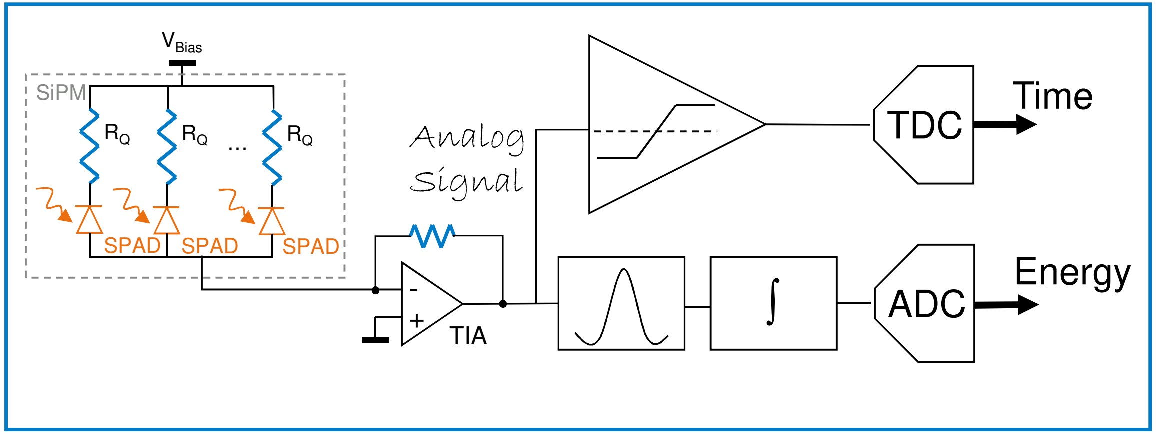
- Arrays of many SPADs, each one with its integrated passive-quenching resistor, labeled as microcells
- All microcells connected in parallel to a common anode and cathode
- The output current of the SiPM is the sum of all the cells, giving a signal proportional to the number of detected photons.

SiPMs

Digital SiPMs

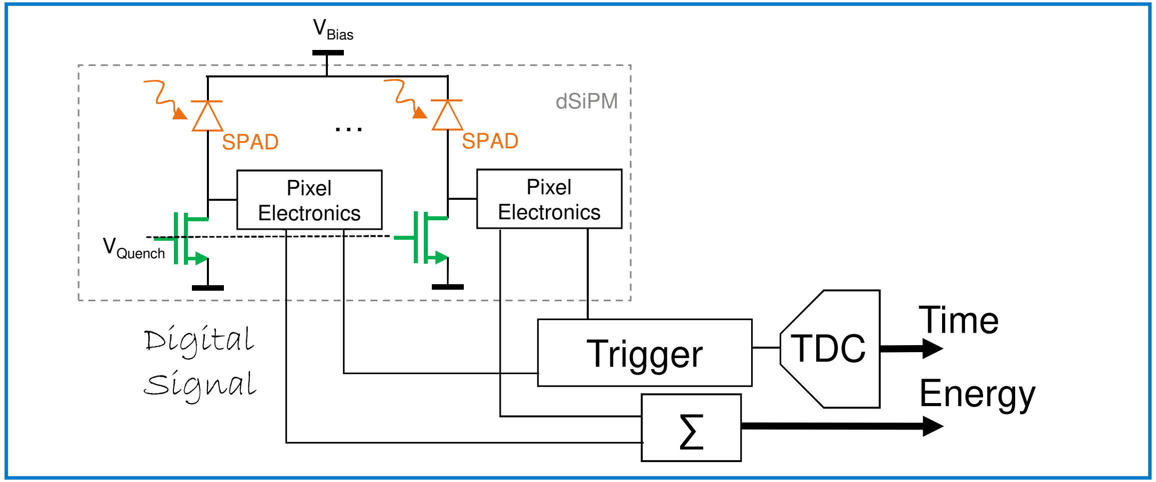
Challenges of "classical" analog SiPMs

- Analog output requires digitization in electronics
- Often sizeable noise rates (typically kHz/mm²)
  - Very often dominated by a few pixels
- No information which pixel was hit



Possible solution: Digital SiPMs

- Take advantage of SiPMs digital nature
  - Small quenching circuitry
  - Inverter as event discriminator
- Photon or hit counter, within pixel possible
- Possibility to switch off noisy pixel
- Hit map readout



32-by-32-pixel digital SiPM-IC

Overview

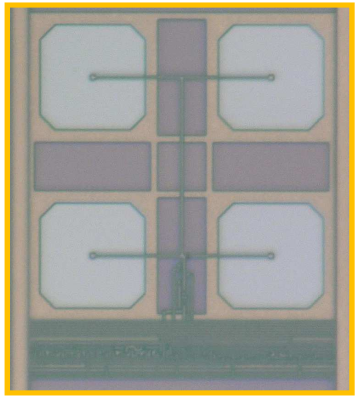
Layout

- 32 x 32 pixels (1 pixel = 4 SPADs)
- In LFoundry's 150-nm CMOS technology
- 70-µm pitch

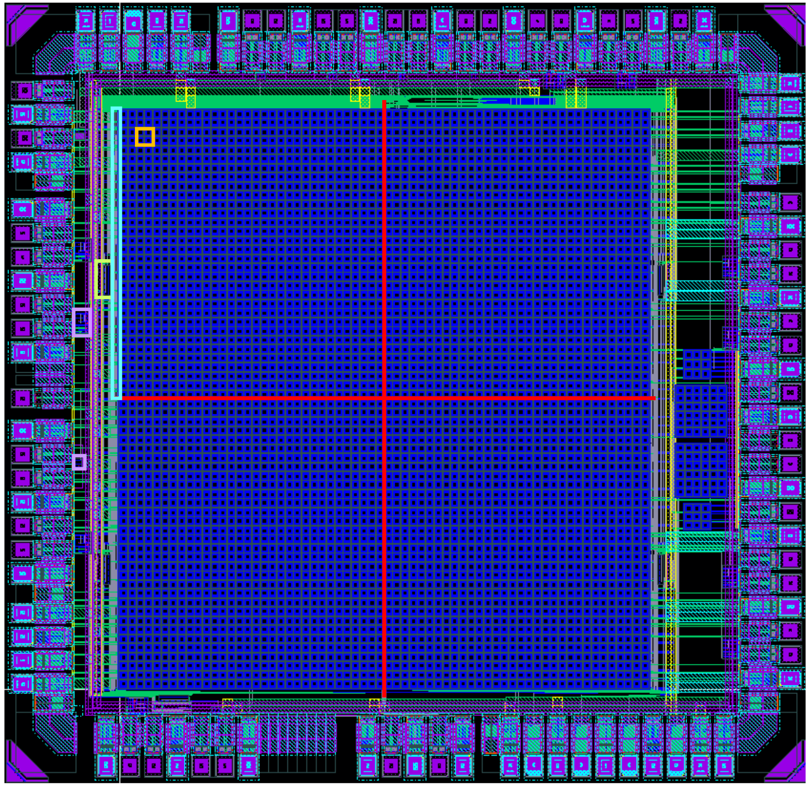
Features

- Full hit matrix readout
- Pixel masking
- Time stamping per quadrant
  - 12-bit TDCs with <100-ps timing resolution
  - Validation logic with adjustable settings
- 1-Gbps LVDS links

69.6 x 76 µm²



ca. 3400 x 3300 µm²

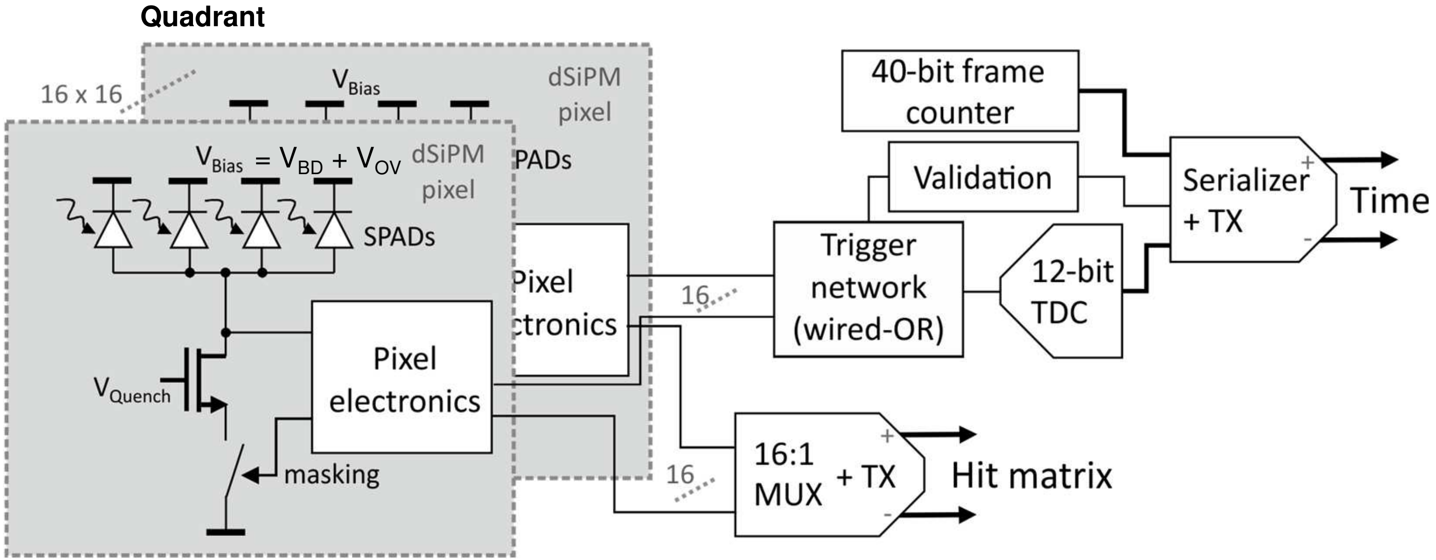


32-by-32-pixel digital SiPM-IC

Quadrant block scheme

The IC is divided into four quadrants

- Outputs of all pixels are combined in a wired-OR
- Fastest pixel signal triggers a running 12-bit TDC
- Validation logic to discard undesirable events
- Hit matrix is readout via a 16-to-1 multiplexer
- Frame-based readout



dSiPM pixel electronics

- Common readout of 4 SPADs
- 3.3-V NMOS transistor front end allowing an overvoltage of max. 3.6 V
- Quenching performed by a globally biased transistor
- Inverter as comparator stage for digital pulse shaping
- SRAM cell for masking
- Deadtime: min. 25 ns
- Power: 10 µW
- Area: 400 µm²

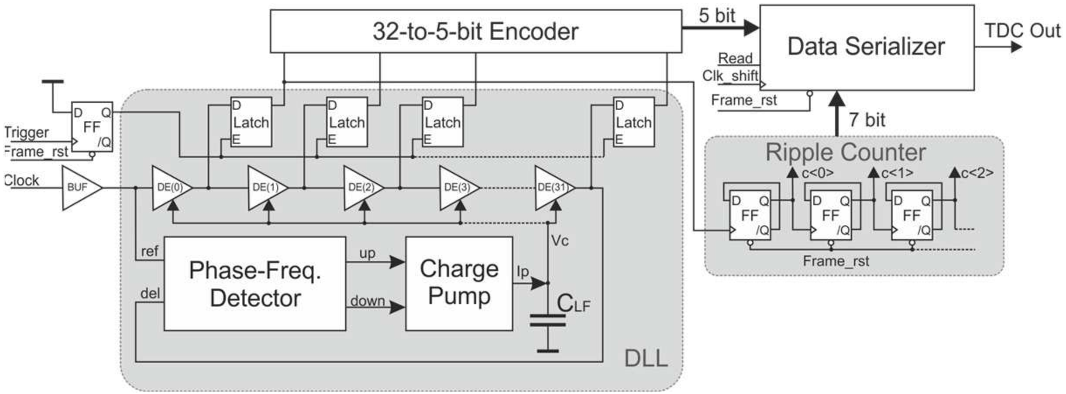
Data rates @ 3-MHz frame clock

- Hit data: 4 * 816 Mbps
- Timing date: 408 Mbps
- Total sustained data throughput of 4 Gbit/s @ 3-MHz frame rate

32-by-32-pixel digital SiPM-IC

Circuit blocks:

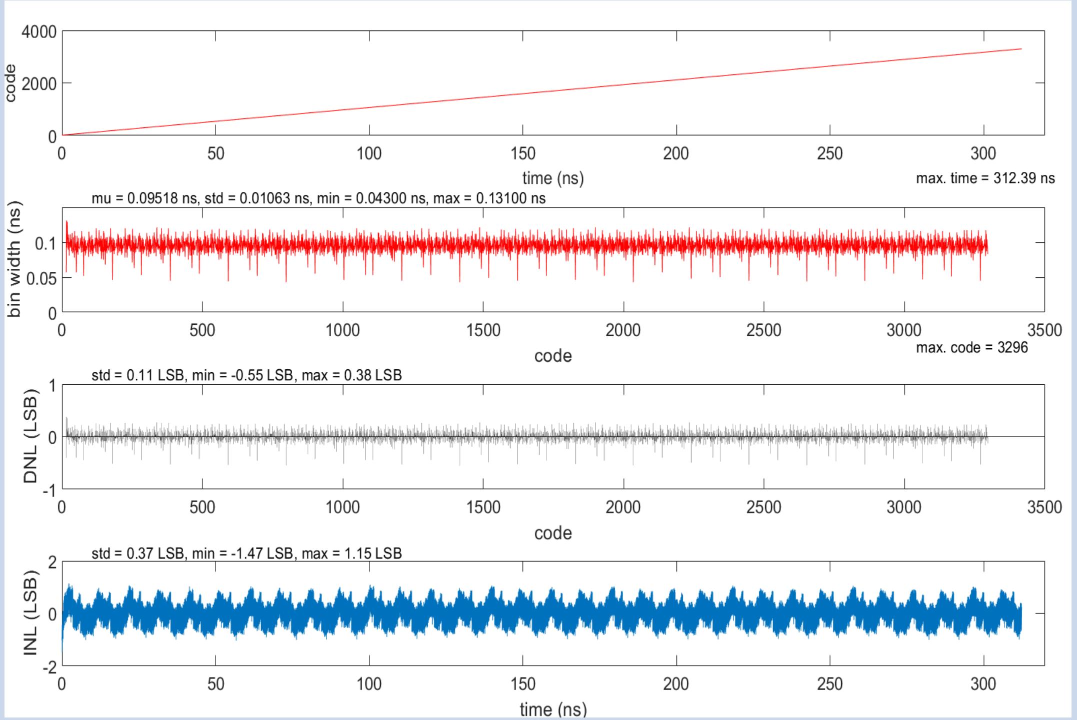
Time-to-digital converter



@408 MHz reference clock

- Time resolution: 95.8 ps, σ = 13.65 ps
- Bit resolution: 11.67 bit
- Dynamic range: 314 ns
- Max DNL = -0.74/0.35 LSB
- Max INL = -1.43/1.39 LSB
- Power: 11 mW @1.8 V
- Area: 78 x 157 µm²

TDC characterization – on separate test circuit of one sample

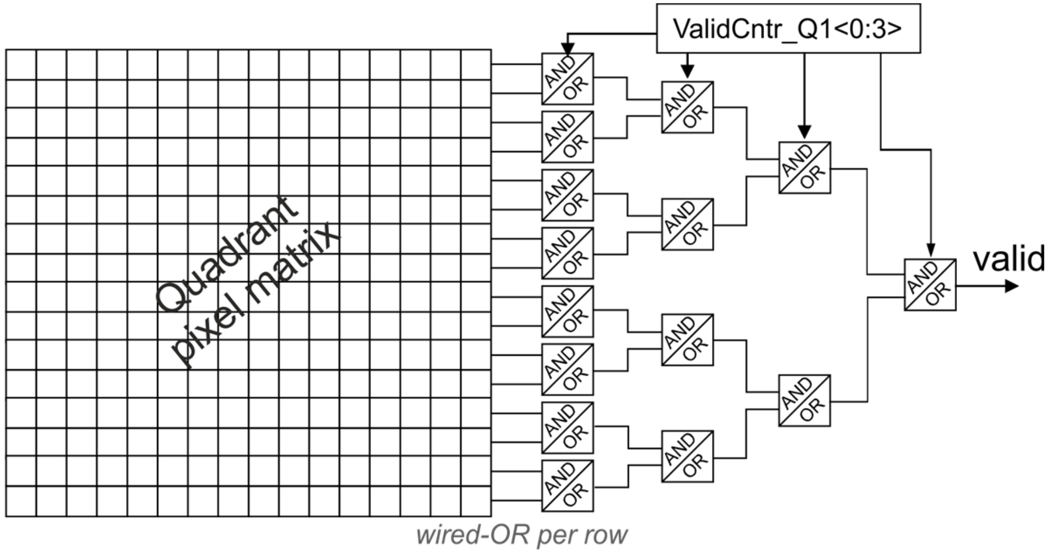


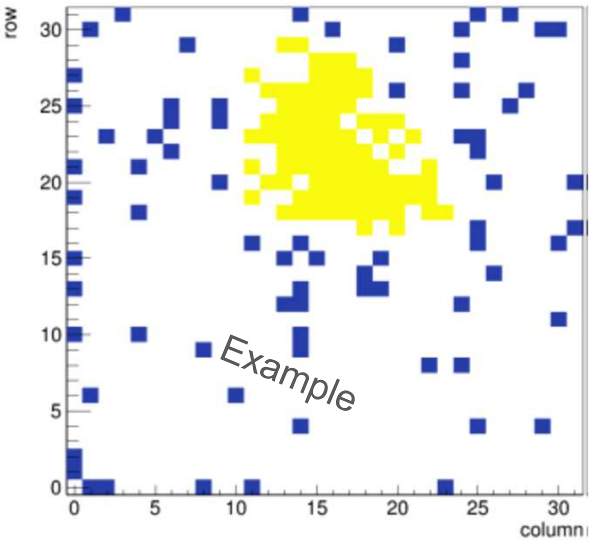
- Trigger input with step size of 1 ps over entire dynamic range
- Bin width: width of each step → time-stamp signal
- DNL: deviation of each bin width to the average value
- INL: deviation to an ideal line fitted into the step curve

32-by-32-pixel digital SiPM-IC

Circuit blocks:

Validation logic





Event validation

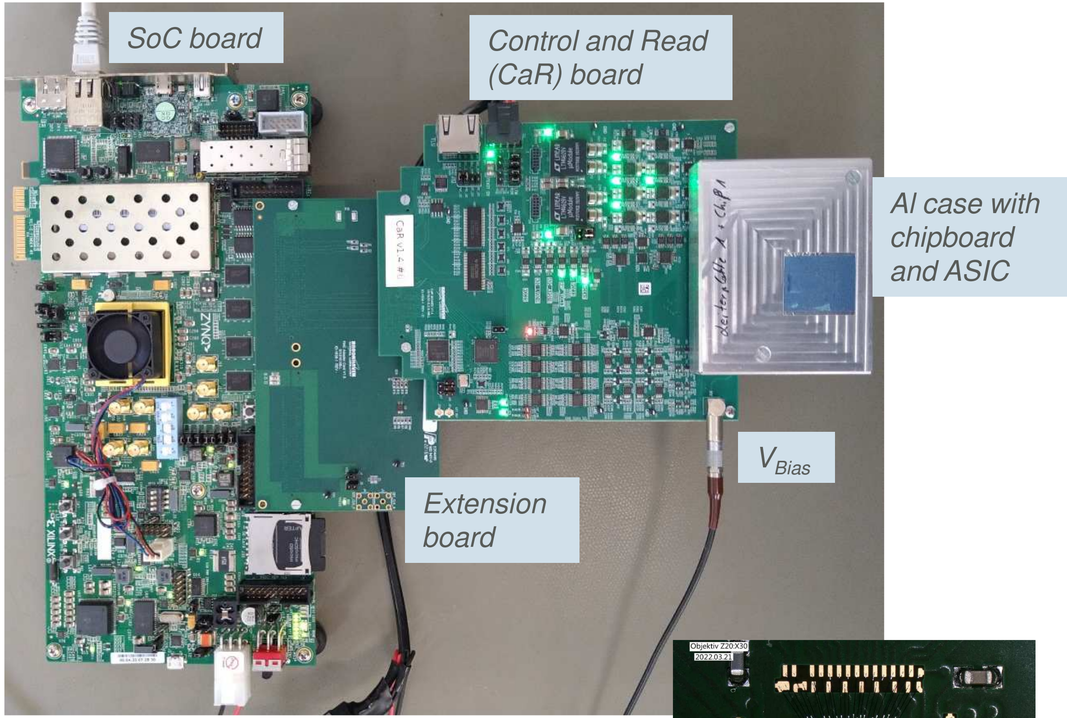
- Four steps
- With each step AND/OR gate configurable

- For cluster identification of simultaneously fired pixel
- For discarding undesirable events

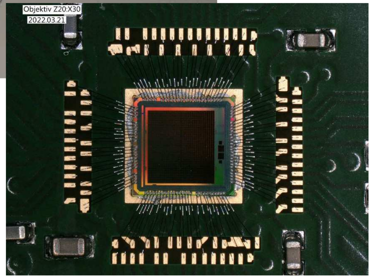
Measurements – in lab

With Caribou DAQ system

- A versatile readout system developed by CERN, BNL, and DESY
- For fast and simple implementation of new detectors
- System on Chip (SoC) Board – CPU and FPGA on same die
  - A CPU runs DAQ and control software
  - An FPGA runs custom hardware for data handling and detector control
- Control and Readout (CaR) Interface Board
  - Physical interface from the SoC to the sensor
  - Peripherals needed to interface and run the chip: power supplies, ADCs, voltage/current references, LVDS links, etc.
- Chip Board – passive & detector-specific components



Lab-test setup



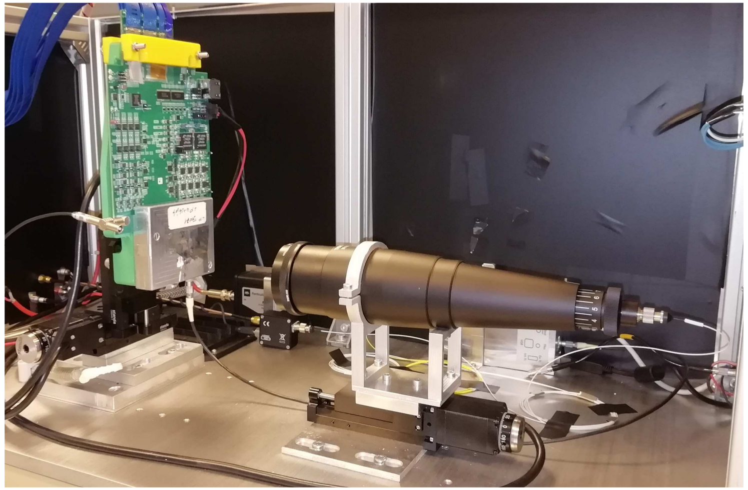
IC on chipboard

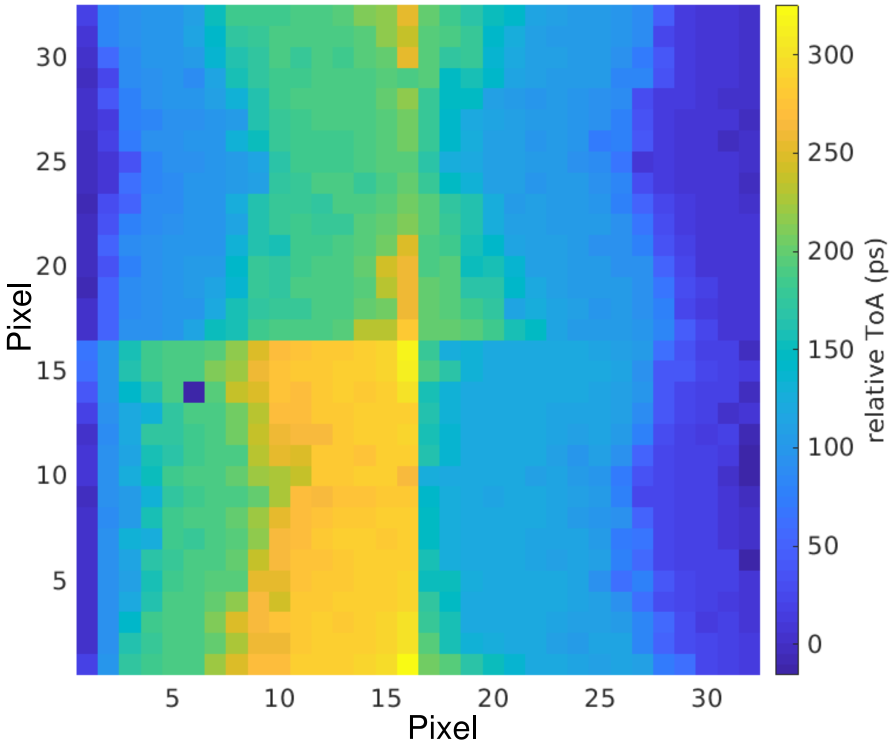
https://doi.org/10.22323/1.370.0100

Measurements – in lab

Propagation delays

- DUT placed on a x-y stage, laser optical system on a z-stage
- 1054 nm pulsed laser, in sync. with the DAQ clock
- Scan chip pixel-by-pixel
  - Only one pixel enabled and directly illuminated
  - Laser spot diameter of ~0.5 mm
  - ToA store
  - Relative ToA = $\mathrm{ToA}_{\mathrm{pixel}} - \mathrm{ToA}_{\mathrm{pixel\ close\ to\ TDC}}$





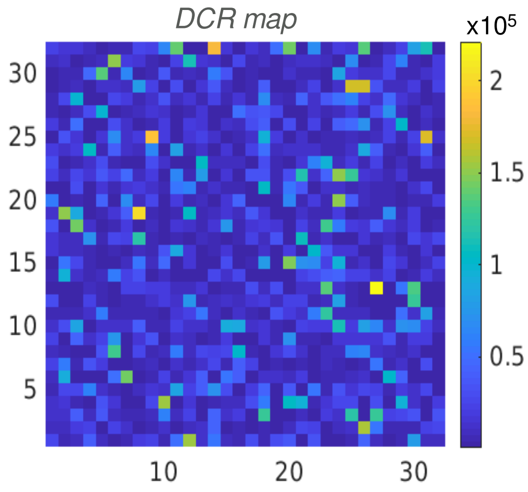
- Clear function of distance to each TDC
- Max. ~326 ps ± 86 ps

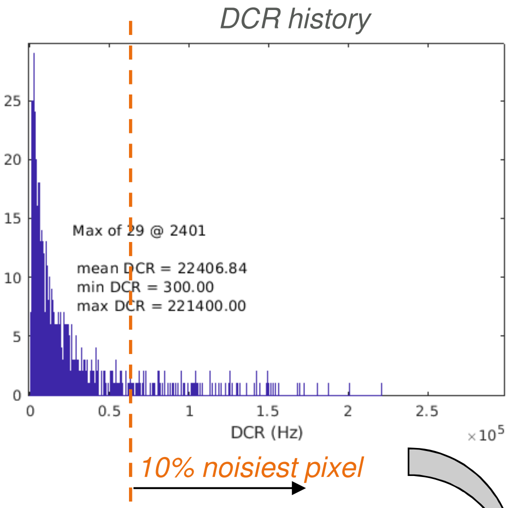
see Daniil's talk: "TCT box: laser box as a user facility"

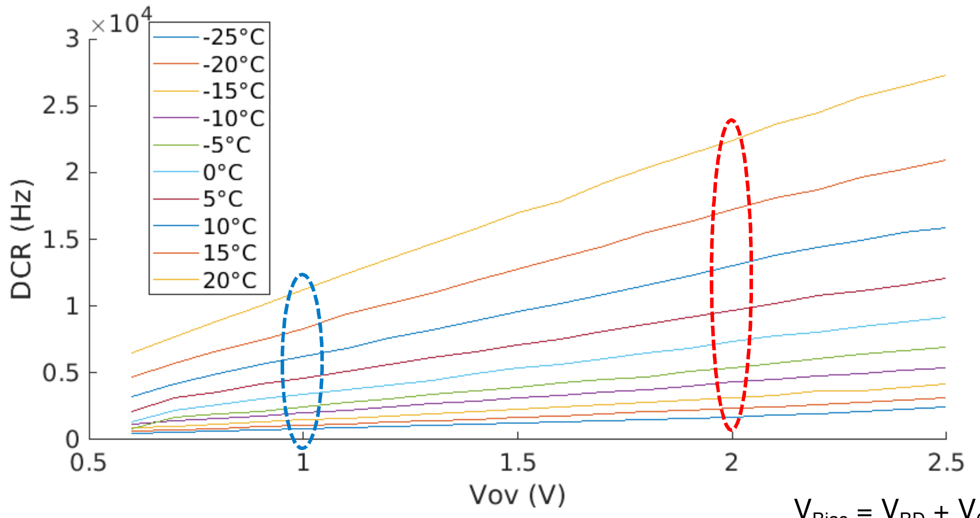
Measurements – in lab

Dark-count rates

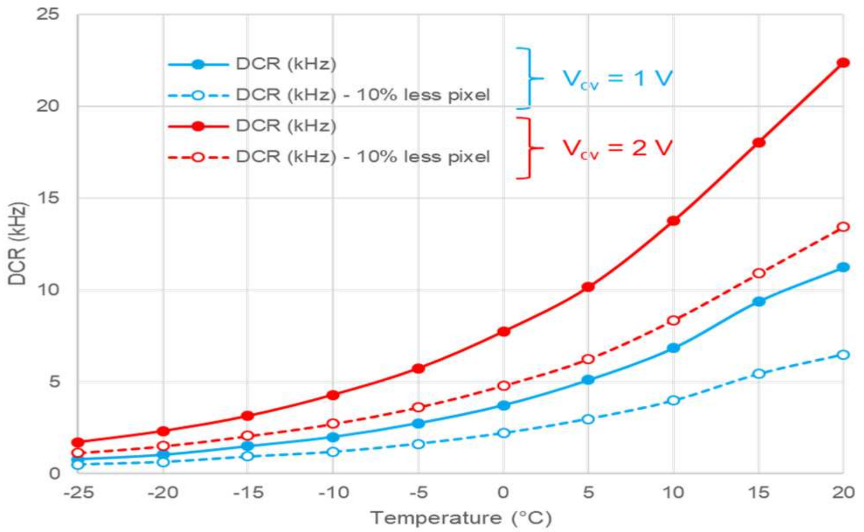
- Thermal generated events in dark conditions
- Strong dependence on temperature and overvoltage
- Dominated by some noisy pixels
  - Pixel masking helps!
- DCR differs from sample to sample, ~25 kHz per pixel at 20°C and V_{ov} = 2 V without masked pixels







$V_{Bias} = V_{BD} + V_{OV}$



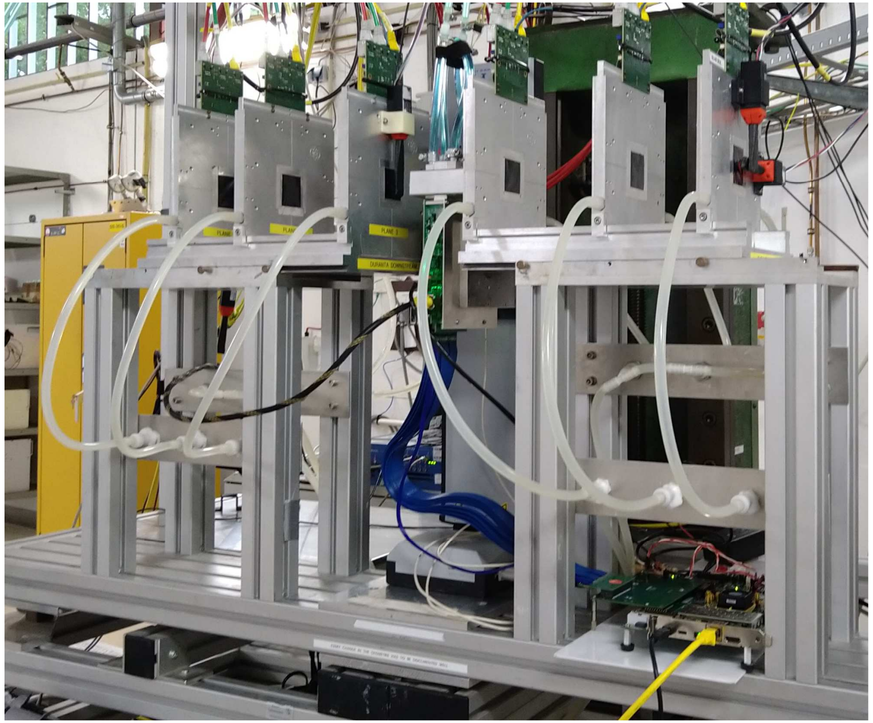
Improvement of ~40%

Conclusion and outlook

DESY's digital SiPM-IC

- Proof-of-principle:
  - Successfully demonstrated
  - Process limitations identified
  - Full detector system can be used
    - E.g. in test beam

    see Gianpiero's talk: "Test beam-characterization of DESY's digital SiPM-IC"



- Possible improvements:
  - Masking of individual SPAD instead of entire pixel
  - LF 110 CIS → DCR reduction
  - Customized SPAD cell → fill factor reduction
  - Multi-layer arrangements → DCR reduction, tracking, …

Infos:

- https://doi.org/10.1088/1748-0221/19/01/P01020
- https://indico.cern.ch/event/1184921/contributions/5576923/

Thank you.

Test beam results are coming soon. ☺

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