



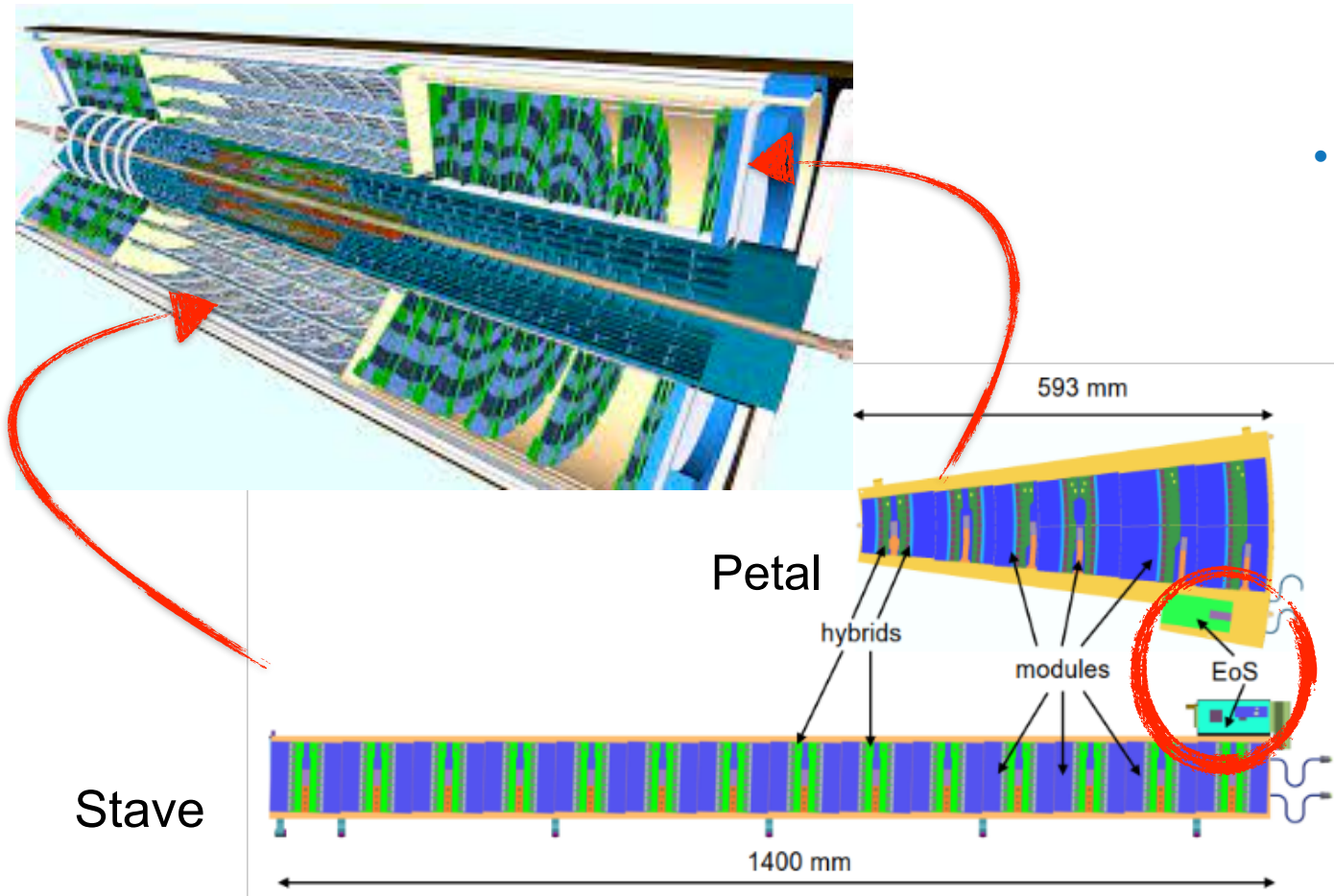
NIELS BOHR INSTITUTE
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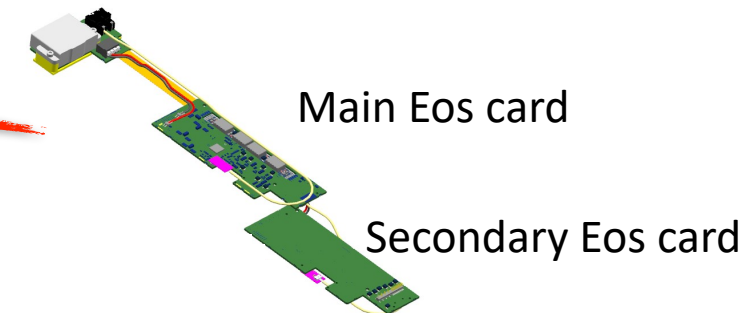
EoS for the ATLAS-ITk-tracker : PCB development for a data multiplexer within a large-scale detector volume

Lukas Bauckhage, Artur Boebel, Harald Ceslik, Mogens Dam, Sergio Diez Cornell, Cameron Garvey, René Stennow Gotfredsen, Peter Goettlicher, Ingrid-Maria Gregor, James Keaveney, Max Van der Merwe, Anders Palmelund, **Sara Ruiz Daza**, Stefan Schmitt, Marcel Stanitzki, Lars Rickard Strom

The ATLAS ITk



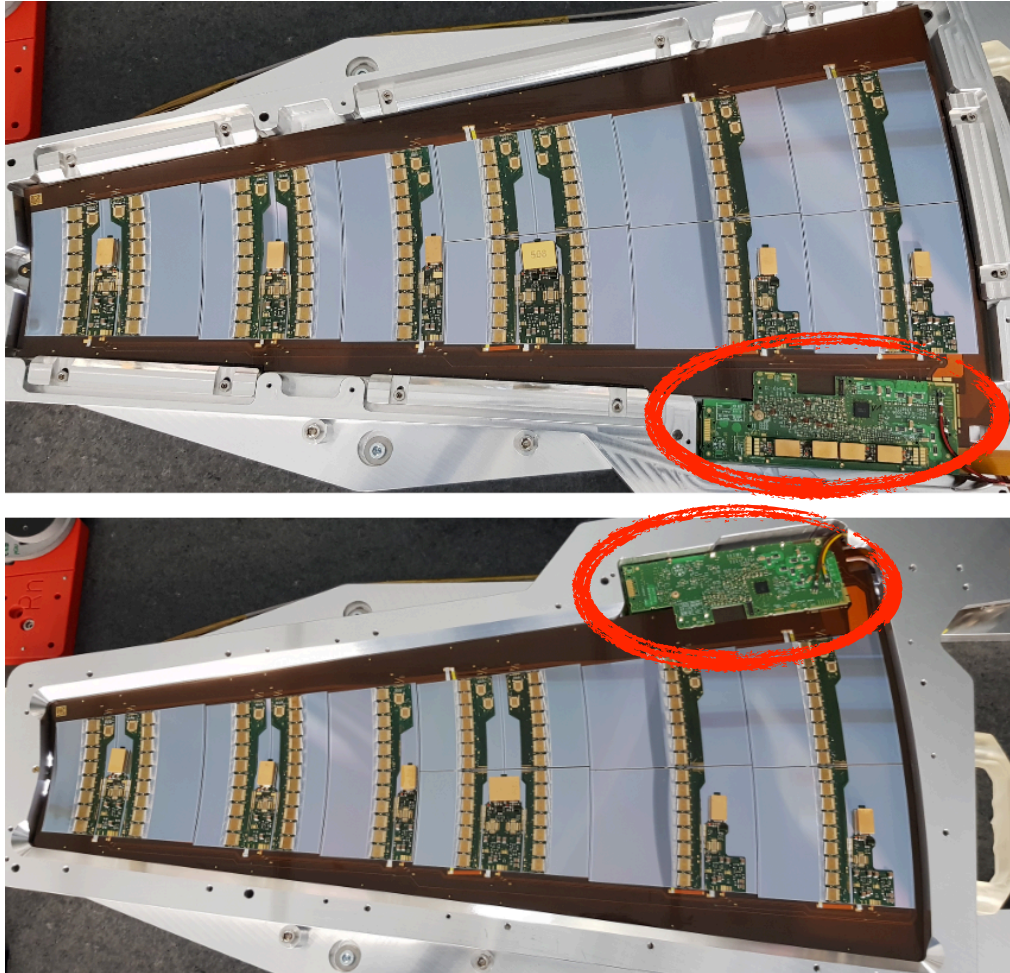
- The Large Hadron Collider will upgrade to **High-Luminosity (HL-LHC)**.
- The ATLAS Inner Detector will be replaced by an all-silicon system, the **Inner Tracker (ITk)**:
 - Pixel detector close to the interaction point.
 - Strip tracker consisting of a barrel (built from “**staves**”) and two end-caps (built from “**petals**”).



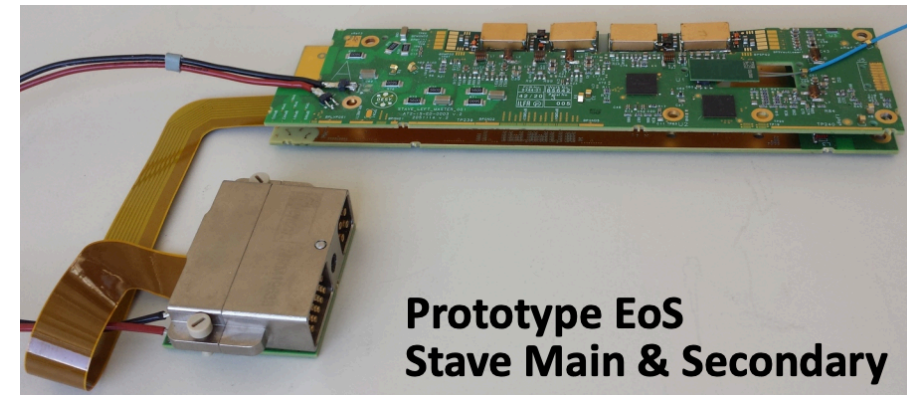
- At the end of each substructure (stave or petal), a pair of main-secondary **EoS card** is placed.

The End-Of-Substructure Card (EoS)

L. Franconi

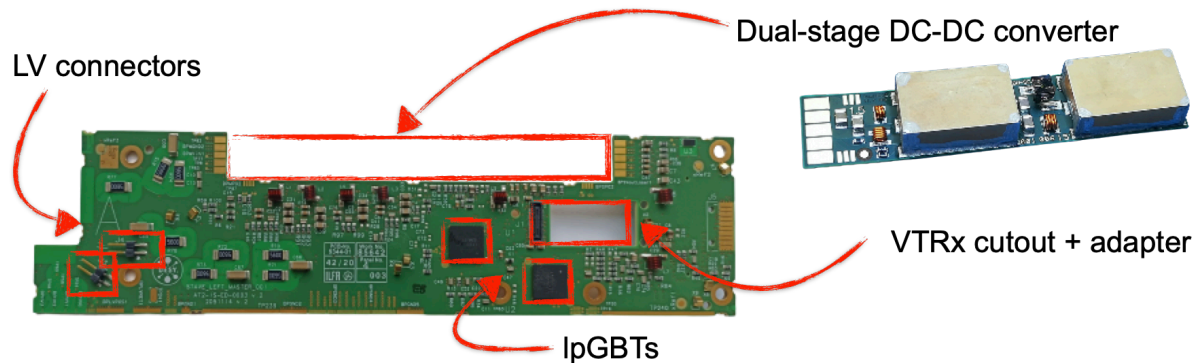
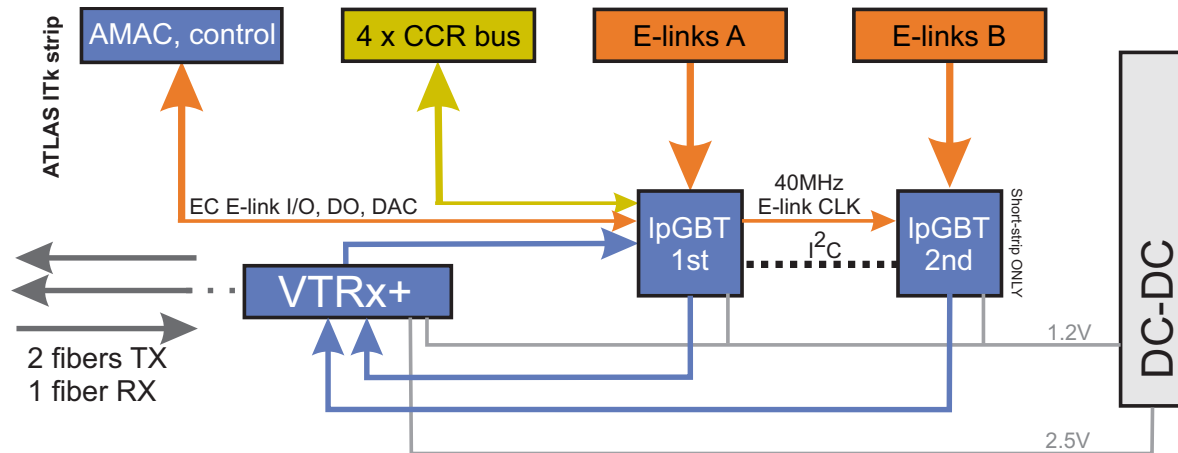


- The EoS cards are the **gateway** between on- and off-detector systems.
 - Supplies LV & HV power
 - Timing, Trigger and Control
 - Detector Control System
 - Send the data off the module



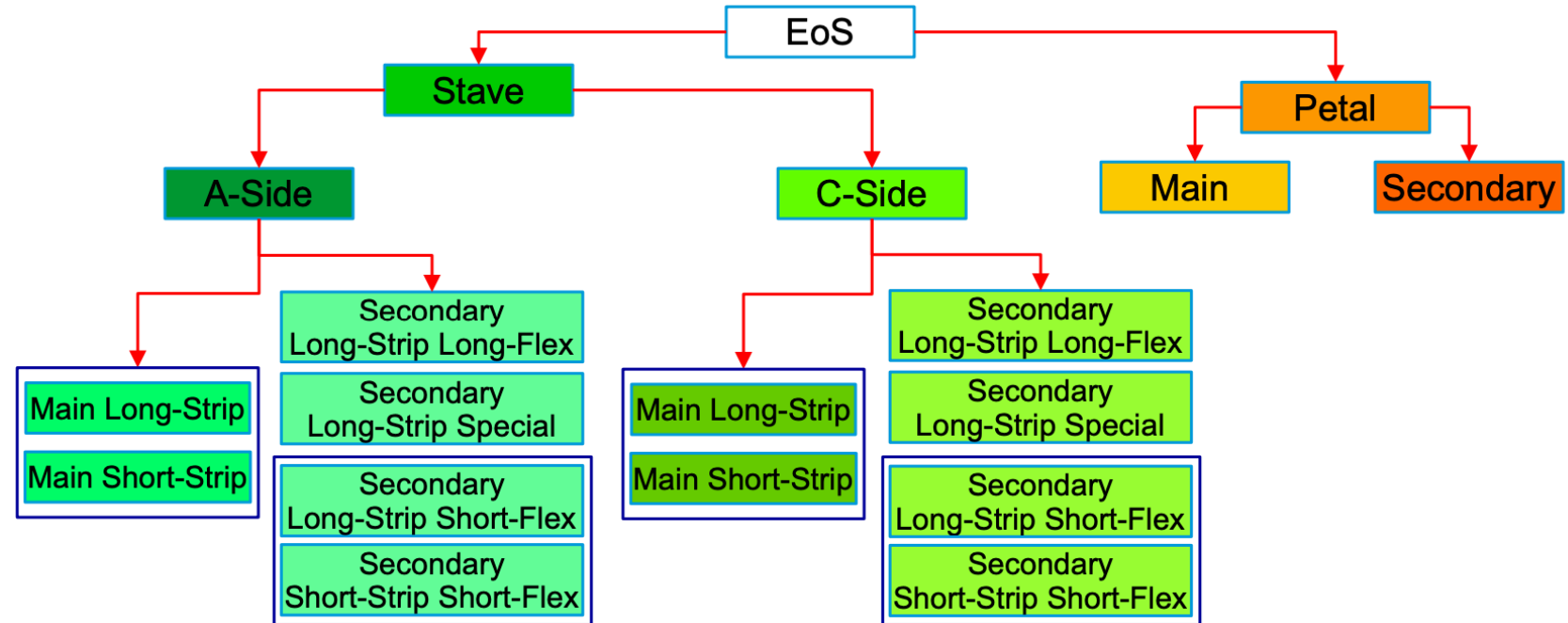
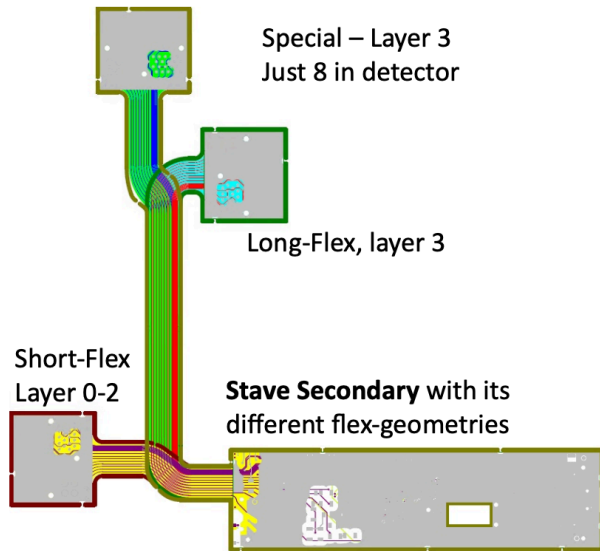
- 11 V for the modules, 1.2 V for the IpGBTs, 2.5 V for the VTRx+ → **Dedicated dual-stage DC-DC converter.**

The End-Of-Substructure Card (EoS)



- **Based on the CERN ASICs for HL-LHC**
 - bPOL's, IpGBT, VTRx+
- **Module Data (E-links)**
 - Up to 14/28 data links @ 640 Mb/s
- **1/2 IpGBTs**
 - Multiplex and serialise the data.
 - 1st IpGBT acts as I²C Master for 2nd IpGBT.
- **VTRx+**
 - Converts electrical signal into optical signals.
 - Data send out via optical fibers.
- **Optical link**
 - 2 TX fibers @ 10.24 Gb/s each
 - 1 RX fiber @ 1.25 Gb/s
- **Clock, Control & Reset Bus**
 - 4 fast control links to the modules @ 160 Mb/s

EoS card flavours



- Physical layout of staves/petals
- Different flex lead geometries
- Variants with one/two lpGBTs

→ **14 different EoS flavours**

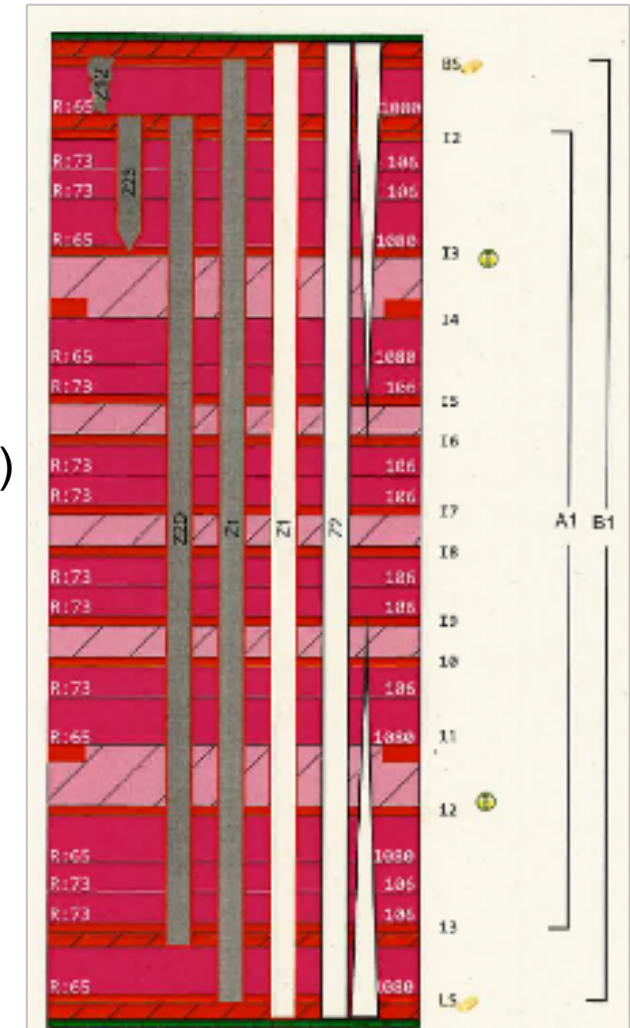
EoS card design

- **Hierarchical design:**
 - Configurable and modular blocks → Blocks reused in the different flavours
 - Re-assignment of gates and pins → Optimisation of the physical layout
 - **14-layer PCB**
 - Total thickness < 5 mm (1.8 mm for PCB & 3.2 mm available for components)
 - Two layers dedicated to impedance-controlled signals.
- All the above constraints
 - +
 - Radiation hardness
 - Geometry dimensions
 - Fine pitch of 0.5 mm

}

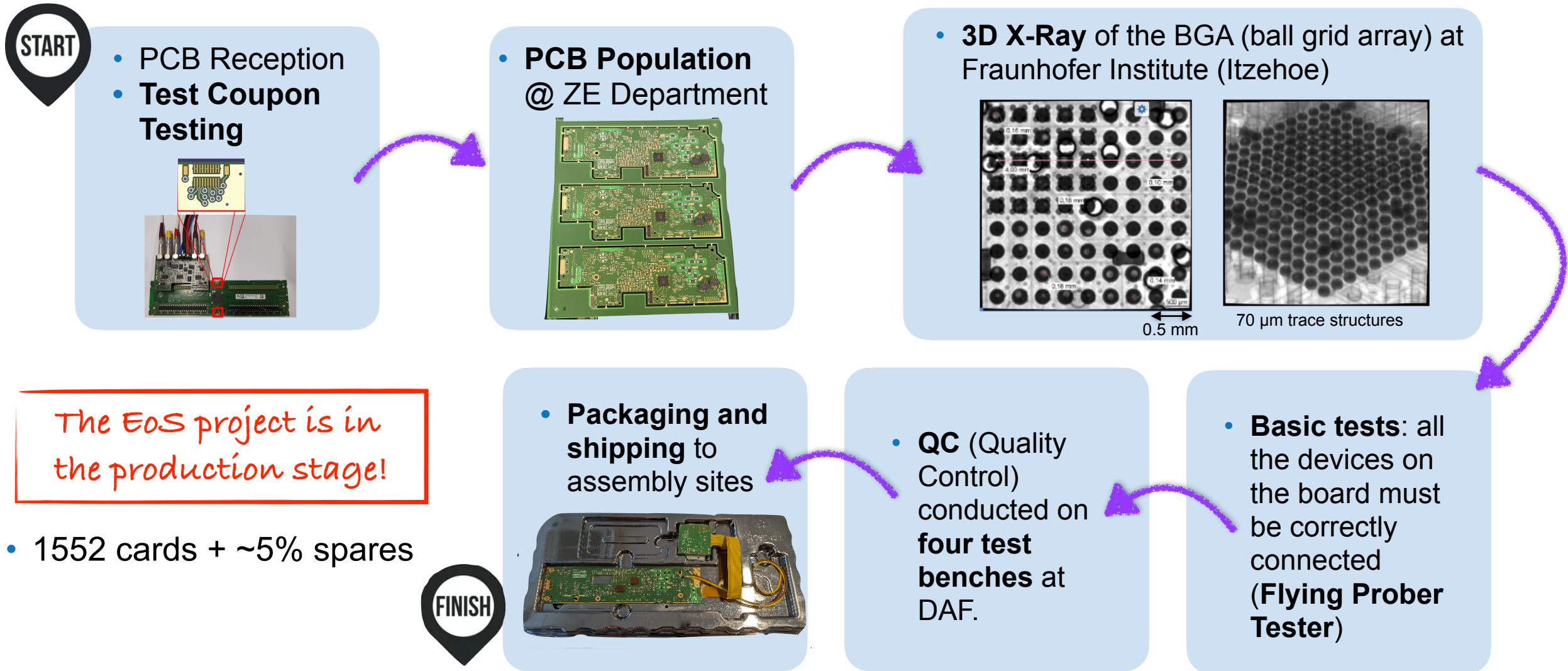
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Vendor-specific design



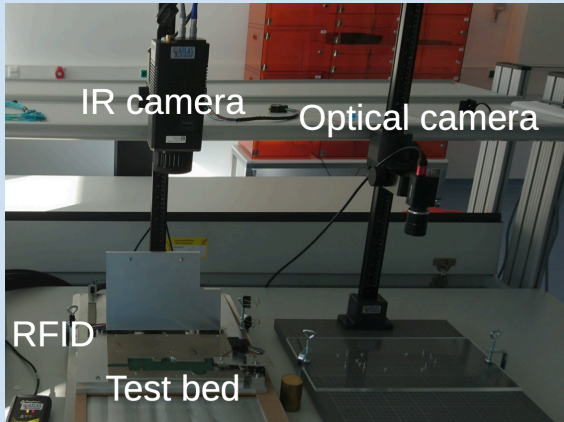
PCB Stack up

Testing workflow



Quality control (QC): 4 test benches @DAF

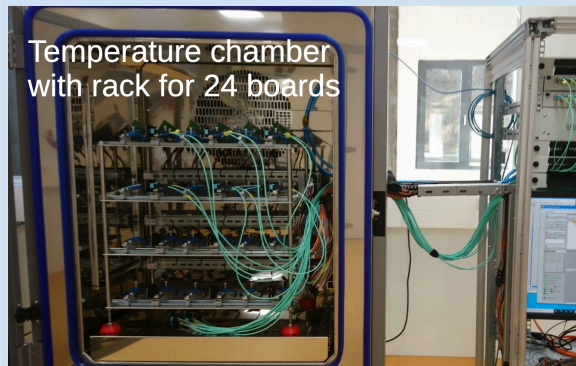
#1



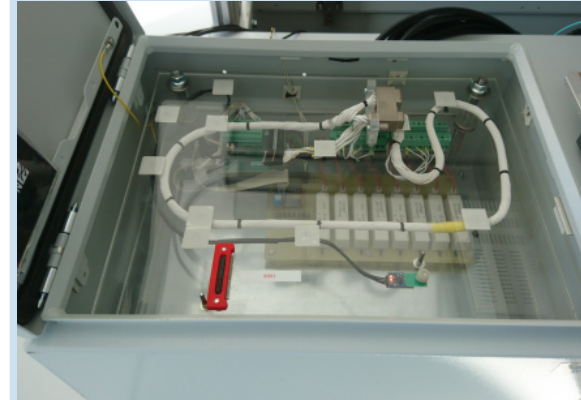
- **RFID** identification.
- **Optical & IR inspections**, dimensions, flatness.
- **Power consumption**.
- **ADC value reading**.
- **Check optical links** (up/down).

#2

- **Thermal stress test**
 - Cycled 10 times from -35°C to 30°C .
 - Power on/off at each cycle.
 - Electrical/functional tests similar to the test bench #1 are repeated.

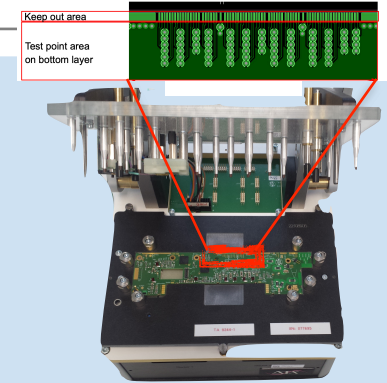


#3

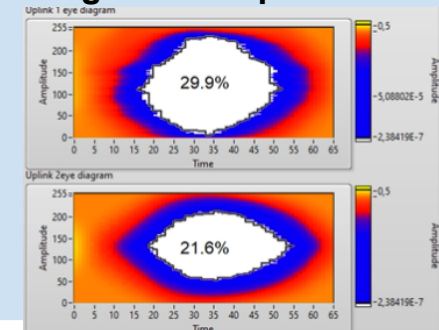


- **HV test**
 - Each HV line is ramped up to 1.1 kV.
 - Monitor of the leakage current every 2 seconds for one minute ($< 5 \text{ nA}$).

#4

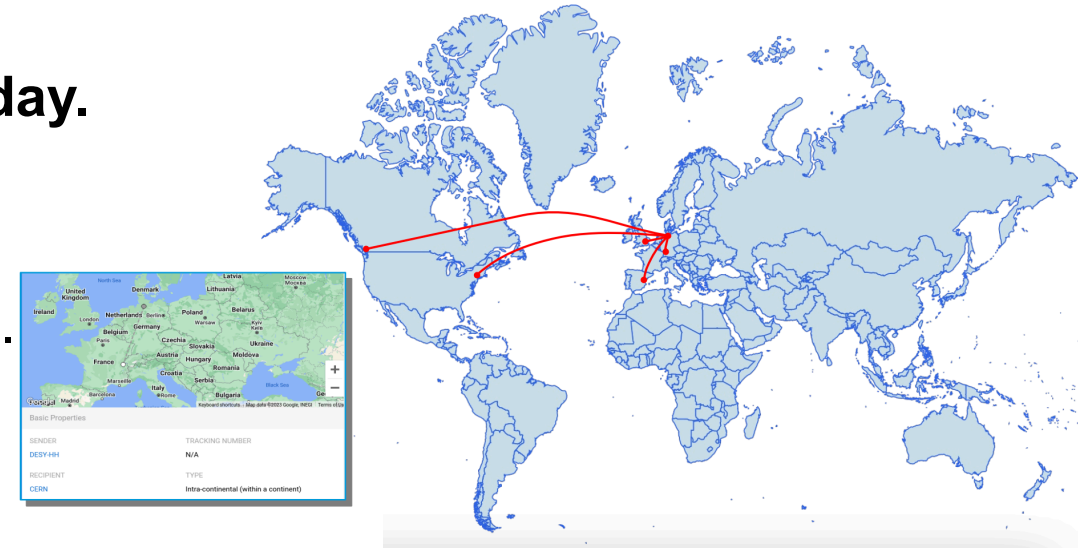


- **Electrical test and bit error rate test (BERT)**
 - Needle probe: test points on a grid of 0.7 mm near the bonding pads.
 - For all 640 Mb/s fast signals.
 - Error rate $< 10^{-12}$
- **Eye-diagrams of up-links**



A decade of EoS & Current status

- **The project has been evolving from 2012/13 to today.**
 - Moving from GBTx to IpGBT
 - Forking more and more variants.
 - But basic approach has remained relatively stable.
 - Getting the most out of project reviews.
- **Status:**
 - Pre-production has been completed - EoS being used at all assembly sites
 - Production has started.
 - Track is being kept in the production database.
- **Timeline** highly dependent on the capabilities of the manufacturer and the boards requested from the assembly sites.



Summary & Outlook

• EoS Cards Overview:

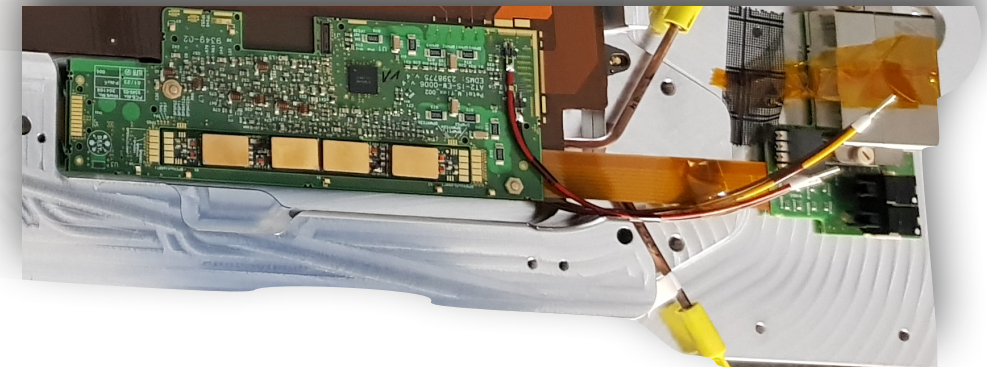
- **Gateway between on- and off-detector systems.**
- Connects up to 28 data lines to IpGBT ASICs and VTRx+ module.
- Manages data serialisation and enables 10 Gb/s optical data transmission to off-systems.
- Powered by a dedicated Dual-Stage DC-DC converter.

• Collaboration:

- **DESY groups**, together with the University of Cape Town and the Niels Bohr Institute.
 - DESY groups: ATLAS, FEA & FEB, FTX and ZE.
- Board population and testing conducted at DESY.

• Current Stage - Production:

- **EoS project in the production stage.**
- Goal: ~ 2000 cards in 14 different flavours.
- Keep track in the production database.



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Thank you!

