

The CMOS-DEPFET DSSC detector for soft X-rays

Stefano Maffessanti

Detector R&D retreat
Hamburg, 19.01.2024

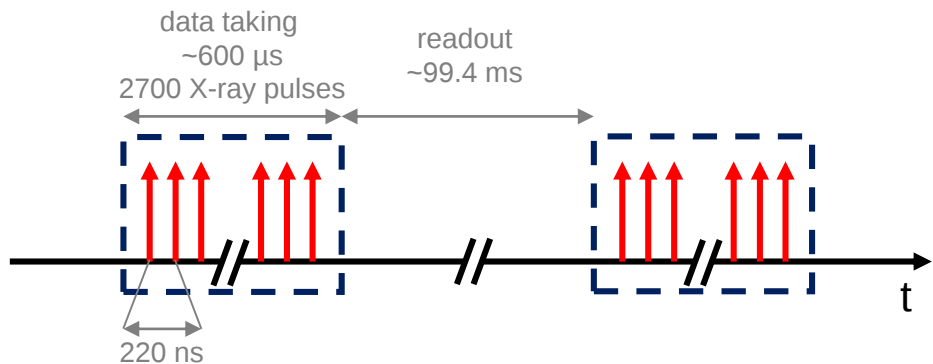
DSSC consortium

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- 3) PNSensor GmbH, München, Germany
- 4) Dipartimento di Elettronica e Informazione, Politecnico di Milano, Milano, Italy
- 5) Sezione di Milano, Italian National Institute of Nuclear Physics (INFN), Milano, Italy
- 6) Dipartimento di ingegneria industriale, Università di Bergamo, Bergamo, Italy
- 7) Zentrales Institut für Technische Informatik, Universität Heidelberg, Heidelberg, Germany
- 8) Deutsches Elektronen-Synchrotron DESY, Notkestr. 85, 22607 Hamburg, Germany
- 9) Department of Molecular Sciences and Nanosystems, Ca' Foscari University of Venice, 30172 Venezia, Italy



DSSC system overview/1

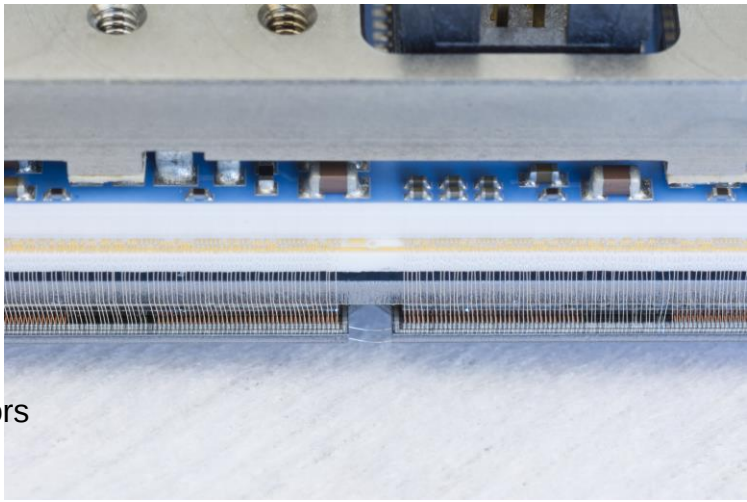
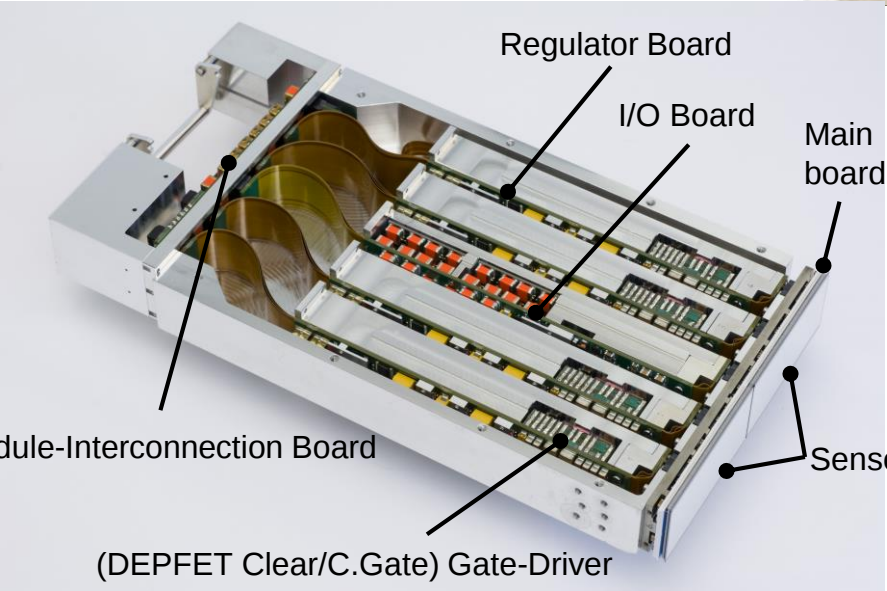
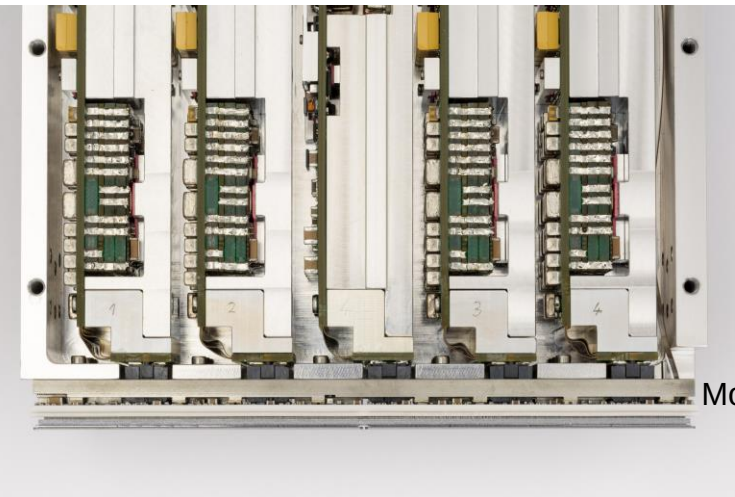
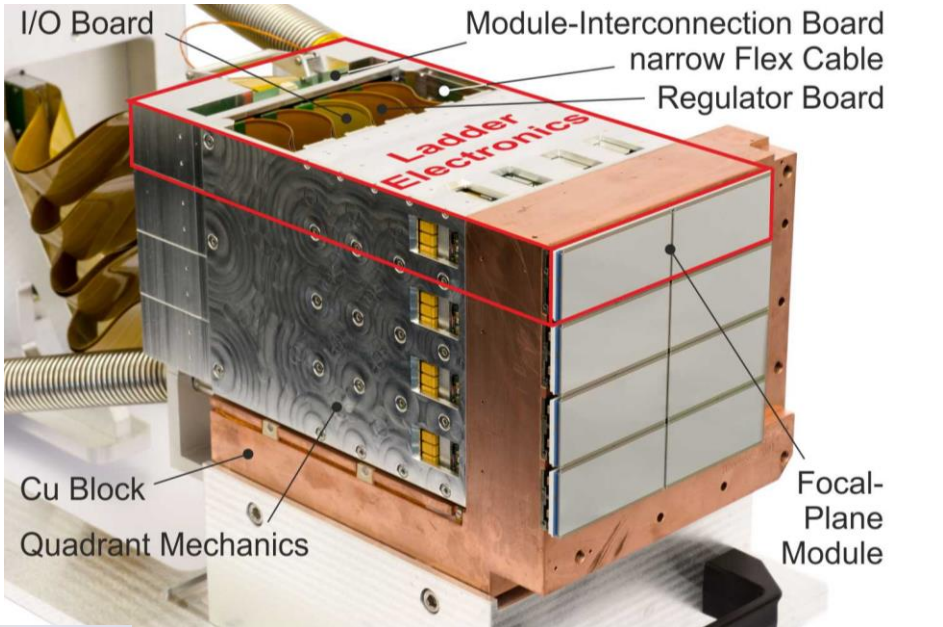
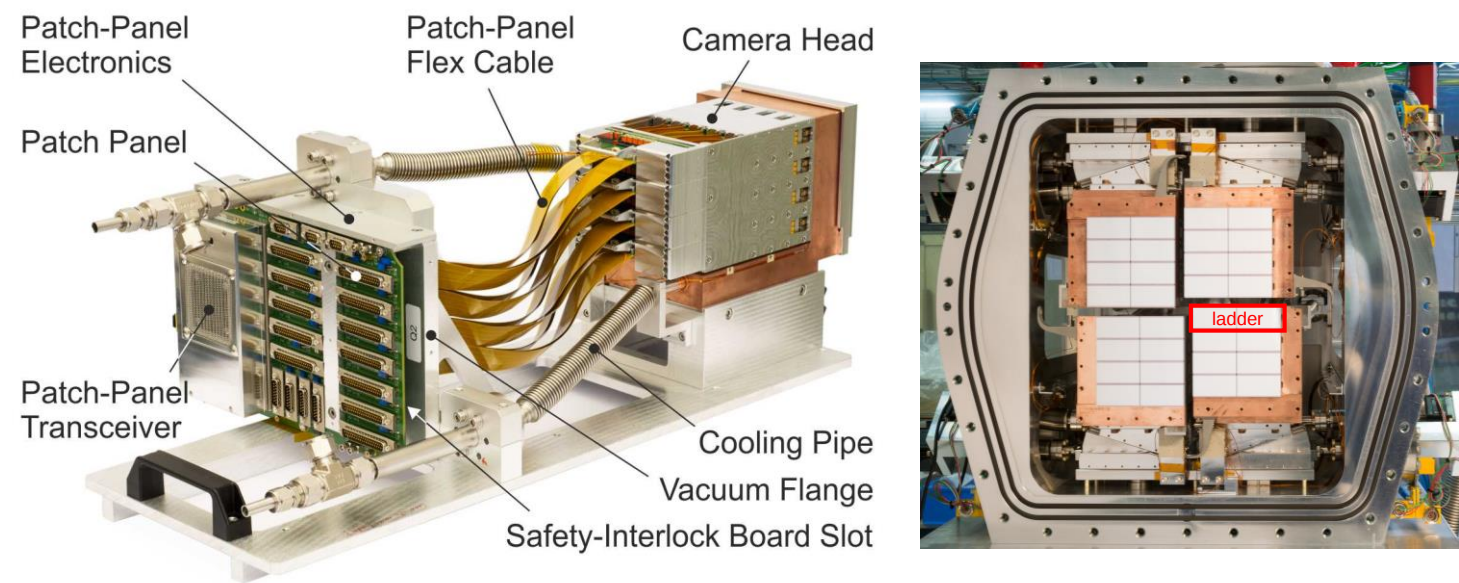


Parameter		Value
Target energy range		0.25 keV – 6 keV
Pixel count		1024 × 1024
Pixel shape		hexagonal
Sensor pixel pitch		~204 μm × 236 μm
Active area		~ 21 cm × 21 cm
Input photon range / pixel / pulse	MiniSDD	2 ⁿ × N -1
	DEPFET	>10 ⁴ *
Achievable noise	MiniSDD	~ 60 e- r.m.s.
	DEPFET	~ 10 e- r.m.s.
Peak frame rate		4.5 MHz
Stored frames per X-ray train		800
Average / peak data rate		134 / 144 Gbit/s
Average power consumption	MiniSDD	~ 260 W
	DEPFET	~ 410 W *
Operating temperature		-20° C optimum for MiniSDD, room T possible

* expected

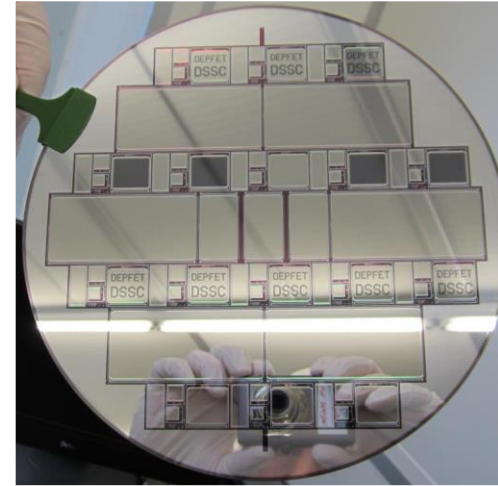
- 2D 1Mpx detector for soft X-rays**
 - 4 quadrants (512 x 512)
 - 16 ladders (512 x 128)**
 - 32 monolithic sensors (256x128)
 - 256 Readout ASICs (64x64)
- Sensors:**
 - DEPFET arrays (2nd camera, under construction)**
 - miniSDD arrays (1st camera, in operation since 2019)
- Readout concept**
 - Full parallel readout**
 - 4.5 MHz peak frame rate**
 - In pixel analog to digital conversion
 - In pixel digital storage** (800 frames) with the possibility to overwrite non-valid frames (VETO)
 - Output average **data rate: 134.4 Gbit/s**
- Power cycling**
 - The camera is **fully powered only during X-ray arrival**
 - expected total power dissipation **412 W** (393 μW per Pixel)
 - expected coolant load in vacuum 298 W (284 μW per Pixel)

DSSC system overview/2

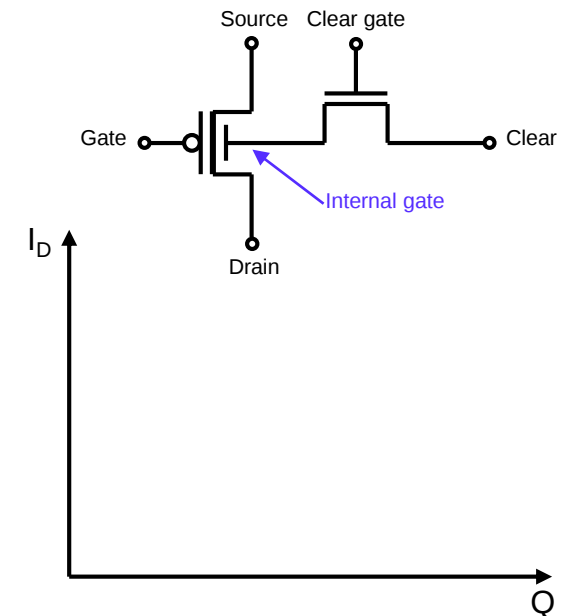
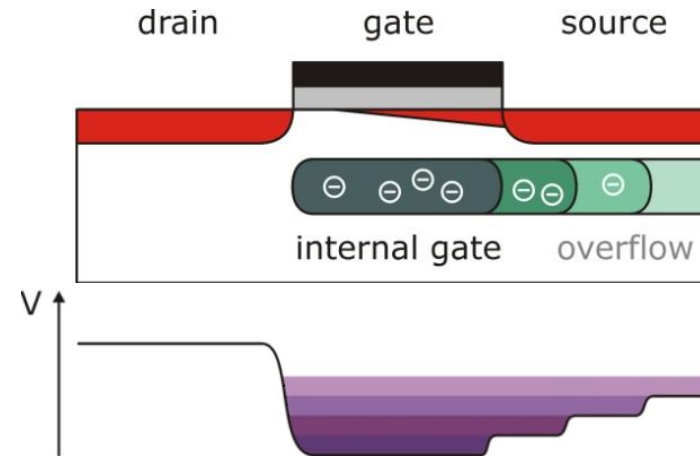
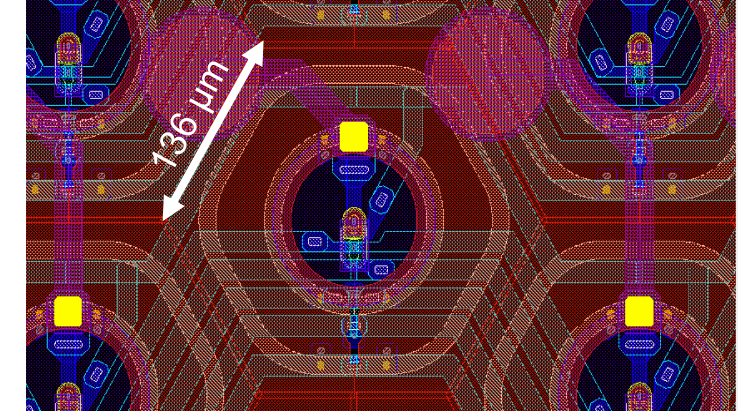


DEPFET sensor

- Sensors fabricated in CMOS foundry (IMS) in fully customized process (front side) and PNSensor (back side)
 - 200 mm (8 inch) wafers
 - 725 μm thickness
 - 256 x 128 pixels
- Active pixels that provide non linear response
 - Low noise for single photon detection
 - High dynamic range
 - Common source configuration (I_{DRAIN} readout)

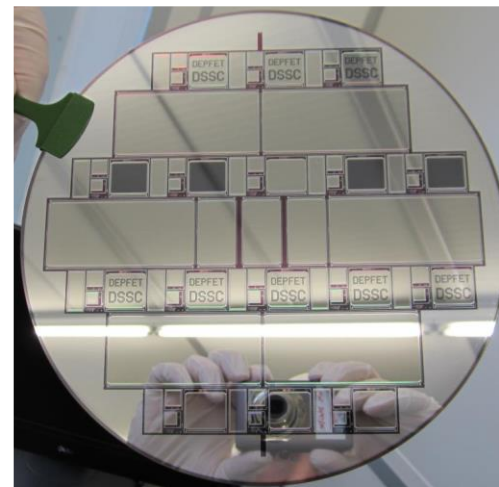


DEPFET Active Pixel

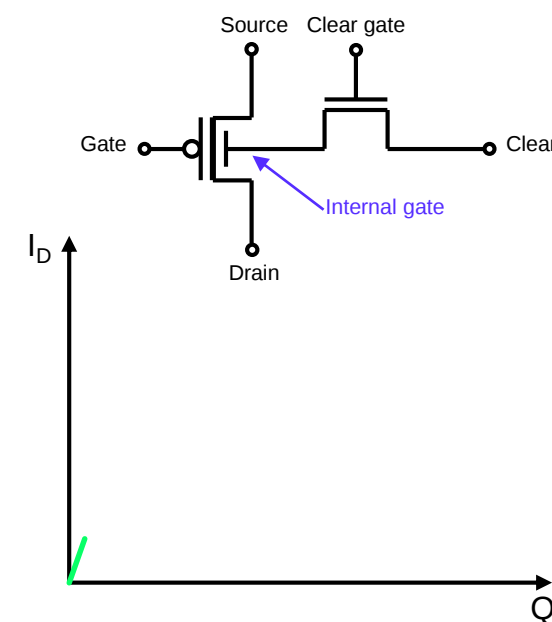
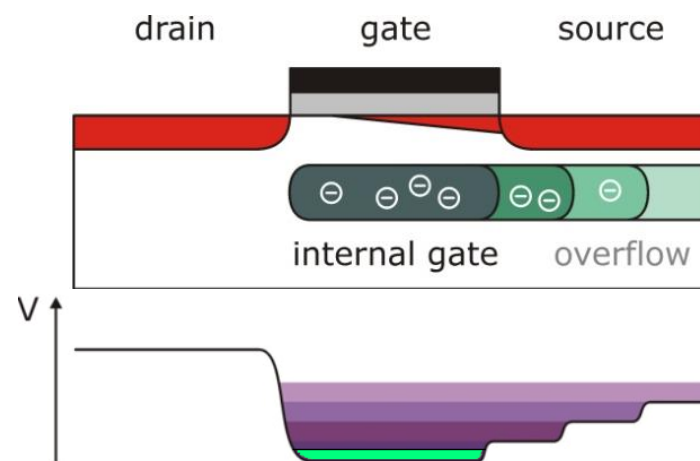
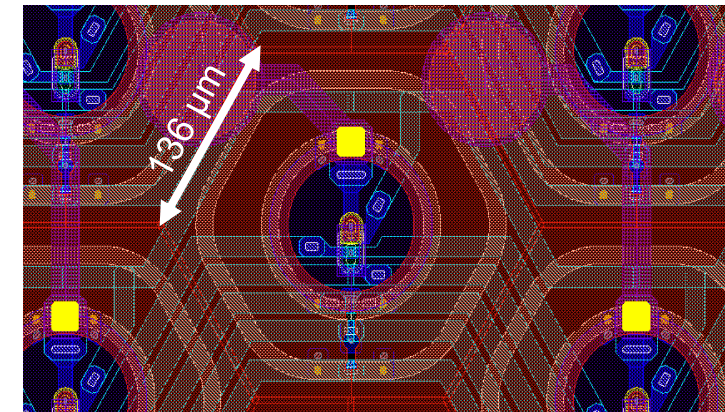


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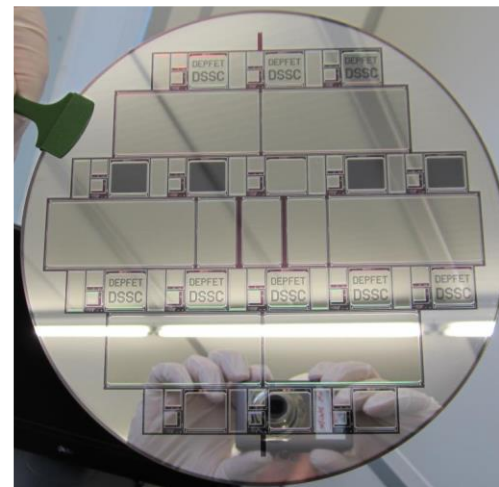


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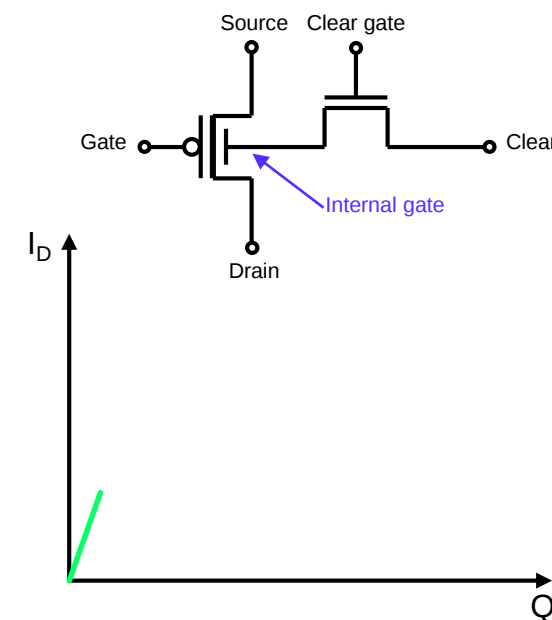
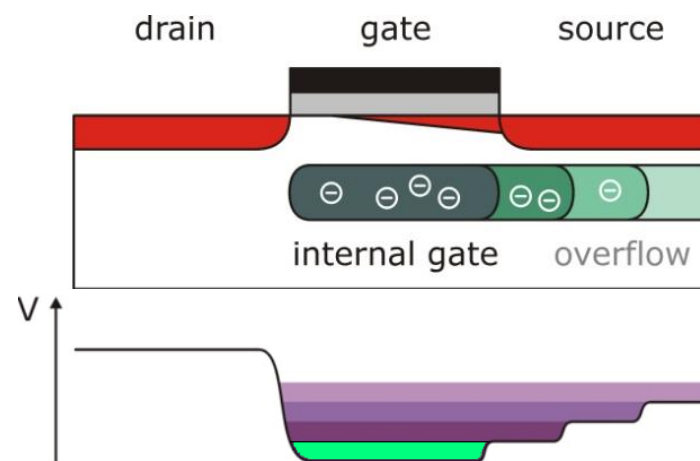
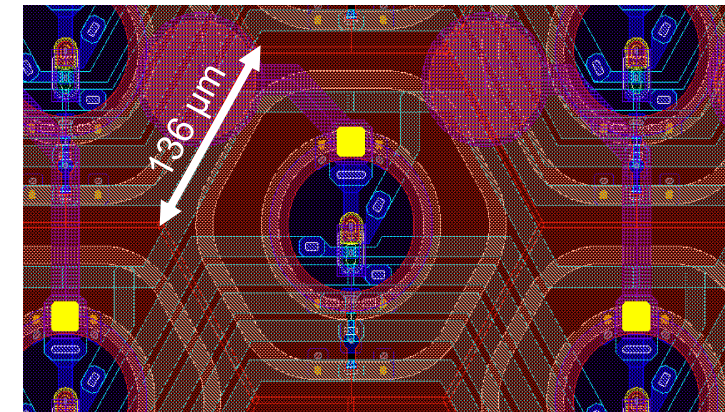


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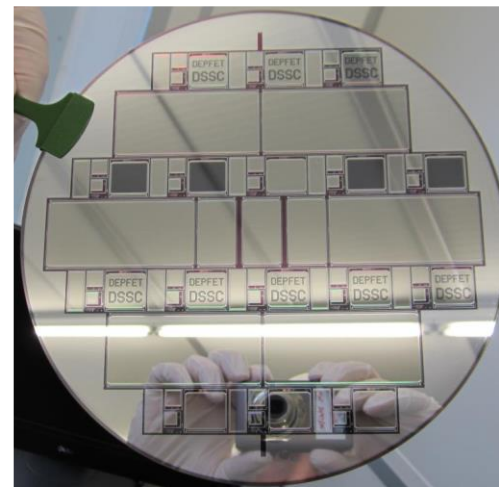


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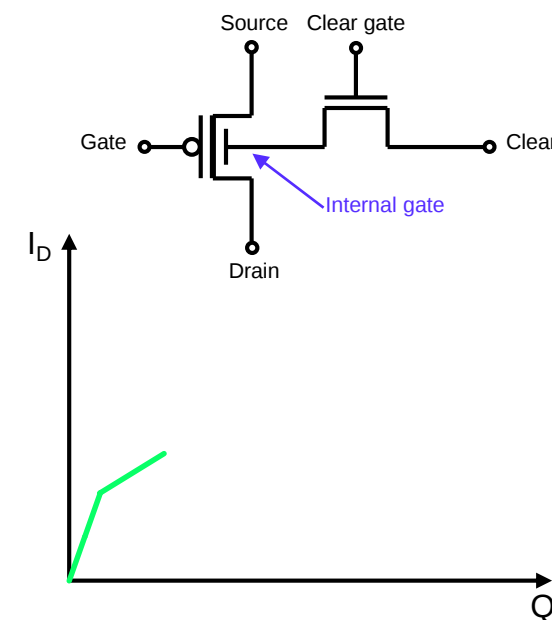
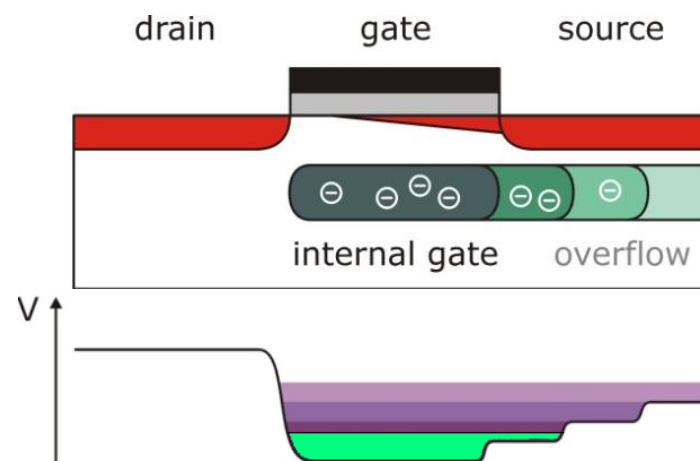
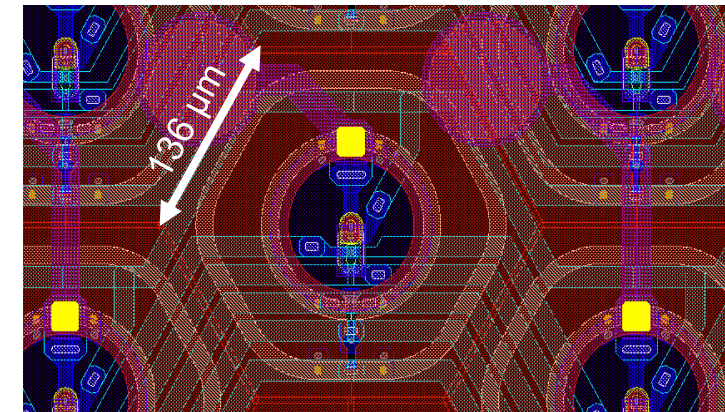


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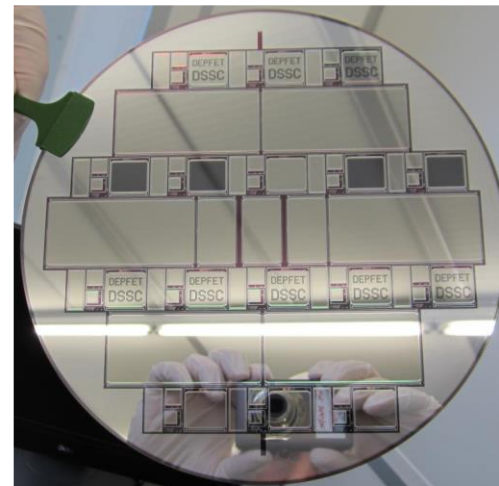


DEPFET Active Pixel

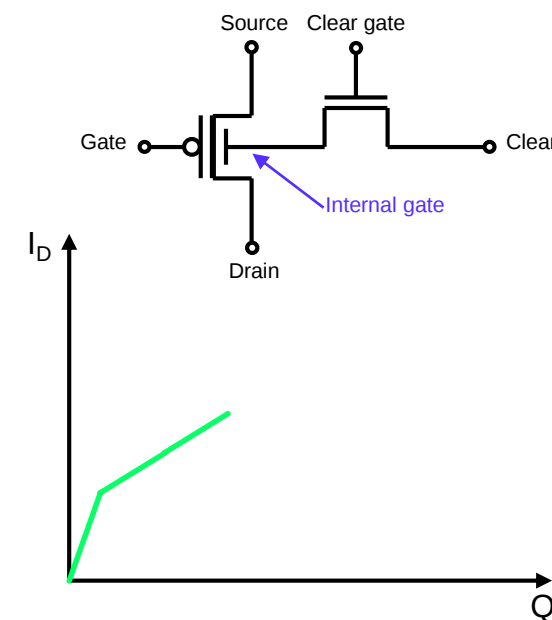
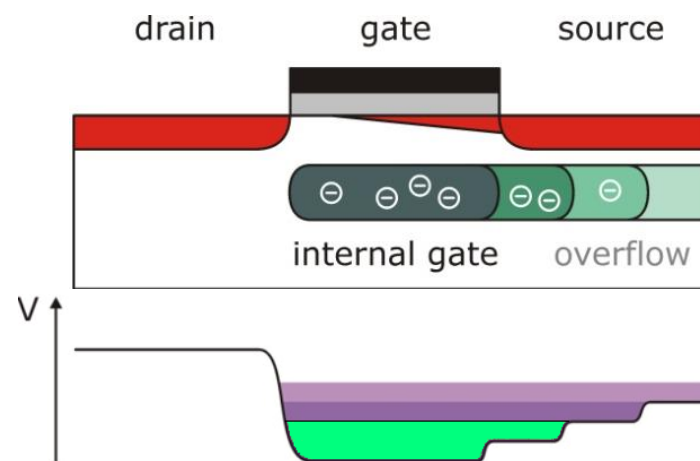
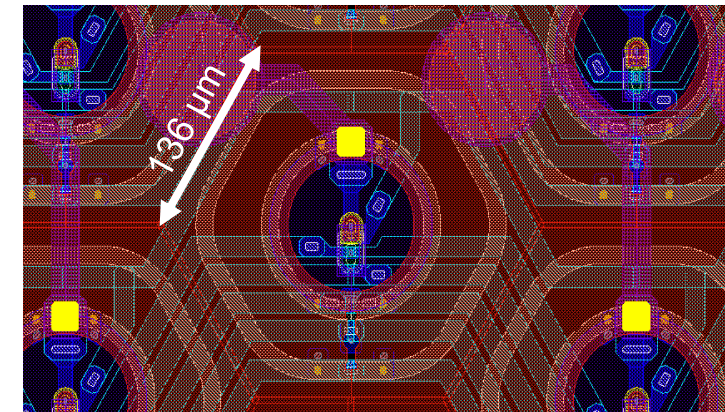


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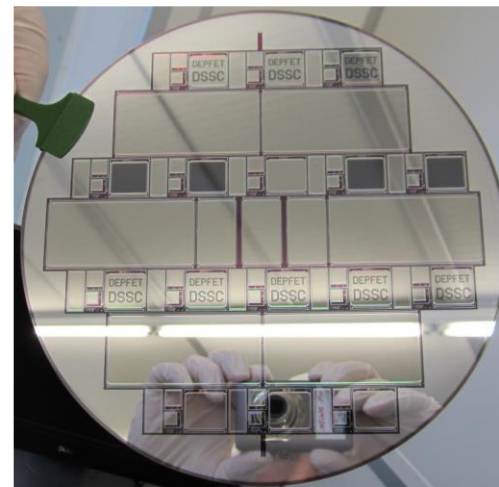


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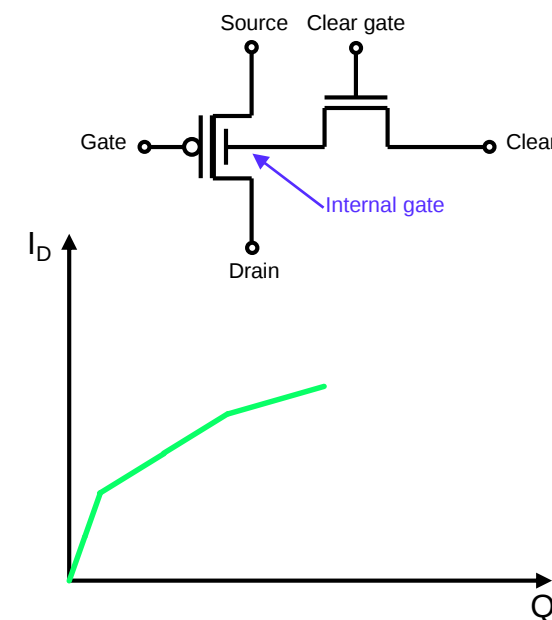
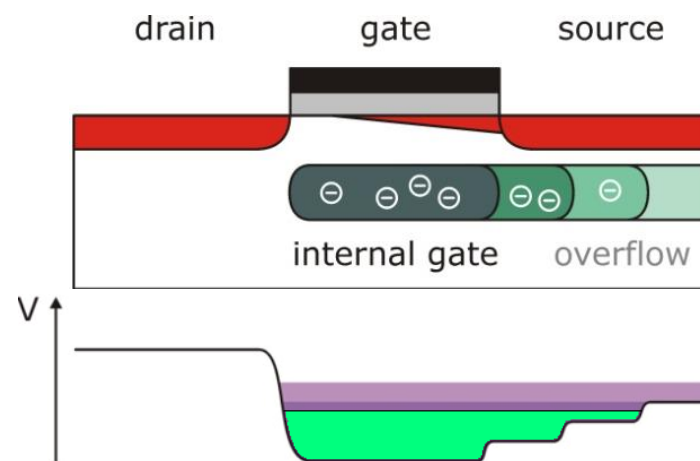
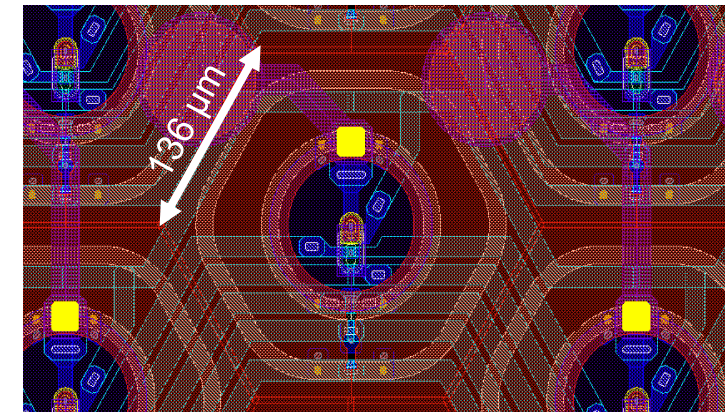


DEPFET sensor

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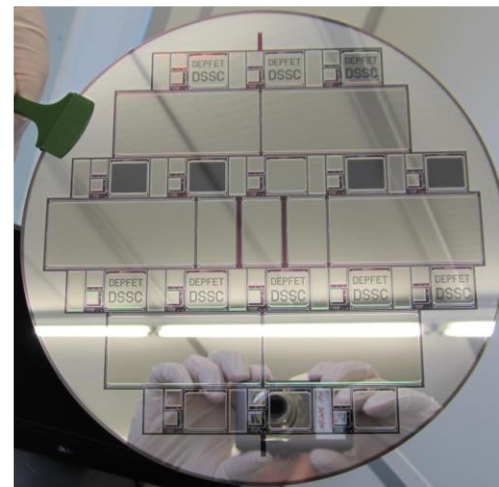


DEPFET Active Pixel

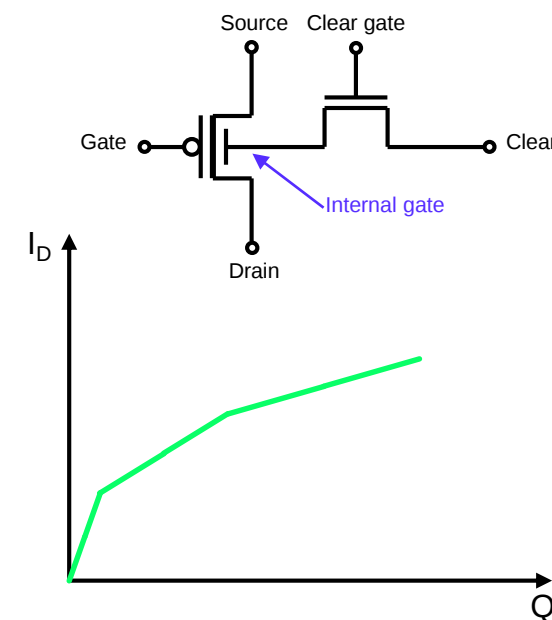
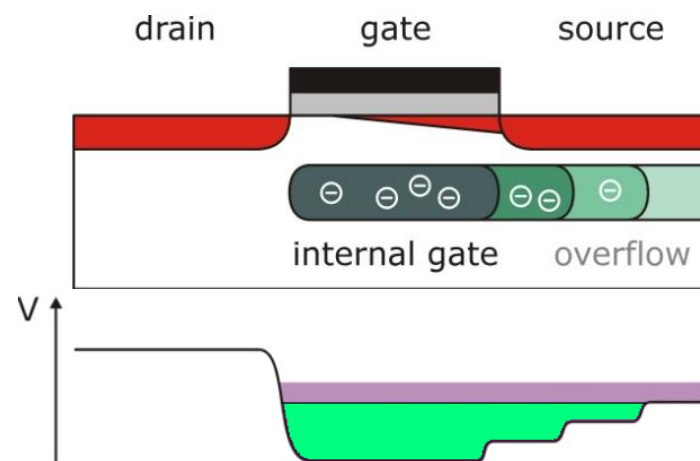
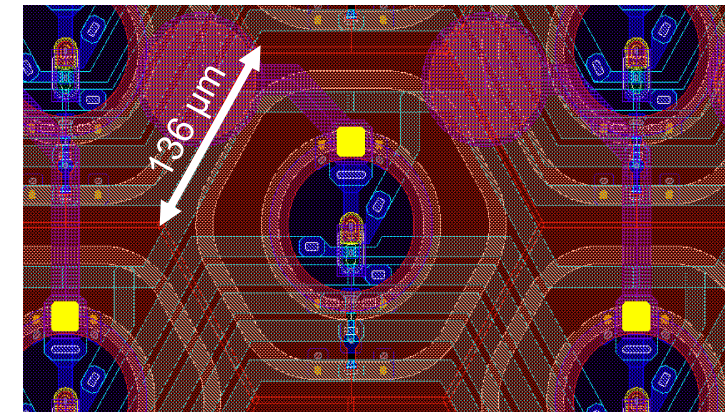


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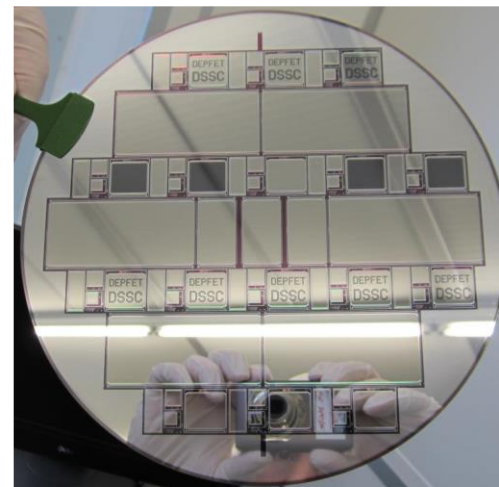


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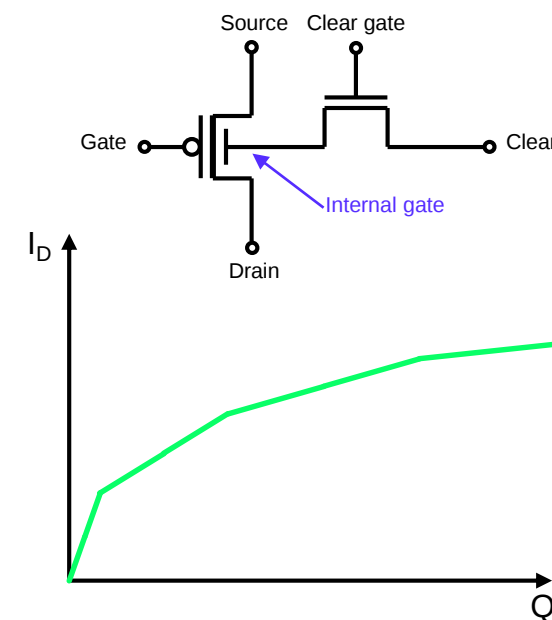
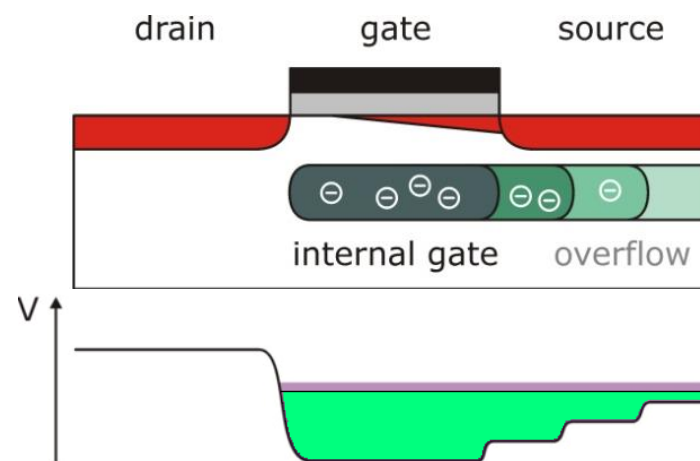
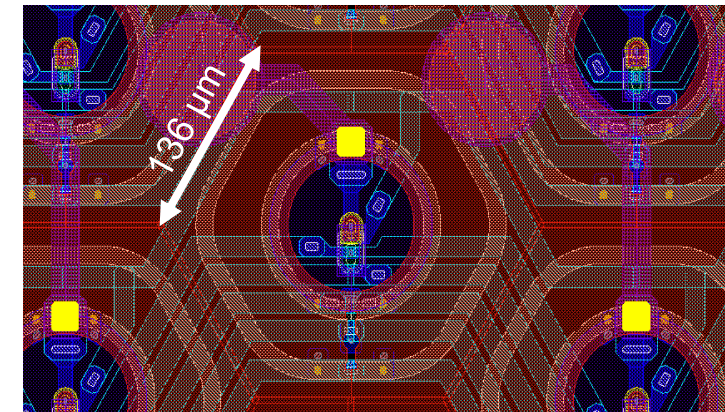


DEPFET sensor

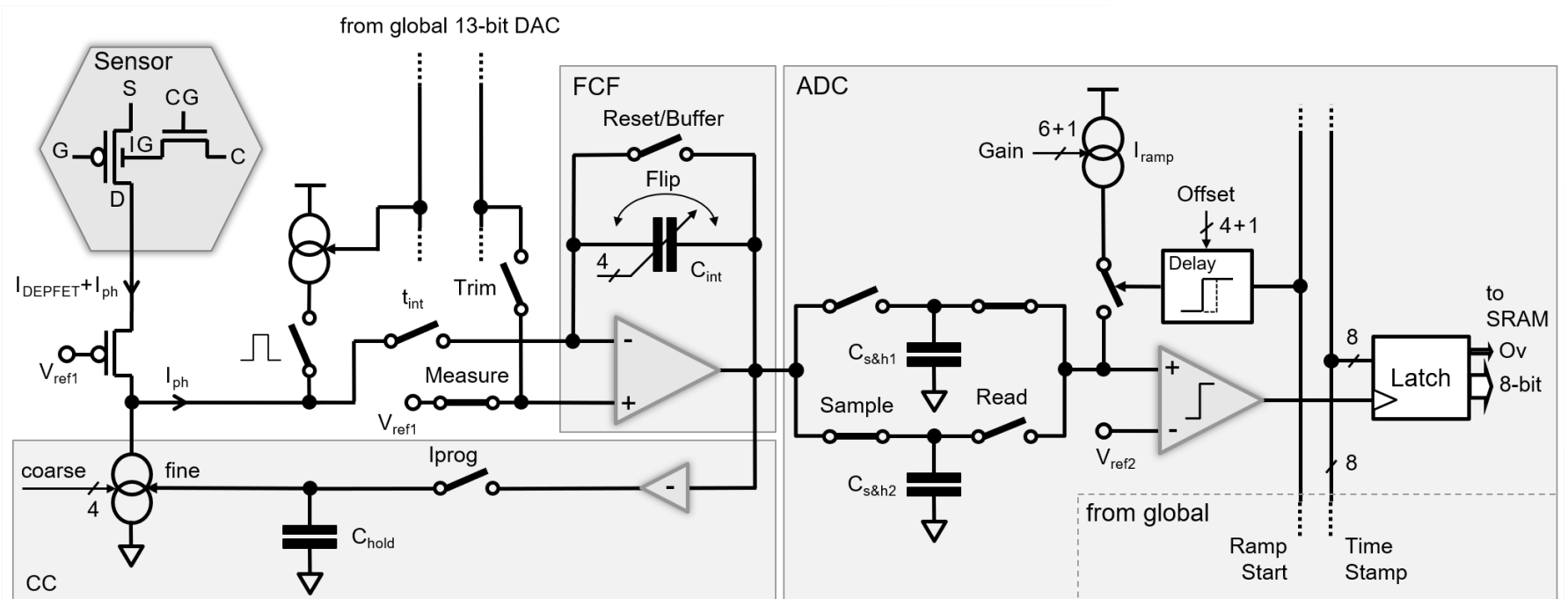
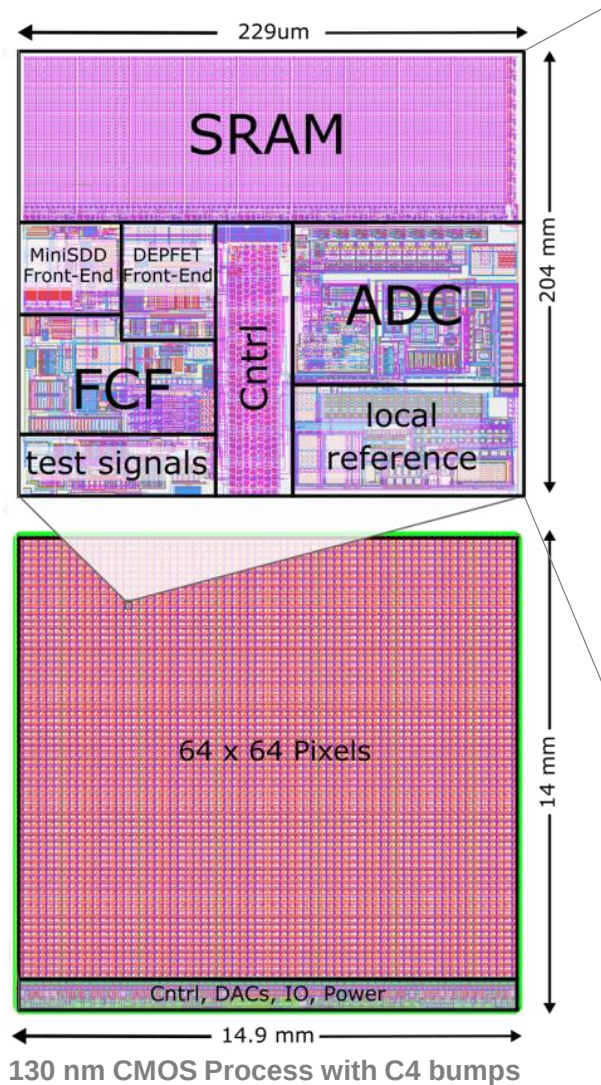
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DEPFET Active Pixel



Readout ASIC

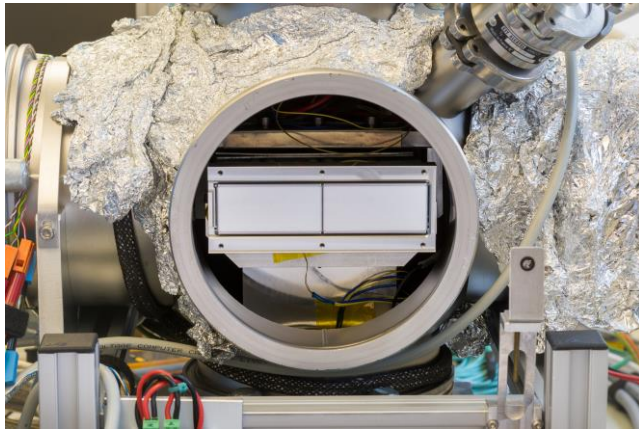


In pixel:

- DEPFET-bias current subtraction circuit (CC)
- trapezoidal shaping filter (FCF) with programmable integration & flat-top times (1.44 ns steps)
- 9-bit in pixel digitizer (ADC) with gain & offset trimming capabilities
- 800 9-bit words SRAM
- Injection circuit(s)

Lab qualification – currents & gain in linear region

- 100 μA /pixel average DEPFET bias current, sensor-wise equalization by adjusting V_S & V_G
- CC trimming for proper baseline subtraction
- ^{55}Fe for absolute calibration in linear region
- ADC fine gain trimming to reduce gain dispersion to $\sim 2\%$ (ADC granularity)

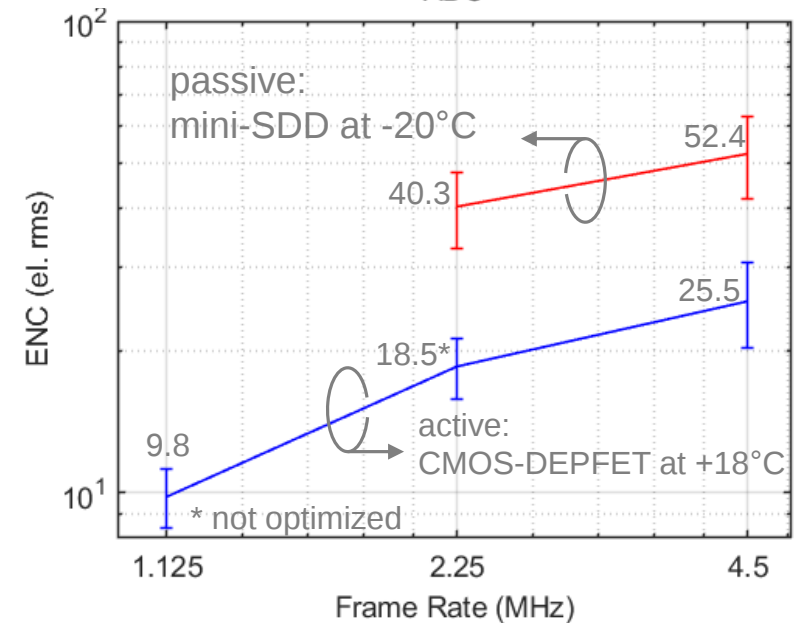
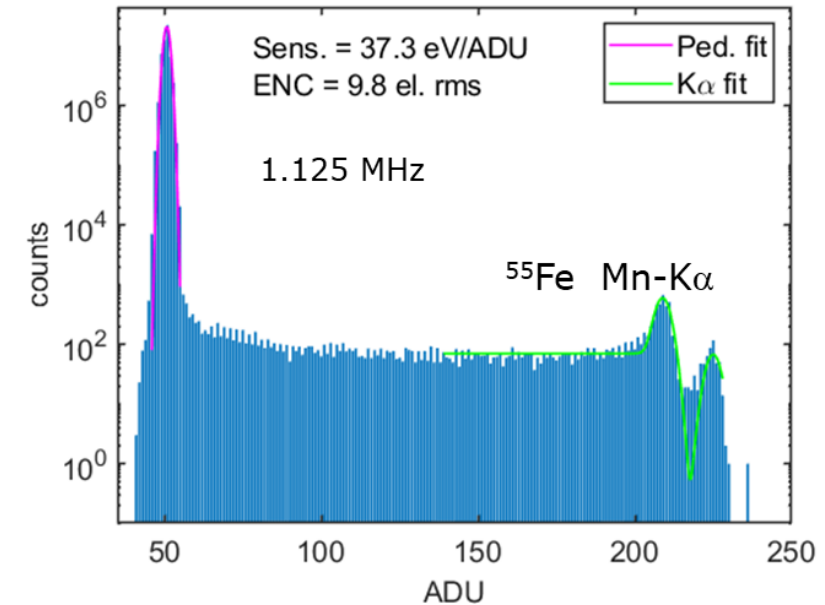
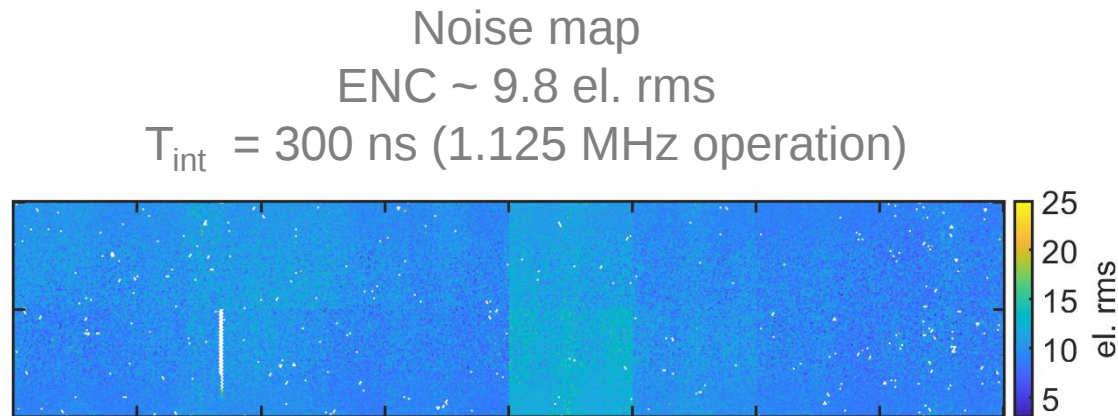


test chamber @ DESY-FEC



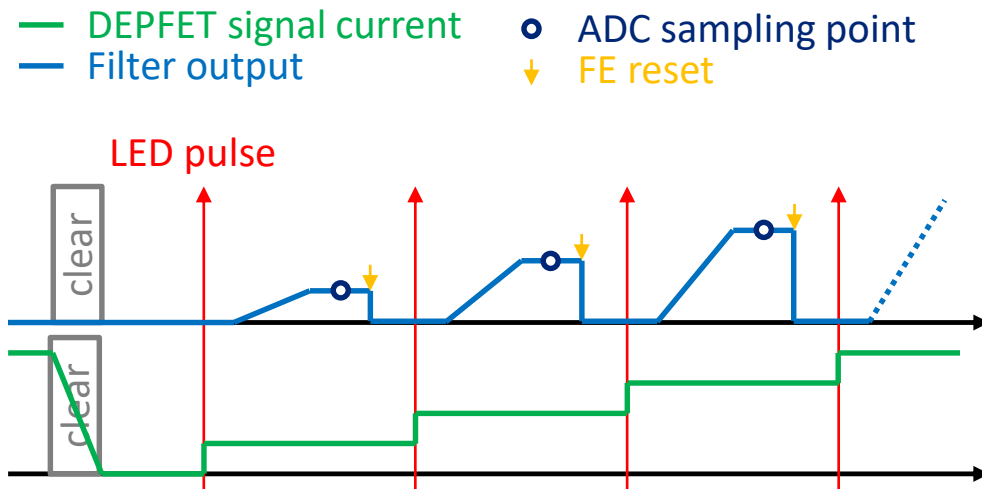
Lab qualification – noise

- 25.5e- rms ENC @ $T_{\text{int}} = 30$ ns operating at 4.5 MHz
- < 10e- rms @ $T_{\text{int}} = 300$ ns achievable at 1.1 MHz
- room temperature operation (18°C)
- more than x2 times better than mini-SDDs

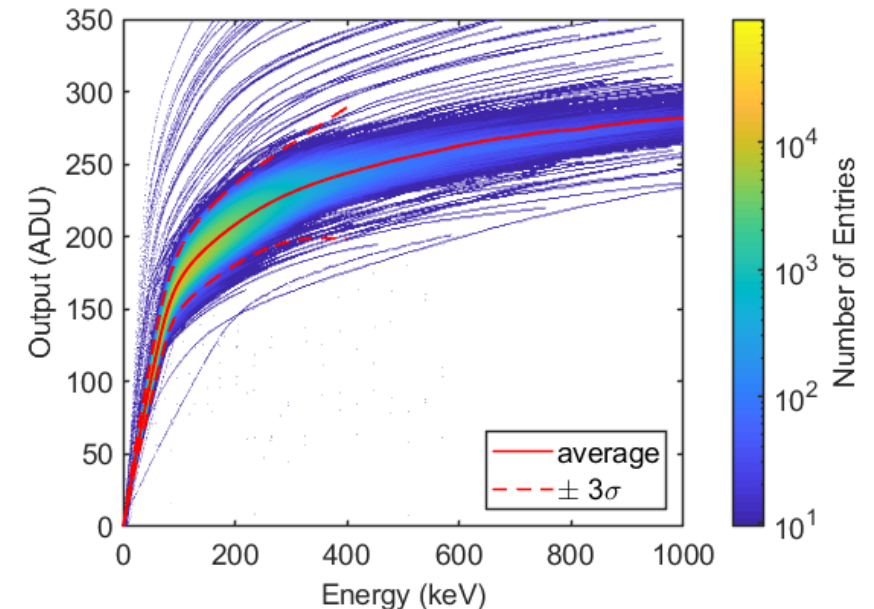


Lab qualification – NL response

- 150nm Al light-blocking filter deposited on backside
- NL response characterization by pulsed high power LED array
- Charge deposited by 400 light pulses integrated into DEPFET internal gate & readout in single integration
- Est. dynamic range: ~ 9000 ph @ 1000 eV/ADU @ 8-bit operation, $> 10^4$ @ 9-bit

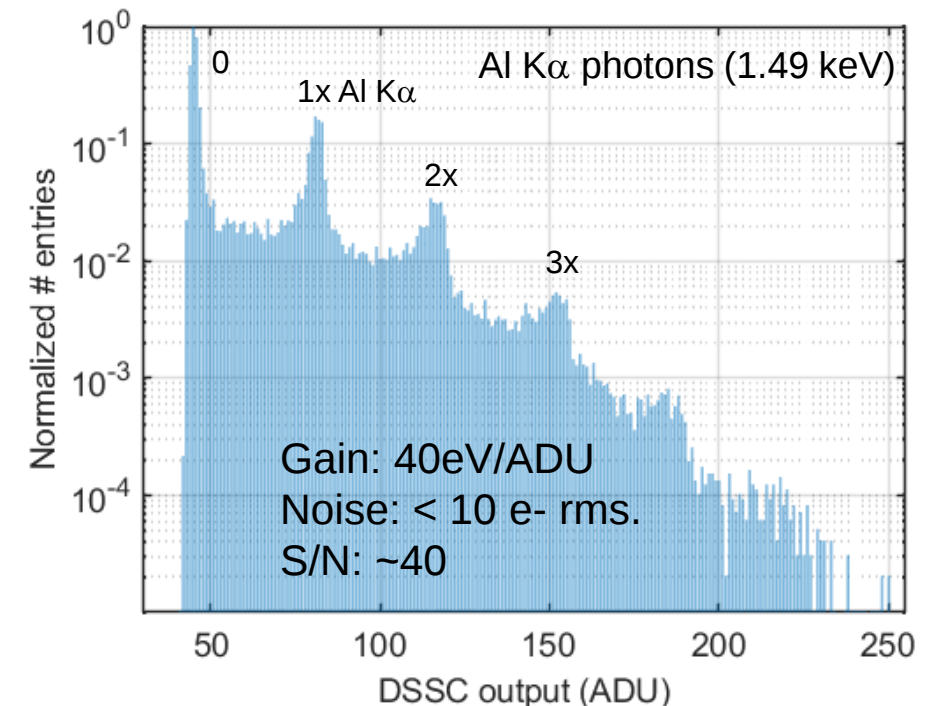
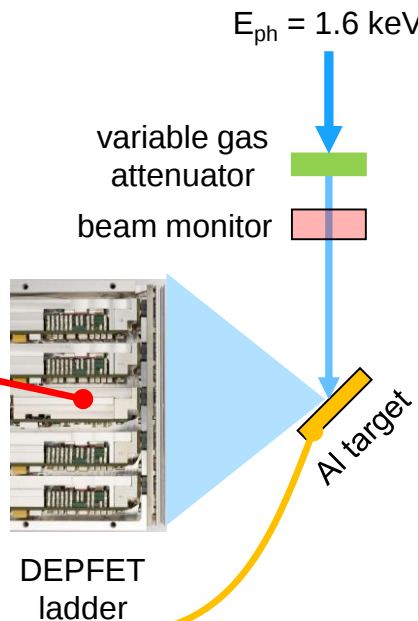
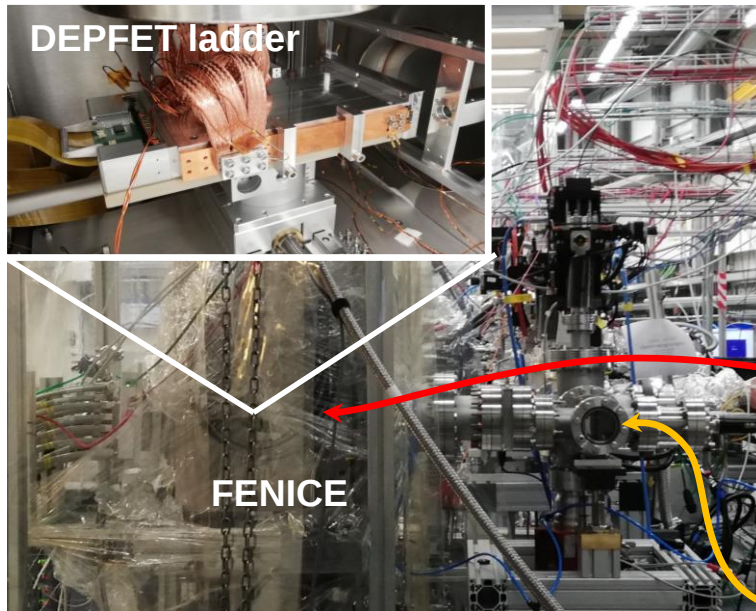


1st kink Energy:
 80.6 ± 5.4 keV
Gain (linear):
473 eV/ADU
DR (@ 473eV ph):
 > 2000 ph



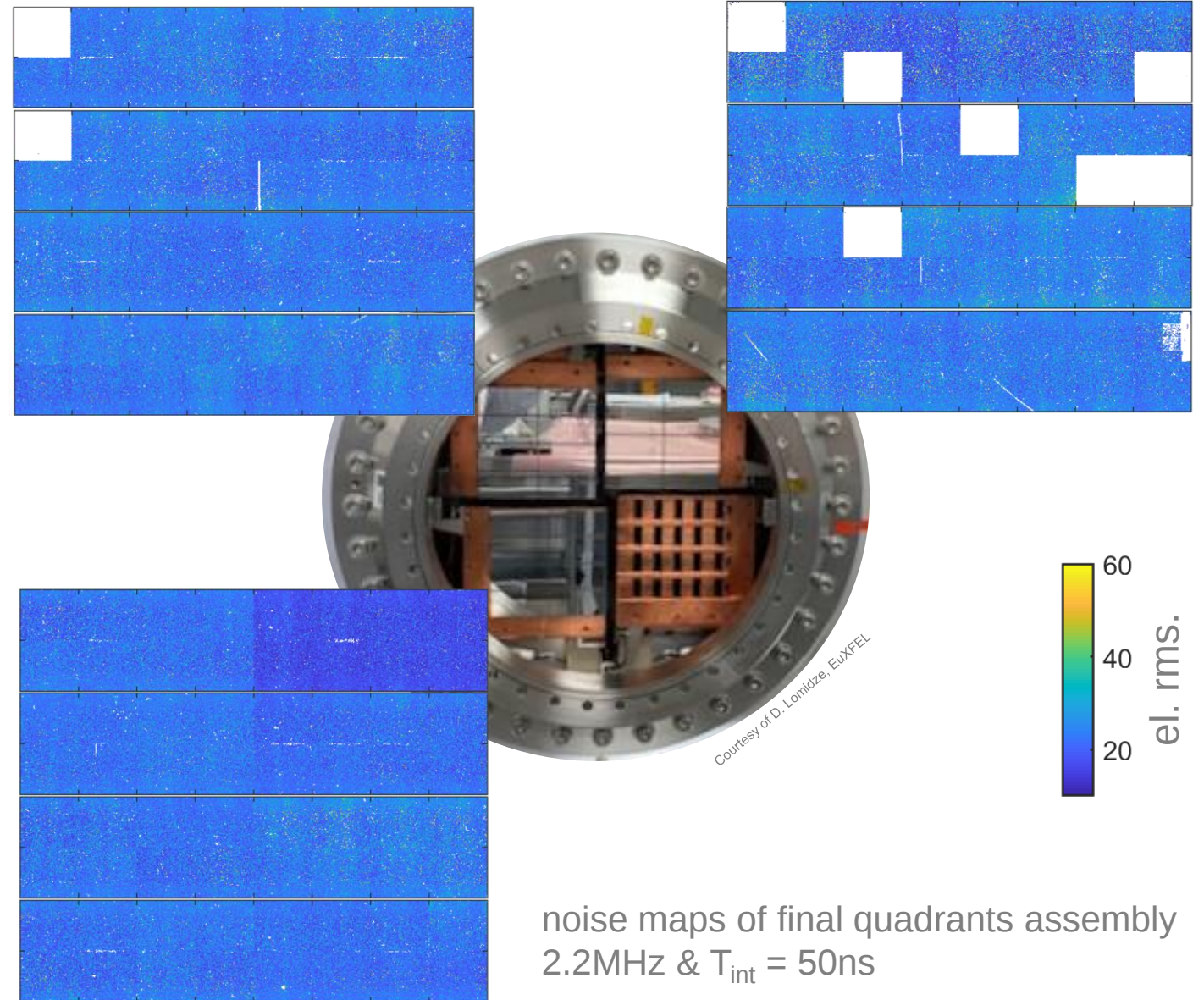
Spectroscopic performance @ XFEL

- 1st prototype characterization at Small Quantum System (SQS) Instrument in two beamtimes @ EuXFEL
- XFEL beam on Al target
- DEPFET ladder mounted in FENICE vessel in a branch of the interaction chamber perpendicular to the XFEL beam in order to collect Al fluorescence photons (Al K α 1.486 keV).



Mass production & camera assembly

- All modules qualified in lab @ DESY:
 - ADC gain & offset trimming capabilities (ASIC verification)
 - I_{bias} estimation and equalization & I_{leak} measurement
 - Low & Hi gain calibration with ^{55}Fe
 - NL response characterization
- 1st sensor production enough to produce 2 quadrants with minor issues, a quadrant populated with spares and a “perfect” single ladder setup



Summary

- The second 1-Mpixel camera will be based on CMOS-DEPFET active pixel sensors will allow single photon detection and high dynamic range simultaneously.
- First operation of a CMOS-DEPFET ladder confirms the expected improvements given by the DEPFET technology
- ENC can be as low as to 9.8 e- rms at 1.1 MHz and room temperature
- Dynamic range is of several thousands 1 keV photons
- Modules have been delivered to EuXFEL and integration finished, testing ongoing
- Waiting for completion of 2nd DEPFET production to fully equip the 2nd DSSC camera

Thank you

Contact

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Synchrotron DESY

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