# The H2M Monolithic Pixel Detector Prototype

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# H2M (Hybrid-to-Monolithic) Pixel Detector Prototype

#### Common design and testing effort between:









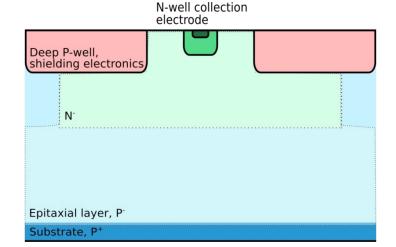


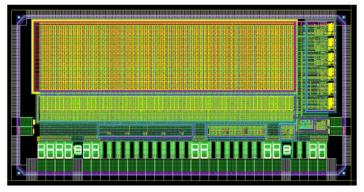
#### Development goals:

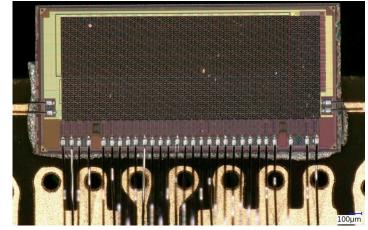
- Study the challenges of porting a known hybrid pixel detector architecture into a monolithic chip
- Exercise digital-on-top design flow and methodology in monolithic process
- Design and test a compact digital cell library

# **Sensor Layout**

- Monolithic pixel sensor designed and fabricated in 65 nm
   CMOS imaging process
  - Pixel matrix: 64 × 16 pixels
  - Pixel pitch: 35 µm
  - Total sensitive area: 2.24 × 0.56 mm<sup>2</sup>
  - Relatively thin epitaxial layer
  - Sensor: n-gap layout
- N-gap layout
  - Additional n-doped layer with gaps around pixel edge
  - Ensure charge collection from pixel edges and corners
  - 2.5 µm gap size

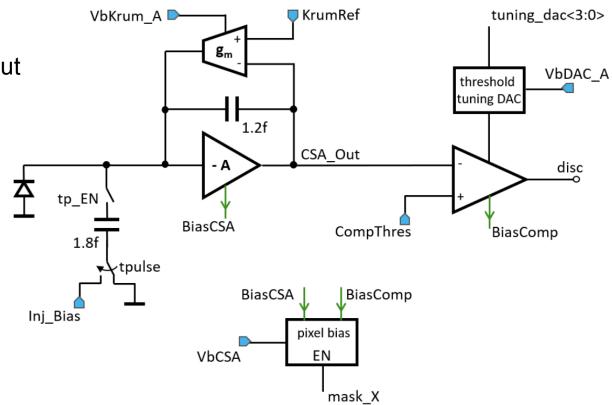






# **Pixel Analog Front-End**

- Charge-sensitive amplifier (CSA)
  - Gain stage and Krummenacher feedback
  - Test pulse injection via capacitance at CSA input
  - Bias set via 8-bit global DAC
- Continuous-time threshold comparator
  - Global threshold via 8-bit DAC in periphery
  - Per-pixel threshold tuning with a 4-bit DAC, global bias DAC to adjust tuning step size
- Mask bit to disable and power down pixel
- Comparator output processed by digital pixel logic



: provided from periphery

→: distributed on pixel level

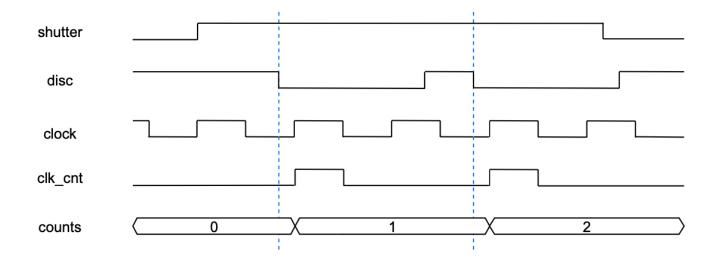
# **Pixel Digital Logic**

8-bit in-pixel counter with 4 different acquisition modes:

- Frame-based acquisition modes
  - Active window defined by external shutter signal
  - Time of arrival (ToA)
  - Time over threshold (ToT)
  - Photon counting
- Triggered binary readout

#### Photon counting mode:

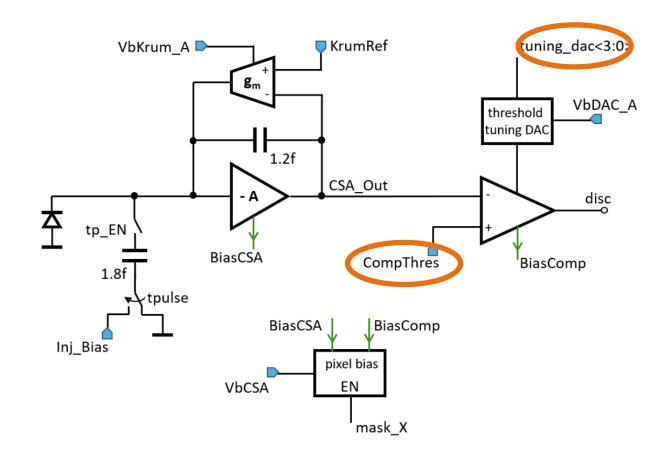
- Triggering on discriminator falling edge
- Counts number of threshold crossings i.e.
   CSA output exceeds comparator threshold



# **Noise Based Pixel Trimming**

- Scanning of pixel threshold for different pixels
  - → per-pixel *tuning\_dac*
- Aim: optimize tuning\_dac settings for minimal threshold dispersion
- Scan of comparator threshold (CompThres)
  - Photon counting mode
  - Number of threshold crossings increase close to pixel baseline
  - Maximum of distribution marks baseline

Repeat threshold scan for all tuning\_dac settings

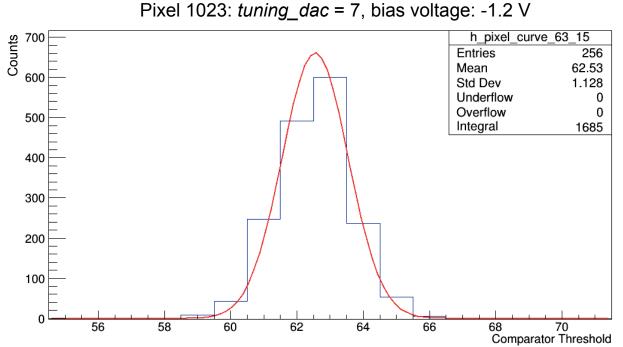


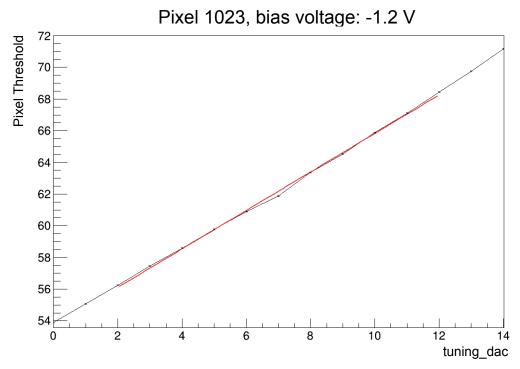
: provided from periphery

→: distributed on pixel level

# **Analysis of Noise Scans**

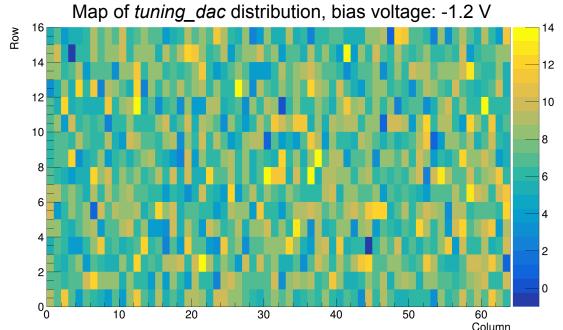
- Gauss fit for all pixels and tuning\_dac settings to find individual pixel threshold
- Select trimming target within threshold range of all pixels
- Find matching tuning\_dac setting via linear fit considering the standard error of the mean SEM =  $\frac{\sigma}{\sqrt{N}}$
- Create mask file with tuning\_dac settings for different pixels



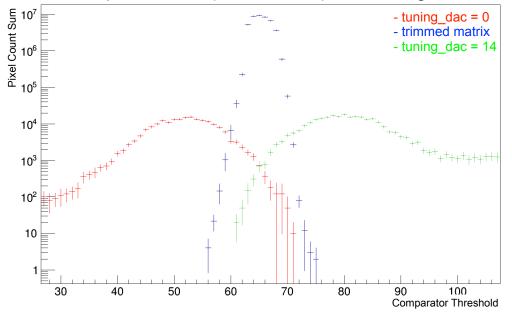


### **Trimmed Pixel Matrix**

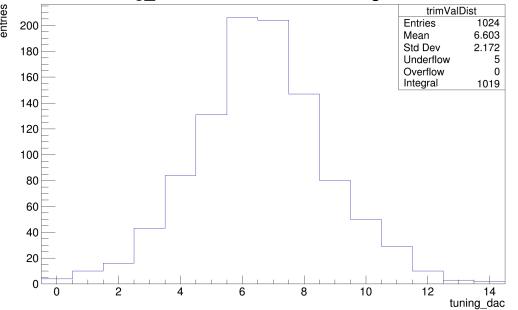
- Scan of comparator threshold shows steep distribution with small standard deviation around trimming target
- Trimming: no trends in pixel matrix observable
- tuning\_dac distribution makes use of full dynamic range
- Approximately 0.5% of the pixels are not tuneable



#### Sum of pixel counts (whole matrix), bias voltage: -1.2 V

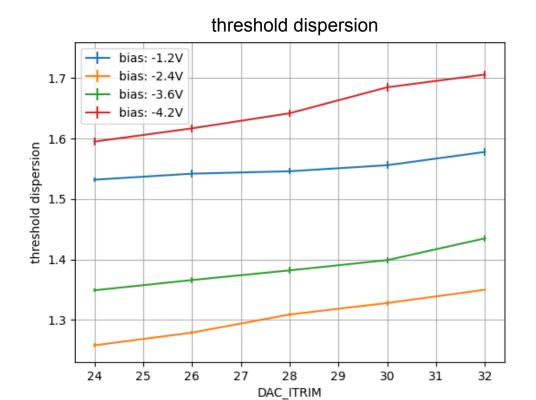


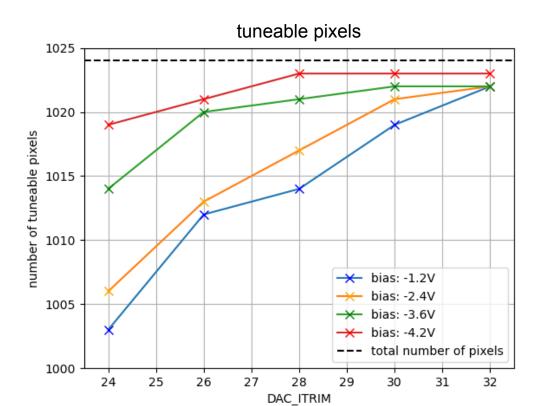
tuning dac distribution, bias voltage: -1.2 V



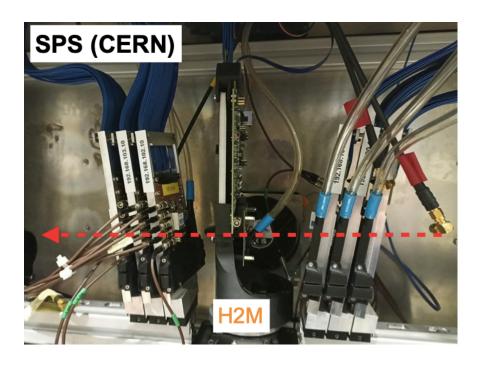
# Global Biasing DAC\_ITRIM Optimization

- Variation of tuning\_dac bias current to adjust tuning step size by changing the pixel slope
  - ⇒ affects range covered by *tuning\_dac* settings, amount of tuneable pixels and threshold dispersion
- Compromise between low threshold dispersion and high amount of tuneable pixels
- Choose operation point for different bias voltages based on these results



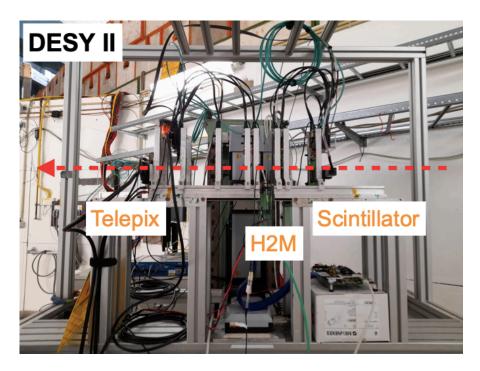


# **Test Beam Campaigns**



#### SPS @ CERN

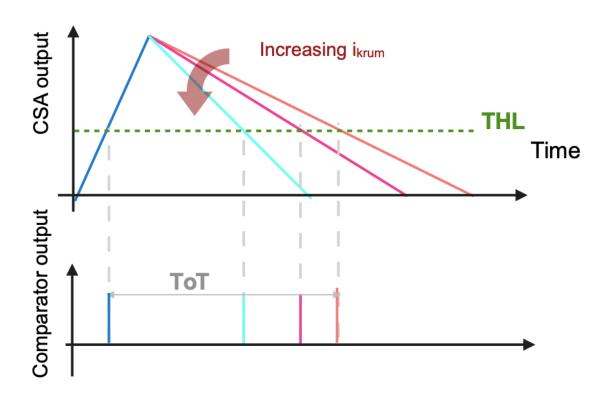
- Beamline H6, 120 GeV/c charged pions
- Timepix3 reference telescope
  - → Pointing resolution ~ 1.8 µm
  - → Track time resolution ~ 1 ns

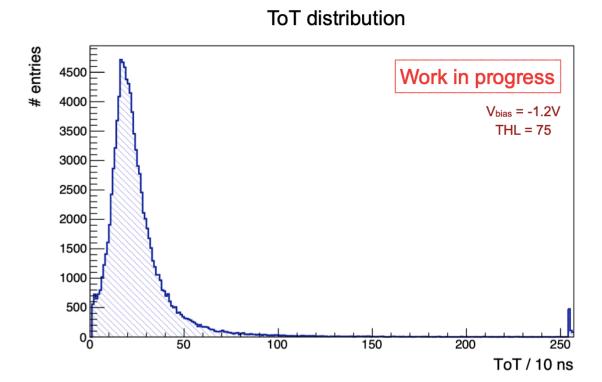


#### **DESY II**

- Beamline 22, electron beam with ~ 4.8 GeV
- Alpide reference telescope
  - → Pointing resolution ~ 3 µm

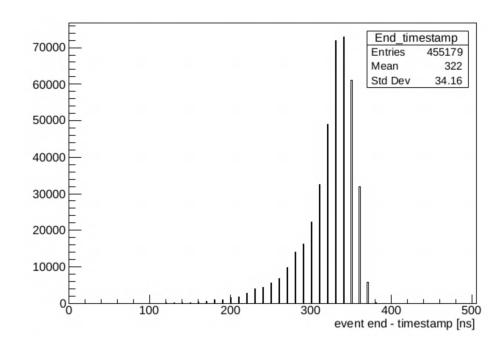
# **ToT Distribution**

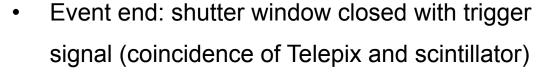




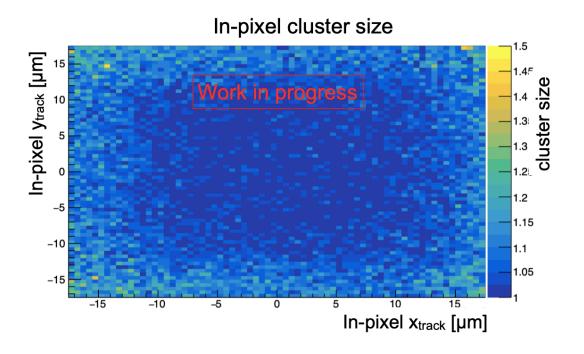
- Return to baseline adjusted with Krummenacher current
  - → ToT distribution used to tune Krummenacher current
- Analysis ongoing for data at different bias voltages and hit detection thresholds

## **ToA and Cluster Size Distribution**





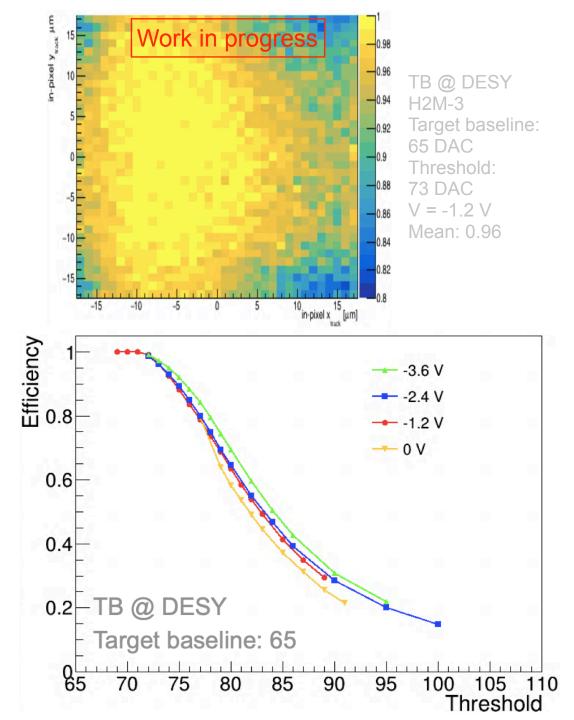
- Timestamp: hit in H2M
- Time resolution  $\approx$  34.16 ns
- Tail in distribution due to time walk



- Dominated by cluster size 1
- Larger cluster size in edges and corners due to charge sharing

# **In-Pixel Efficiency Map**

- Unexpected in-pixel efficiency pattern observed
  - For different bias voltages (less pronounced at larger bias voltage)
  - At different hit detection thresholds
  - In both tested assemblies (H2M-2 and H2M-3)
  - During test beams at SPS and at DESY II
- Seems to be related to the position of the analog and digital part of the front-ends



# **Summary & Outlook**

#### **Summary**

- Full hybrid design ported into monolithic chip in 65 nm
   CMOS imaging process
- Successful first laboratory measurements
  - Implementation and optimization of pixel trimming procedure
  - Chip features work as intended
- First test beam campaigns at SPS and DESY II
  - Chip DAQ works as intended
  - ToT and ToA modes successfully tested
  - Integration with reference planes and trigger signal

#### **Outlook**

- Front-end parameter optimization
- Charge calibration for the test beam characterization of the used samples
- Testing of photon counting mode and triggered binary readout
- Further analysis of test beam data for different acquisition modes
- Studies of efficiency patterns
- Comparison of test beam results and simulations

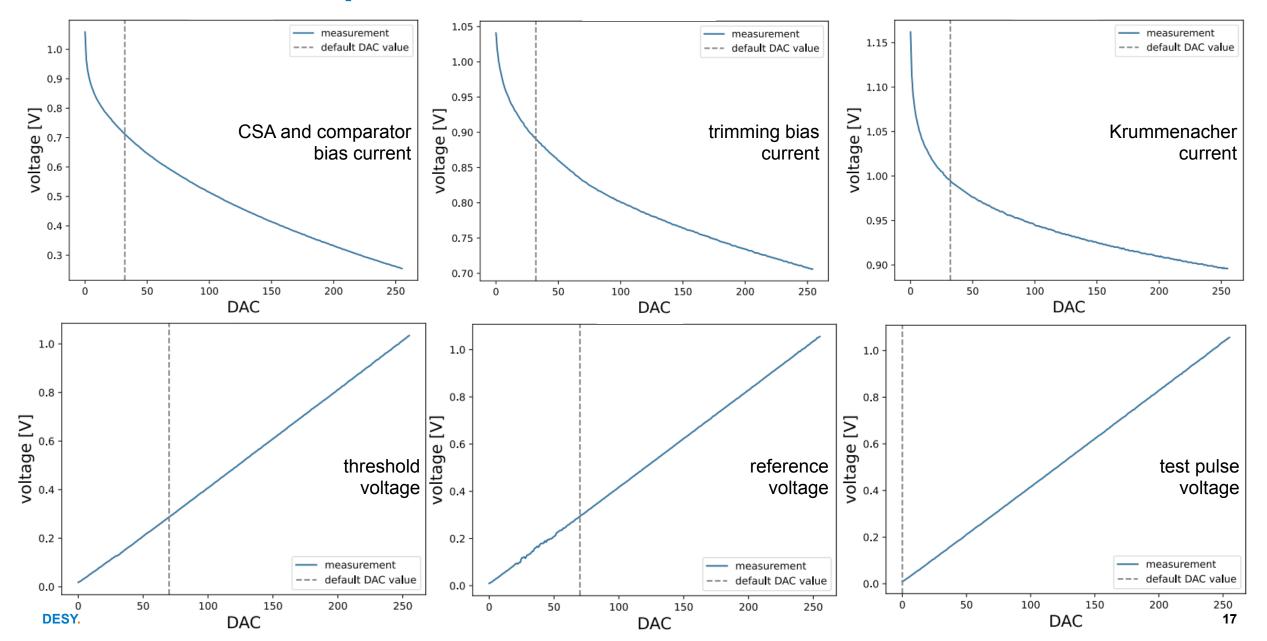


#### **Contact**

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Tangerine
judith.schlaadt@desy.de

# **Backup Slides**

# **DAC Scans - Expected Behaviour Observed**



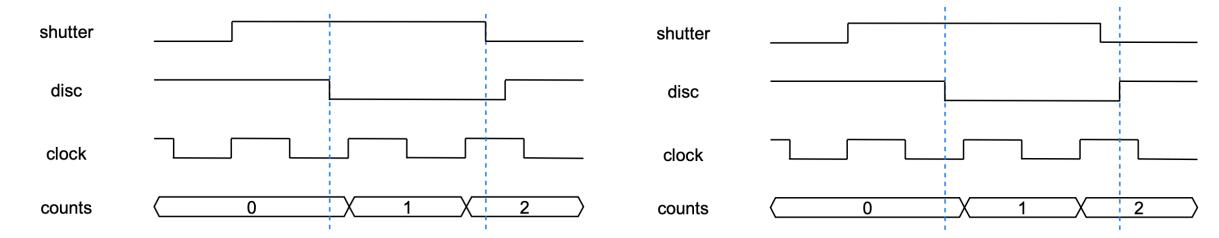
# **Frame-based Acquisition Modes**

Time-of-arrival (ToA)

- Triggering on discriminator falling edge
- Counts number of acquisition clock cycles until shutter window closes
- 100 MHz acquisition clock: 10 ns binning

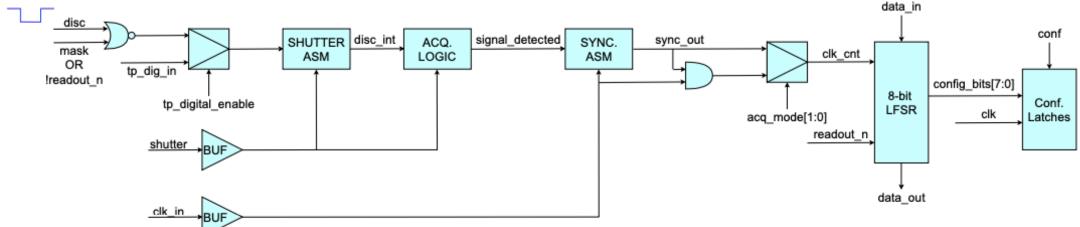
Time-over-threshold (ToT)

- Triggering on discriminator falling edge
- Counts number of acquisition clock cycles until discriminator signal rising edge
- ToT ~ collected charge (after calibration)



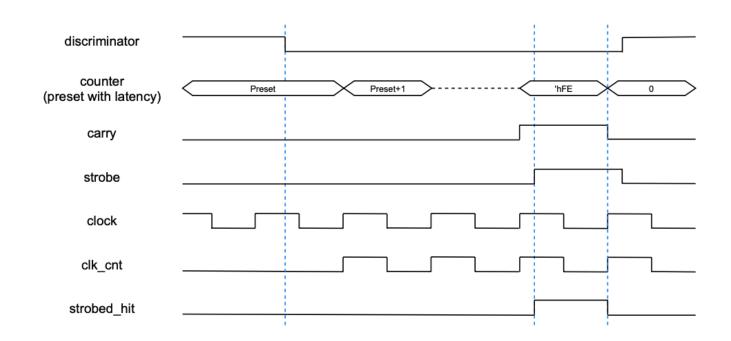
# Pixel Digital Logic: Frame-based Acquisition Modes

- Discriminator output: readout or masking
- Digital test pulses: enabling overwrites discriminator output
- Shutter asynchronous state machine (ASM): discards trigger outside of shutter window
- Acquisition logic (ACQ. LOGIC): produces signal based on used acquisition mode
- Synchronising logic (SYNC. ASM): synchronises signal to acquisition clock
- Counting → data stored in 8-bit linear-feedback shift register (LFSR); 8-bits for pixel configuration
  - Readout: 8-bits shifted from top to bottom of column
  - Configuration: 8-bits shifted from bottom to top of column and set to pixels



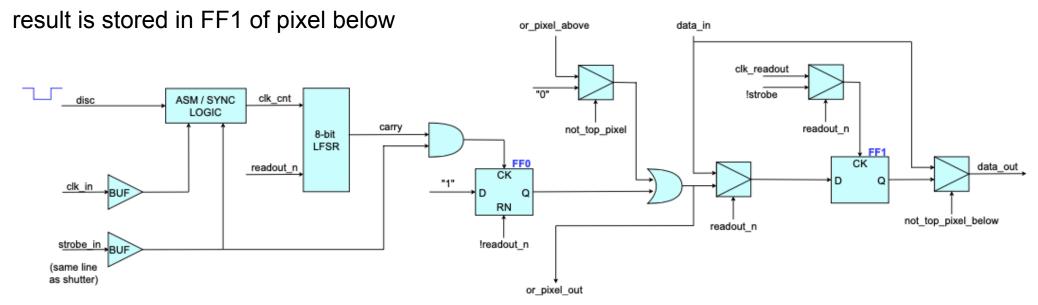
# **Triggered Binary Readout**

- Counter preset with trigger latency value
- Triggering on discriminator falling edge
   ⇒ starts counter at preset value
- Carry signal produced as soon as counting reaches overflow
- External strobe signal provided, synchronised with acquisition clock
- Hit: carry and strobe signal in coincidence
- Variable configuration: pixel stores its own hit or combines data from group of pixels



# Pixel Digital Logic: Triggered Binary Readout

- External strobe signal is distributed analogously to shutter signal
- Hit when carry and strobe signal are in coincidence: flip-flop (FF0) is set
  - ⇒ Result registered to flip-flop (FF1) after delay (one clock cycle after strobe signal rises)
  - ⇒ Readout of FF1
- Possible to combine information of several pixels via not\_top\_pixel configuration of pixel below:
  - not\_top\_pixel = 0: hit will be stored in FF1 and read out
  - not\_top\_pixel = 1: FF0 is input to FF0 of pixel below; information of both pixels is ORed and



# **Tuning DAC**

#### Mapping

- Implemented in peary
- tuning\_dac 0: most negative comparator offset voltage
- tuning\_dac 7: zero comparator offset voltage (no shift)
- tuning\_dac 14: most positive comparator offset voltage

#### Threshold *tuning\_dac* control bits for DAC\_ITRIM 82 nA

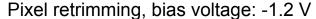
tuning_DAC					Comp.	Comp. offset
<0>	<1>	<2>	<3>	DAC#	current (nA)	voltage (mV)
0	0	0	0	0	+370.6	+41
0	1	0	0	2	+318.8	+35
0	0	1	0	4	+266.4	+29
0	1	1	0	6	+213.8	+23
0	0	0	1	8	+161.0	+17
0	1	0	1	10	+107.8	+12
0	0	1	1	12	+54.3	+6
0	1	1	1	14	0	0
1	1	1	1	15	0	0
1	0	1	1	13	-54.3	-6
1	1	0	1	11	-107.8	-12
1	0	0	1	9	-161.0	-17
1	1	1	0	7	-213.8	-23
1	0	1	0	5	-266.4	-29
1	1	0	0	3	-318.8	-35
1	0	0	0	1	-370.6	-41

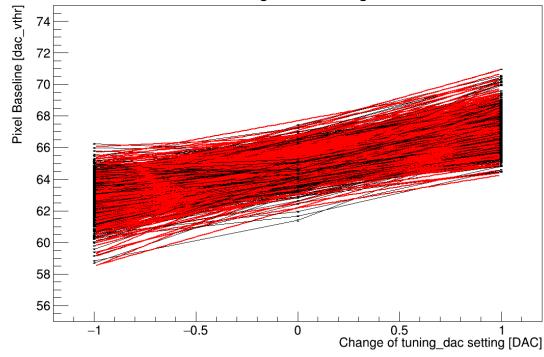
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# **Pixel Retrimming**

Re-evaluation of fractions of the matrix:

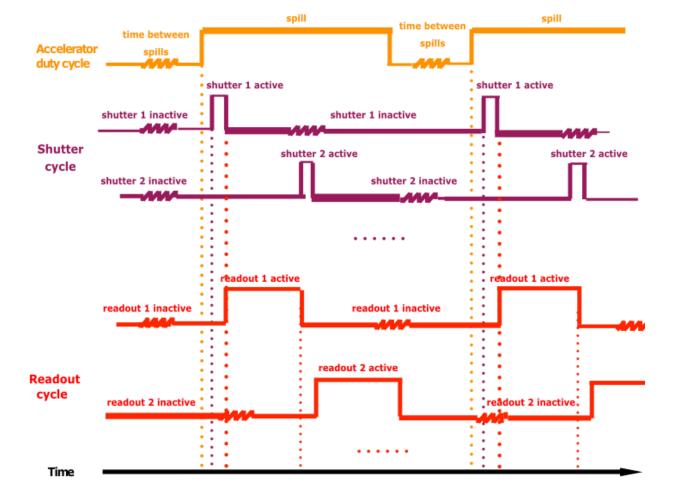
- Performing two more noise scans with tuning\_dac settings above and below the initial setting
- Combine these information and redo linear fit for all pixels in "region of interest"
  - ⇒ changes *tuning\_dac* setting for approximately 40% of the pixels
- Retrimming only slightly reduces threshold dispersion
  - ⇒ indicates stable voltage supply within pixel matrix

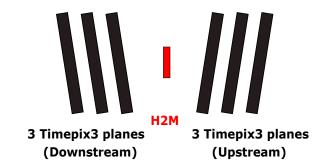




Method	Mean	Standard Deviation
Lin. Fit	66.28	1.63±0.01
Retrimming	65.35	1.57±0.01

# Test beam measurements @ SPS

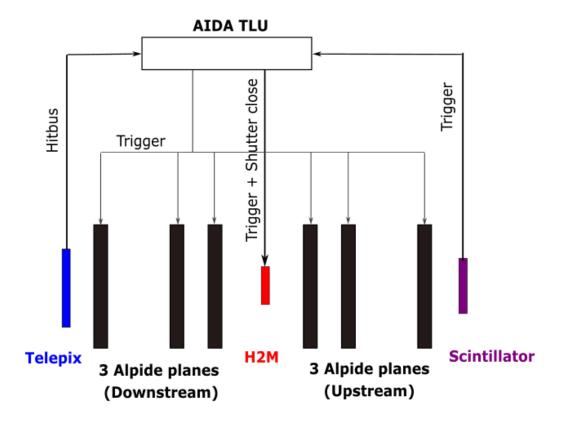




 Trigger Logit Unit (TLU): provides global clock (40 MHz) and T0 for the telescope and DUT.

- H2M:
- ToT mode
- Gated with SPS spill signal
- Shutter window of 150 µs
- Readout time ~ 500 μs
- Timepix3:
  - In data-driven mode
  - Selecting region of interest (ROI)

# **Test Beam Measurement @ DESY**

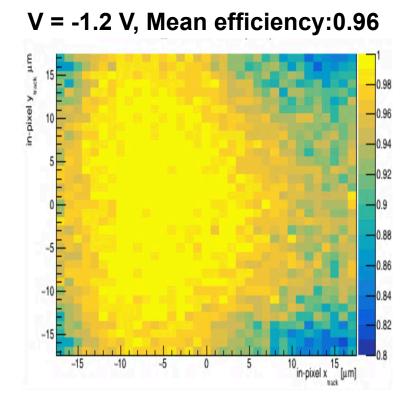


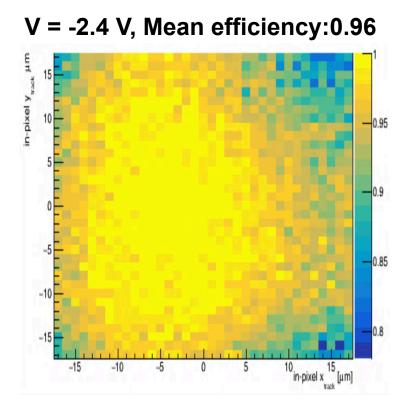
• Trigger Logit Unit (TLU): provides global clock (40 MHz) and T0 to all devices.

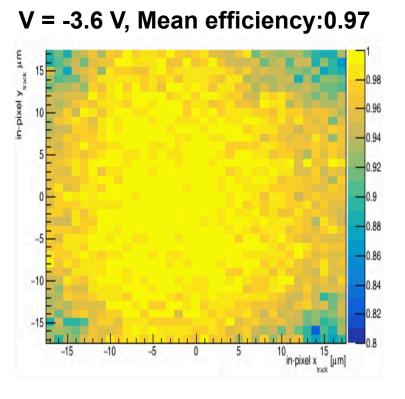
- Trigger signal:
  - Coincidence of Telepix AND scintillator
  - ROI defined on Telepix
- H2M:
  - ToA mode
  - Shutter opened after previous readout
  - Shutter closed with trigger signal
  - Readout time ~ 500 μs

# In-pixel efficiency maps: threshold = 73

Target baseline: 65

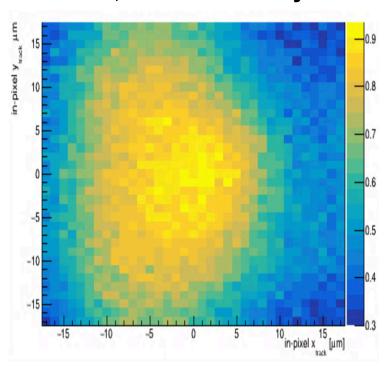




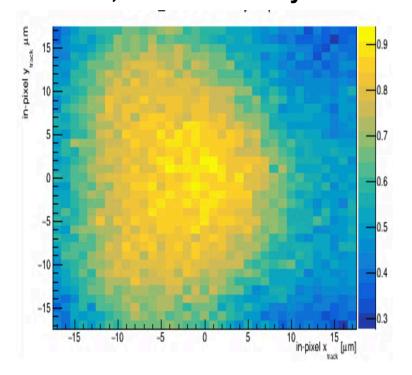


Pattern less visible at higher bias voltages

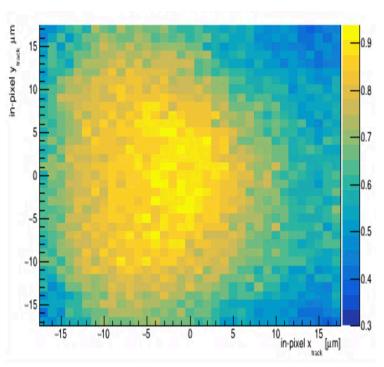
V = -1.2 V, Mean efficiency: 0.63



V = -2.4 V, Mean efficiency: 0.65



V = -3.6 V, Mean efficiency: 0.69



Pattern still visible at higher bias voltages

# **Caribou Data Acquisition System**

