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QUANTUM UNIVERSE

CMS HGCal Software

Calibration and Electronics Mapping

DESY R&D Retreat January 19 2024

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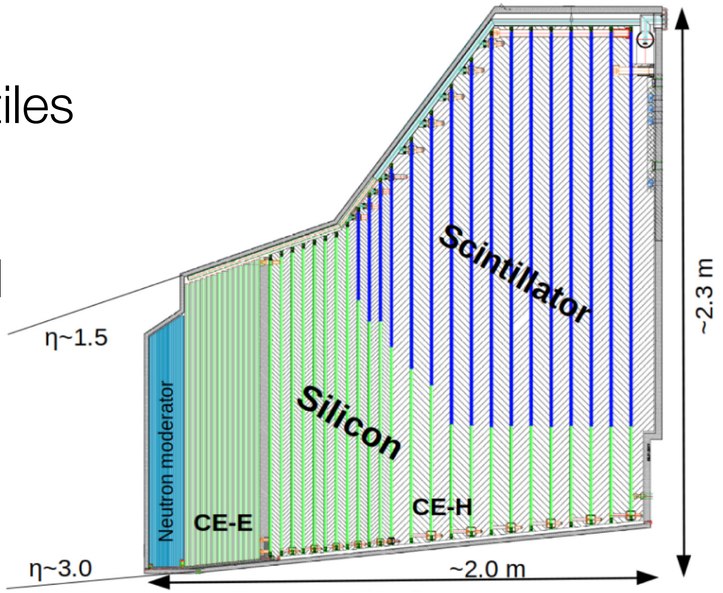
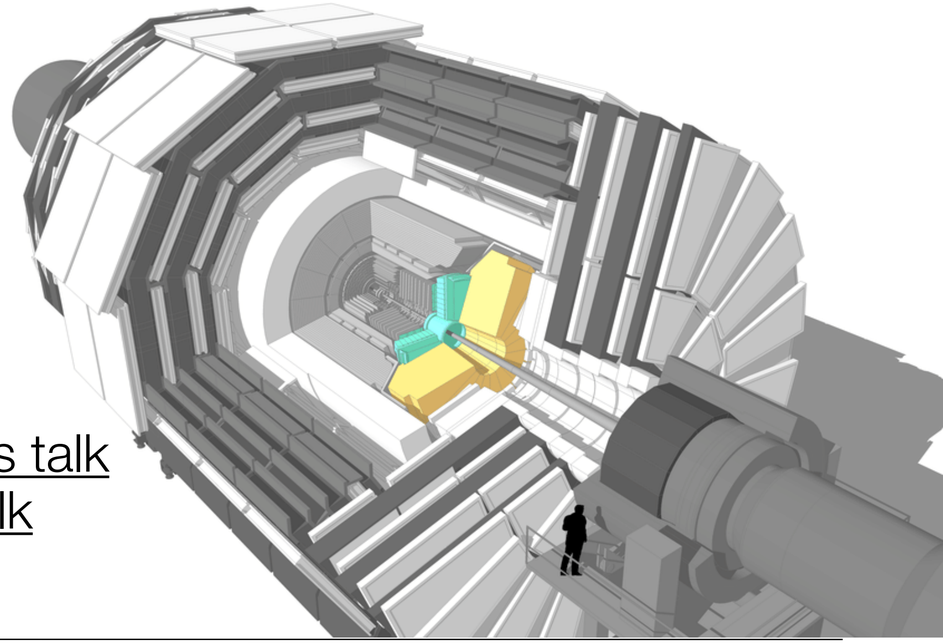
The High Granularity Calorimeter (HGCal)

Part of the CMS Upgrade: to replace the existing **endcap** Preshower, Electromagnetic Calorimeter (ECAL) and Hadronic Calorimeter (HCAL)

47 layers covering $1.5 < \eta < 3.0$:
CE-E: Si sensors
CE-H: Si sensors and Scintillator tiles

6M Silicon channels in total
240k Scintillator channels in total
with SiPM read-out





DESY HGCal efforts:
Design & Tests of Tilemodules for the CMS HGCAL - see Gabriele's talk
QC for tiles and Tilemodules for the CMS HGCAL - see Ji-Hao's talk
CMS HGCal Software: Calibration and Mapping - this talk

CMS HGCal Software

DESY Contributions

Total event size of HGCal expected to be 2.5-3.5 MB → approx. 40% of the total CMS event size

→ Important to be able to decode this data **fast** enough to not compromise the time spent on the CMS High Level Trigger (HLT)

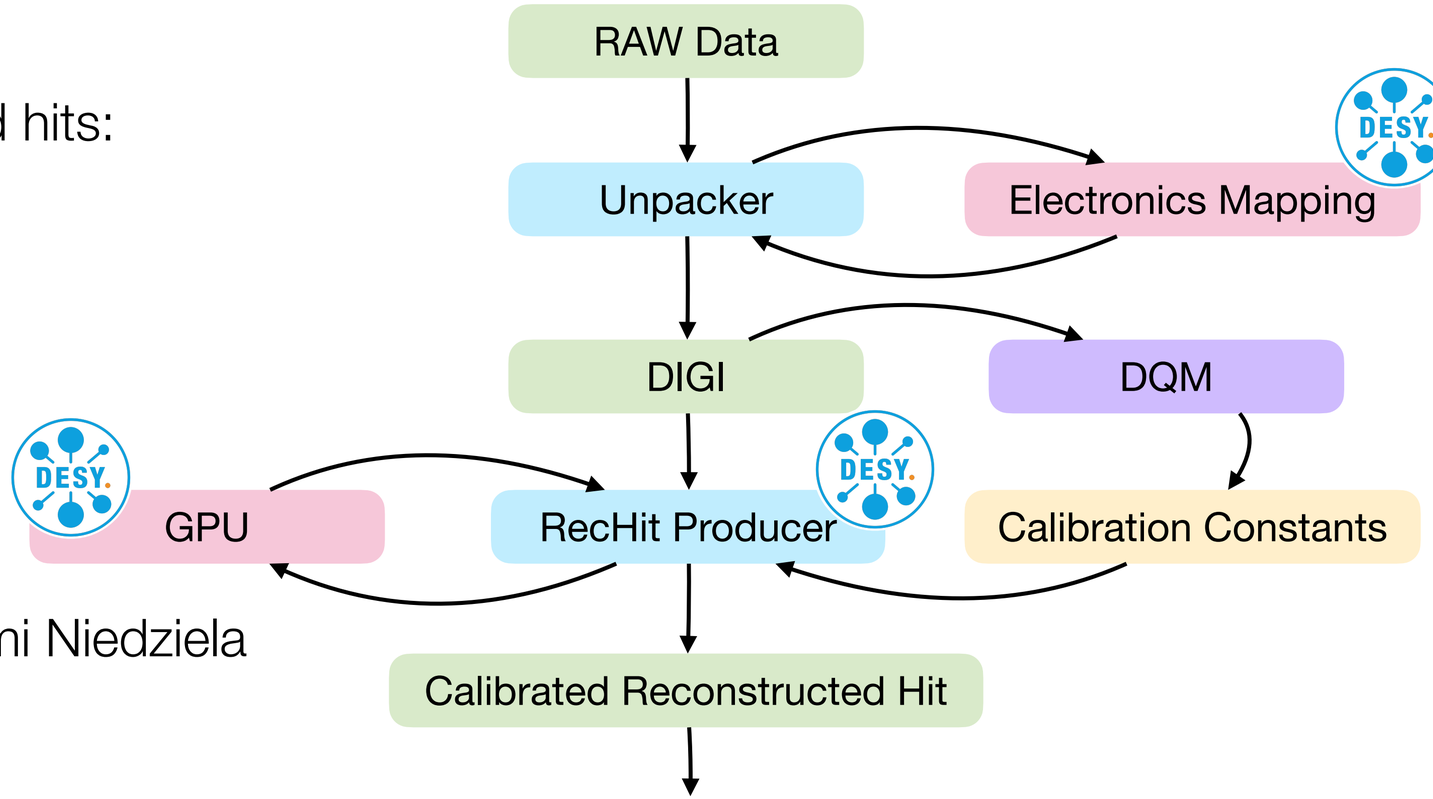
From Raw Data to Calibrated reconstructed hits:

Raw data to DIGI format by the unpacker

- **Electronics Mapping** - Lovisa Rygaard

DIGI to Calibrated Reconstructed Hits by the RecHit Producer

- Calibration Constants from DQM
- **Calibration Calculations on GPU** - Jeremi Niedziela



Electronics Mapping

HGCal Electronics Mapping

We need to be able to efficiently geometrically identify a sensor when unpacking the raw data, and to emulate the packing of digis using geometrical simulation:

Electronic Identifiers: ⟷ **Geometrical Identifiers**

Using IDs stored as 32-bit words in CMSSW:

HGCal Electronics ID

	Range	#bits
Common mode channel flag	1	1
FED ("S-link x DAQ")	0-575	10
Capture Block	0-9	4
ECON-D idx in capture block	0-11	4
ECON-D eRX	0-11	4
½ ROC channel	0-36	6

⟷

HGCal Scintillator Detector ID

	#bits
type	2
ring	8
iphi	9
layer	5
z-side	1
trigger	1
SiPM size	1
detector type	4

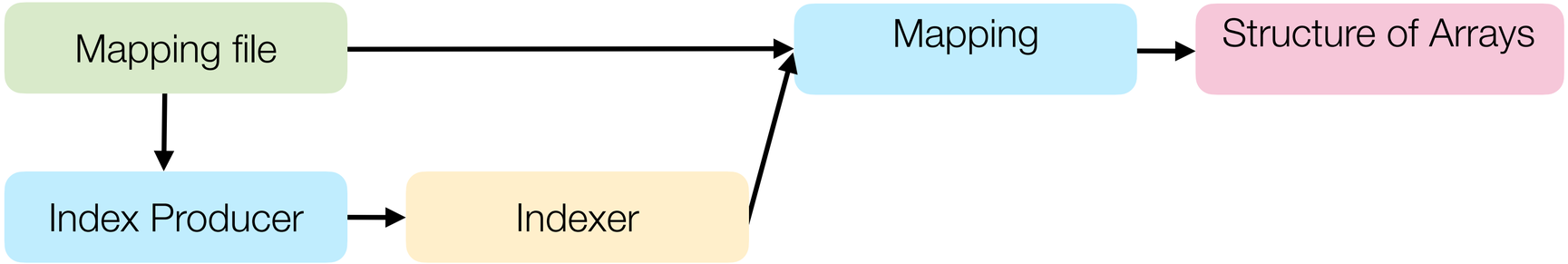
HGCal Silicon Detector ID

	#bits
type	2
cell u	5
cell v	5
wafer |u|	4
sign wafer u	1
wafer |v|	4
sign wafer v	1
layer	5
z-side	1
detector type	4

We do this by mapping out all necessary ID information to uniquely identify each module and cell

HGCal Electronics Mapping

Workflow



The mapping files contain all electronic and geometrical information of each module and cell
→ 3 text files: 1 for all module types, 1 for Si cells, 1 for SiPM-on-tiles

The Mapping Producer parses the mapping files and store the information in Structure Of Arrays (SoA)
→ used for running on GPU (with the alpaka library)
→ 2 SoAs: Module SoA and Cell SoA

The Index Producer and the Indexer provides dense indices of modules and cells which are assigned to the SoAs
→ modules and cells of same type are grouped together to optimize the memory assignment for types with varying sizes

Mapping file

Silicon Geometry

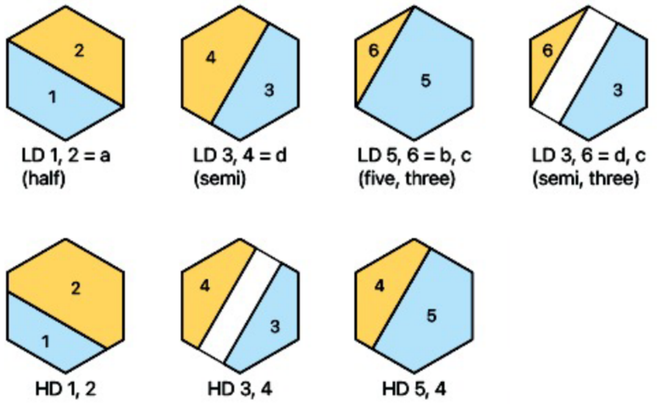
Modules and Cells

The geometrical position of a sensor is given using the variables

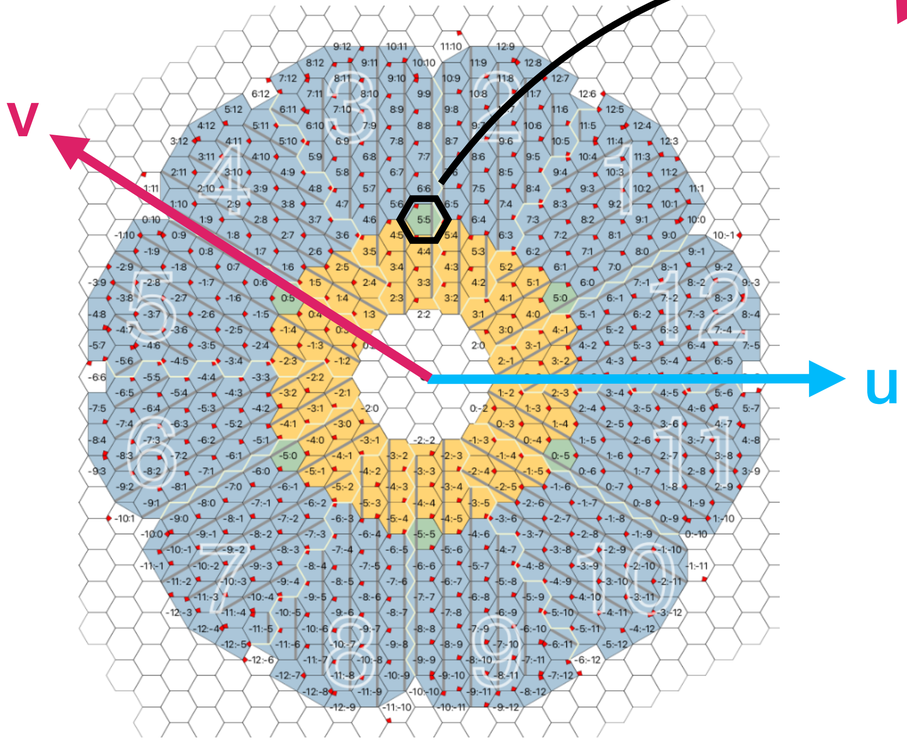
- u
- v

Mapping the geometrical positions is done in two steps:

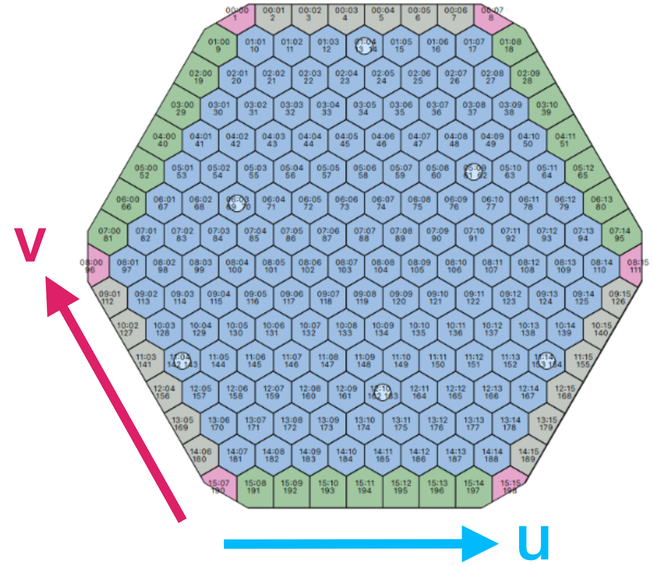
- module location in a layer
- cell location in a module



Modules



Cells



Mapping file

Scintillator Geometry

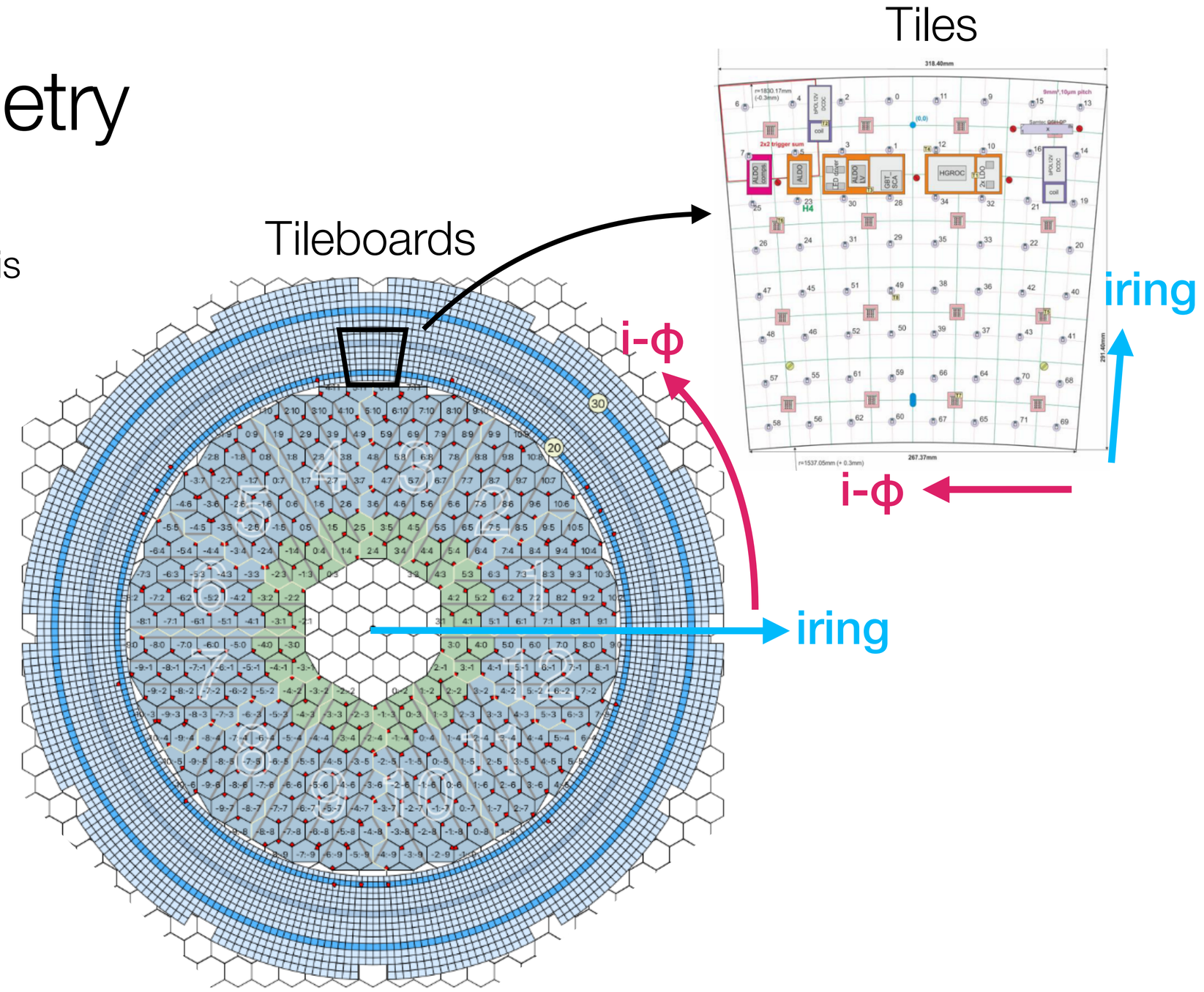
Tileboards and Tiles

The geometrical position of sensor is given using the variables:

- iring
- i-ϕ

Mapping the geometrical positions is done in two steps:

- tileboard location in a layer
- tile location on a tileboard



Structure of Arrays

Stores all information needed for the Electronics and Detector IDs

Raw Electronics ID is calculated as: **Module eleid + Cell eleid**
for both Si and SiPM SoAs

Similarly, the raw Detector ID is retrieved as: **Module detid + Cell detid**
for Si SoA
The raw Detector ID for SiPM dependents on combined information of module and cell → created using a help function with input from both SoAs

Module SoA	Cell SoA
z-side	iscalib
isSiPM	isSiPM
typeidx	typeidx
u / iring	u / iring
v / iphi	v / iphi
celltype	cellidx
fedid	chip
slinkidx	half
captureblock	seq
econdidx	rocpin
captureblockidx	triglink
eleid	trigcell
detid	trace
	t
	eleid
	detid

Time of retrieving the raw ElectronicsId and Silicon DetectorIds 6M times:

Raw value	Method	Time to retrieve
Electronics ID	module eleid + cell eleid	0.7 µs
Silicon Detector ID	module detid + cell detid	0.3 µs
Scintillator Detector ID	getSiPMDetectorID(zside, plane, module u, celltype, cell u, cell v)	2ms

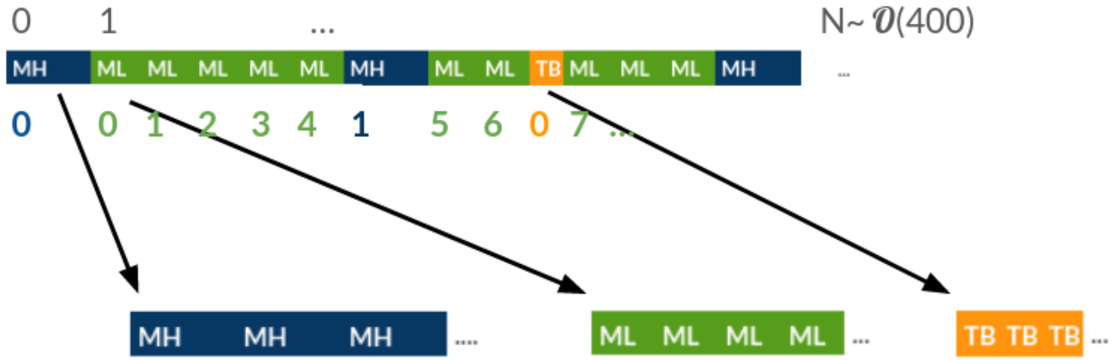
Compared to retrieving SiPM DetectorId 390k times

This only has to be done once at the start when filling the SoAs, and not event by event

Indexing

MH: HD Module
ML: LD Module
TB: Tileboard

The sequence of the indices for the SoAs correspond to the sequence of the readout channels of the modules



The dense indexing for a fixed system with N components is given as:

$$rtn = i_N \times \left\{ \max_{n-1} + i_{n-1} \times \left[\max_{n-2} + i_{n-2} \times (\quad \cdots \quad) \right] \right\}$$

max elements expected in category N-1

index for category N-1

However, different modules have different packet sizes

→ the dense indexing is implemented **separately for each module type**

Modules of the same type are **grouped together** and the offsets for the modules types in the readout sequence are pre-computed

The index of each readout-type is assigned the same value for the modules and cells

→ can be used to determine if a cell is part of a module

Calibration

HGCal Calibration

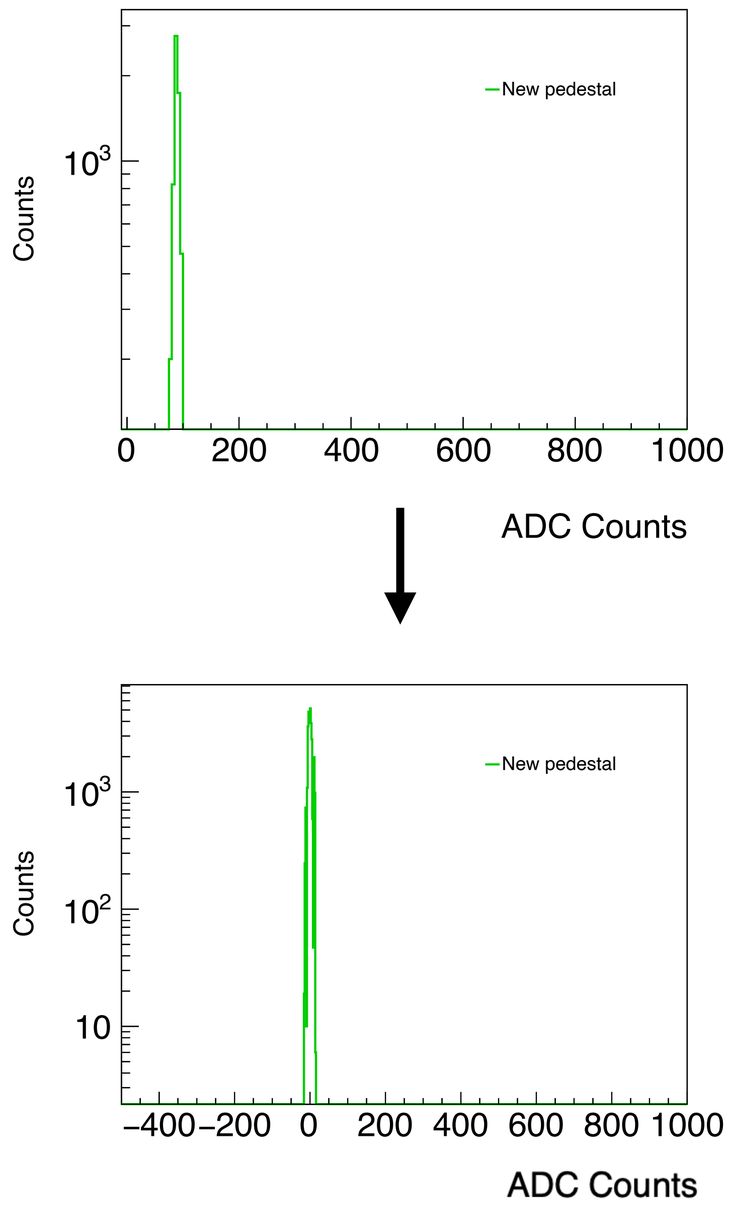
The calibration of the digis are handled by the RecHit Producer

- accessing calibration constants
- deciding which calibrations to apply
- preparing collections of digis
- creating RecHit objets with needed information

Each hit has to be **calibrated**:

- ADC vs. ToT mode,
- pedestal,
- Common Mode,
- previous bunch crossing,
- …
- ADC/ToT to energy conversion.

Example on the right → pedestal subtraction

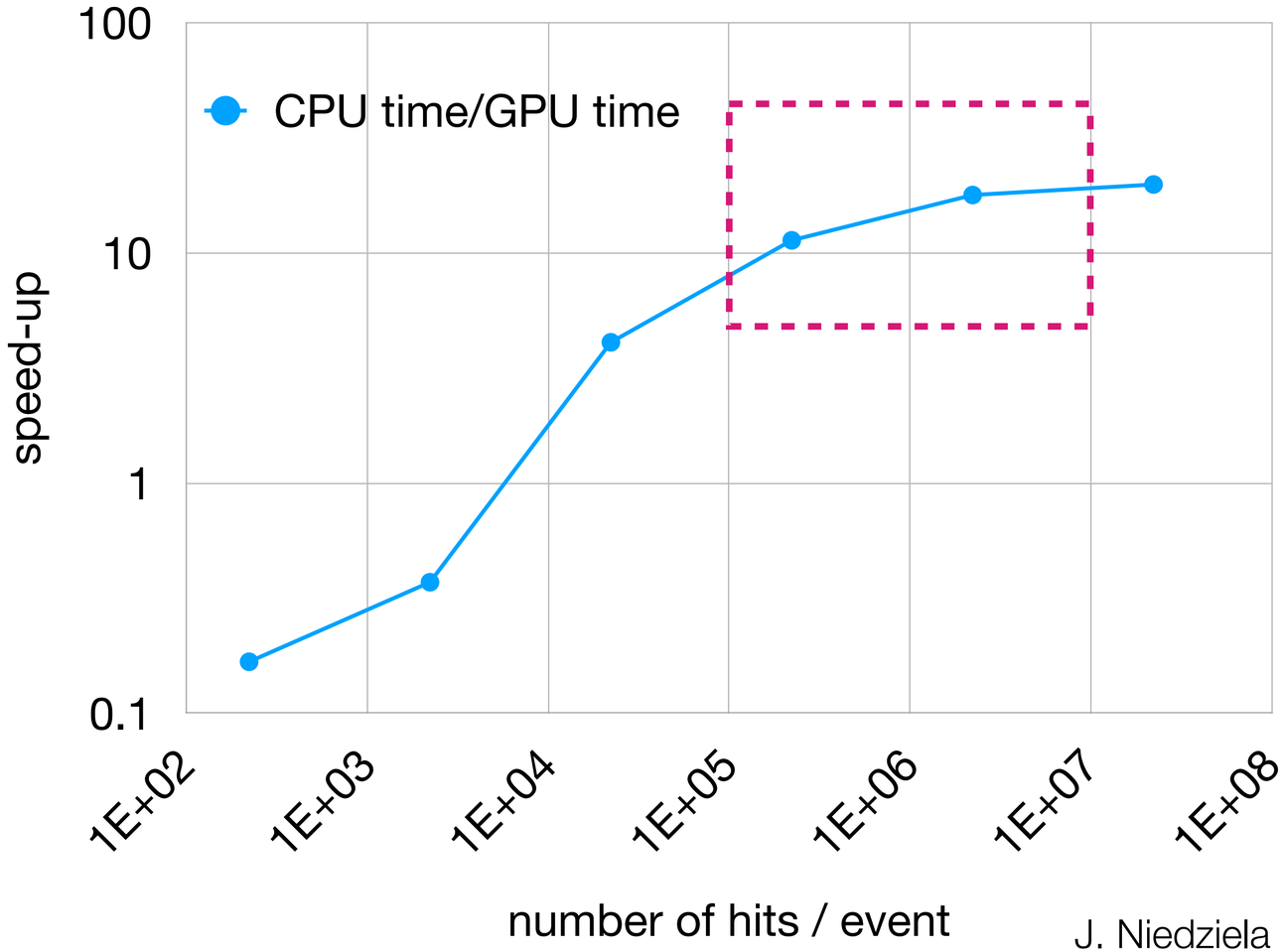


HGCal Calibration

These operations have to applied to **large collections** and all operations have to be **very fast** to fulfill the trigger timing requirements

Calibration implemented with **GPU/CPU support:**

- for operations which RecHit Producer needs to perform calibration
- **factor 10 speed-up** for a realistic number of hits/event
- validating on test-beam data



J. Niedziela

Summary and Status

The ongoing DESY efforts to the HGCal Software:

Calibration:

Implemented GPU/CPU support for calibration calculations with a **factor 10 speed-up**

Validation is done on test-beam data

Electronics mapping:

Successfully implemented **efficient mapping** between electronic and geometrical identifiers

Logic completed for implementation in the **official CMS Software** CMSSW_14_0_0_pre2

Geometry mapping to be updated again at a later stage as it is still being updated

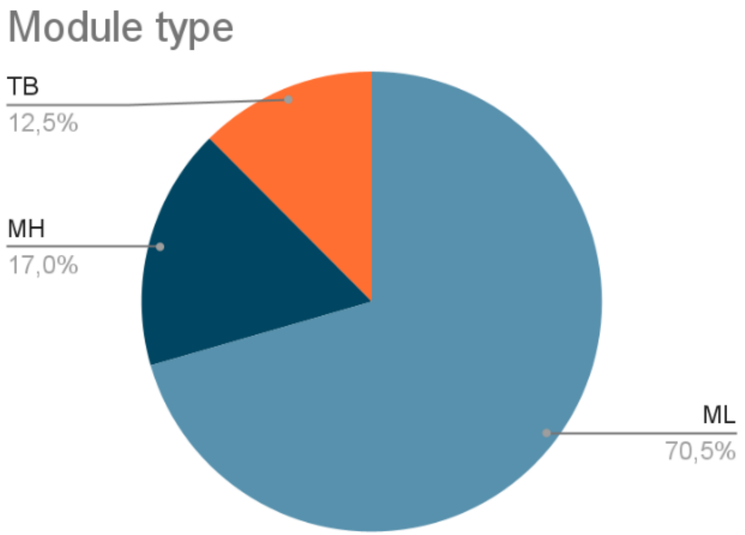
Simulation of SiPM-on-tile stack in DESY testbeam:

Simulation work just started

Backup Slides

Raw Data Sizes

The size of the packets by each module is most probably corresponding to the ML type with 6 eRx but can vary widely



Typecode		Counts / 120 deg	#eRx	Max #words	EDMS
MH-F	HD 0	727	12	468	2809974
MH-T	HD 1	14	4	156	n/a
MH-B	HD 2	52	8	312	2810066
MH-L	HD 3	26	4	156	2889486
MH-R	HD 4	26	4	156	n/a
ML-F	LD 0	2934	6	234	2805119
ML-T	LD 1	136	3	117	2909078
ML-B	LD 2	130	3	117	2720157
ML-L	LD 3	46	3	117	2966387
ML-R	LD 4	44	3	117	2962095
ML-5	LD 5	208	5	195	2906983

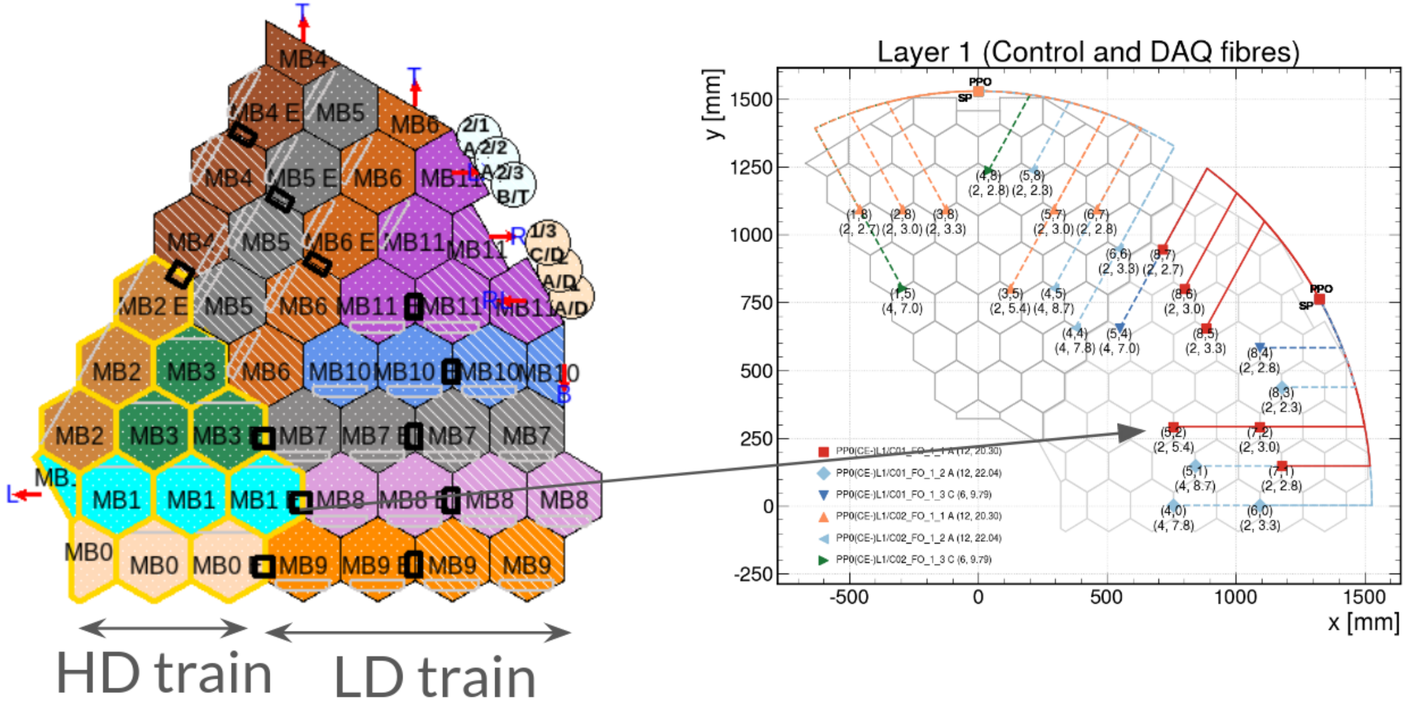
The unpacker will recieve a sequence of complicated structure and packets of widely varying size and has to order them by module type in the SoA

Module Type Sequence

The backend groups data in 120 degree sectors and sends out sequencial module data interleaved with some "fine structure" headers

The sequence of the module types is “arbitrary” because:

fiber groups from each cassette contain data from different modules (PP0 connectors)groups of PP0 connectors are further mixed between layers to balance throughput (PP1/PP2)



Mapping file

SiPM module types

The newest version of the SiPM module layouts within each layer

Layer Overview: No. Channels and ROCs, Dimensions.

This is for "second optimization". The outer rings in FH are not included in ASCII table on tab "Layer_Data" (BV currents!). Some inner rings deleted.

CE-H: layers former FH 9-12

r [mm], inner	ring	34	35	36	37
					L/R: 2x6tiles
2179.20	h24				
2148.16	h23				
2117.15	h22			L/R: 2x5tiles	
2086.13	h21		L/R: 2x5tiles	120chns	144chns
2056.44	h20				
2026.75	h19		96chns	2 HGCROCs	2 HGCROCs
1997.06	h18	L/R: 2x5tiles	2HGCROCs	302x372mm²	349x380mm²
1968.64	h17		227x364mm²		
1940.22	h16	60chns			
1911.79	h15	**1 HGCROC**			
1884.59	h14	139x348mm²			
1857.38	h13	**K5**	**K8**	**K10**	**K12**
1830.17	h12				
1804.12	h11				
1778.07	h10				
1752.03	h9				
1727.09	h8				
1702.16	h7				
1677.22	h6	144chns	144chns	144chns	144chns
1653.35	h5	2 HGCROCs	2 HGCROCs	2 HGCROCs	2 HGCROCs
1629.48	h4	293x319mm²	293x319mm²	293x319mm²	293x319mm²
1605.61	h3				
1582.76	h2	**J12**	**J12**	**J12**	**J12**
1559.91	h1				
1537.05	h0				
		J12: 8mm	J12: 8mm	J12: 8mm	J12: 8mm

A6 - Board Type

10 degree-Tileboard, 0.834° tiles

Tileboard recess at Si-Interf.

cassette infrastructure not assembled

Connector/HGCROC Pos.

4mm² SiPM, cast tiles

4mm² SiPM, molded tiles

9mm² SiPM, cast tiles

CE-H: layers former BH 13-22

r [mm], inner	ring	38	39	40	41	42-43	44-45	46-47
2594.79	42				L/R: 1x2 tiles	L/R: 1x2 tiles	L/R: 1x2 tiles	
2539.39	41			L/R: 1x3 tiles				
2483.99	40							G5:
2430.96	39		L/R: 1x3 tiles	56chns	64chns	64chns	64chns	no L/R types
2377.93	38		40chns	1HGCROC	1 HGCROC	1 HGCROC	1 HGCROC	40chns
2327.16	37	L/R: 1x3 tiles	1HGCROC	360x443mm²	416x452mm²	416x452mm²	416x452mm²	1HGCROC
2276.40	36	24chns	251x424mm²					251x424mm²
2227.80	35	147x406mm²	**G5**	**G7**	**G8**	**G8**	**G8**	**G5**
2179.20	34	**G3**						
2132.67	33							
2086.15	32	64chns	64chns	64chns	64chns	64chns	64chns	64chns
2041.61	31	1 HGCROC	1 HGCROC	1 HGCROC	1 HGCROC	1 HGCROC	1 HGCROC	1 HGCROC
1997.08	30	349x380mm²	349x380mm²	349x380mm²	349x380mm²	349x380mm²	349x380mm²	349x380mm²
1954.44	29							
1911.80	28	**E8**	**E8**	**E8**	**E8**	**E8**	**E8**	**E8**
1870.99	27							
1830.17	26							
1791.10	25							
1752.03	24	64chns	64chns	64chns	64chns	64chns	64chns	64chns
1714.62	23	1 HGCROC	1 HGCROC	1 HGCROC	1 HGCROC	1 HGCROC	1 HGCROC	1 HGCROC
1677.22	22	293x319mm²	293x319mm²	293x319mm²	293x319mm²	293x319mm²	293x319mm²	293x319mm²
1641.41	21							
1605.60	20	**D8**	**D8**	**D8**	**D8**	**D8**	**D8**	**D8**
1571.33	19							
1537.05	18							
1504.23	17							
1471.42	16	40chns	40chns	96chns	96chns	96chns	96chns	96chns
1440.00	15	1HGCROC	1HGCROC	2 HGCROCs	2 HGCROCs	2 HGCROCs	2 HGCROCs	2 HGCROCs
1408.59	14	159x268mm²	159x268mm²	354x268mm²	354x268mm²	354x268mm²	354x268mm²	354x268mm²
1378.52	13	**C5**	**C5**					
1348.45	12	C5: 8mm	C5: 8mm					
1319.66	11							
1290.87	10							
1263.31	9			**B11 / B12**	**B11 / B12**	**B11 / B12**	**B12**	**B12**
1235.75	8							
1209.37	7							
1182.99	6							
1157.73	5			B11: 5mm	B12: 0mm	B11: 5mm		
1132.48	4						48chns	48chns
1108.30	3						1HGCROC	1HGCROC
1084.12	2						145x206mm²	145x206mm²
1060.98	1						**A5 / A6**	**A5 / A6**
1037.83	0						A5/A6: 0mm	A5/A6: 0mm

10 degree-Tileboard, 1.25° tiles