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Digital readout electronics for segmented detectors
A Si(Li) Compton Polarimeter Demonstrator

Joint activity of AP(GSI), EE(GSI), IPE(KIT)

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Motivation

We have: Segmented Semiconductor Detectors with VME / NIM readout electonics

- pro: modular, reliable
- con: loss of detector features, form factor, power, heat, costs per channel

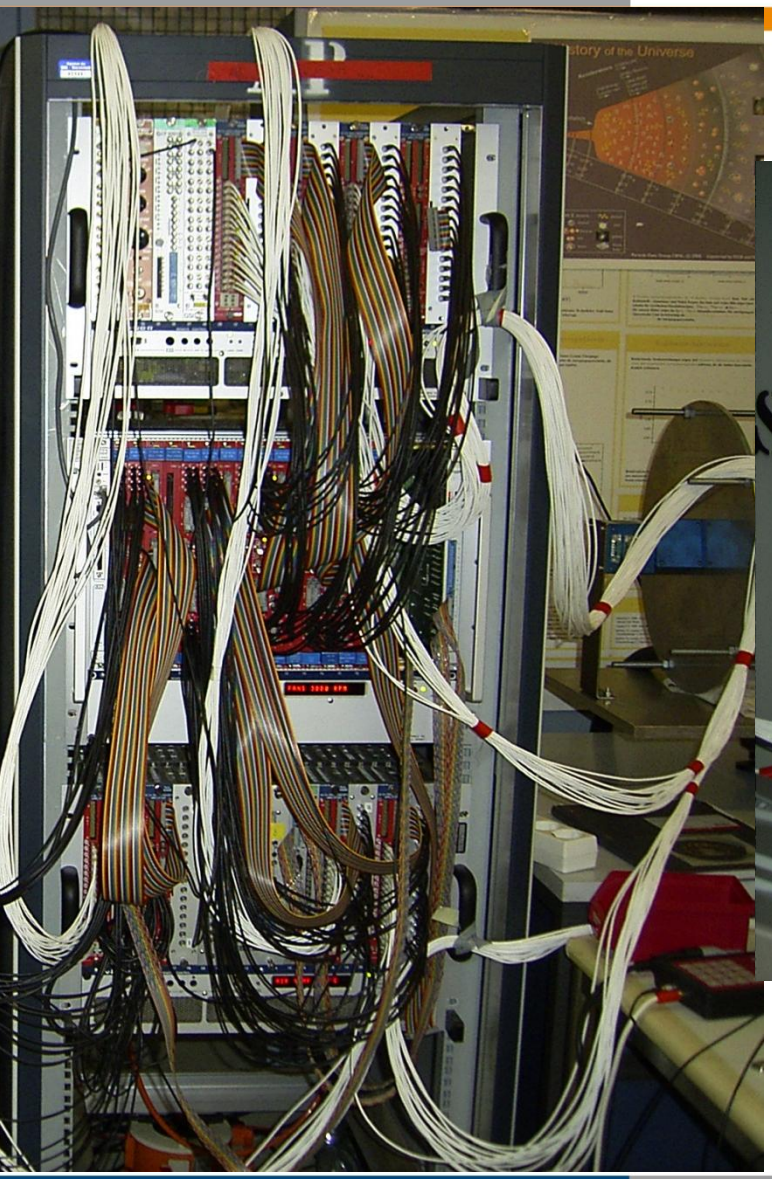
We want: a „blue print" for detector readout electronics for segmented detectors incl. DPP

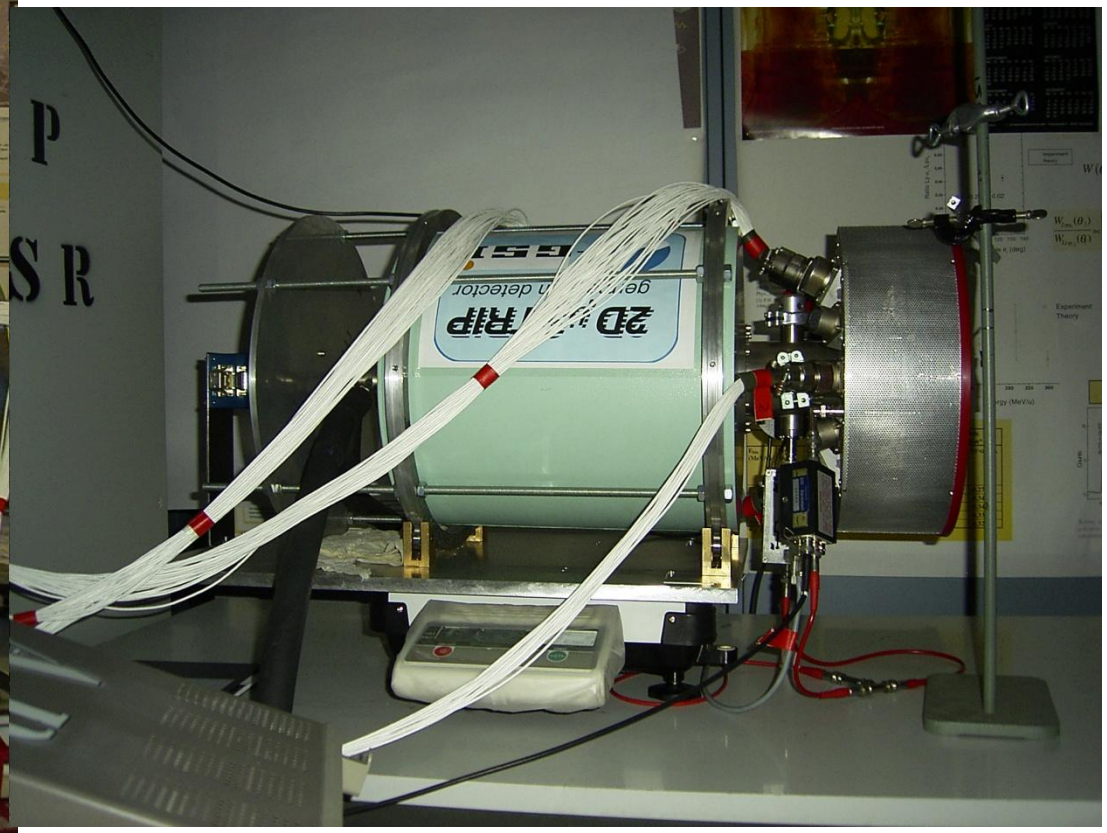
- access additional signal features (eg. sub strip resolution by image charge readout)
- higher rate acceptance
- double hit correction / pileup reduction
- scalable: (1 ch to 1000 ch)
- compact form factor, less power and heat
- reduced cost per channel

Strategy:

- build a first demonstator with existing hardware (if available)
  -> Si(Li) - DSSD (thick) + Digital Readout + DAQ enviromennt
- DPP (Digital Pulse Processing) of simple signals should be done on FPGA onboard directly
- DPP of complex signals/event histories on dedicated computing hardware (KIT)

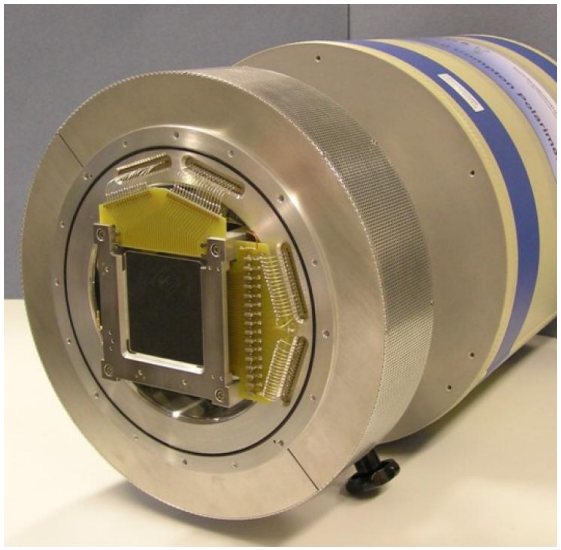
Typical setup with VME/NIM electronics





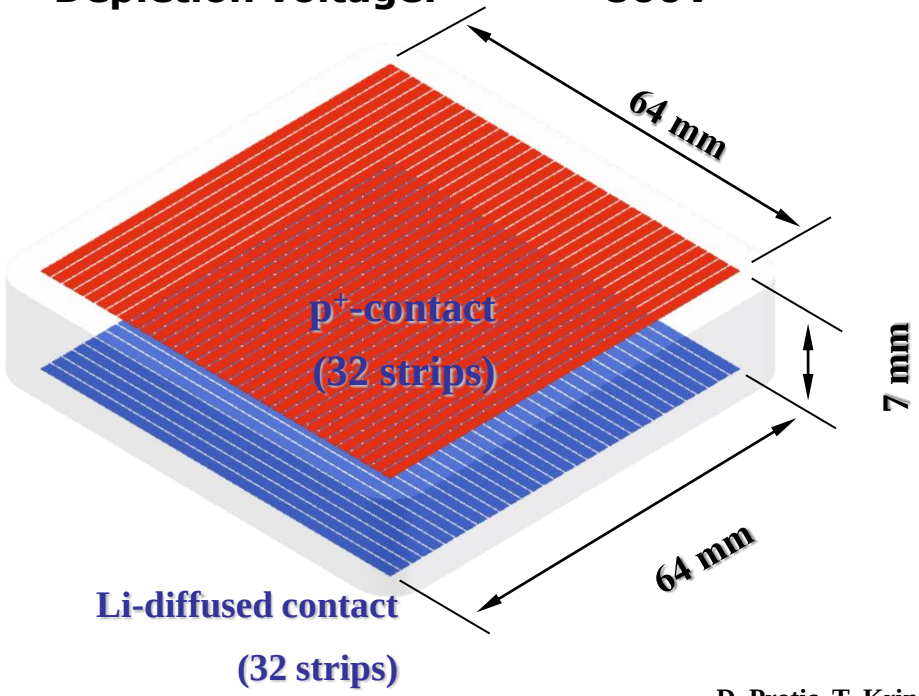
Planar structured semiconductor detectors

2D Si(Li)-strip-detector



Crystal: p-type silicon
Thickness: 7 mm
Size: 74 x 74 mm²

Depletion voltage: 800V

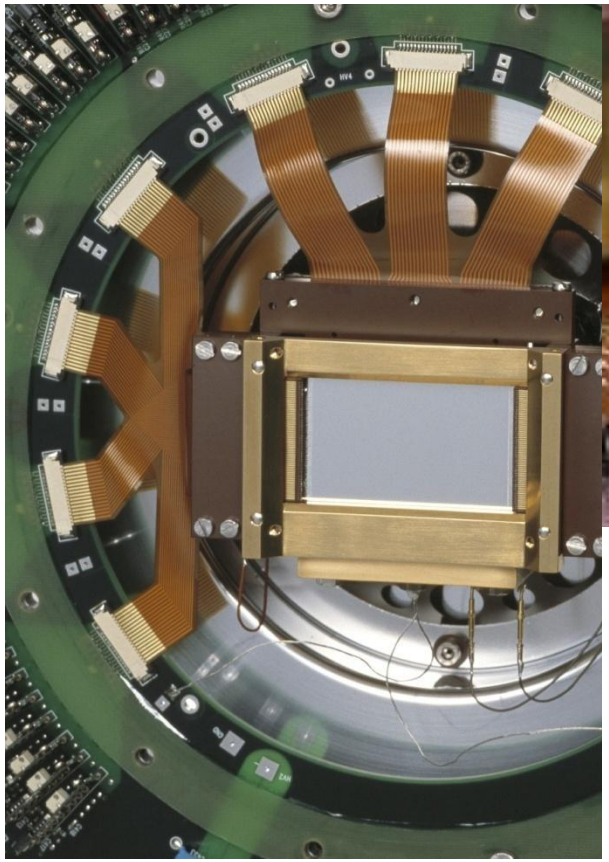


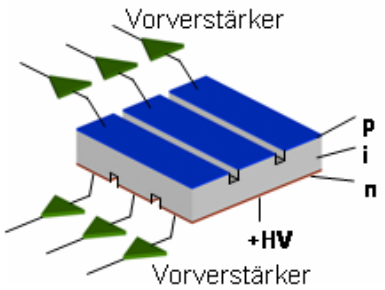
Position sensitive structure

Stripes per contact :	32
Strip length:	64 mm
Strip width:	2 mm
=> 1024 stripsel total	
Isolation gap:	~50 µm
Active area:	4100 mm²

D. Protic, T. Krings;
IKP, JZ-Jülich (now Semikon GmbH)

Planar structured semiconductor detectors
2D Ge(i)-µ-strip-detector





Crystal size (sensitive area)

height: 32 mm

width: 56 mm

thickness: 11 mm

absorption (photons): ~100% for 60 keV

~80% for 122 keV

front: 128 strips, 250µm pictch

back: 48 strips, 1167µm pictch

=> 6144 Pseudopixel

resolution: ~2.1 keV @ 60 keV

weight: ca 50 kg

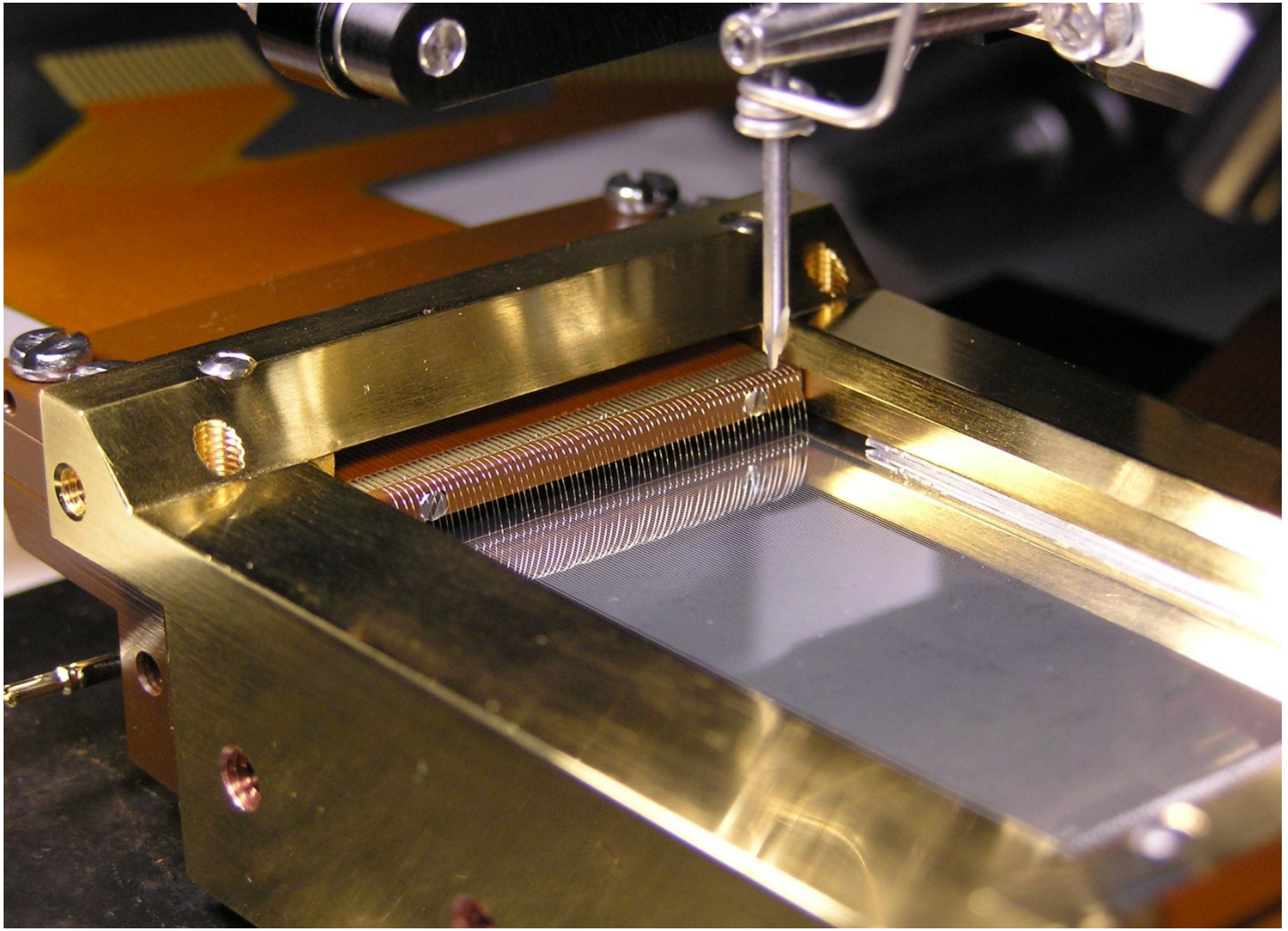
LN2 – consumption: 2 kg per day

crystal-temperature: -160 C

Energy, Timing, Position

D. Protic, T. Krings;
IKP, JZ-Jülich (now Semikon GmbH)

Detector during wire bonding



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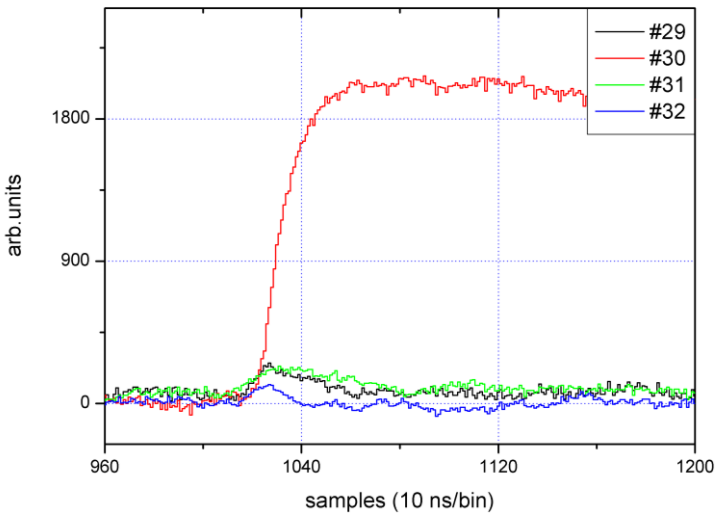
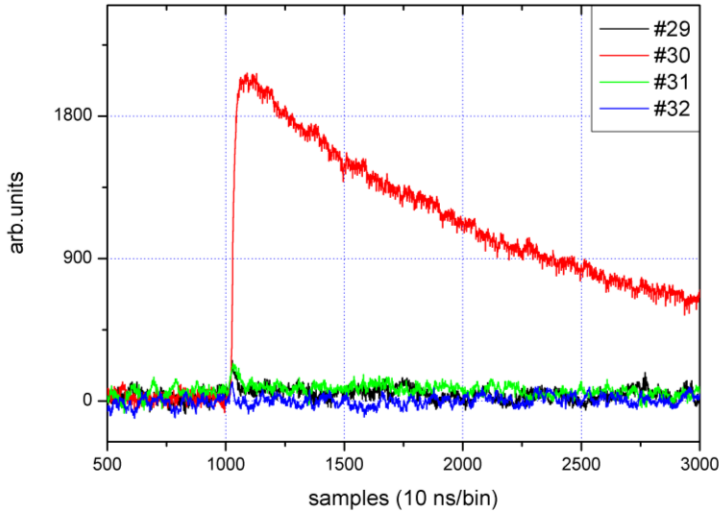
IKP, JZ-Jülich (now Semikon GmbH)

Detector signals (resistive feed back preamp)

Rise time (10/90): ~ 120 ns
Decay time (10/90): ~ 1000 µs
Gain (per MeV): 55 mV
⇒X-ray (E=100 keV): ~ 5-6 mV

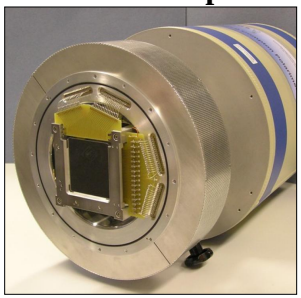




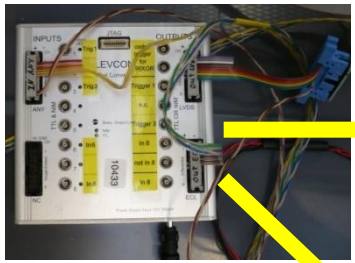
Dynamic range (0 keV - 300 keV)
for our applications: 0 mV to 15 mV

New readout chain

Si(Li)-Polarimeter with SiliVer-Amplifier

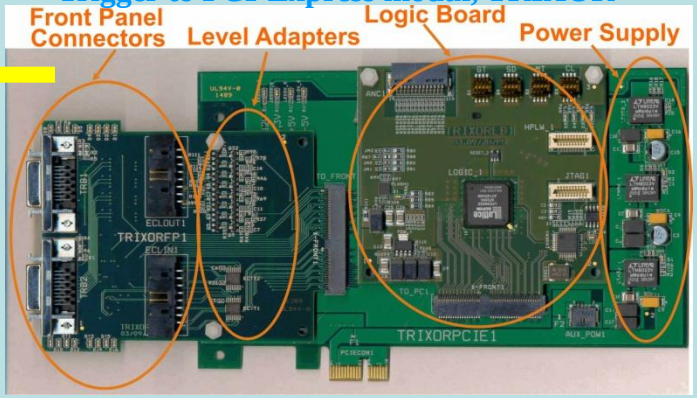


LEVCON

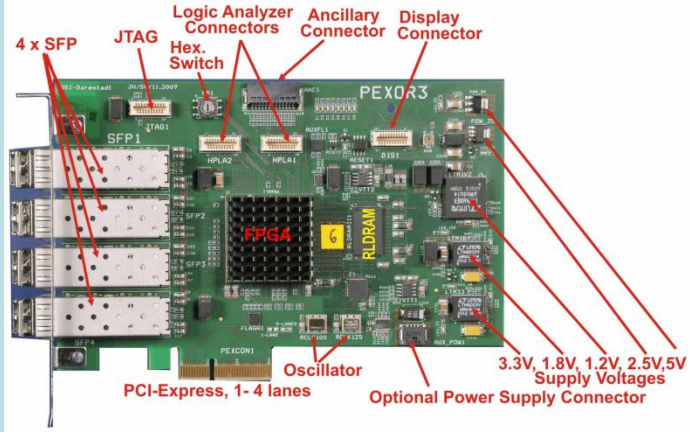


PC (PCIe, GBit-LAN, LYNX, MBS)

Trigger to PCI-Express modul, TRIXOR

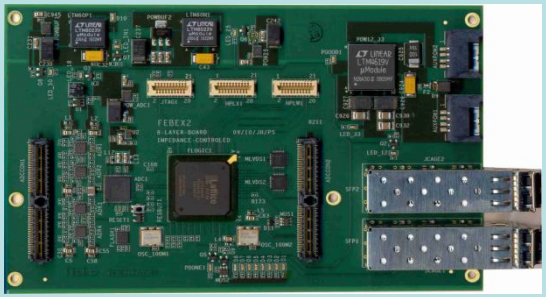


PCI-Express Optical Receiver, PEXOR3



Twisted pair cables

Febex2



Fiber 1.6Gbit

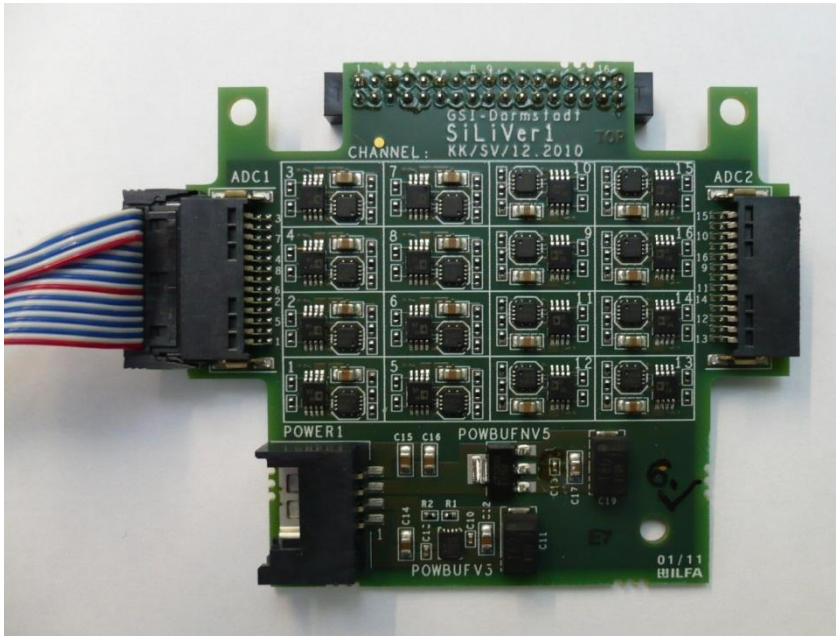
FEBEX2 - 8 channel pipeline ADC Front End Board with optical link Extension.

SiLiVer
A single-ended to differential fast linear amplifier

HELMHOLTZ ASSOCIATION

SiLiVer – Amplifier

2 stage fast linear amplifier (K. Koch, GSI-EE)
band width (-3dB,-6dB): 250 MHz, 500 MHz

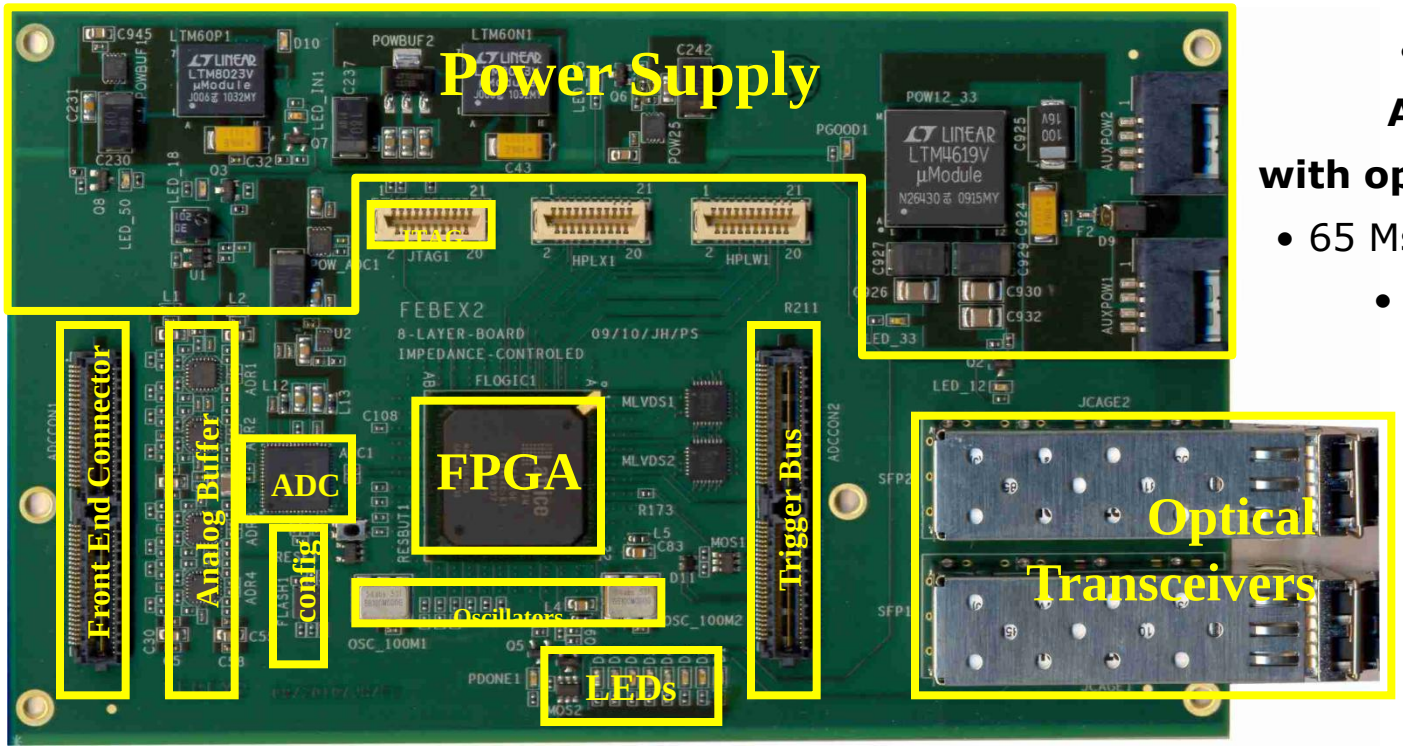


1. stage G=+20, 0.95nV/sqrt(Hz)
single-ended to single-ended

2. stage G=+2, 20nV/sqrt(Hz)
single-ended to differential

Requirement: compact form factor ->
will be/is mounted inside the preamp housing

Febex2 – Frontend ADC board



- **8 channel pipeline ADC Front End Board with optical link Extension.**
- 65 Ms/s at 12 bit resolution
- contains trigger logic, time stamp logic
- 8 differential analog inputs +/-1V
- 16 differential LVDS I/O
- 2 fiber optic data transceivers (2.5 Gb/s SFP)

Hardware design and coordination: **J. Hoffmann (GSI-EE)**
FPGA code development: **W. Ott (GSI-EE), S. Minami (GSI-EE)**
MBS-readout: **N. Kurz (GSI-EE)**

Trigger

Option 1: external trigger

external trigger -> LEVCON -> TRIXOR(PC) -> LEVCON -> FEBEX2

Option 2: Self triggering system

All channels are sampled continuously.

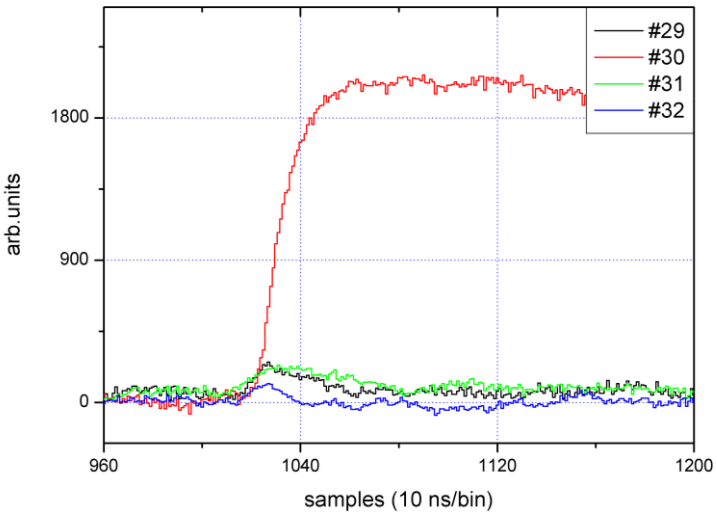
An intelligent trigger algorithm in the FPGA of the FEBEX2 detects true events and sends a trigger signal to LEVCON.

FEBEX2 -> LEVCON -> TRIXOR(PC) -> LEVCON -> FEBEX2

Count rate capability – raw data

512 sample points/(strip * event): (512 * 2 byte -> 1 kByte/(event*strip)
512 samples / 65 MS/s = **7-8 µs window**

on average 4 strips for each event: **4 kByte/event** or 32 kBit/event



Principle data transfer **limit** 1.6 GBit (200 MByte/s)
corresponds to **50 kEvents/s** for raw data

Data reduction for online removal of data belonging to channels that detected only noise is implemented.

Current Status

- all individual parts are produced
- DAQ: FEBEX2, LEVCON, TRIXOR, PLEXOR are tested and ready
- DAQ and SiLiVer show expected behaviour with puls generator
- started to integrate SiLiVer boards into Si(Li)-Polarimeter housing (last week)

Next Steps

Next Steps:

- reduce noise pickup
- take raw data for detailed offline analysis of DPP algorithms
- implementation of a simple but reliable online analysis into FPGA for (E,t,x)
- FIRST EXPERIMENTS

Near Future:

- KIT: select/develope dedicated hardware and complex algorithms to extract additional features from the detector signals (eg. image charge signals)
- move from discrete preamps to mixed ASICs: better resolution without huge numbers of cooled FETs (maintenance issue)
- low energy spectroscopic x-ray µ-strip detectors (2 keV – 20 keV)