

MPSoC- und RFSoC-basierte FPGA Entwicklungen bei DESY

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Agenda

1. Einführung
2. Unsere aktuellen Entwicklungen
3. Werkzeugkasten

Einführung

Portfolio und Gemeinsamkeiten

Lizensierungsstrategie

- Wir fördern ein Ökosystem
- **DESY hat nahezu alle Entwicklungen lizenziert: Für uns und für Dritte (Motivation für Vortrag)**
- Strategie: Konzentration auf die Applikation; Einkauf von „nicht spannender Infrastruktur“

AMC

DAMC-FMC2ZUP

Zynq Ultrascale+ MPSoC based Dual FMC/FMC+ Carrier Board with D1.1 RTM support



DAMC-FMC1Z7I0

Cost-Optimized IO Controller Board with one FMC socket



DAMC-TCK7

AMC Data Processing and Telecommunication Module



DAMC-UNIZUP



ADVANCED MEZZANINE CARDS

AMC boards (Advanced Mezzanine Card) are the key components of a MicroTCA system. Within the MicroTCA 4 crate, AMCs are placed in the front of the crate. They are connected by a high-speed backplane that carries serial links, power and management data. Every AMC card is monitored and managed. This allows hot-plug, hot-swap, health monitoring and thermal management of the modules.

There are six standard sizes of AMCs: single and double width as well as compact, mid-size and full-size height. Every combination of width and height is valid. The power consumption of an AMC is divided into 3.3V management power plus 12V payload power. AMC boards are used for digital processing. On every AMC board there is a controlling unit called MMC (Module Management Controller). Plugging in the AMC board to the MTCA crate connects the board to the backplane of the crate. The backplane ensures the connection of the AMC boards with every other AMC board in the crate. Plus, every AMC board is connected to the MCH (MicroTCA Carrier Hub), which is the overall management card of the MTCA system. The MCH gives management power to the AMCs first. This power is used to check if everything is ok with the AMC. If the MMC, the managing unit on the AMC detects no problems on the board, the MCH gives payload power to the AMC.

Clustering of AMCs in the system is possible.

DAMC-FMC25

AMC Dual HPC-FMC Carrier



DAMC-FMC20

AMC Dual FMC Carrier Board



X2TIMER

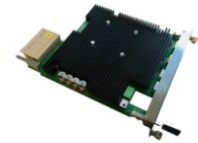
AMC Fast Timing System



RTM

DRTM-MXC

Mobile GPU Carrier



DRTM-AD84

RTM 8Ch ADC, 4Ch DAC



DRTM-PZT4

RTM 4 Channel Piezo Driver



REAR-TRANSITION-MODULES

RTMs, the rear-transition-modules, are extension boards that are placed in the back of the MicroTCA 4 crate. They directly connect to the front AMCs via the Zone 3 connector. The possibility to separate analogue and digital functions by moving sensitive analogue electronics to the RTM is one of the key strengths of MicroTCA 4.

DRTM-DWC8VM1

RTM 8 Channel Down-Converter 1 Channel Up-Converter



DRTM-LOG1300

eRTM Local Oscillator Generation



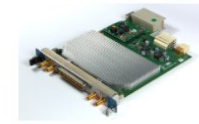
DRTM-VM2LF

RTM 2 Channel Vector Modulator Low Frequency



DRTM-DWC10

RTM 10 Channel Down-Converter



DRTM-DS8VM1

RTM 8-Channel Direct Sampling 1-Channel Vector Modulator



DRTM-VM2HF

RTM 2 Channel Vector Modulator High Frequency



DESY MMC Stamp

FMC

DFMC-DS800

FMC Direct-Sampling A-D Converter



DFMC-AD16

FMC 16-channel A-D Converter



DFMC-TESTADP

FMC Loopback Adapter



FPGA MEZZANINE CARDS

FPGA Mezzanine Card (FMC) is a standard defining I/O mezzanine cards and corresponding carrier boards. Huge ecosystem of carrier boards, both in MicroTCA format and standalone boards, provides a good prototyping platform, suitable for experimental physics and industrial applications. The FMC mezzanine format provides additional degree of modularity for a lot of I/O applications, such as ADC and DAC boards, or communications boards.

DFMC-MD22

FMC 2 channel stepper motor driver



DFMC-UNI-I/O

FMC Multi-Purpose I/O Board



DFMC-SFP4

FMC 4-Channel SFP+ Adapter

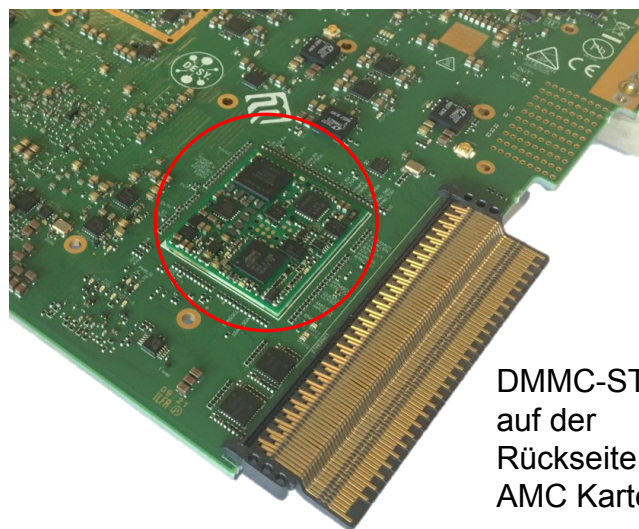
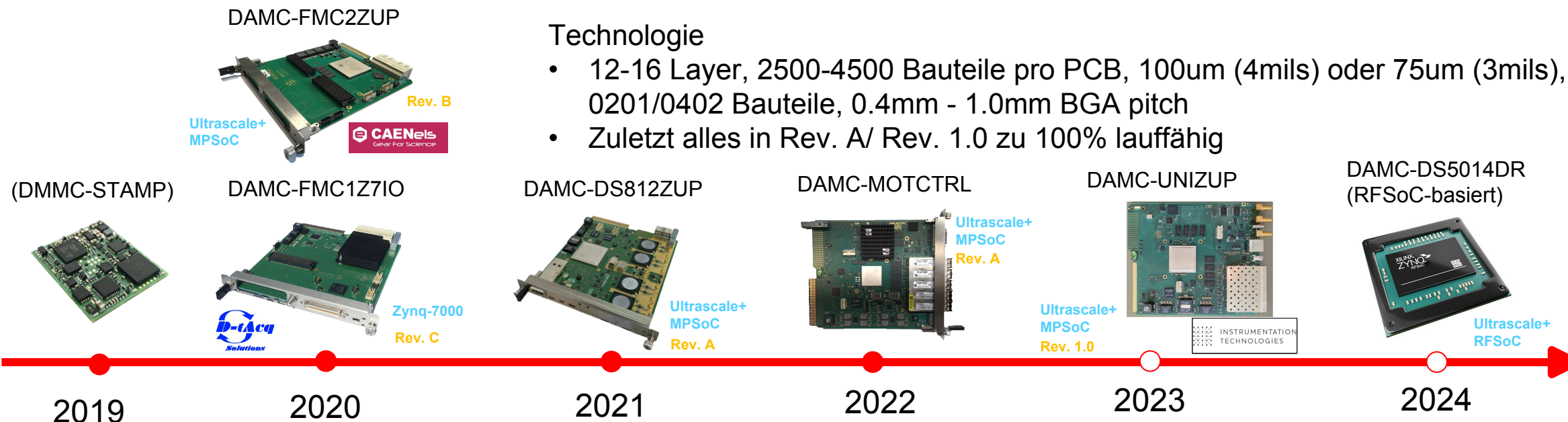


Alle SoC-Entwicklungen der letzten Jahre

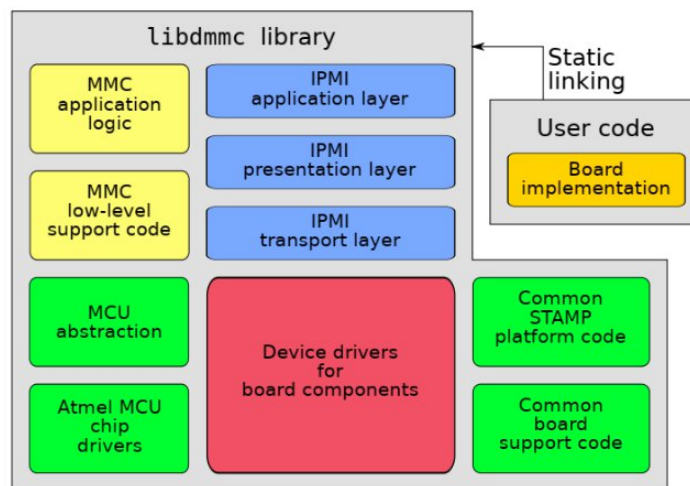
Gemeinsamkeit 1: Boards basieren alle auf DMMC-STAMP

Technologie

- 12-16 Layer, 2500-4500 Bauteile pro PCB, 100um (4mils) oder 75um (3mils), 0201/0402 Bauteile, 0.4mm - 1.0mm BGA pitch
- Zuletzt alles in Rev. A/ Rev. 1.0 zu 100% lauffähig



DMMC-STAMP
auf der
Rückseite der
AMC Karte



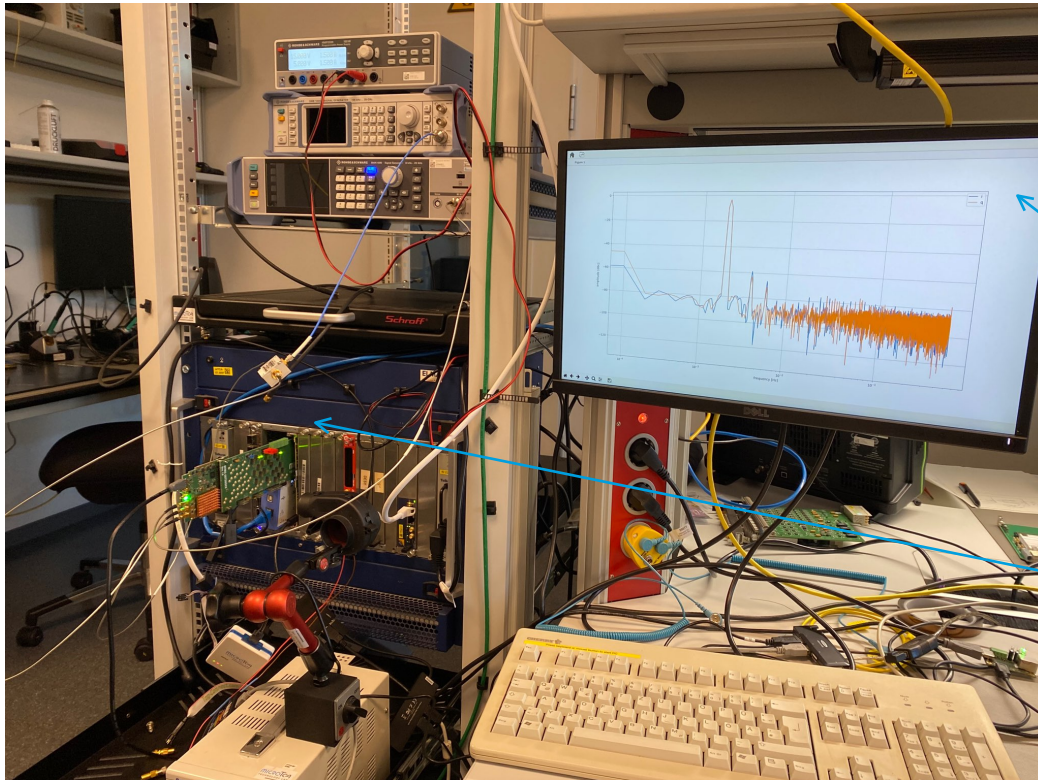
- Komplettes Software-Framework
- 95% Wiederverwendung
- Kompatibilität mit allen uns bekannten MCHs
- In-System-Update (von MMC und FPGA)
- Serial-over-IPMI (remote Zugriff auf die FPGA und MMC UART)
- Über 1000 Stück produziert
- vom 30 Partnern verwendet
- 100% Test im Nadel-Test-Adapter



MPSoC?

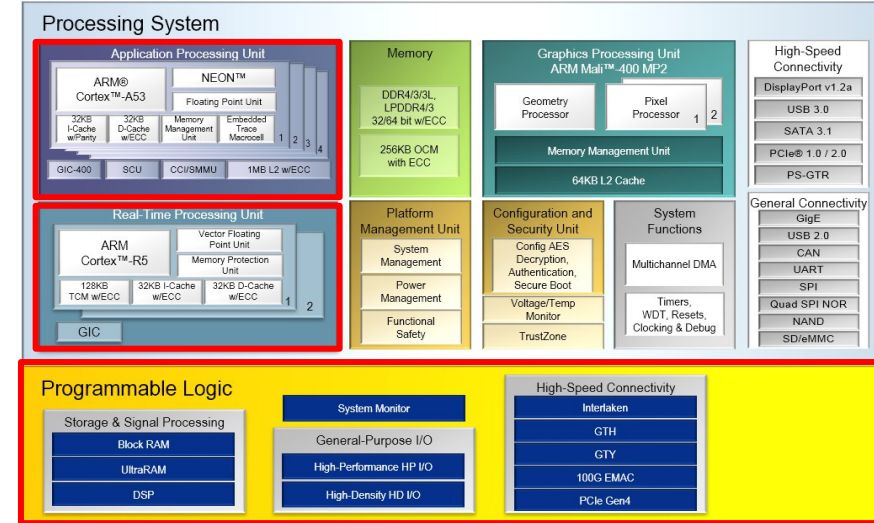
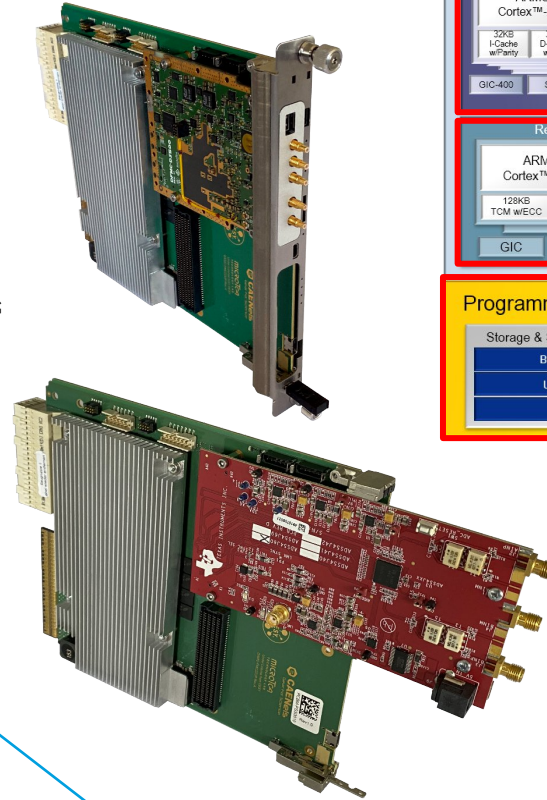
Gemeinsamkeit 2: Prozessor im FPGA

- Alles ist SoC-basiert
- Prozessorzentrischer Ansatz (“Raspberry Pi im FPGA”)
- Veränderte Methode: “on-the-fly”, “Wiederverwendung” und “Baukasten”, „low-code“
- Stichworte: IP-Module, Linux, Python



Courtesy of J. Marjanovic and S. Farina

DESY DAMC-FMC2ZUP Board



- DAMC-FMC2ZUP Board führt grafischen **Linux Desktop** aus (Displayport)
- Zusätzlich: Web-Server mit Jupyter
- DAMC-FMC2ZUP sammelt Daten von FMC-DS500; Ausgabe mit. **Python Matplotlib**



Embedded Computing



In Zukunft keine FPGAs mehr ohne Prozessor

- Magie ist auf den ersten Blick unscheinbar
- Von außen: Micro-SD Slot, USB-C Anschluß

Von innen:

- “großer” ARM Cortex-A53 Processor
- Dual- oder Quad-Core bis 1.5GHz per Core
- Boards führen Yocto Linux aus
- USB-C Anschluß ermöglicht komplette PC Funktionalität
 - HDMI
 - USB für Keyboard, Maus und USB-Sticks
 - Ethernet-Anbindung
- PCIe Root Complex: Board kann komplettes CPU Modul ersetzen (Anhängig von Rechenleistungsbedarf)



<https://www.delock.de/produkt/87297/merkmale.html?g=1107>

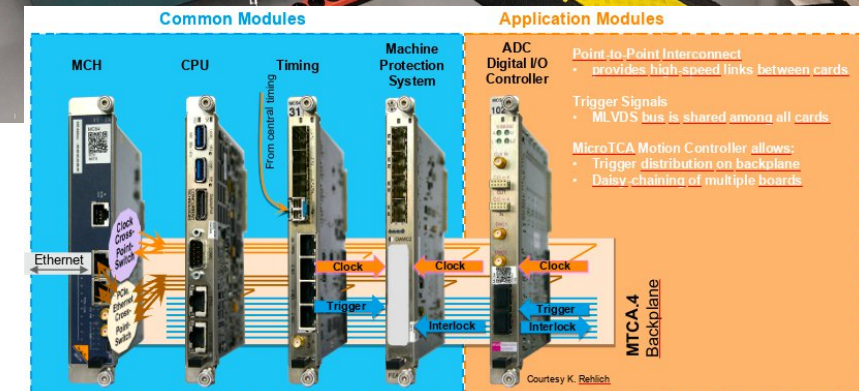
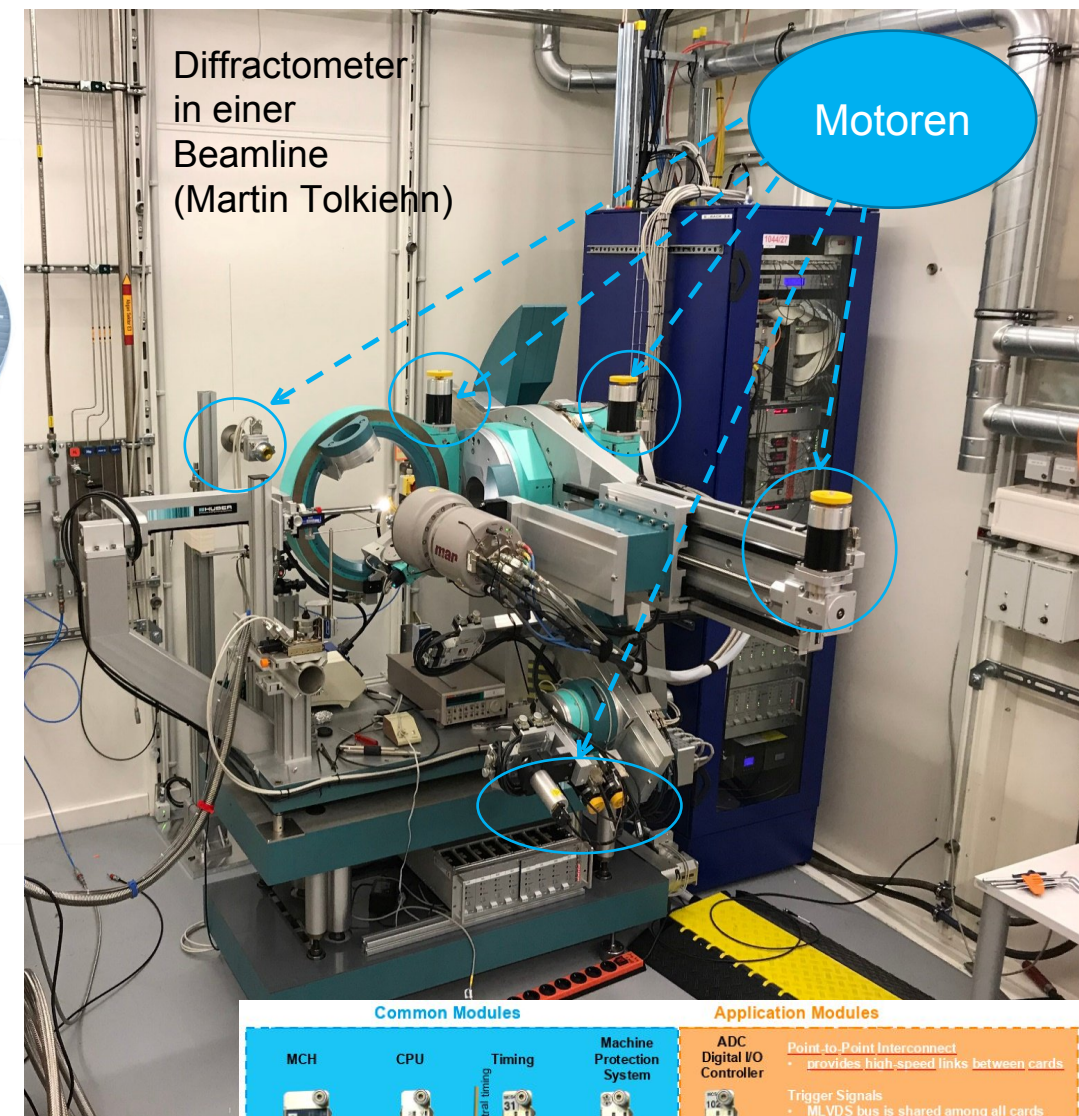
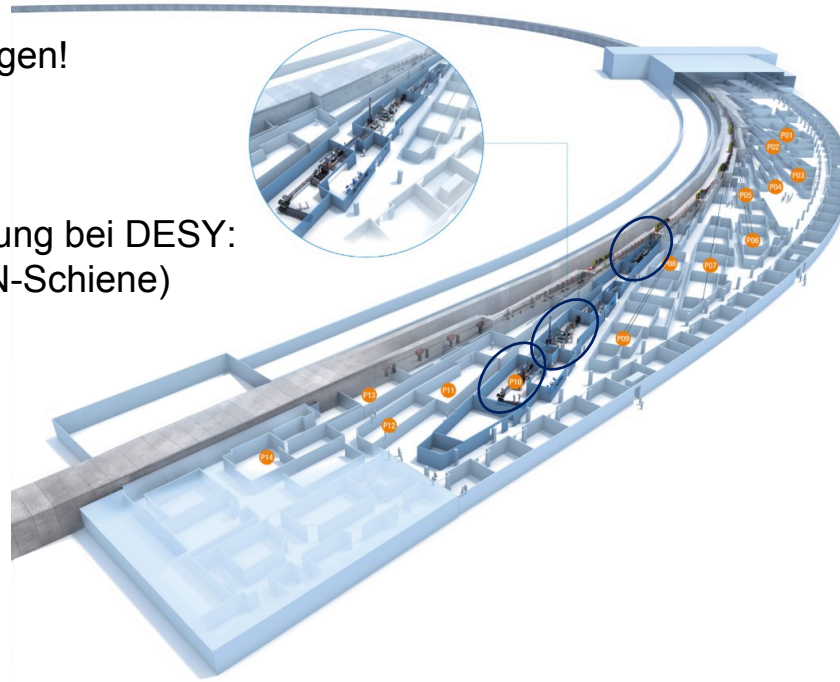


Unsere aktuellen Entwicklungen

MicroTCA Motion Controller

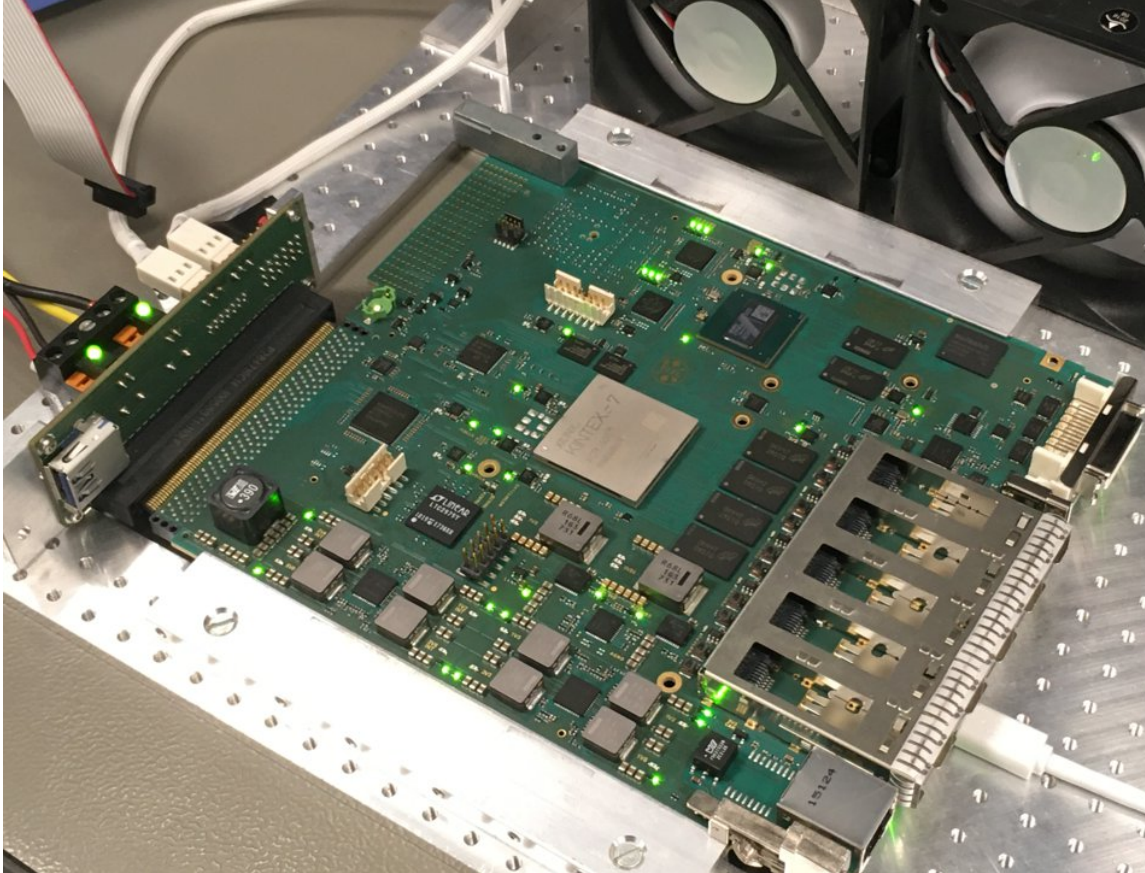
MicroTCA Motion Controller

- DESY muss Motoren bewegen!
- Beliebte Bewegungssteuerung bei DESY:
 - Beckhoff EtherCAT (DIN-Schiene)
 - OMS MAXv (VME)
- Die MicroTCA-Infrastruktur ist für Petra IV geplant
 - Ein **Ersatz für VME-Systeme** ist erforderlich
 - Nicht Verfügbar: DESY Eigenentwicklung
- DAMC-MOTCTRL: Ersetzt 6 VME Karten
- Steuert (min.) **48 Motoren/Achse pro Karte** (FW-abhängig)
- **Skalierbare Verbindung mehrerer Karten im Crate und campusweit**
- **Positionsgetriggerte Datenerfassung** im Zusammenspiel mit anderen MicroTCA-Karten
- Fokus auf Kosten (Lizenzierung geplant)



MicroTCA Motion Controller Hardware

„Die Hardware ist da“



- Board in Rev. A voll funktionsfähig
- Kein einziger Patch-Draht

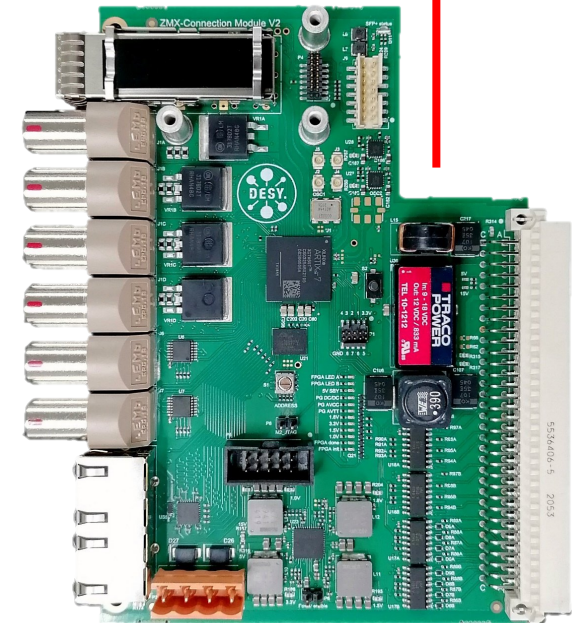
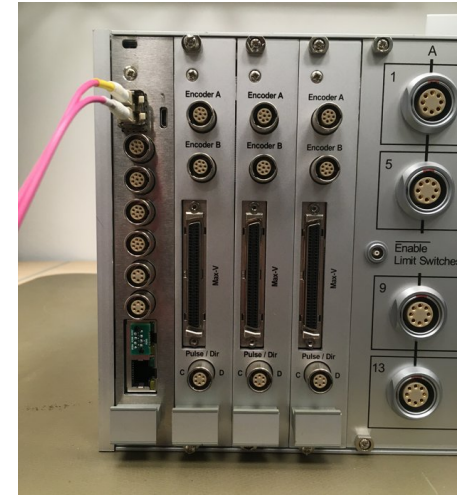
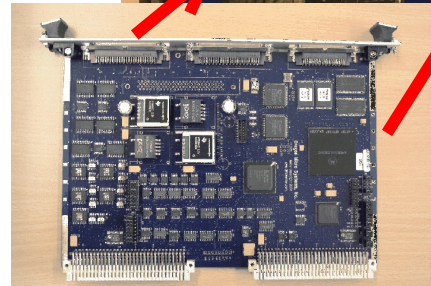
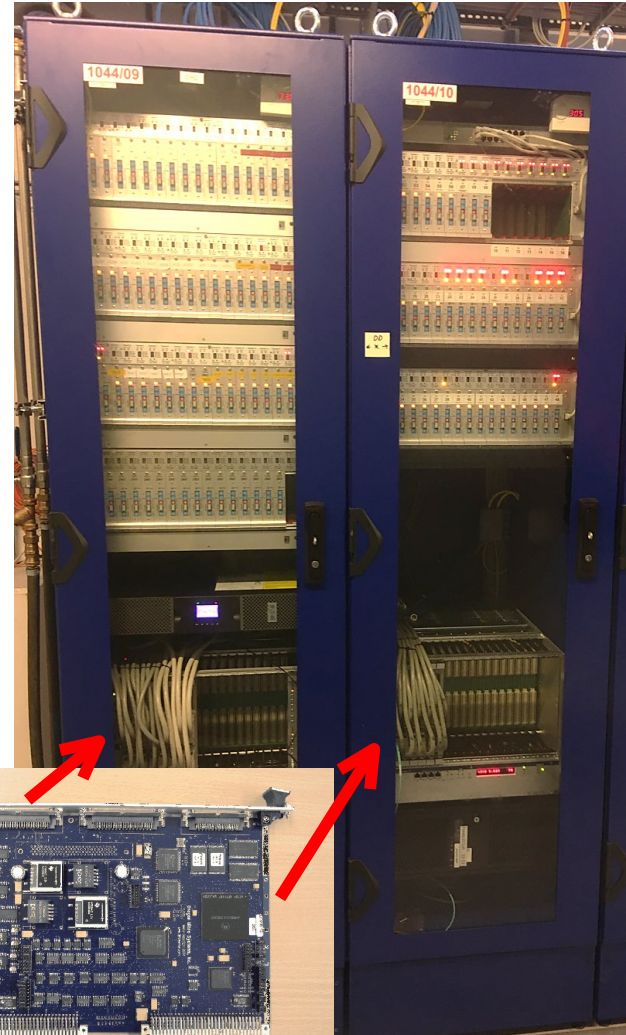


Heterogener Ansatz

- MPSoC (2 GB DDR4) und FPGA (4 GB DDR3)
- **MPSoC:**
 - „Raspberry Pi“ im FPGA (Yocto Linux)
 - Nicht-Echtzeitaufgaben
 - Kommunikation mit anderen Karten
- **Kintex-7:** Echtzeitsteuerung
 - 5 SFP+-Ports (1 Gbit/s bis 10 Gbit/s)
 - 3x Motorschnittstellen, 2x Ringtopologie
 - HW-Unterstützung: CAN EtherCAT, SERCOS

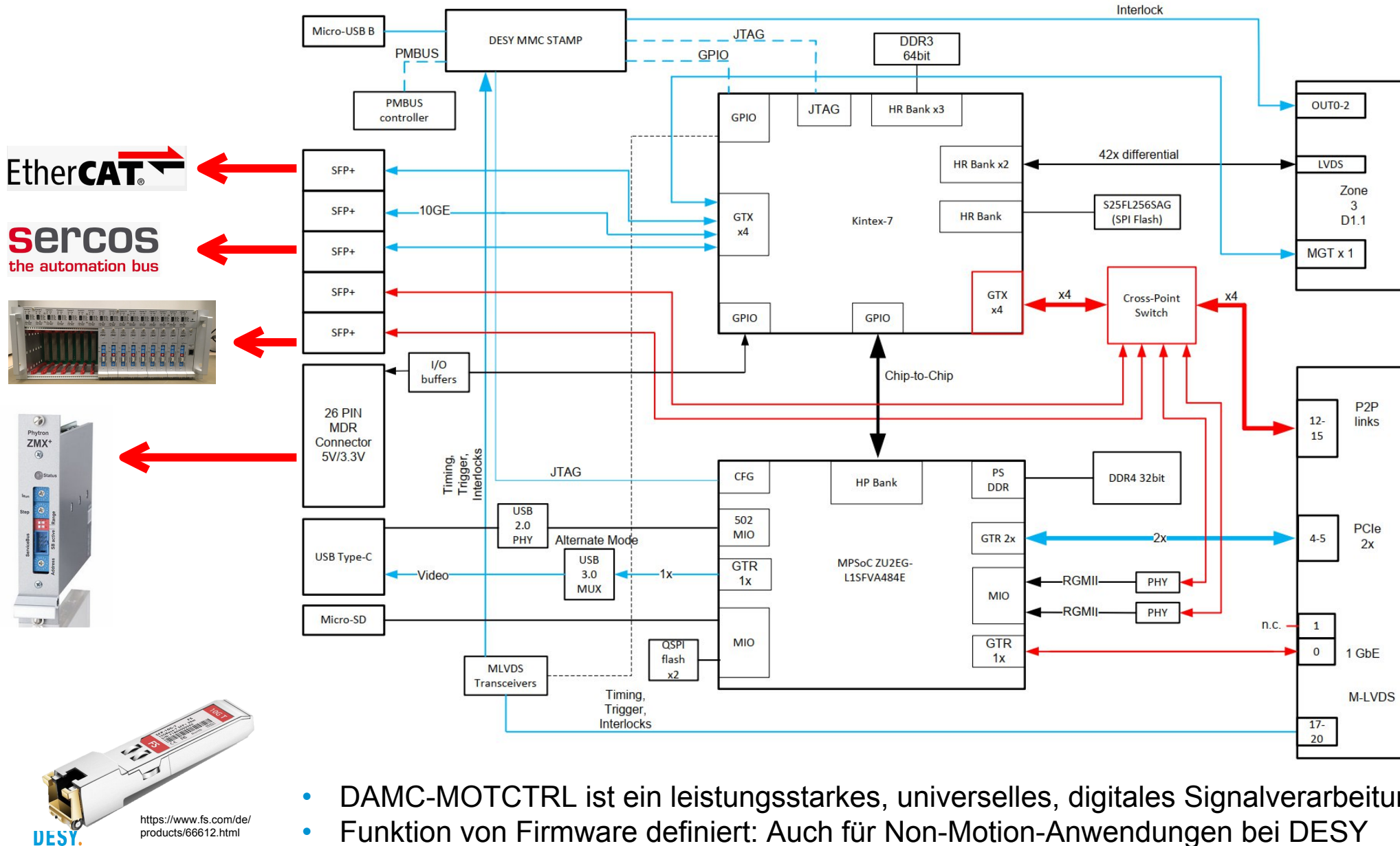
Wiederverwendung bestehender Hardware

- Beamlines verfügen über hunderte von vorhandenen Motortreibern



- Rückwärtskompatibilität
 - „Retrofit“-Lösung entwickelt
 - Entwicklung einer Artix-7 basierten FPGA Karte für bestehenden Überrahmen
 - Ausschließlich optische Anbindung der Motor-Treiber-Überrahmen
 - Weiterverwendung der teuren Infrastruktur

MicroTCA Motion Controller: Blockdiagramm

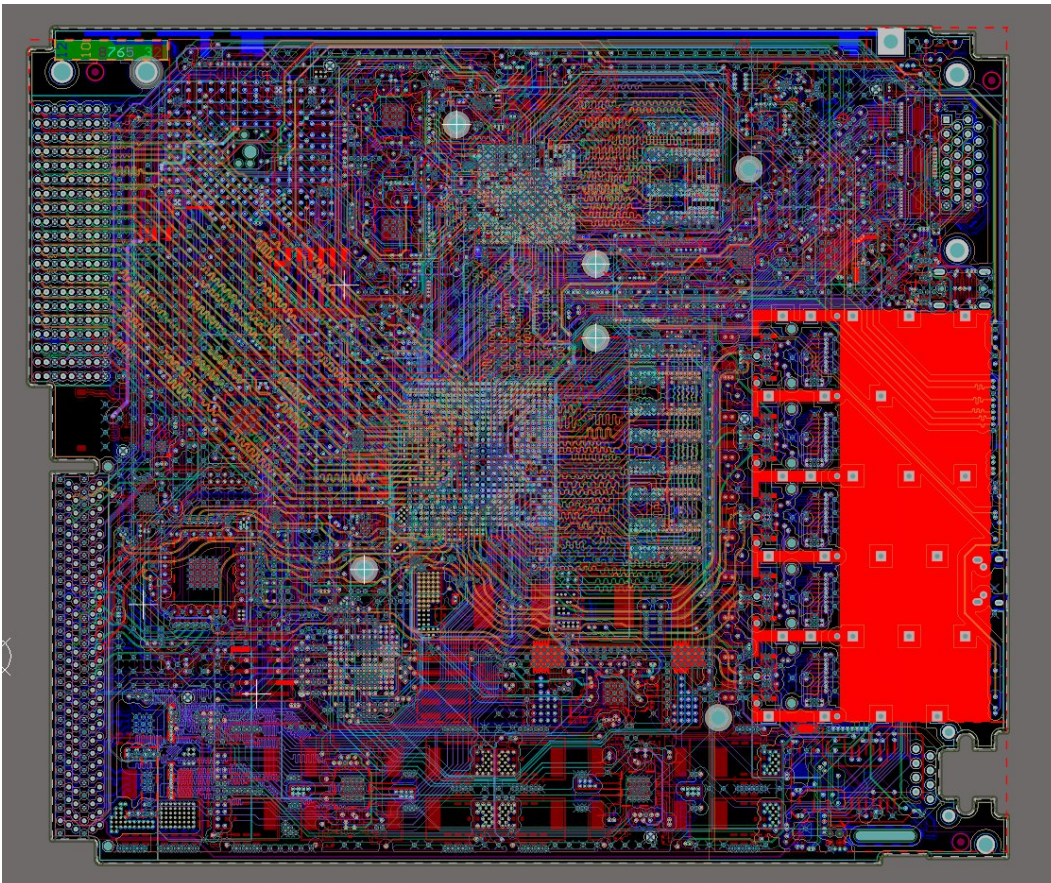


- DAMC-MOTCTRL ist ein leistungsstarkes, universelles, digitales Signalverarbeitungsboard.
- Funktion von Firmware definiert: Auch für Non-Motion-Anwendungen bei DESY

MicroTCA Motion Controller

Hardware Details

- Kostenoptimiert: 12 Lagen: Megtron-6, 100um Technologie
- 0402 Bauteile (unsere „größte“ Technologie)
- Diskretere DC/DC Converter (z.B. 1.0V, 40A)
- „Runde“ Leiterbahnen (> 10 Gbit/s)
- Präzise Längen Anpassung: besser 1ps / ~0,15mm
- PCB Herstellung in China (NCAB/Sengyi)



Coating
25 Galvanic Cu
17 Copper
56 FR408HR
52 FR408HR
17 Copper

150 FR408HR

17 Copper
68 FR408HR

75 FR408HR
17 Copper

150 FR408HR

17 Copper
68 FR408HR

75 FR408HR
17 Copper

50 FR408HR
17 Copper

75 FR408HR
68 FR408HR

17 Copper
150 FR408HR

17 Copper
75 FR408HR

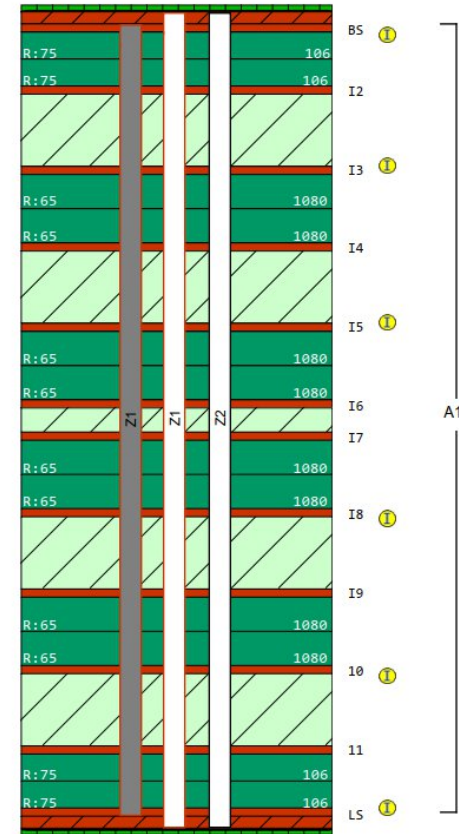
68 FR408HR
17 Copper

150 FR408HR

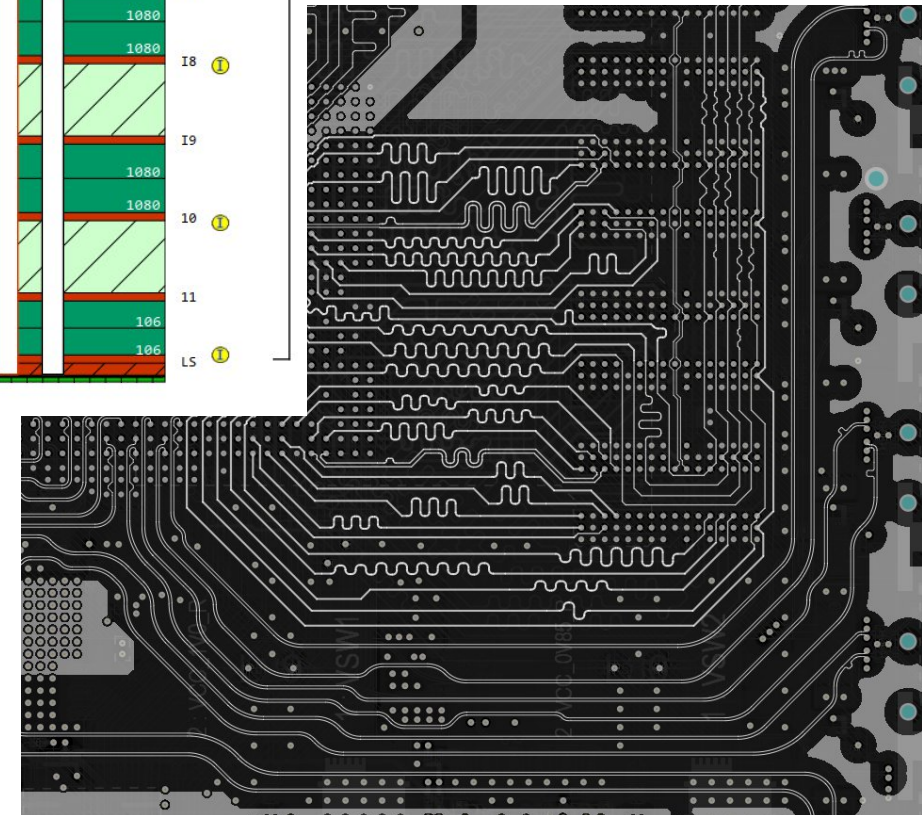
17 Copper
52 FR408HR

56 FR408HR
17 Copper

25 Galvanic Cu
Coating

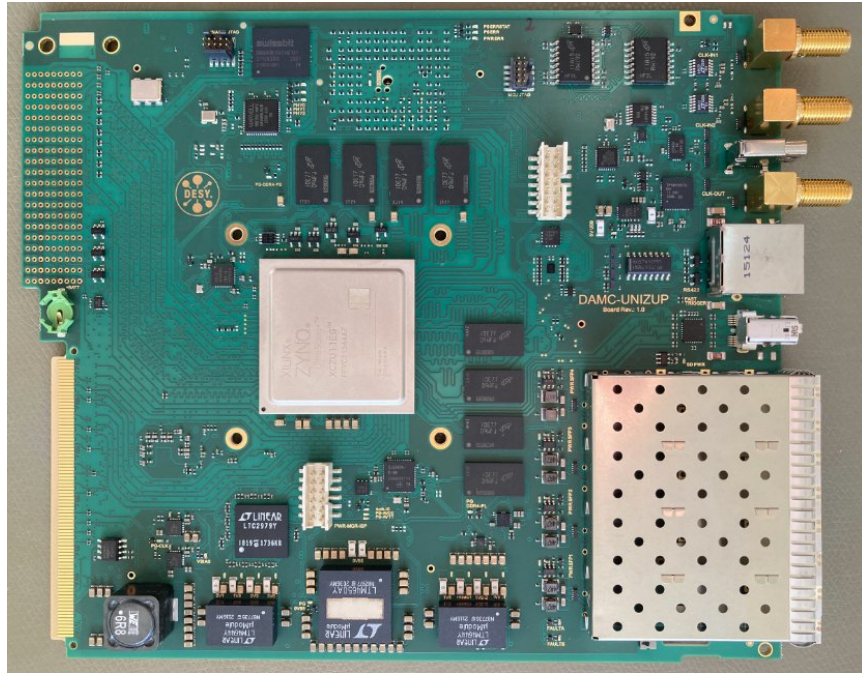


SYE Europe
<https://sy-europe.com>
SYE Europe



DAMC-UNIZUP

DAMC-UNIZUP: Universelles, kostenoptimiertes MPSoC Board



“Kleine Schwester” vom DAMC-FMC2ZUP

- “Low-Cost” Karte mit kleinerem FPGA: hunderte Einheiten bei Petra IV geplant.
 - 14 statt 16 Lagen, 0402 Bauteile, jedoch 0201 Kondensatoren
- Für ein I-TECH BPM Lösung (“Libera Brilliance+ Nachfolger”) als RTM konzipiert

Merkmale:

- Board erbt die Technologie vom DAMC-FMC2ZUP
- Universelles MPSoC Board mit leistungsfähiger **RTM Anbindung**
- High-Performance FPGA: Zynq UltraScale+ **ZU7CG...ZU11EG**

Neuheiten

- **2 x 64bit breite** DDR4 interfaces (insges. 8GB RAM)
- **4 Integrierte SFP+** Steckplätze mit 16.375 Gbps (nicht 28 Gbps GTY)
- Anschlüsse für “**Slow trigger**” und “**Fast trigger**” am Front Panel
- 2 Front Panel Clock Eingänge via SMA, 1 Ausgang



INSTRUMENTATION
TECHNOLOGIES

Inherited features:

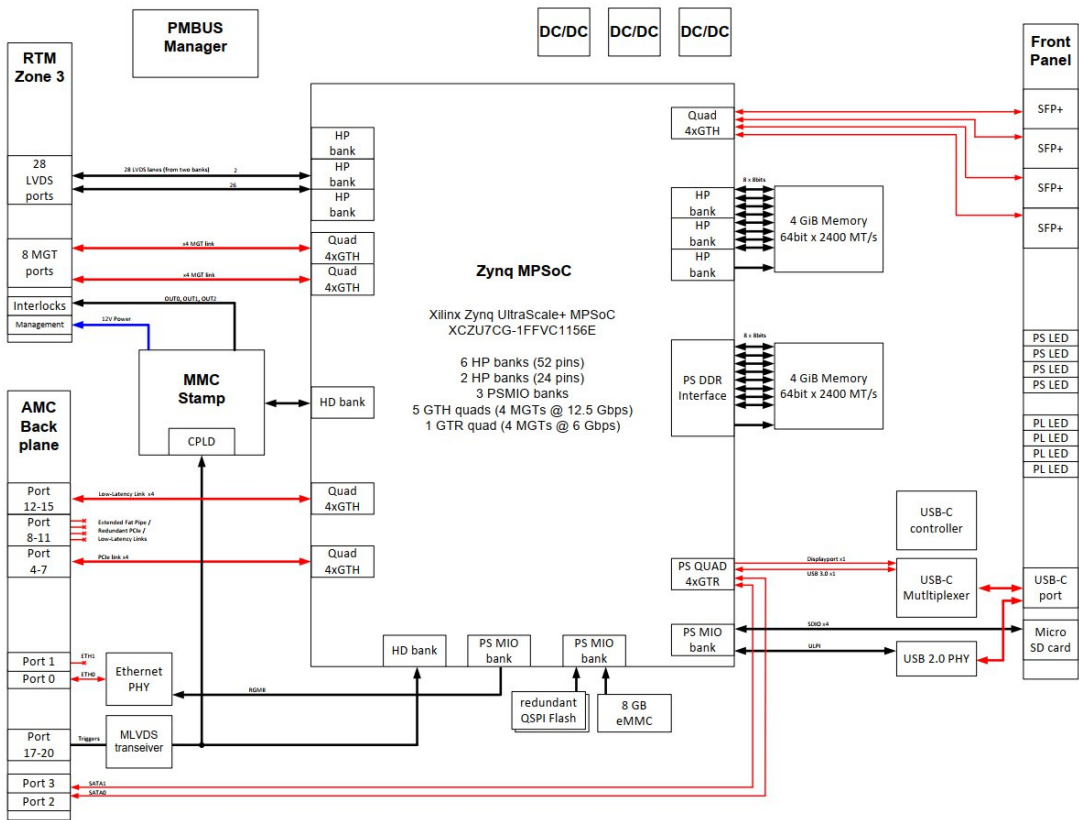
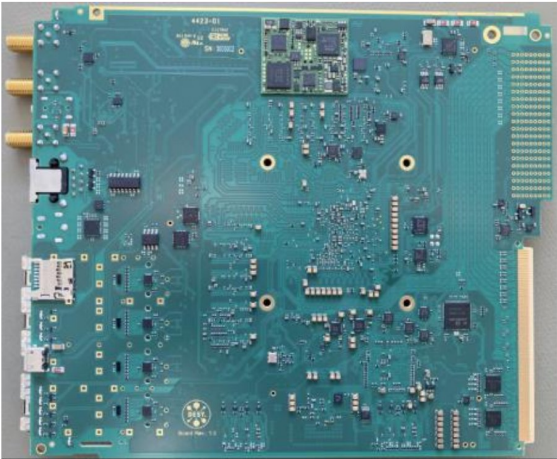
- Quad-Core ARM Cortex-A53 @1.5 GHz, Dual-Core ARM-R5 RT @600 MHz and Mali-400 MP2 graphics
- PCIe x4 (**x8** option on supported systems); Gen.3 supported
- **USB type-C Alternate Mode Display Port** for standalone operation (no need for additional AMC CPU Module)
- Flexible clocking scheme and front panel connector for external clock input and **White Rabbit support**
- Supported by all Xilinx development tools (e.g. Vivado HLx)



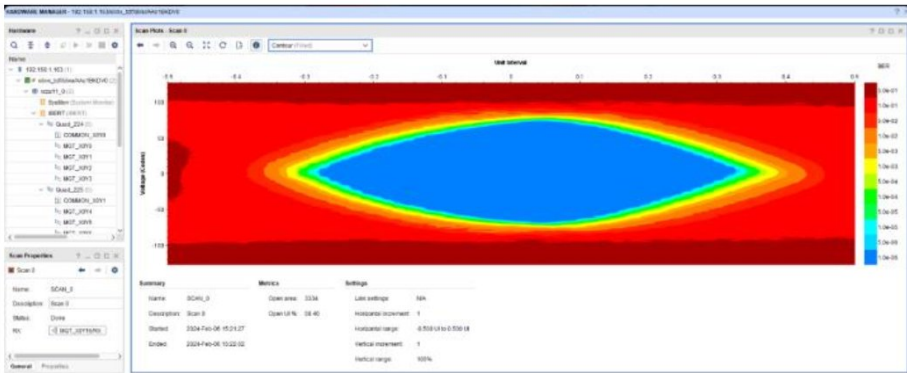
DAMC-UNIZUP

Board wurde speziell für RTM-Applikationen entwickelt

- Erste 3 Prototypen gebaut
- Sehr gute Ergebnisse in Rev. 1.0, 100% der Funktionen in Betrieb
- RTM Klasse D1.2 oder D1.3 Anbindung zum MPSoC (Bestückungsoption)
 - D1.2: **38 LVDS** Paare und **4 MGTs** → z.B.. parallel ADCs auf RTM
 - D1.3: **28 LVDS** Paare und **8 MGTs** → z.B. JESD204B ADCs auf RTM



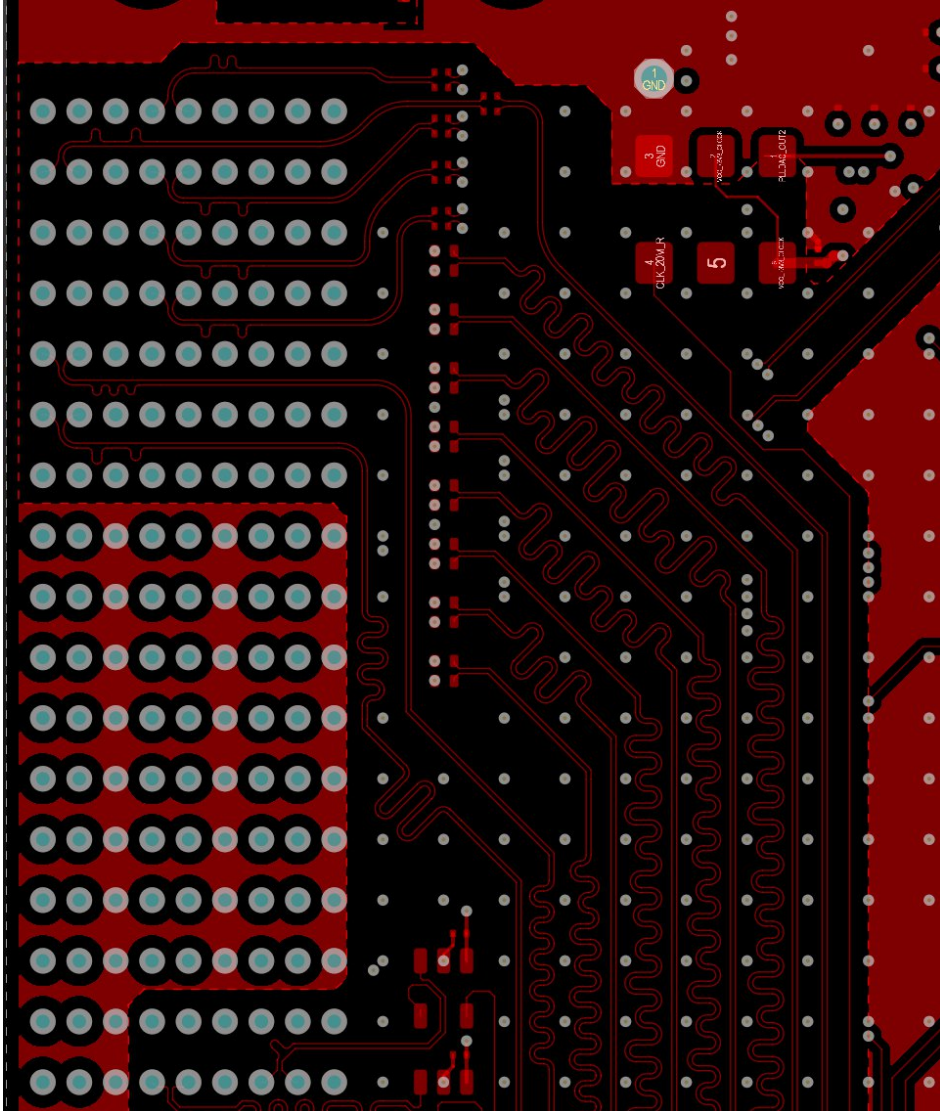
SFP+ Augendiagramm:



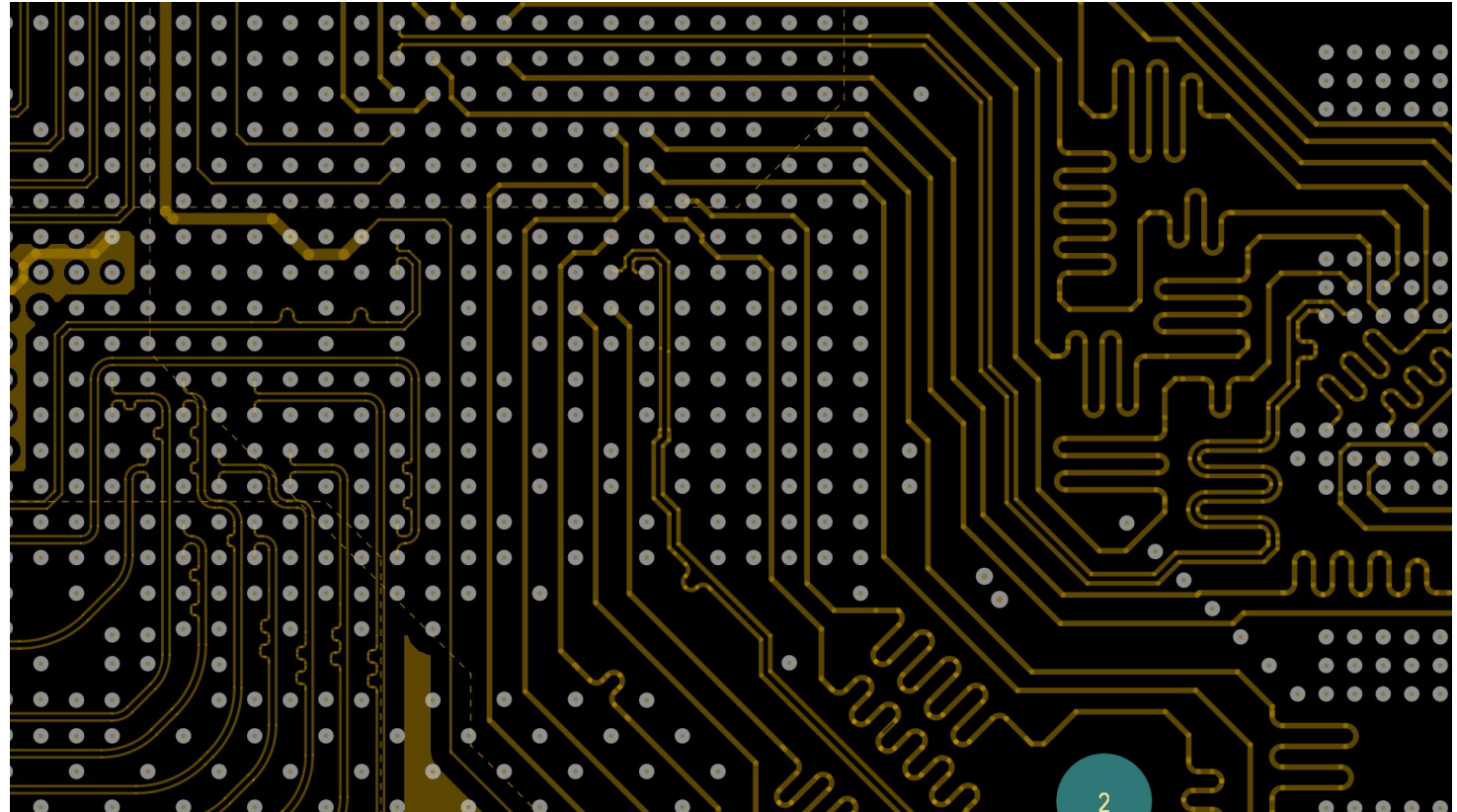
Name	TX	RX	Status
Ungrouped Links (0)			
Link Group 0 (4)			
Link 0	Quad_228/MGT_X0Y16/TX (xczu11_0)	Quad_228/MGT_X0Y16/RX (xczu11_0)	10.313 Gbps
Link 1	Quad_228/MGT_X0Y17/TX (xczu11_0)	Quad_228/MGT_X0Y17/RX (xczu11_0)	10.313 Gbps
Link 2	Quad_228/MGT_X0Y18/TX (xczu11_0)	Quad_228/MGT_X0Y18/RX (xczu11_0)	10.313 Gbps
Link 3	Quad_228/MGT_X0Y19/TX (xczu11_0)	Quad_228/MGT_X0Y19/RX (xczu11_0)	10.307 Gbps

Layout-Details

Nichts ist trivial, alles ist schnell



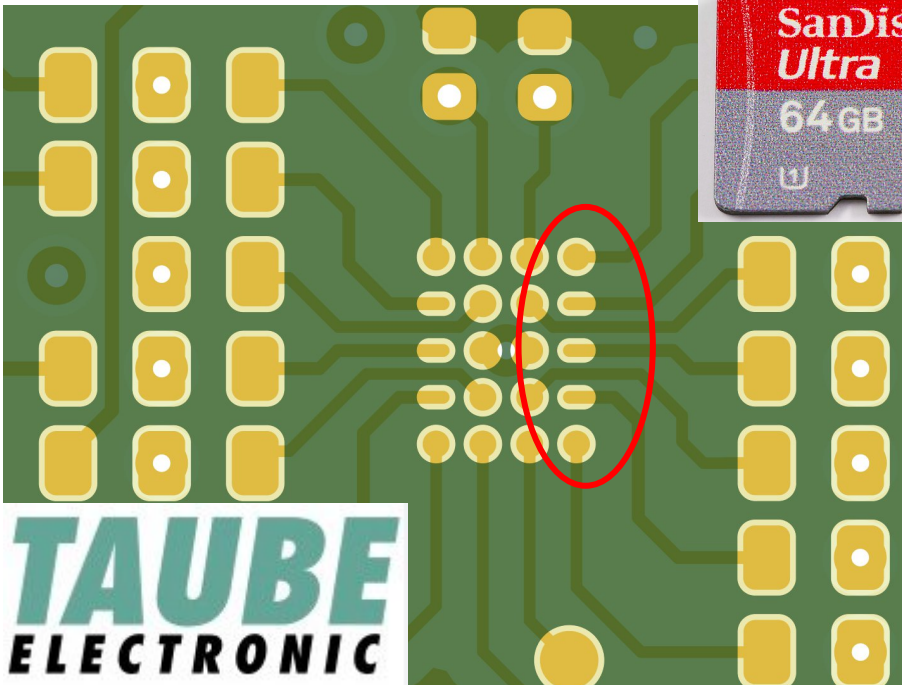
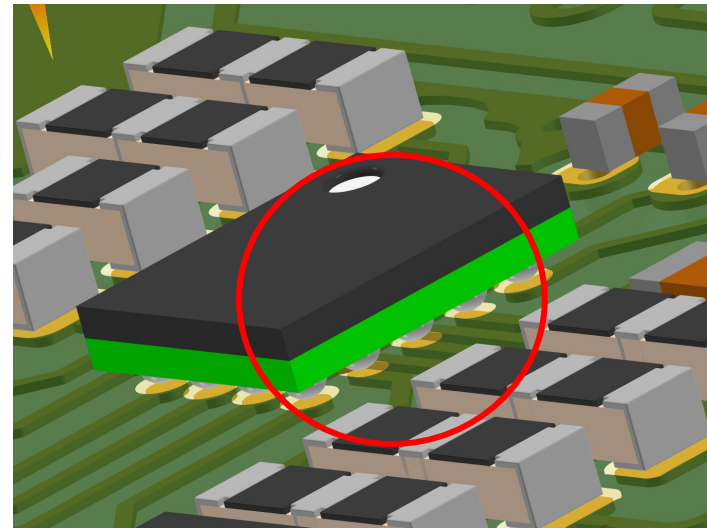
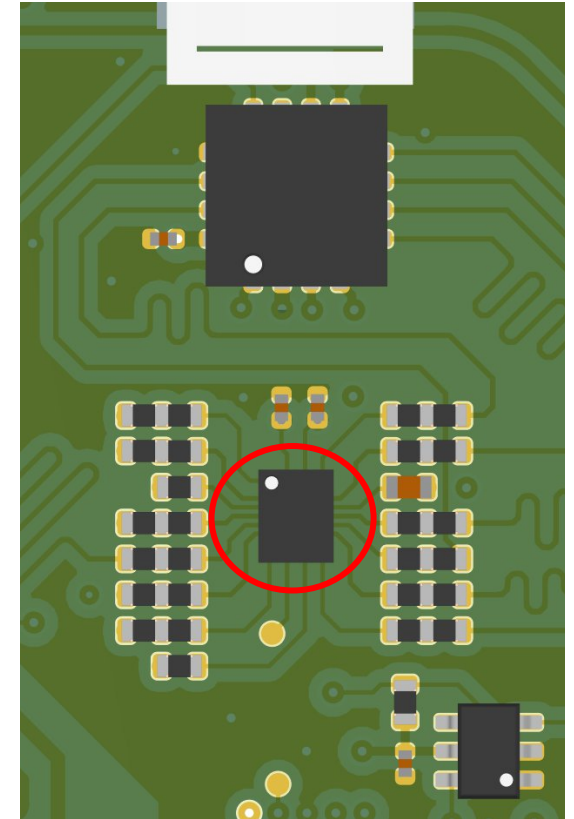
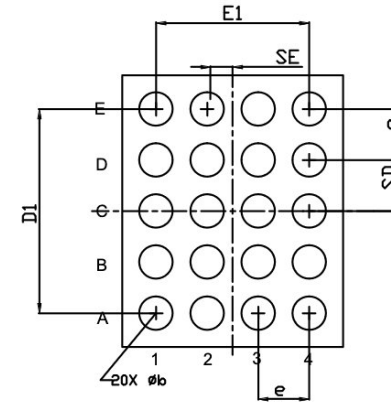
- Herausforderung: 100um Technologie, kein HDI (nur “ganze” Vias)
- LVDS: 1250 Mbit/s (625 MHz): DDR4: 2666 MT/s (1.3 GHz), Serielle Transceiver (MGTS): 16.375 Gbps
- Fast alles wird im Layout abgerundet
- 100% Längenausgleich, sofort (In der Regel besser 1ps / 0.15mm)
- Via in Pads, “GSS-Vias”, Berücksichtigung der Stub-Länge je Layer
- Sandwich-Aufbau: SIG-GND-SIG-GND ... Power, Power, ... GND, SIG



Noch ein Trick...

Herausforderung PI4ULS3V4857GEAEX SD 3.0 Translator

- Bidirektionaler Pegelumsetzer mit variabler Spannung nötig (SD3.0)
- BGA-Pitch: 0.4mm (nur 2 Bausteine aus der Handytechnik verfügbar)
- unmöglich in 100um Technologie (0.8mm Pitch nötig)
- Keine Lösungen auf dem Markt
- Ansatz: "Rasieren der Pads" und hoffen, das es klappt
- Bestückt bei Taube (Herausforderung "verheimlicht")
- hat geklappt - Lohn: 100 Megabytes pro Sekunde SD-Karten-Transferrate (Abhängig von Karte)



```
root@UNIZUP-001 ➡ dd if=/dev/zero of=./TestingFile bs=100M count=10 oflag=direct
10+0 records in
10+0 records out
1048576000 bytes (1.0 GB, 1000 MiB) copied, 17.2029 s, 61.0 MB/s
root@UNIZUP-001 ➡ dd if=./TestingFile of=/dev/null bs=100M count=10 oflag=dsync
10+0 records in
10+0 records out
1048576000 bytes (1.0 GB, 1000 MiB) copied, 11.2052 s, 93.6 MB/s
root@UNIZUP-001 ➡
```

DRTM-8SFP+

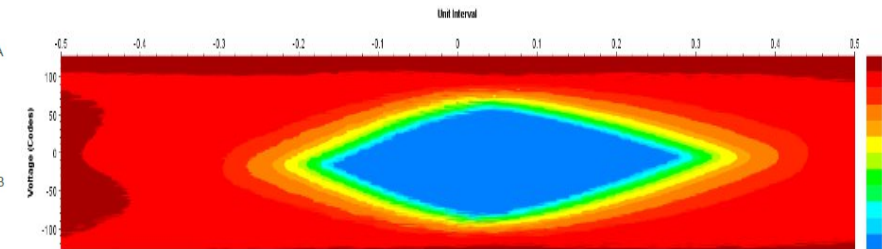
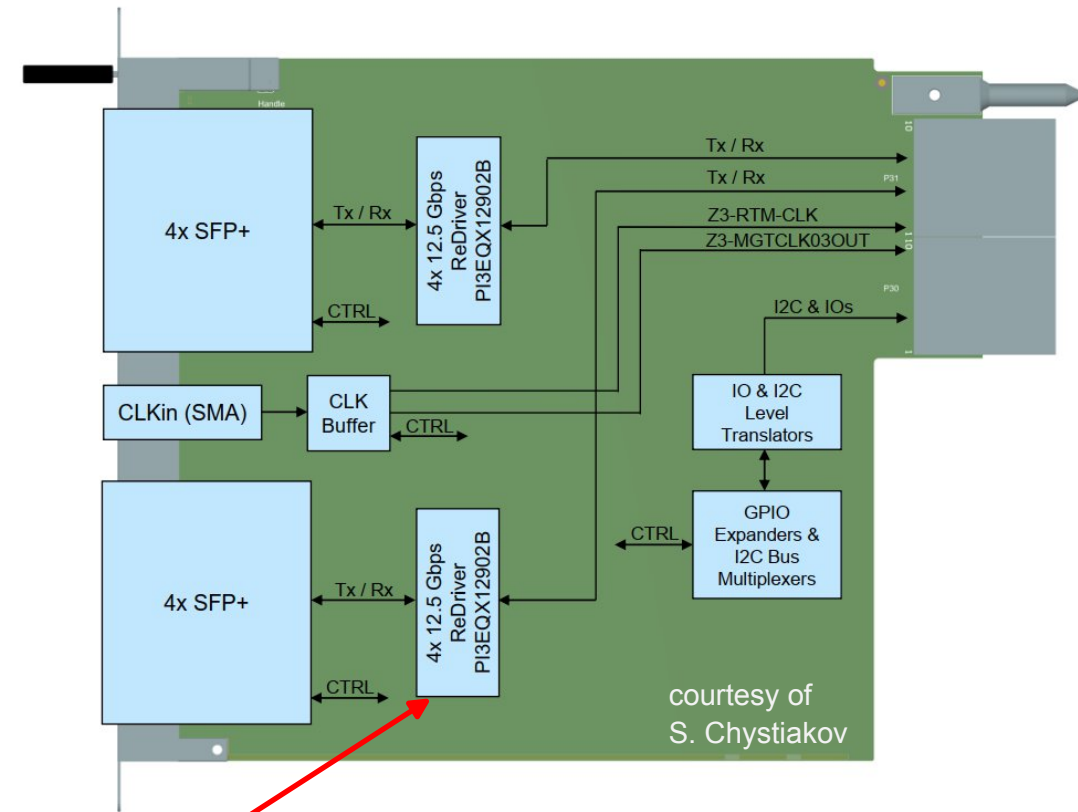
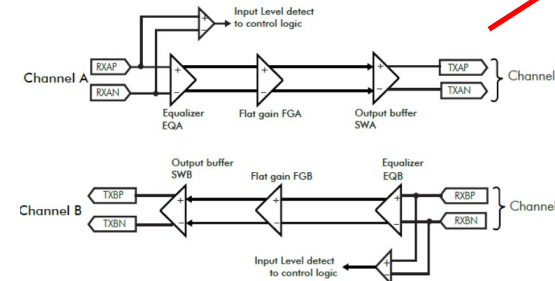
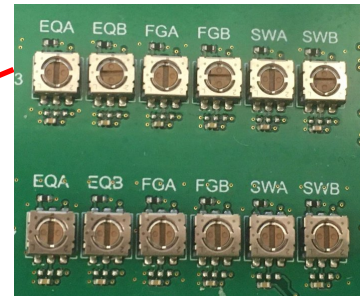
DAMC-8SFP+

DRTM-8SFP+ Breakout Board

- 1 zum 8 MGTs zum RTM (für DAMC-UNIZUP)
- Entwickelt für 12.5 Gbps: nicht trivial
- Erster Einsatz von „analogem“ Equalizer
- Entwicklungszeit: 3 Monate
- Low-cost Leiterplatte und Komponenten
- Hergestellt im „PCB-Pool“ von Leiton (Berlin)
- Material: Panasonic R-1566W



LEITON



Name	TX	RX	Status	TX Polarity Invert	RX Polarity Invert	Bits	Errors	BER
Ungrouped Links (0)								
Link Group 0 (4)								
Link 3	Quad_224/MGT_X0Y3/TX (xczu11_0)	Quad_224/MGT_X0Y3/RX (xczu11_0)	10.313 Gbps	☐	☒	8.597E12	0E0	1.163E-13
Link 2	Quad_224/MGT_X0Y2/TX (xczu11_0)	Quad_224/MGT_X0Y2/RX (xczu11_0)	10.313 Gbps	☒	☒	8.597E12	0E0	1.163E-13
Link 1	Quad_224/MGT_X0Y1/TX (xczu11_0)	Quad_224/MGT_X0Y1/RX (xczu11_0)	10.313 Gbps	☒	☐	8.597E12	0E0	1.163E-13
Link 0	Quad_224/MGT_X0Y0/TX (xczu11_0)	Quad_224/MGT_X0Y0/RX (xczu11_0)	10.313 Gbps	☒	☐	8.597E12	0E0	1.163E-13

Verbesserung der Signalintegrität mittels Re-Driver

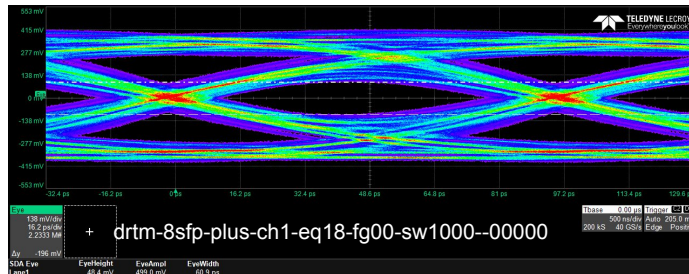
Erste Verwendung eines analogen Equalizers

- Super kritische Verbindung auf DAMC-UNIZUP
- 10.315 Gbps (bis 12.5 Gbps)
- Schlechte Verbindung:
 - Über zwei 0-Ohm Brücken
 - und über Erni-Stecker
- “Warnung: geht nicht” – eben doch, wenn man es richtig macht:

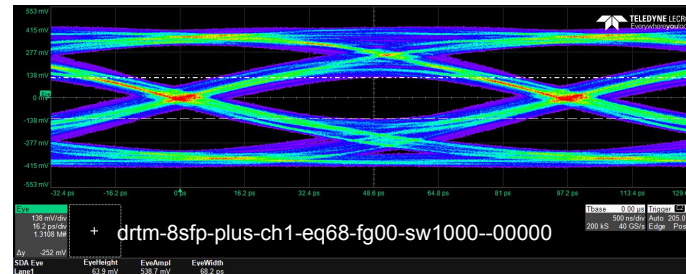
PI3EQX12902B: 4 Konfigurationen möglich

	Equalizer setting (dB)				
	@2.5GHz	@3GHz	@4GHz	@5GHz	@6GHz
1	1.8	2.6	4.5	6.6	8.9
2	3.7	4.7	6.7	9.4	11.7 (Default)
3	5.1	6.3	8.7	11.2	13.5
4	6.8	8.2	10.8	13.2	15.3

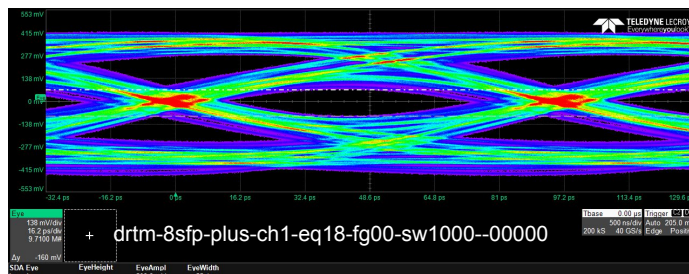
gute Verbindung (1-1): 5 GHz: +6.6dB



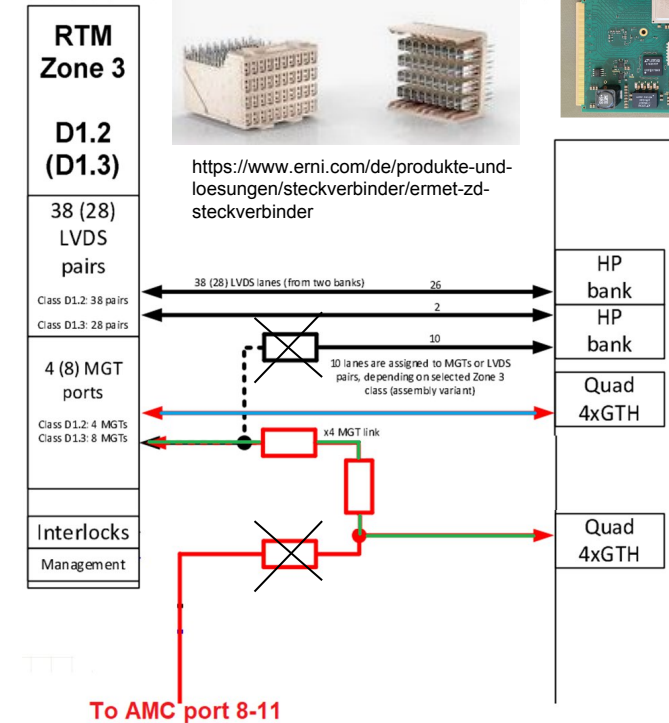
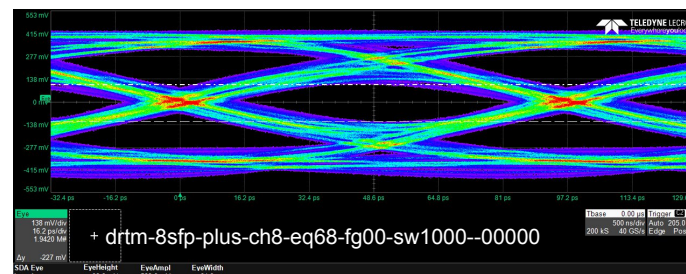
gute Verbindung: 5 GHz: +13.2dB



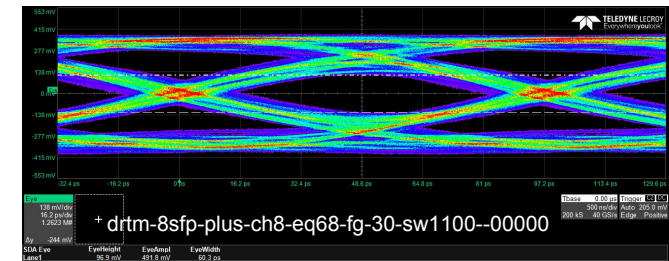
schlechte Verbindung: 5 GHz: +6.6dB



schlechte Verbindung: 5 GHz: +13.2dB



Schlechte Verbindung
13.2dB, 1100mV Level, -3.0dB “flat gain”



DAMC-RFSoc



Photo:
<https://www.avnet.com/wps/portal/silica/products/product-highlights/xilinx-rfsoc/>

Die Basis: DAMC-DS812ZUP

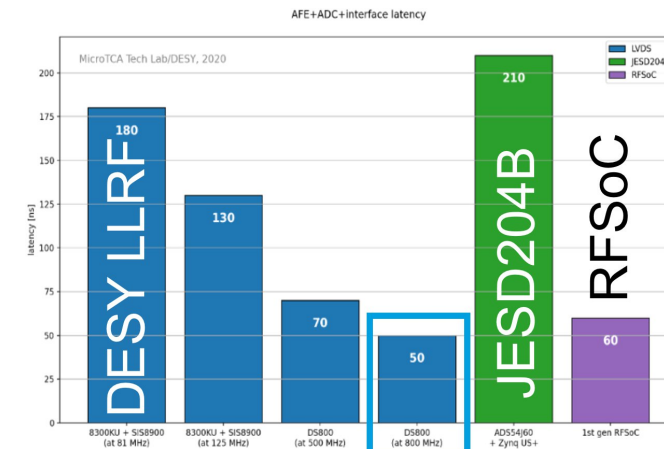
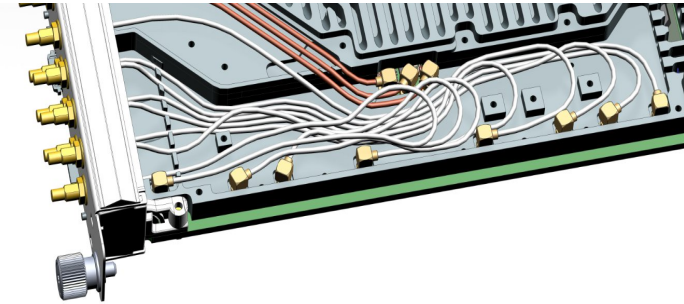
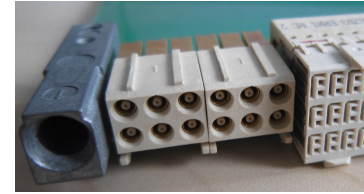
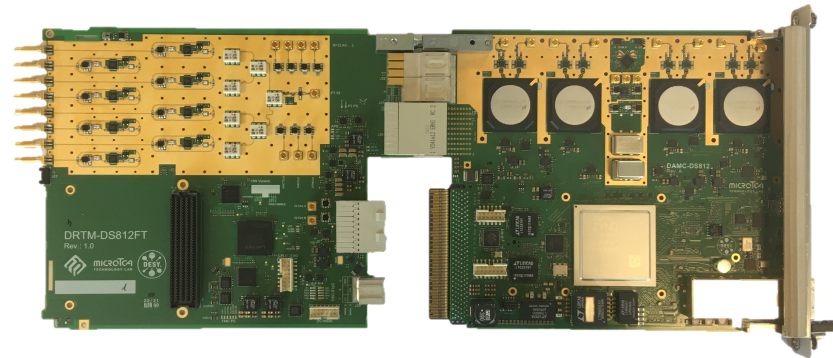
DAMC-DS812ZUP



Wir haben: 8-Kanal 800 MSPS Digitizer
Wir wollen: 8-Kanal 5 GSPS Digitizer + 10 GSPS DAC
Lösung: AMD/Xilinx RFSoc

Was wir übernehmen:

- Koaxiale Zone-3 Verbindung
- Frontpanel/ Backplane Konzept über RF Coax-Kabelbäume
- Front Panel: Scope-Applikation möglich

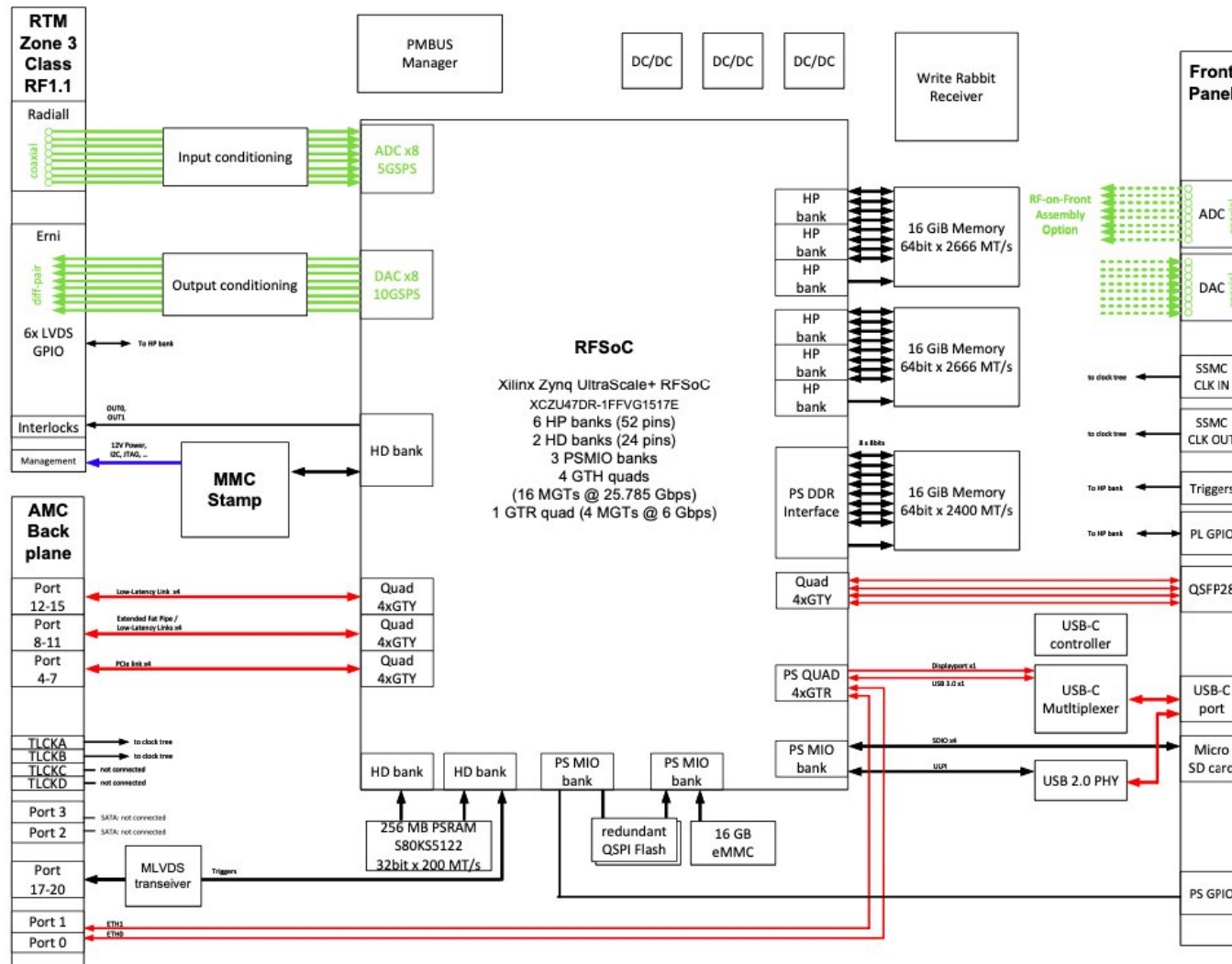


Main Features:

- 2.7GHz input BW, 12bits, 8-channels (Amplifier Bandwidth: 4.8 GHz)
- 50ns end-to-end latency
- **Coaxial analog Zone 3 RF1.0 Class**
- RF input from front panel or RTM: 800 MSPS / 1600 MSPS
- On-board PLL: 14fs jitter

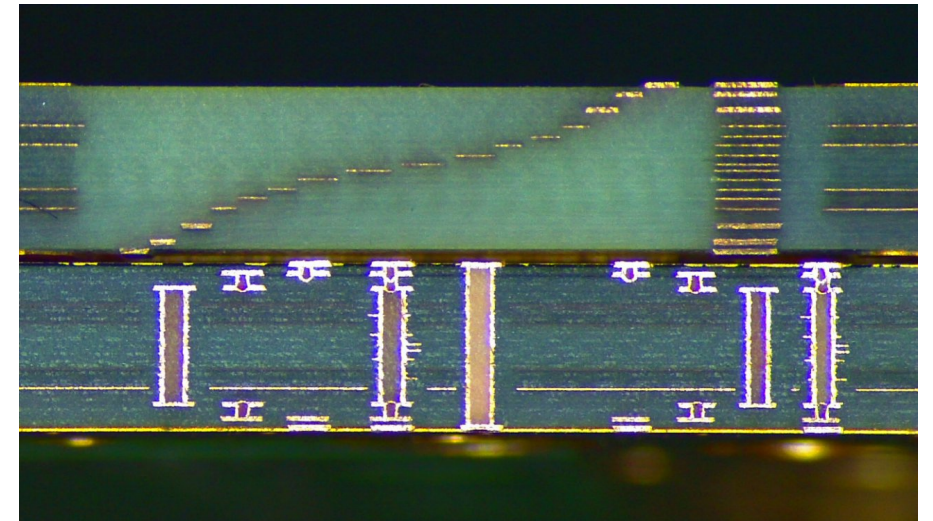


DAMC-DS5014DR: RFSoC



Eckdaten

- 8x 14 bits **ADC**, 5 **GSPS**, 6GHz analoge Bandbreite
- 8x 14 bits **DAC**, 10 **GSPS**, 4GHz analoge Bandbreite
- DC- und AC-Betrieb (Bestückungsoption)
- Megtron-6, 16 Layer, 75um Technologie
- Voller HDI-Lagenaufbau, 0201 Bauteile
- 2 Lagen Microvias, Stacked Microvias, staggered Microvias/blind Vias



„Werkzeuge“ für die Community

Was wir anbieten können...

Creative Commons License



Community Support

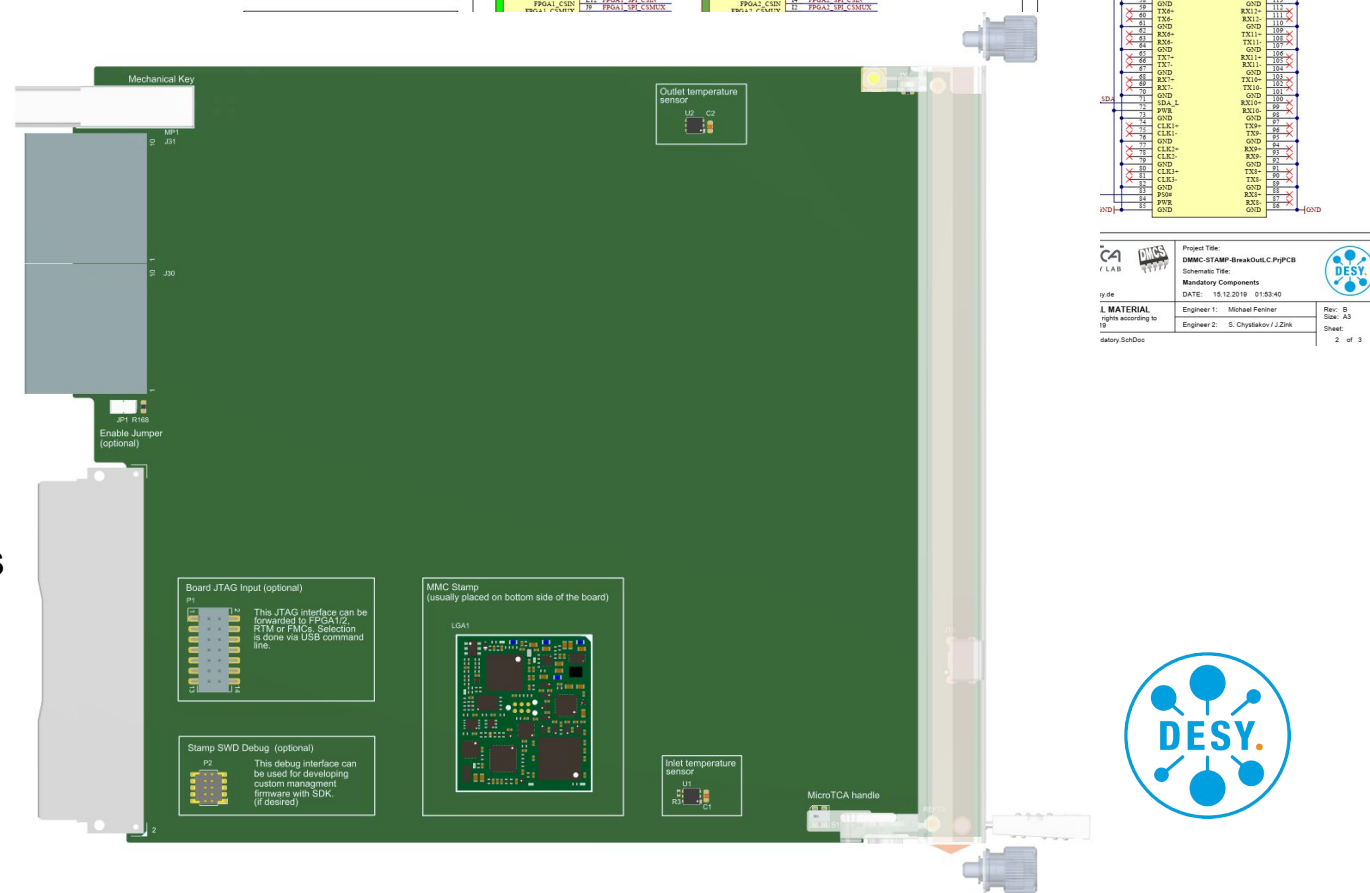
Fully MicroTCA compliant “empty” board

- ## Purpose: facilitate development

- Allows design migration (e.g. from VME)
- Source design files (Altium Designer) are provided
 - Schematics
 - PCB

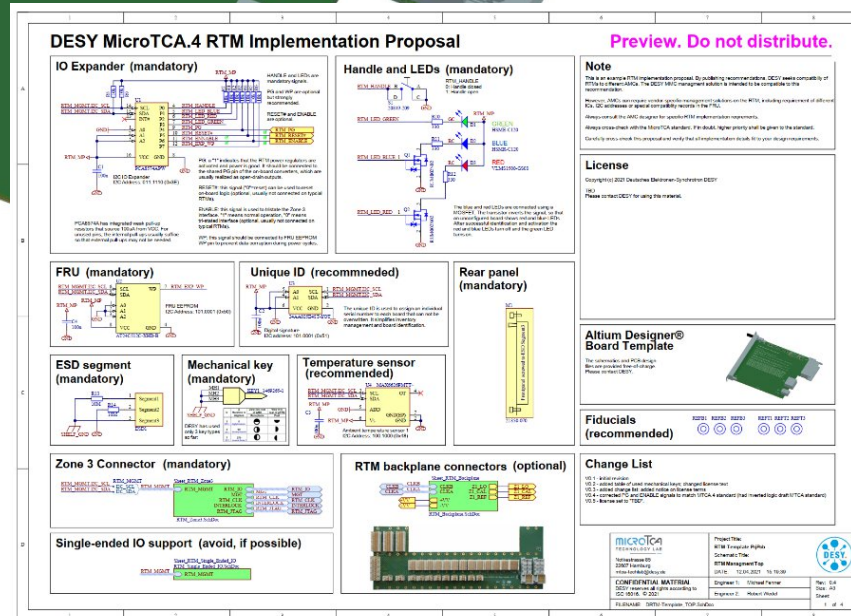
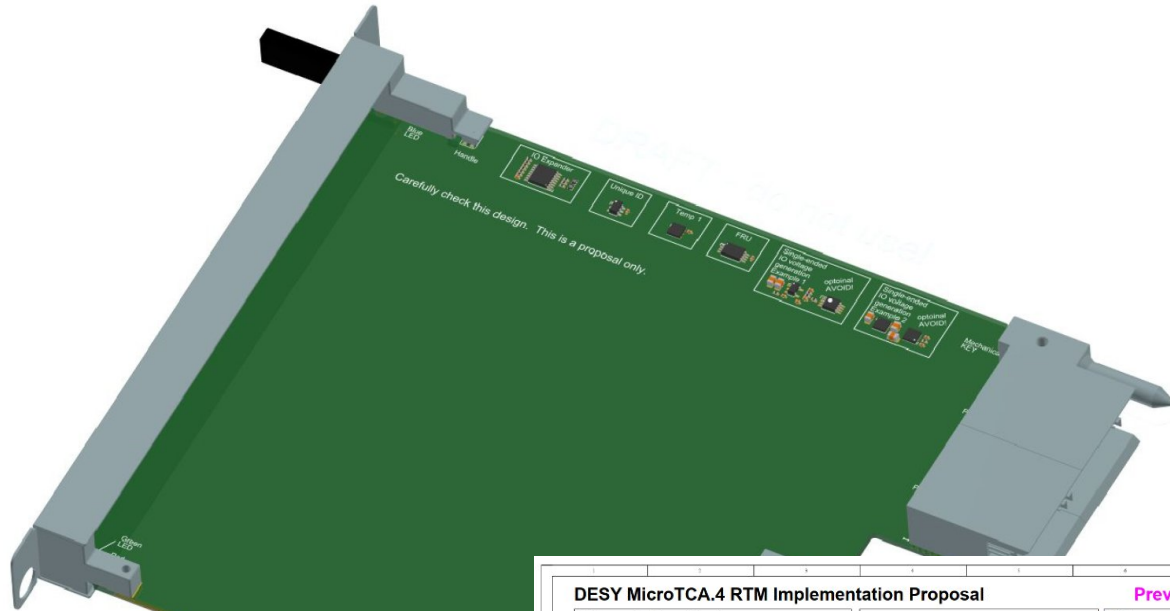
Components:

- MMC SoM, LEDs, Connectors, Temperature Sensors
- USB Interface for management and status

[illegible]

RTM Template

Community Support



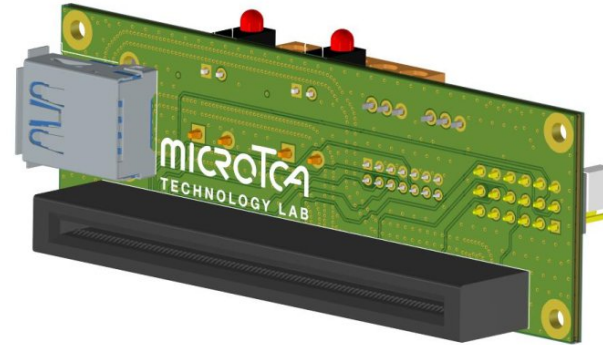
- We also provide a RTM Template
- Complete guide and “empty board” for own MTCA RTM designs → Altium Designer Template
- MTCA Standard leaves freedom for RTM interface implementation (vendor-specific) → risk of non-interchangeable AMC-RTM pairs
- DESY has a “class concept” → Interchangeable boards
- DESY collected and documented best design practices beyond the standard

Tools: MicroTCA Bring-up adapter

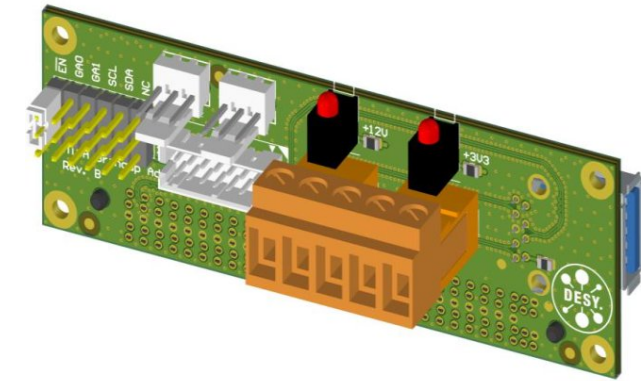
Community Support



Bottom view



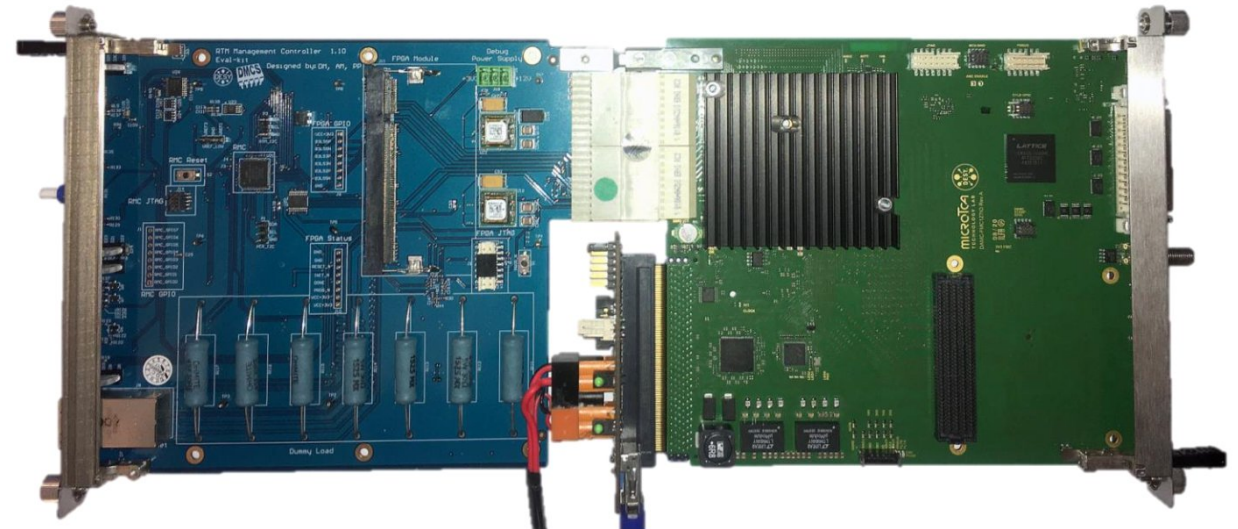
Top view



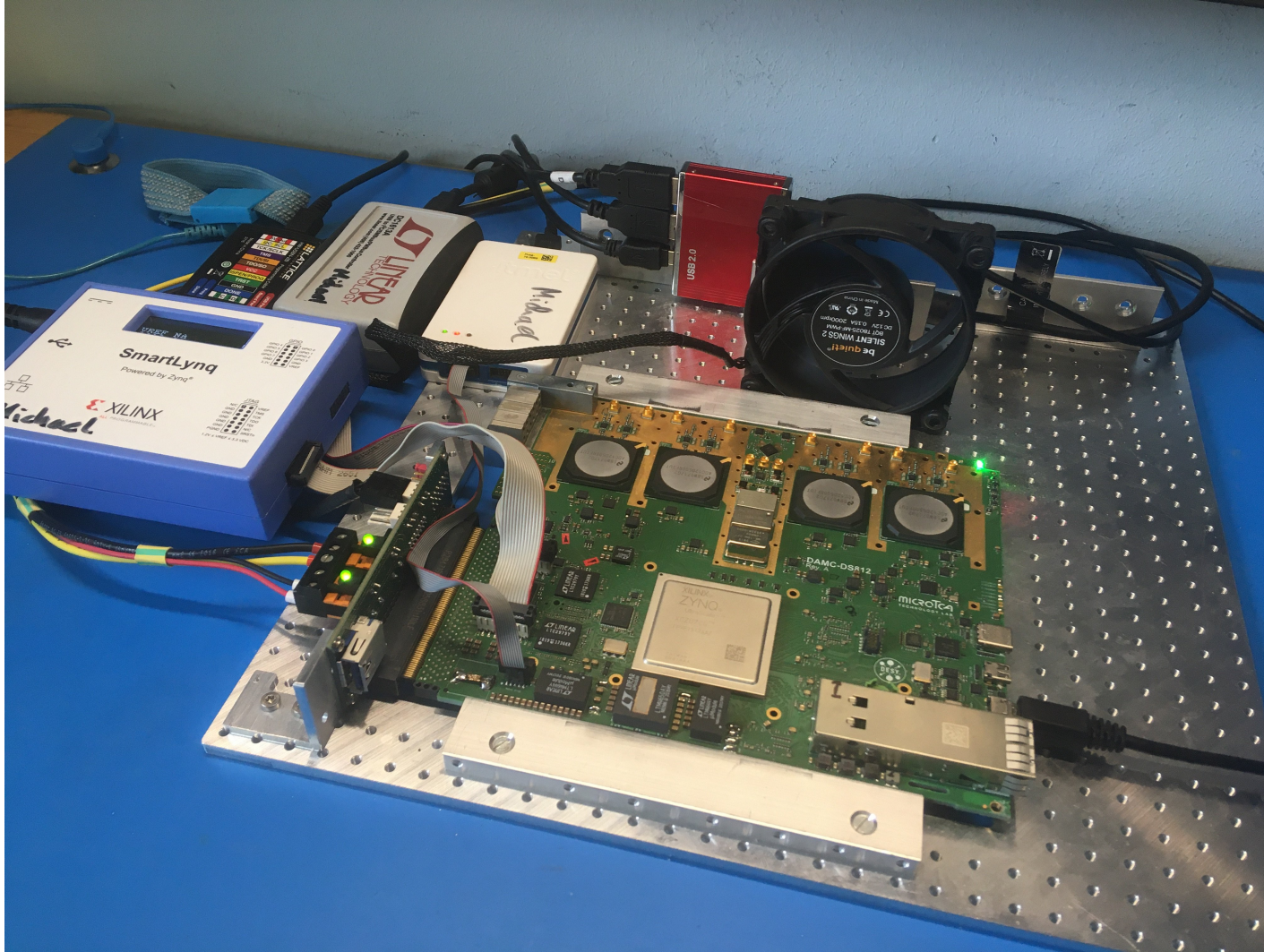
- Allows to connect power **and** PCIe to boards on the bench
- Mechanically compatible with RTMs
- PCIe option allows operate a MTCA board “inside a PC”



<https://rk.edu.pl/en/risers-and-adapters-non-standard-gpu-connection/>

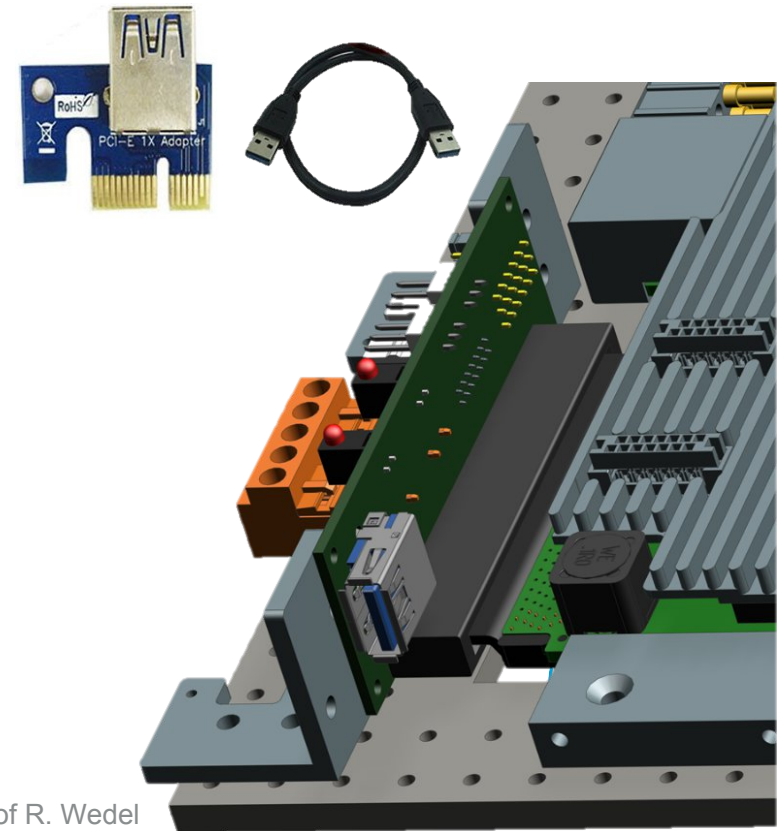


Typical Lab bring-up Setup

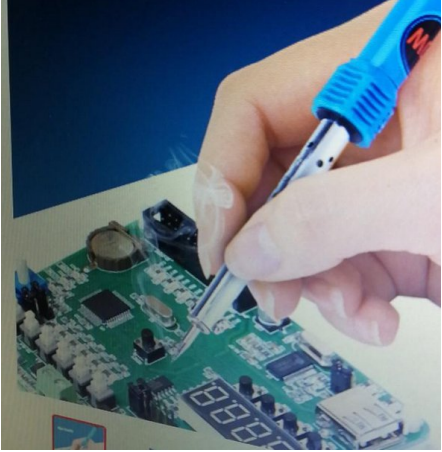


- Flexible and handy tools
- DESY provides them on request:
 - bring-up PCB production files
 - Aluminium frame production files

Write an email to me if you are interested in these designs.



Thank you!



-> https://www.reddit.com/r/electronics/comments/d62qwi/karen_hold_it_like_you_were_soldering/

Contact

DESY. Deutsches
Elektronen-Synchrotron

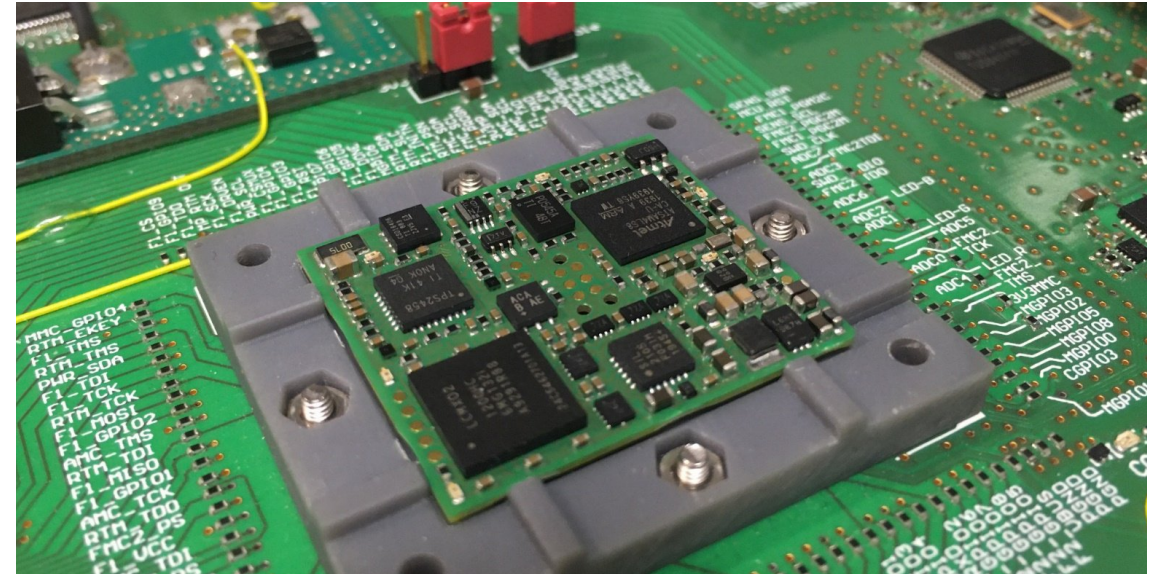
www.desy.de

Michael Fenner
MSK
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+49 (0) 40-8998-1885

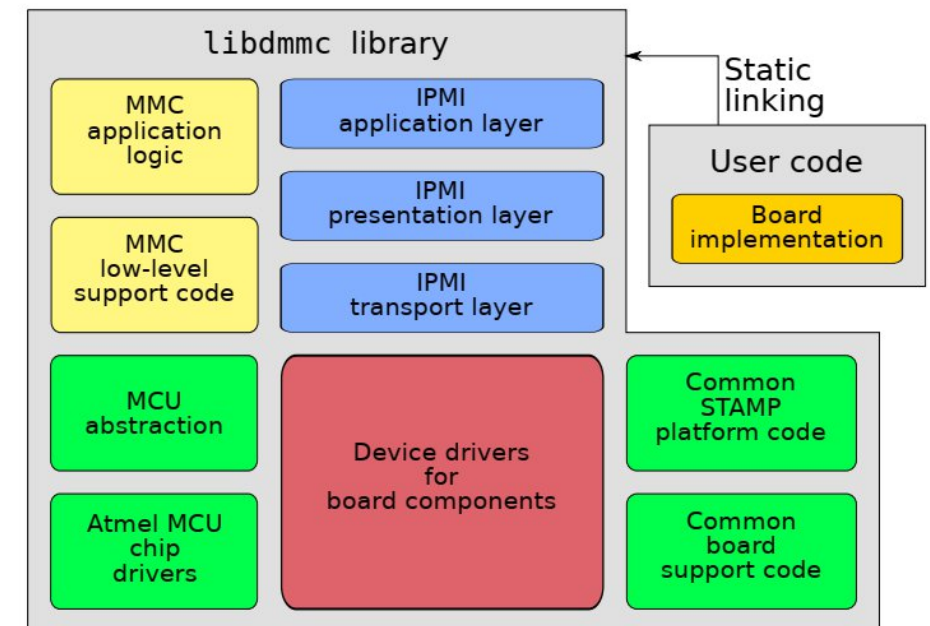
Backup

DMMC-STAMP

- ▶ System on Module (SoM)
 - ▶ 25.5 x 29.5 x 2.3 mm
 - ▶ Pre-programmed firmware
 - ▶ Evaluation board available (BoB)
- ▶ Software Development Kit (SDK)
 - ▶ MMC firmware customization
 - ▶ DESY MMC Software Library (libdmmc)
 - ▶ Example implementations (BoB, DAMC-FMC2ZUP)
- ▶ Open Source Tools and Templates
 - ▶ AMC and RTM Altium Designer Templates
 - ▶ mmcterm: serial over IPMB
 - ▶ bin2hpm: create HPM files for IPMI upgrade
 - ▶ frugy: read and write FRUs
 - ▶ cpld-img-tools: bitstream conversion for Lattice CPLDs



Post-Production test of DMMC-STAMP



Courtesy of Patrick Huesmann

DMMC-STAMP BoB (Break out Board)

