AKADEMIA GÓRNICZO-HUTNICZA
IM. STANISŁAWA STASZICA W KRAKOWIE
AGH UNIVERSITY OF KRAKOW

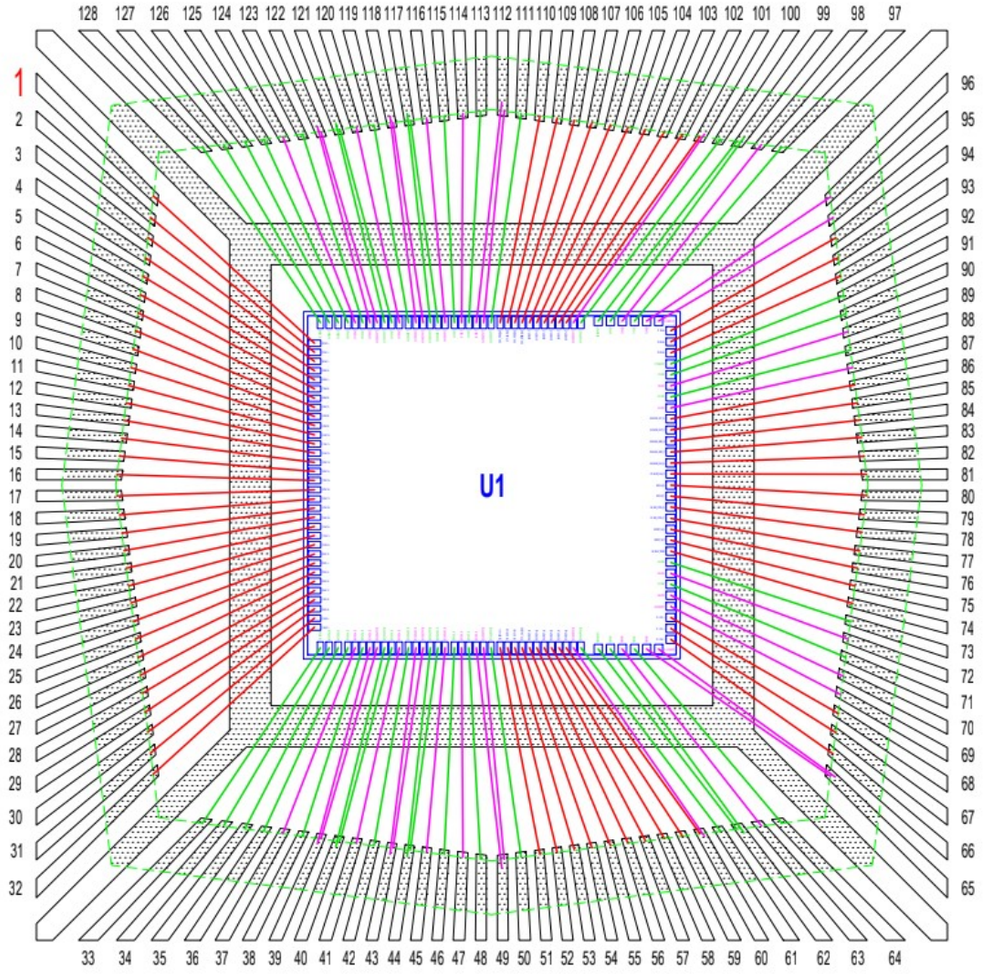
# Readout status and plan

ECAL working group meeting, 24.01.24

# Current readout status – **FLAXE ASIC**

- Technical details about packaging fixed (bonding scheme, marking)
  - We should get final confirmation and shipping date around 10th of February

- The expected shipping date of ~1000 packaged ASICs is around ~April 2024

## Current readout status – **FLAXE ASIC**

- With the bonding scheme fixed, I just (this week) started the design of:
  - Single FLAXE ASIC test board – required for ASIC verification and characterization
    - Schematic almost done, PCB not started yet
    - This board have to be ready till the end of Q1 2024 (before ASICs arriving)
  - FEB design
    - Lot of issues still to be resolved (like connector from FEB to patch panel)
    - At least the “front-end” (fanout connectors, ASICs placement and decoupling) should be done asap (hopefully before Valencia meeting) since it is needed for the fanout and HV flex design by Yan
    - Foreseen to be ready till the end of Q2 2024

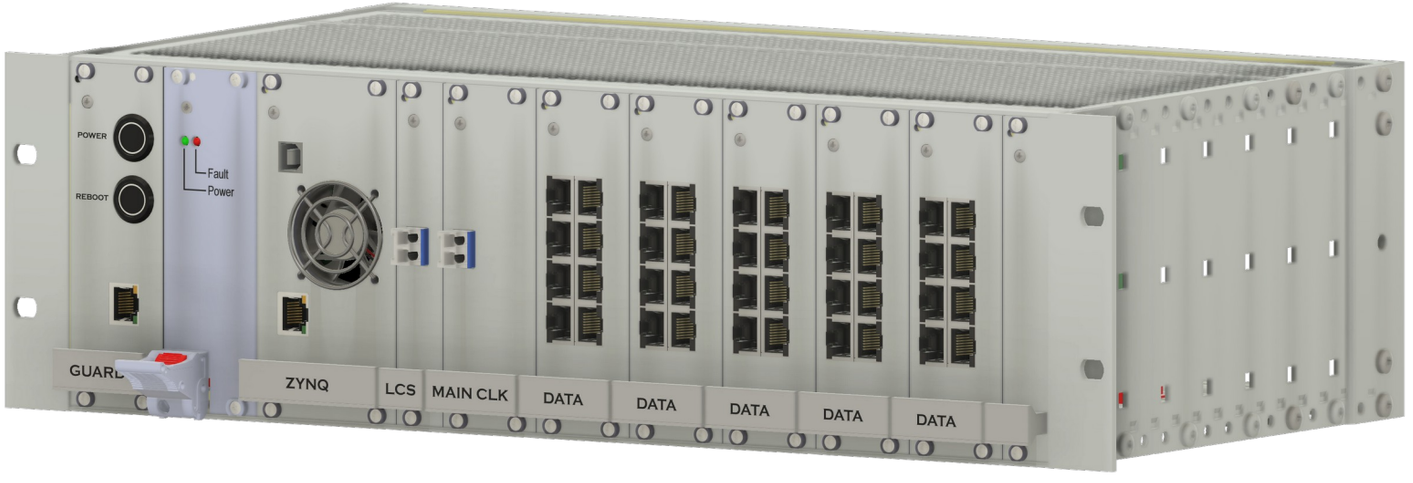
# Current readout status – **DAQ hardware**

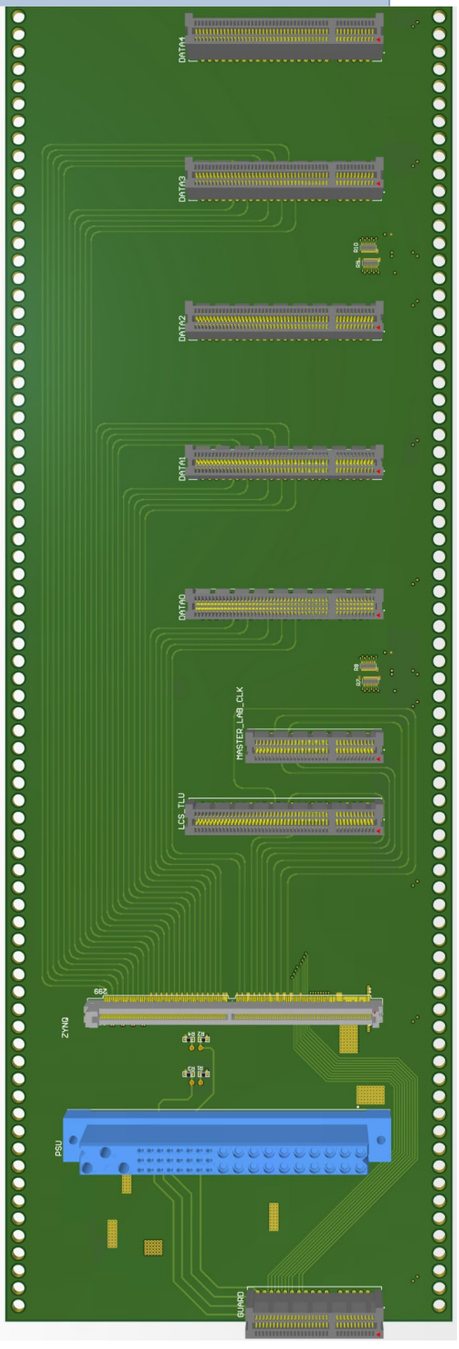
DAQ hardware (PCBs and mechanics) in progress:

- Mechanic is fixed (19” Eurorack from nVent Schroff)
  - 3D model with all cards and connectors prepared and verified
  - One rack already bought for tests

- PCBs:
  - Backplane almost ready (schematic and PCB)
  - Cards in progress (schematics in progress,
    PCB – only mechanics-related components placed)

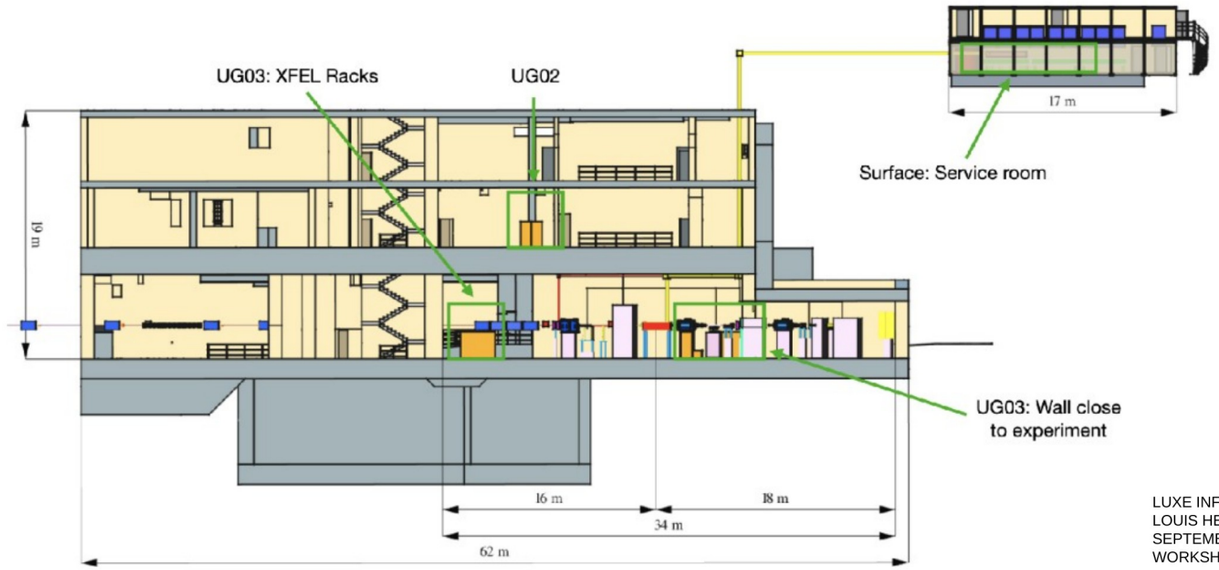
**Target: complete DAQ (one rack) and FEB (how many?)**
**for testbeam in Q3 2024**



# Current readout status – **data and clock transmission medium**

We have tested the cables (and fibers) to communicate DAQ rack with the FEBs in the cavern (~60m)




LUXE INFRASTRUCTURE
LOUIS HELARY
SEPTEMBER 4TH 2023 - LUXE WORKSHOP

- **Position foreseen for backend electronics:**
  - In UG03 (not accessible during data-taking).
  - In UG02 (potentially accessible at every time but for short stay and space limited).
  - In surface building (further away), space to be understood.

| Area | Length |
|---|---|
| UG03: Side north wall | 7 m |
| UG03: EuXFEL rack | 16 m |
| UG02 | 26 m |
| Surface: service room | ≈ 50 m |

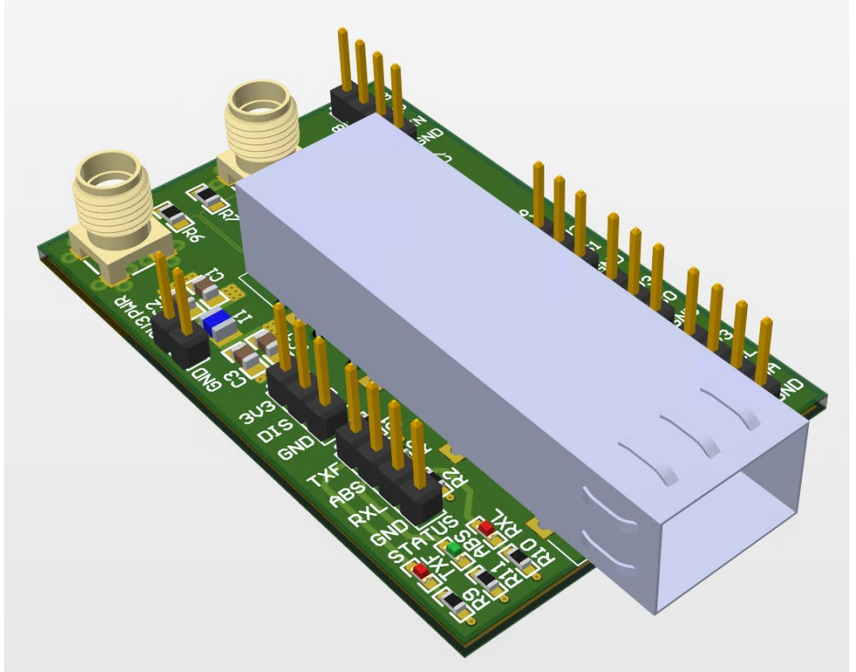
**Targets:**

- Find a medium to transmit the system clock and acquisition control signal from DAQ to the cavern with long-term phase drift <1ns
- Check if Cat6/6a RJ45 cables (widely available and cheap) can be used to send data from the cavern to the DAQ

# Current readout status – **data and clock transmission medium**

**Test setup:**

- Signal generator providing 20MHz square wave
  - Custom “SFP breadboard” PCB,
    commercial 1Gbps SFP modules (GBC PHOTONICS SF-MM85055D-GP, FOUNDRY TXN31111000001),
    50m long multi-mode fiber (OM2 Qoltec 54030)
  - 50m long, low-loss 50Ω coaxial cable
    Siva Cavi RF240LTA (1.4 EUR / m)
  - 50m long Cat6a RJ45 cable
    Logilink CQ3143S
- High speed scope measuring the signal delay and jitter
- Climatic chamber




**Test program**

- Delay and jitter measurements for temperature in range from -20 to +50 $^{o}$C
- *Delay and jitter measurements for varying humidity (not done yet)*

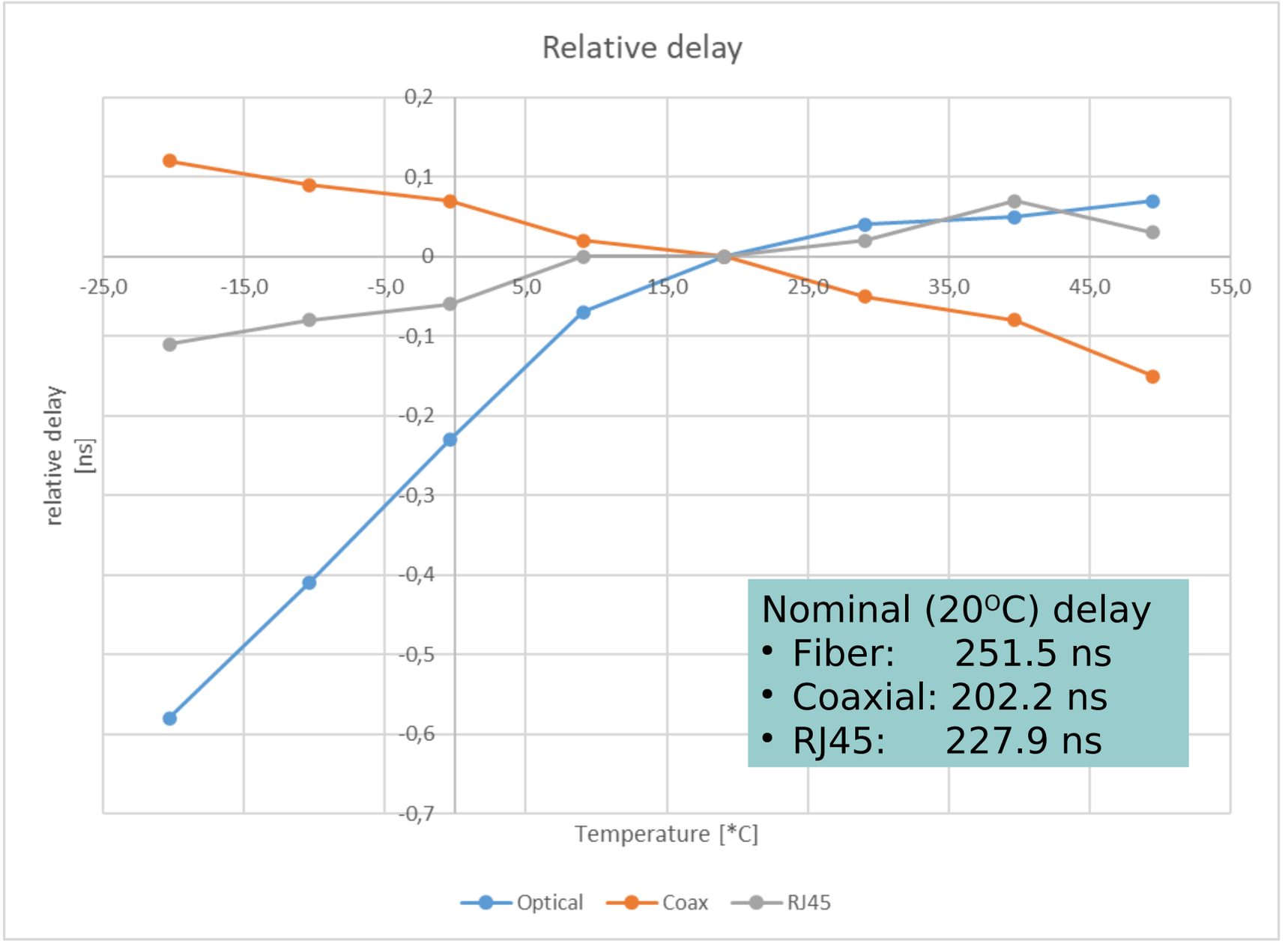
# Current readout status – **data and clock transmission medium**

## Delay drift

All three medium have drift <1ns

Fiber is surprisingly the worst one ranging from -0.6ns to +0.1ns!!

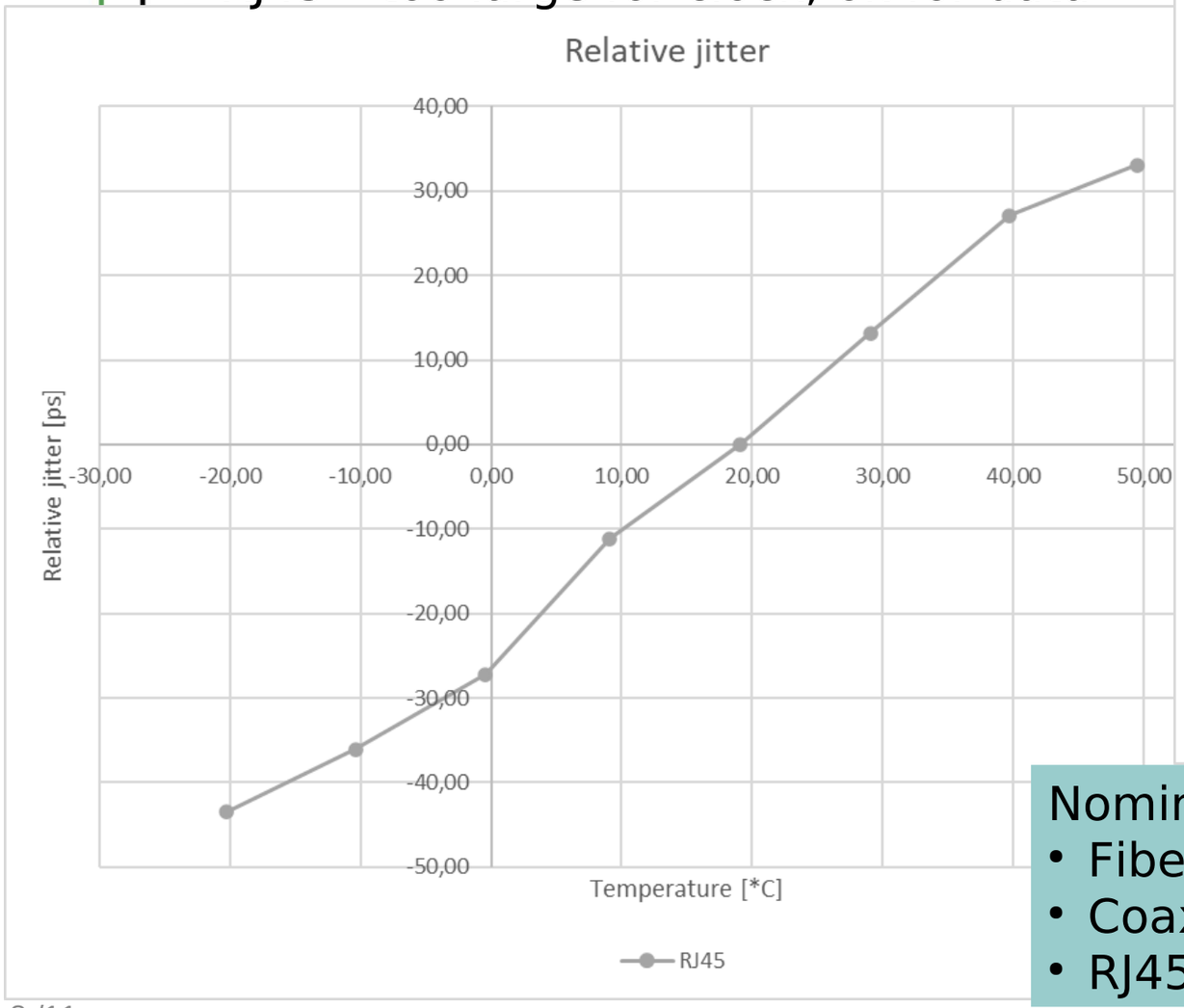
Coaxial cable seems the best choice, with drift < ±150ps

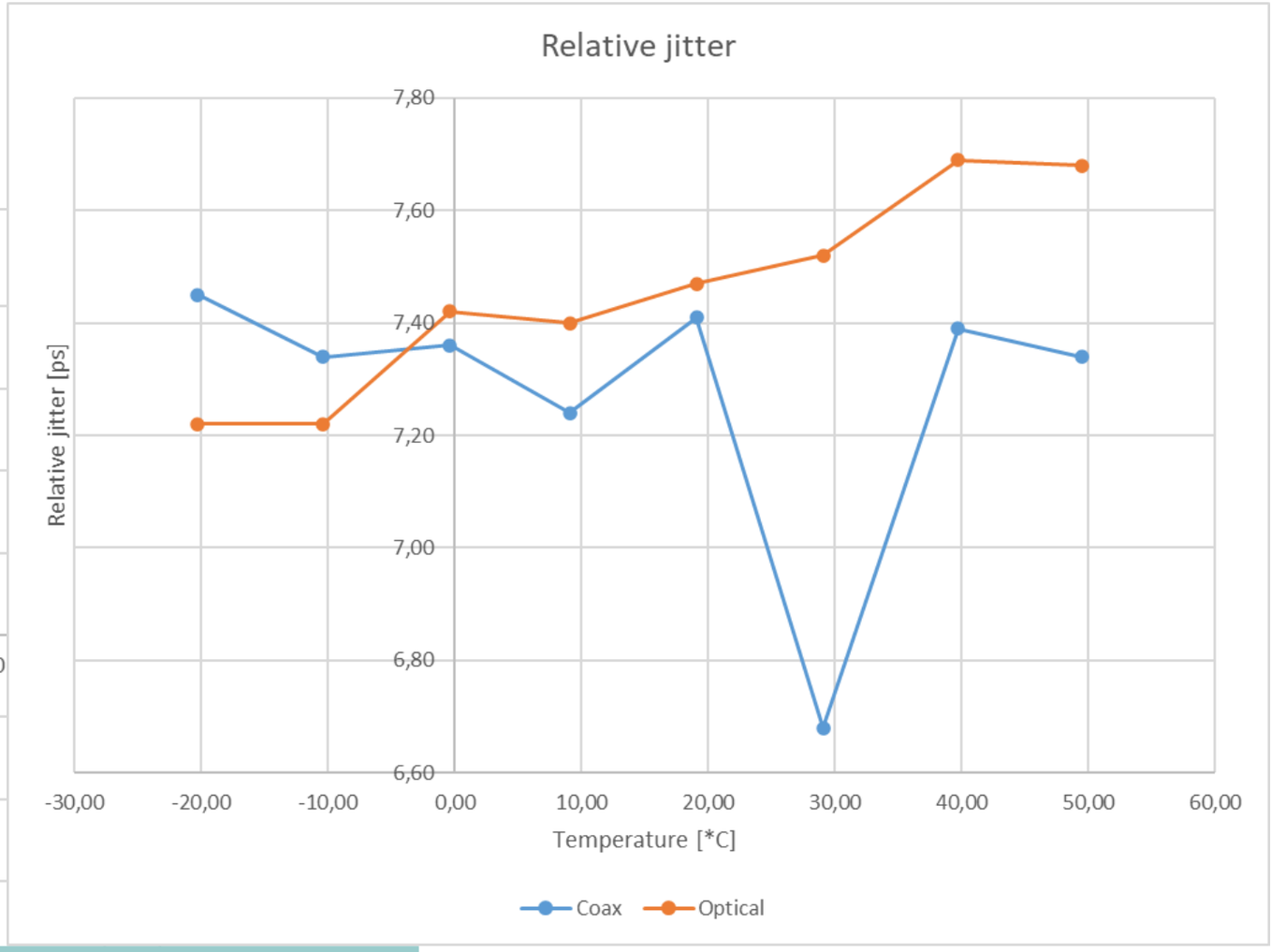


# Current readout status – **data and clock transmission medium**

## Relative jitter

RJ45 – too large for clock, ok for data




Nominal (20°C) jitter
- Fiber: 7.4 ps
- Coaxial: 7.4 ps
- RJ45: 161 ps

Fiber, coaxial – ok!

# Current readout status – **data and clock transmission medium**

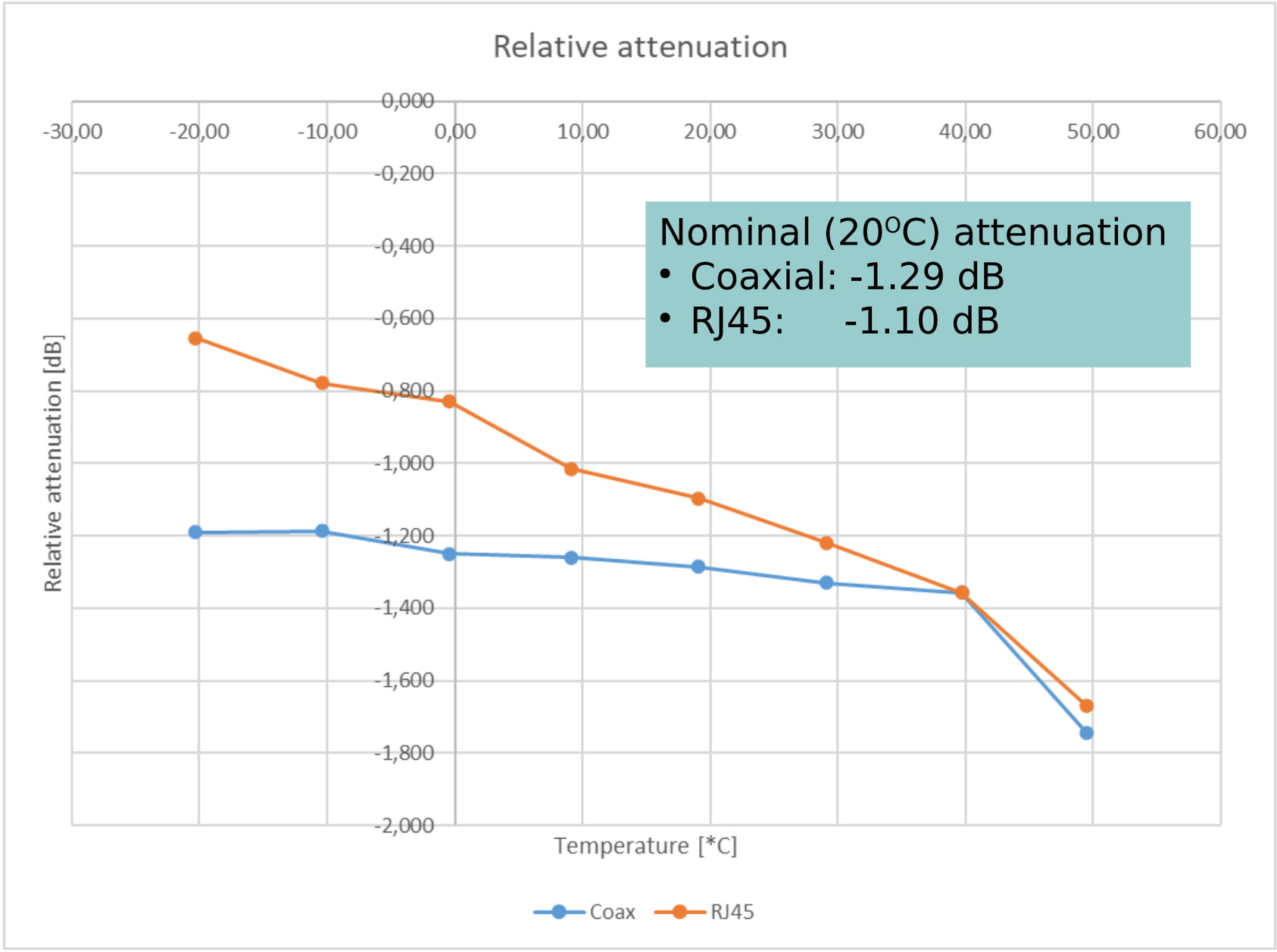
## Attenuation

Both coaxial and RJ45 attenuation well suited for clock and data transmission:

Worst case is -1.8dB (80% of original amplitude) after 50m.

We can expect less than -3.5dB (67% of the original amplitude) after 100m

*No attenuation data for fiber since SFP receiver recreates the electrical signal*



# Current readout status – **summary and schedule**

| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Task | | January | February | March | April | May | June | July | August | September | October |
| 1 | FLAXE test PCB design | | | | | | | | | | |
| 2 | FLAXE test PCB fabrication | | | | | | | | | | |
| 3 | Test setup development (miniDAQ) | | | | | | | | | | |
| 4 | FLAXE verification | | | | | | | | | | |
| 5 | FLAXE characterization | | | | | | | | | | |
| 6 | FEB design | | | | | | | | | | |
| 7 | FEB fabrication | | | | | | | | | | |
| 8 | DAQ PCB design | | | | | | | | | | |
| 9 | DAQ PCB fabrication | | | | | | | | | | |
| 10 | DAQ hardware tests | | | | | | | | | | |
| 11 | DAQ firmware development | | | | | | | | | | |
| 12 | Possible DAQ PCB redesign | | | | | | | | | | |
| 13 | System tests and debug (FEB + DAQ) | | | | | | | | | | |
| 14 | **Testbeam** | | | | | | | | | | |

*Comments:*

- Currently I am working on all of this completely alone
  - Most likely a (very good) master student should join within ~month
  - Together with Dawid they can take all the “verification / characterization / tests” tasks leaving me with all the design
  - Please understand that I am not able to take care of the TB data integrity in parallel
- There is no place in schedule for EUDAQ software! There will be DAQ software of course, but not integrated with EUDAQ without help from others!

## Current readout status – **summary and schedule**

- One of the the main showstoppers – clock and other signals distribution – resolved
- No info about ASICs fabrication progress (no bad info is a good info),
  ASICs expected ~April
- Hardware design in progress, no delay or showstoppers so far
- Firmware not yet started, but (at least for the first testbeam) it is not a huge task
- No time to prepare EUDAQ integrated software. Can someone with:
  - C/C++ experience,
  - EUDAQ knowledge (or willing to learn)

  help to develop it? (not now, rather end of Q2 2024)
- We are searching for post-doc (software or hardware oriented would be best)
- **Our goal is a testbeam at the end of Q3 2024 with at least one FEB (layer)**
- We need dose and neutron equivalent flux estimation in the space above the ECAL to
  - start the patch panel PCB design!
  - complete the FEB design!