Pixel chip testing at DESY

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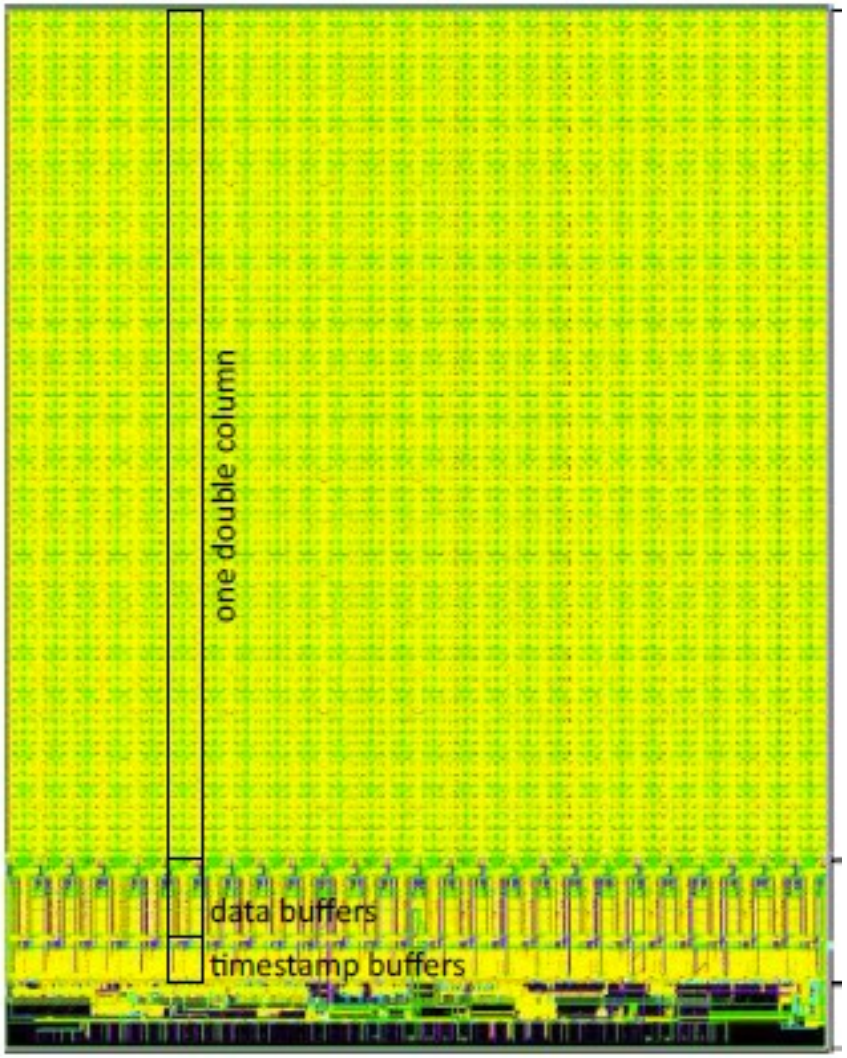
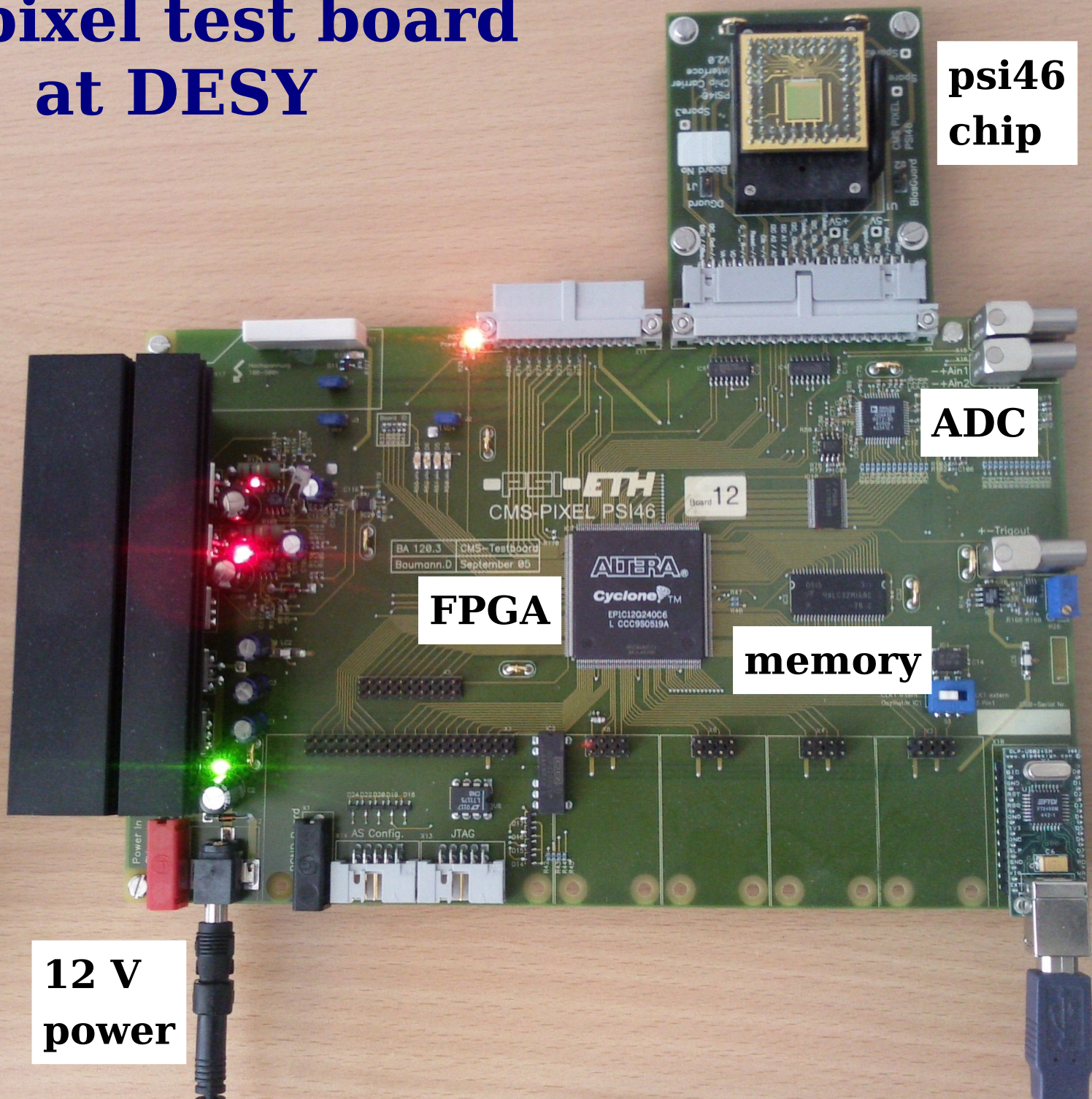
CMS Tracker Upgrade 31.5.2011



- Test board setup
- Chip parameters tuning
- Individual chip test
- Test chips with sensor

PSI pixel test board at DESY



Configuration

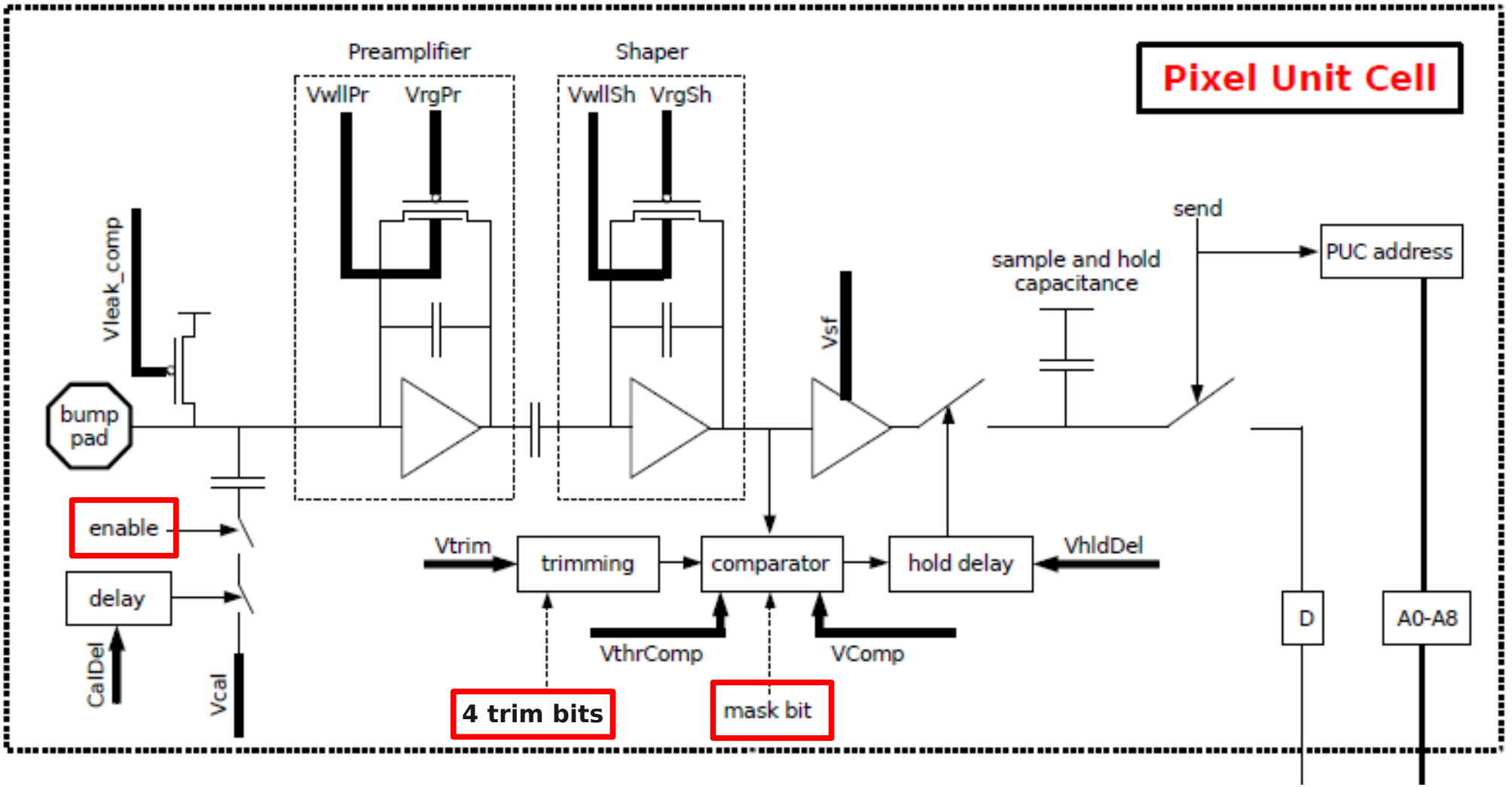
- Configuration files for test board and readout chip imported from PSI:
  - board name,
  - define single chip setup (no TBM),
  - run in 40 MHz mode,
  - set 28 DACs and Control Registers on the ROC.
- Some DAC parameters need to be tuned individually for each chip.
- Complete test: ~15 min. per chip
- Check root histograms and save configurations

psi46 DACs

1	Vdig	6
2	Vana	150
3	Vsf	160
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	130
11	Vtrim	7
12	VthrComp	124
253	CtrlReg	0
254	WBC	20

13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	55
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VIColOr	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	125
27	RangeTemp	0

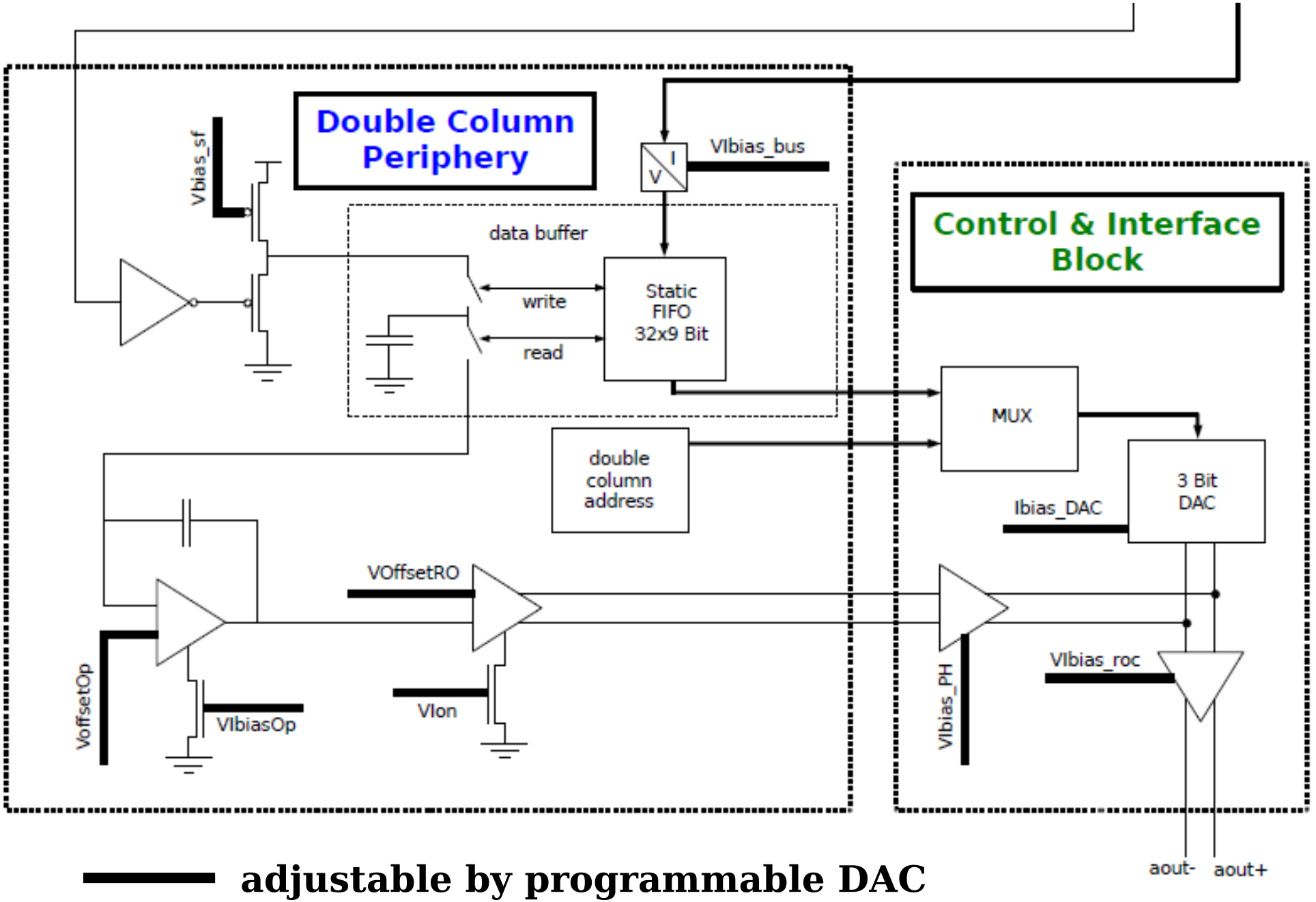
psi46 pixel readout chip



adjustable by programmable DAC, per ROC

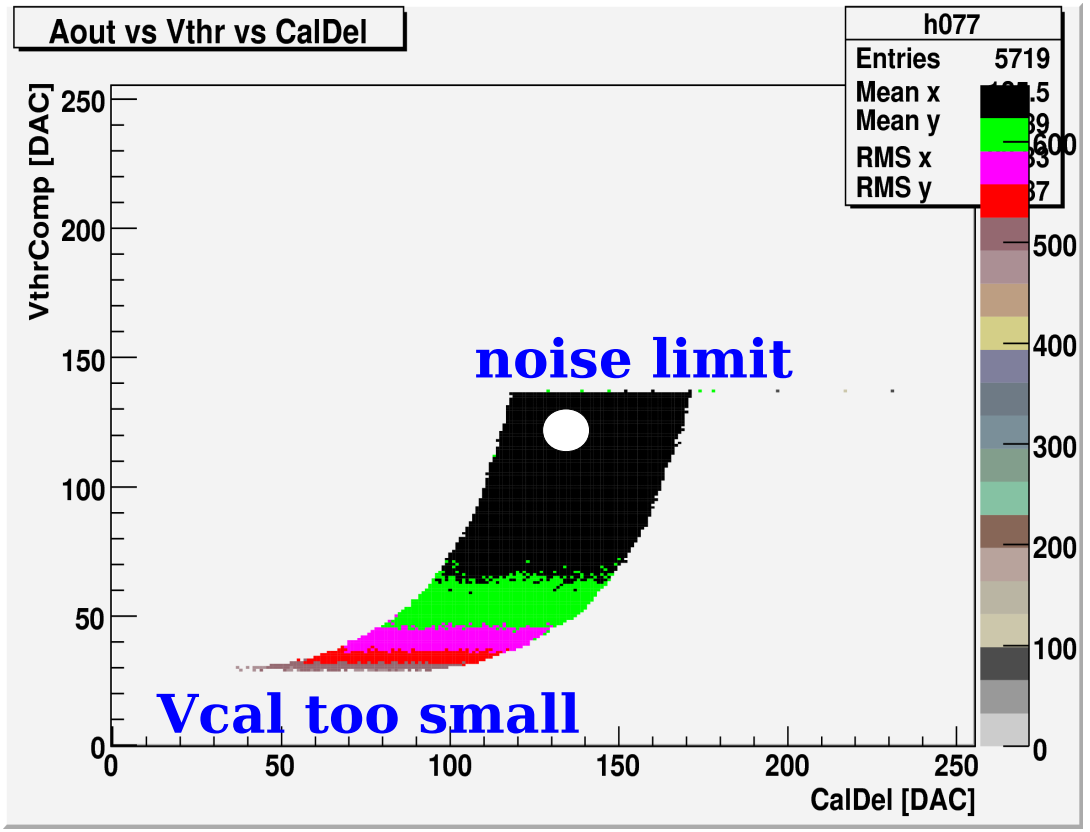
programmable register, per pixel

psi46 pixel readout chip

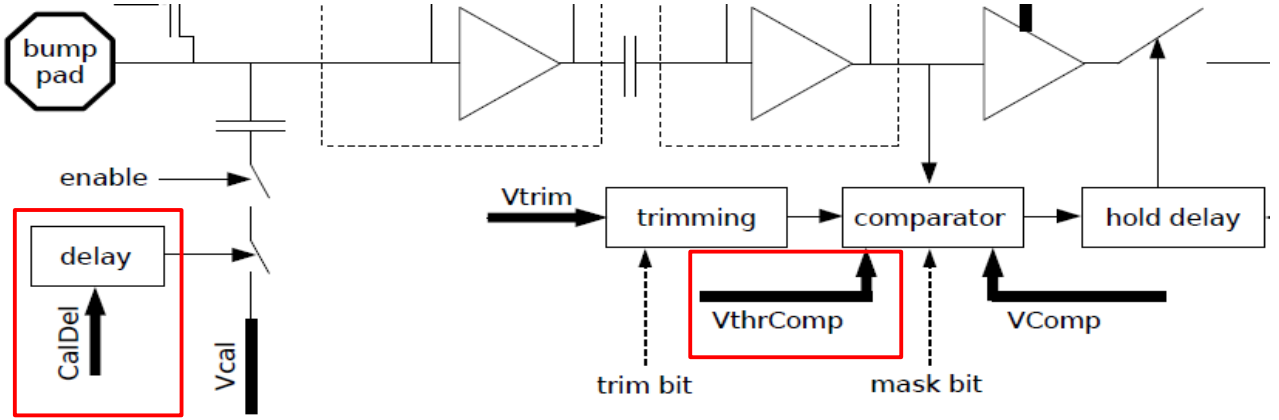


adjustable by programmable DAC

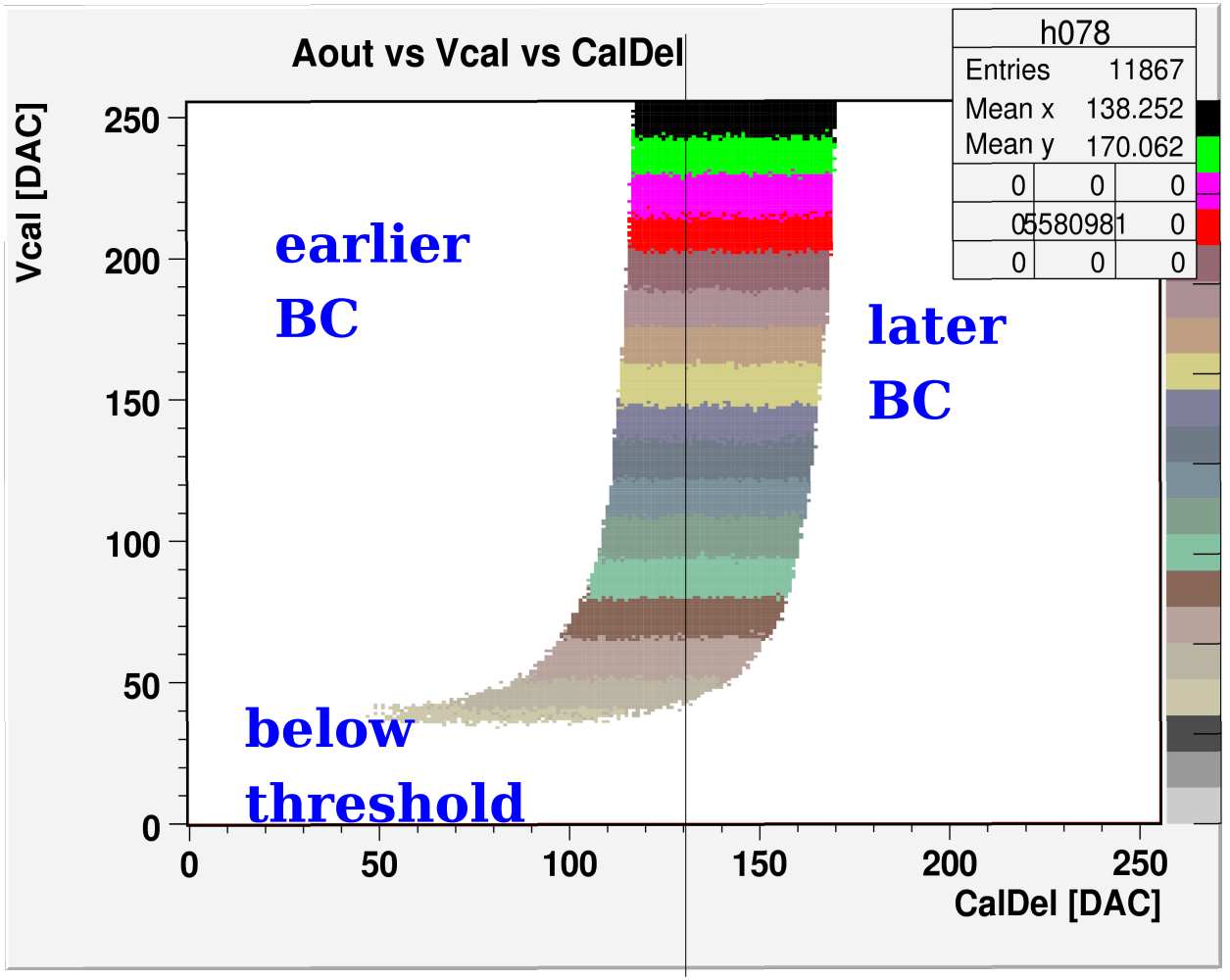
Working point in VthrComp – CalDel space

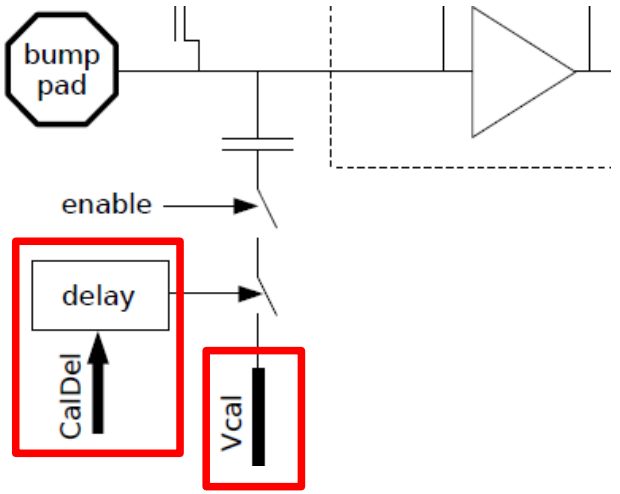


- Send calibrate signals for each pair of VthrComp-CalDel and count number of readouts.
- PSI: used values lie as far away as possible from the edges.
- DESY: working point moved to the top close to noise limit: VthrComp=125.



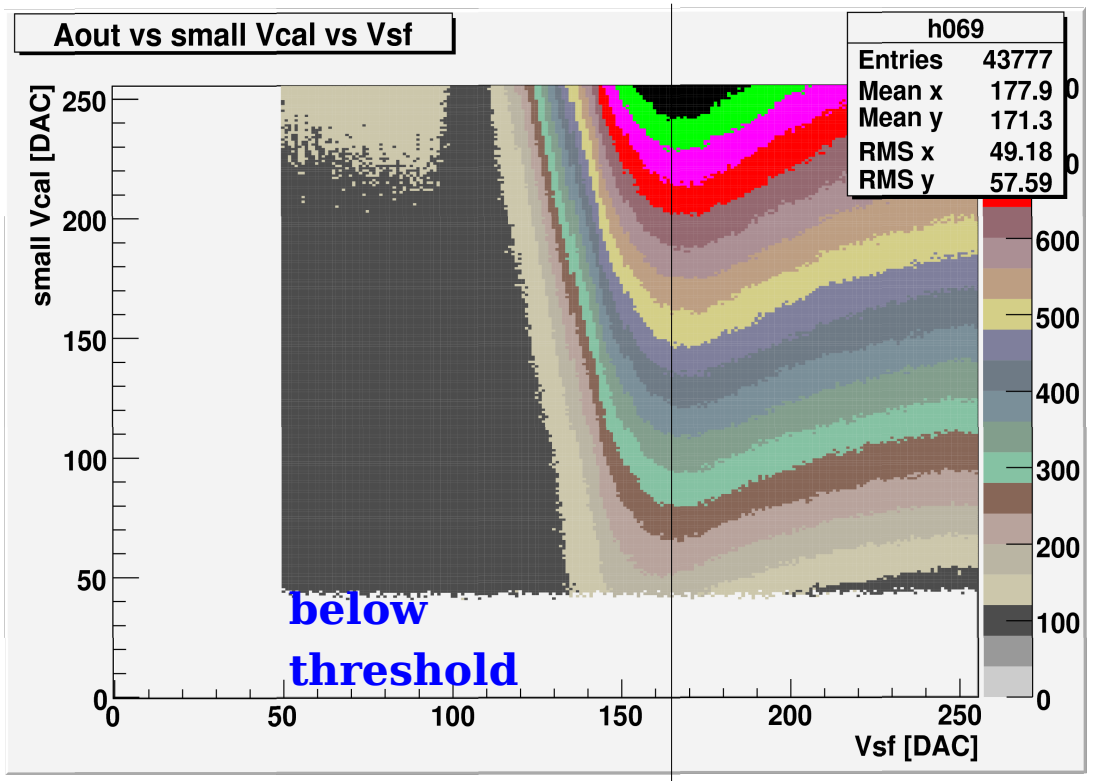
Calibrate timing



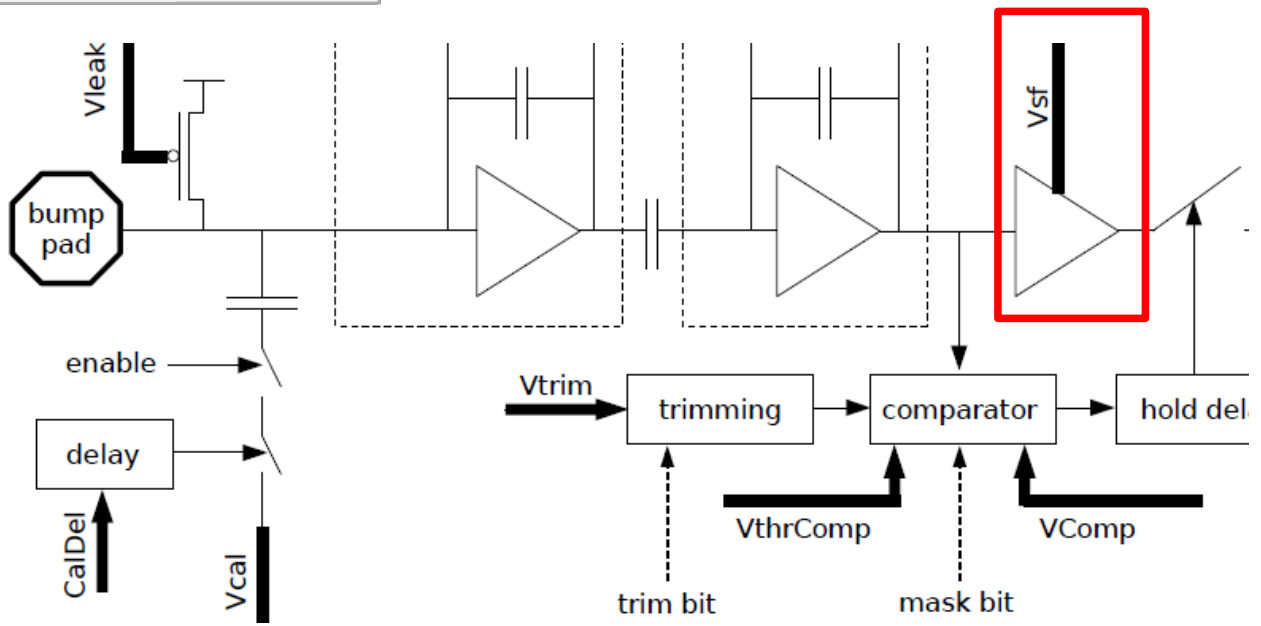


- Window is 1 BC wide.
- We choose 130 for CalDel (delay of internal calibrate signal to trigger).
- Fixed VthrComp=optimal

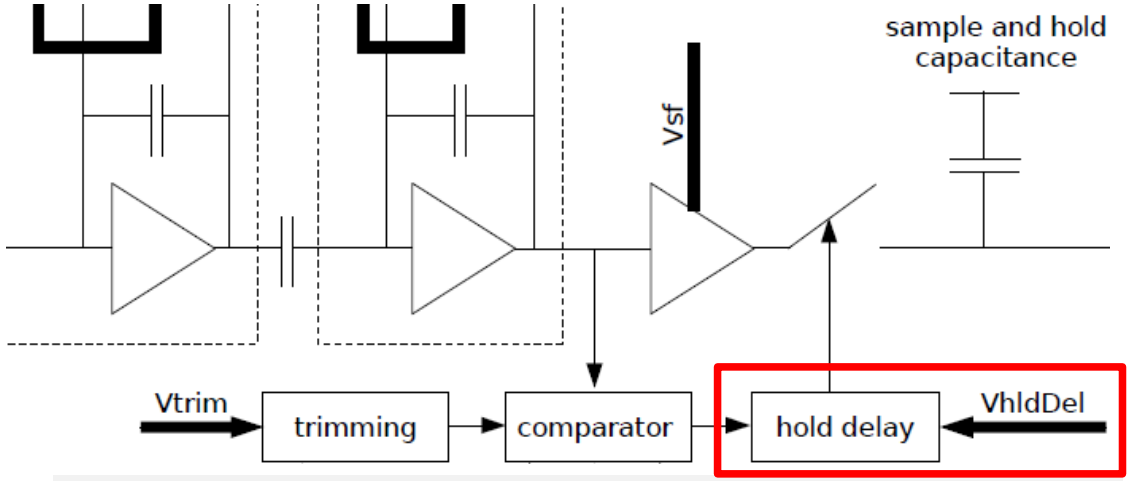
Linear range vs Vsf

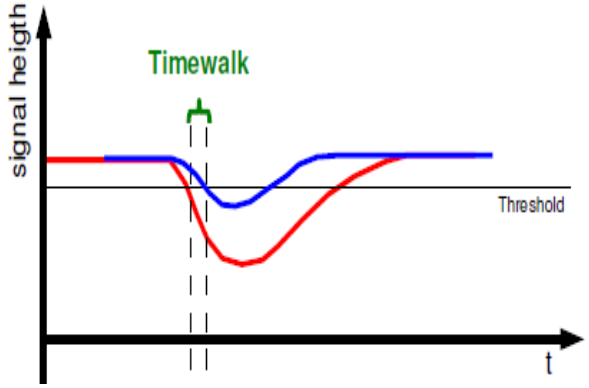


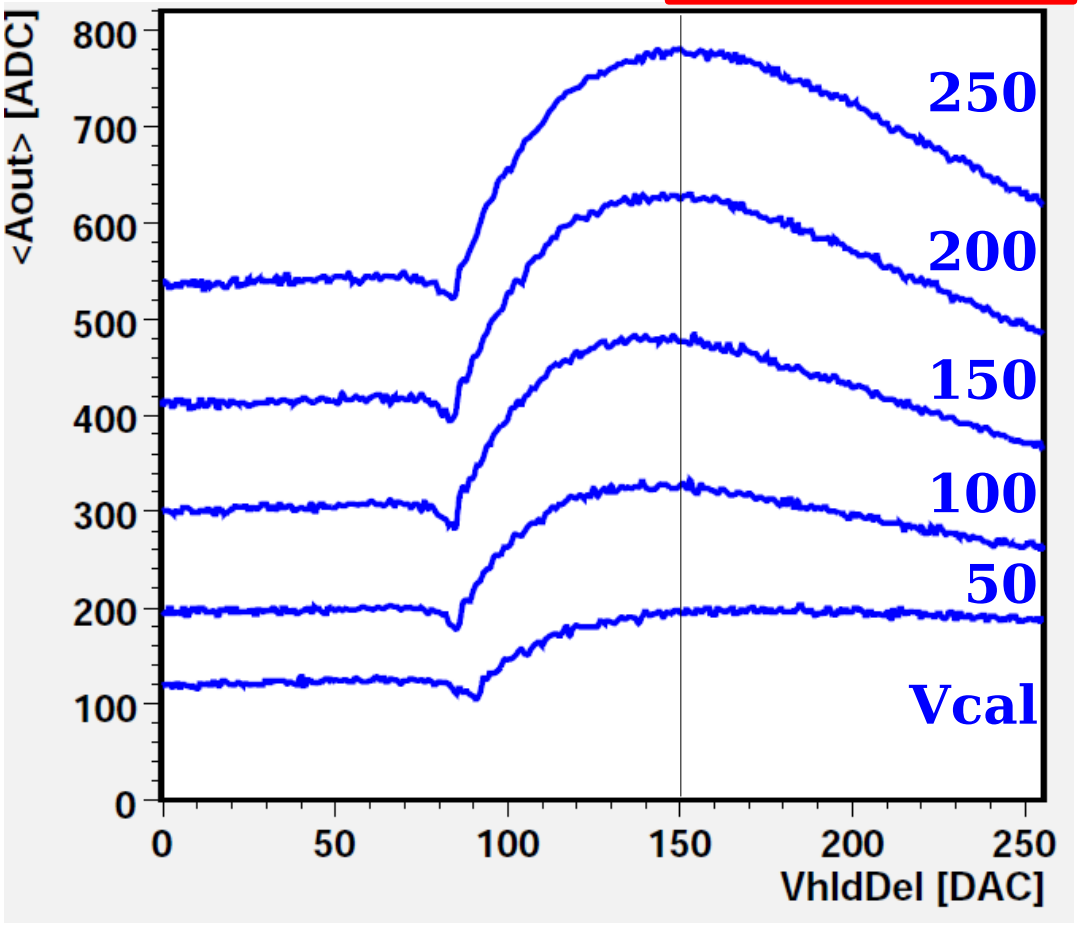
- Analog pulse height vs calibrate amplitude and source follower voltage.
- Crucial DAC to get a linear behavior of the pulse height – important for spatial resolution using charge sharing.



Sample and hold timing

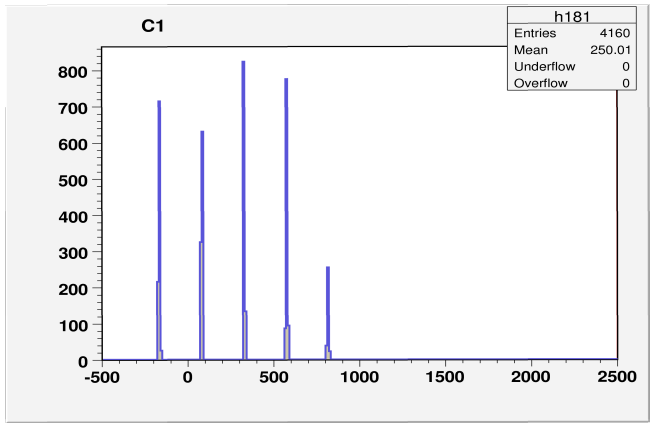


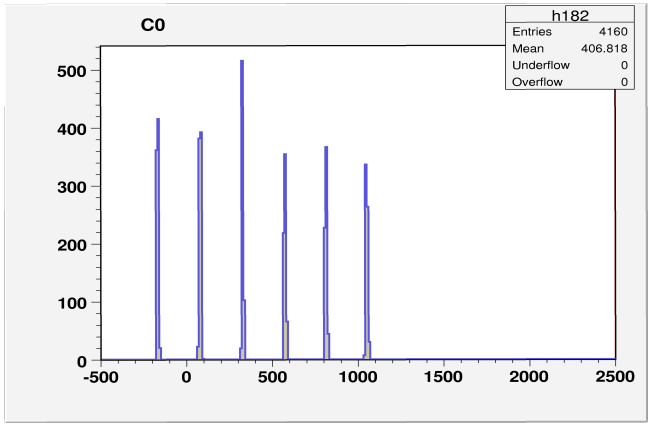




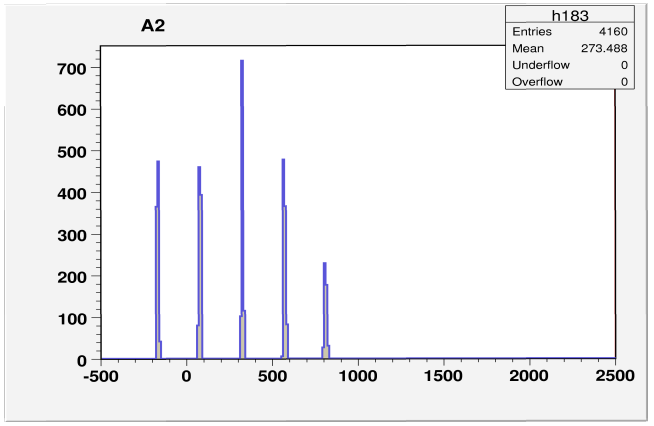
- Position of maximum depends on pulse height (Aout):
  - bigger PH signal cross threshold earlier (time walk).
- DAC 150 is compromise

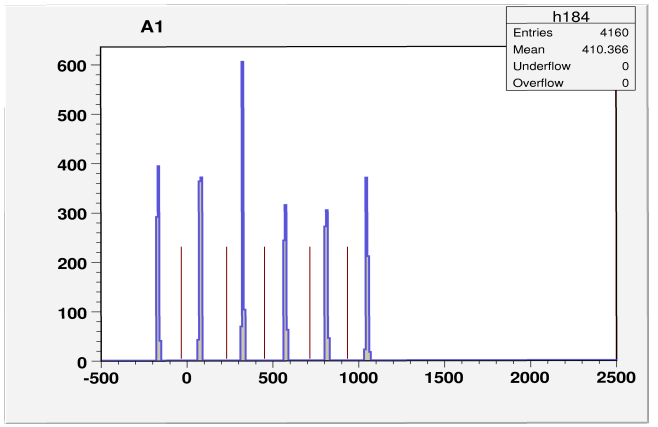
Pixel address

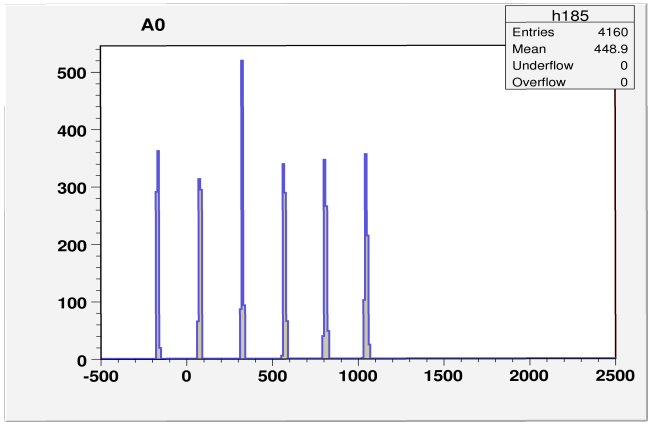




Pixel address in 5 signals:
C1,C0 d-columns 0..25
A2, A1, A0 rows 0..79
each with 6 analog levels.
All well separated.
Decode → col, row.

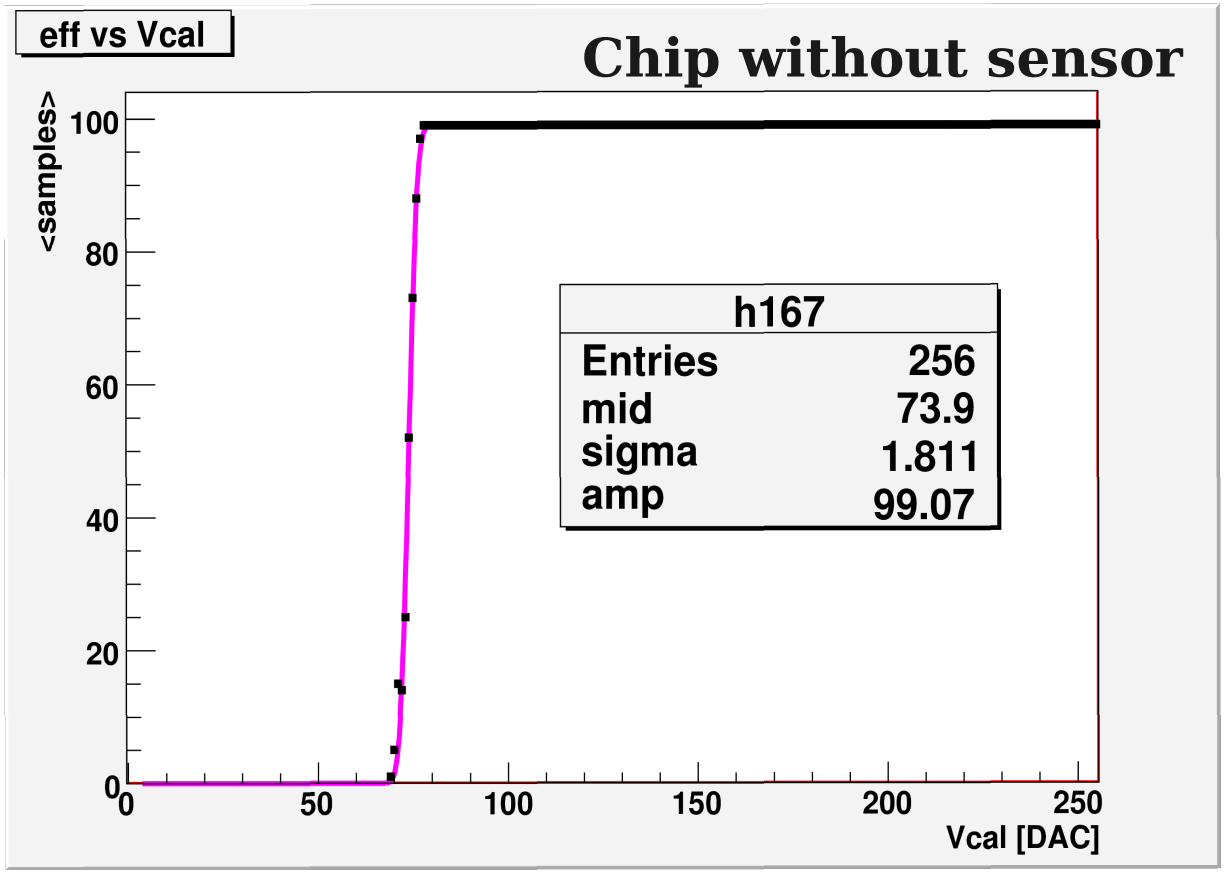






Decoding limits are placed in the centers between two neighboring peaks

Threshold curve



- S-curve: pixel eff. vs amplitude of calib. signal
- Fixed threshold
- Scan Vcal
  - 99 times
- count valid readouts
- threshold curve fit:
  - error function
    - width = noise
    - noise = 1.8 DAC
    - = 117 electrons.
  - fitting procedure developed at DESY

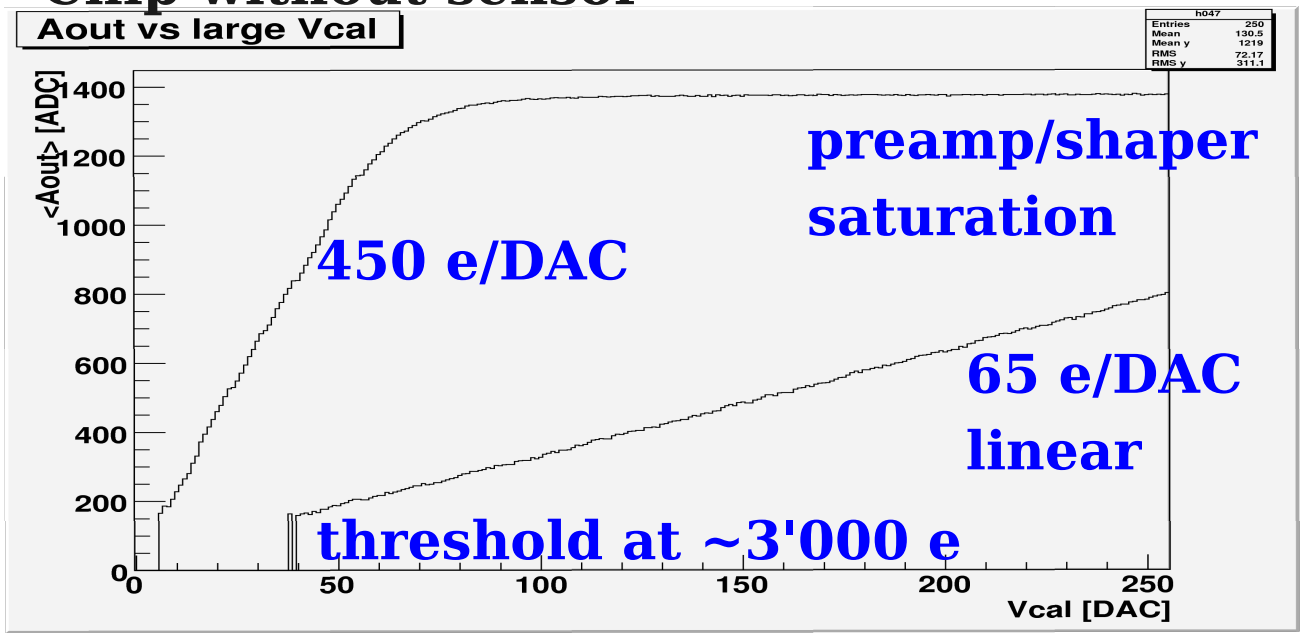
DACs for different chips

chip	Vsf	VhldDel	VthrComp	Vcal	CalDel
0	165	150	124	200	130
1	156	150	120	235	150
2	170	150	130	220	140
3	160	150	124	210	135
4	150	130	120	190	140
5	145	140	120	215	140
6 sensor	140	140	110	215	140
7 sensor	140	150	100	215	140
8 sensor	155	145	100	215	125

Test chips with sensor

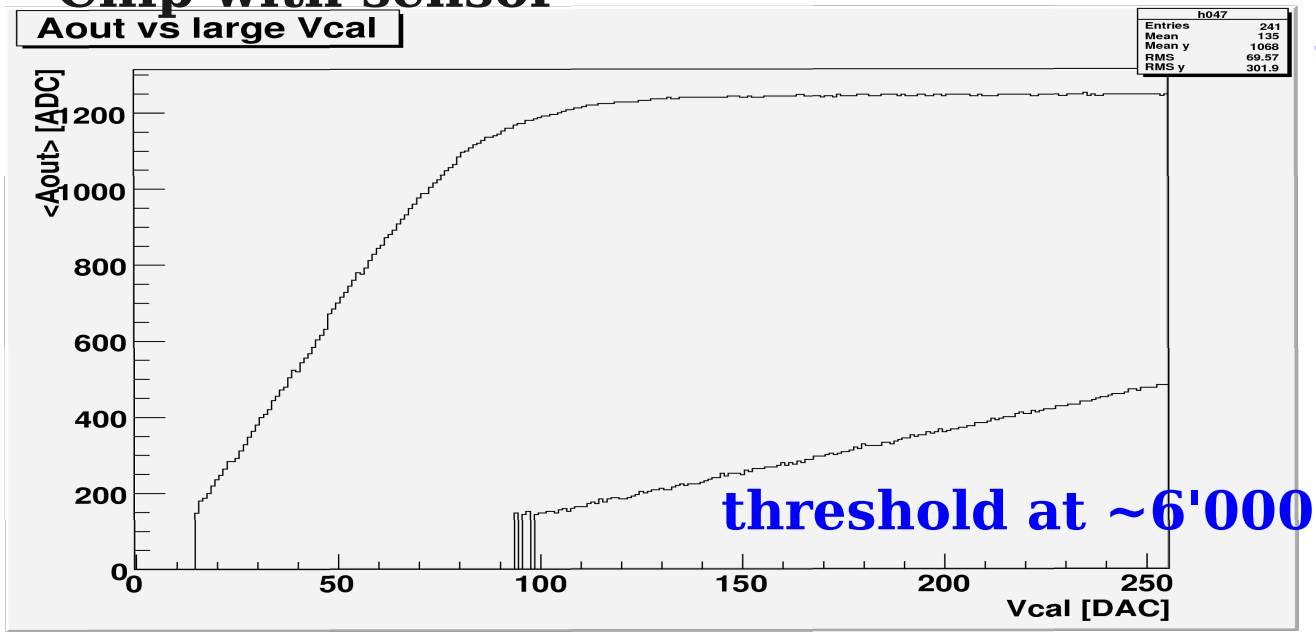
Gain and linear range

Chip without sensor



- Analog PH vs calibrate amplitude.
- 2 Vcal ranges (PSI X-ray calibration):
  - CtrlReg 0 or 4,
  - 65±5 e/DAC,
  - 450 e/DAC.

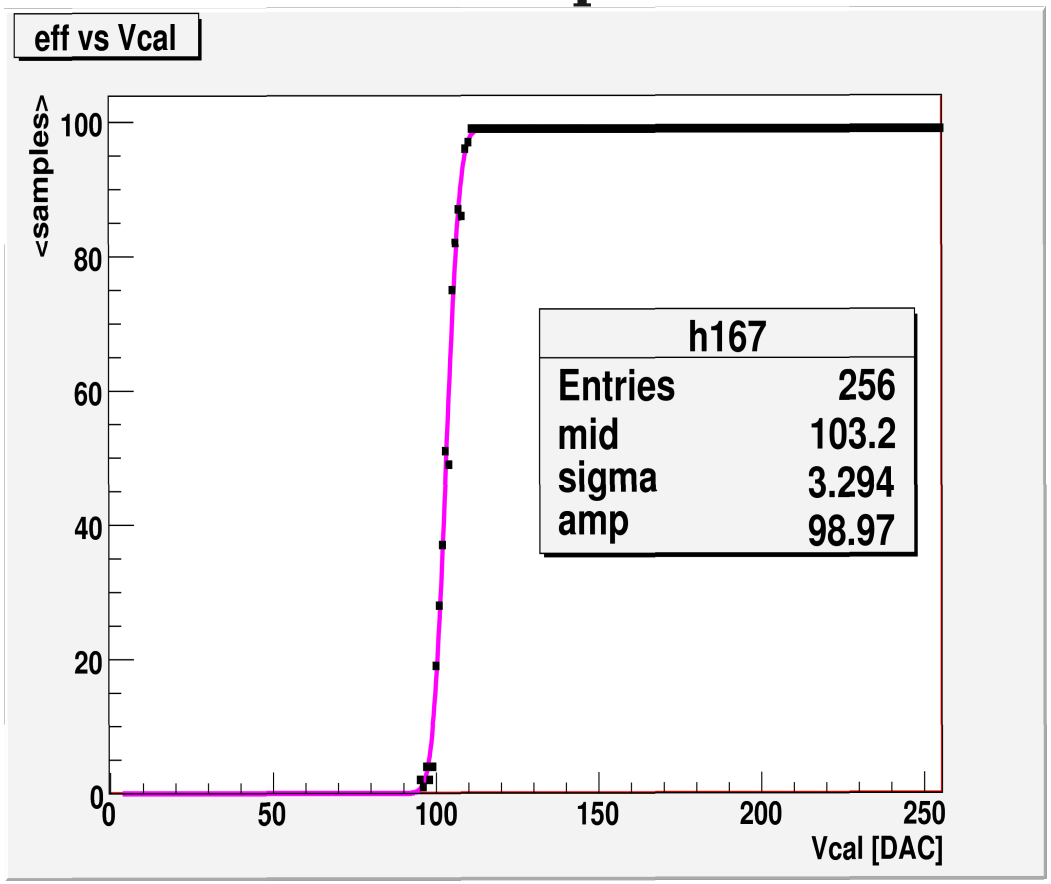
Chip with sensor



- Saturation around 36.000 e (No sensor) and 54.000 e (with sensor)

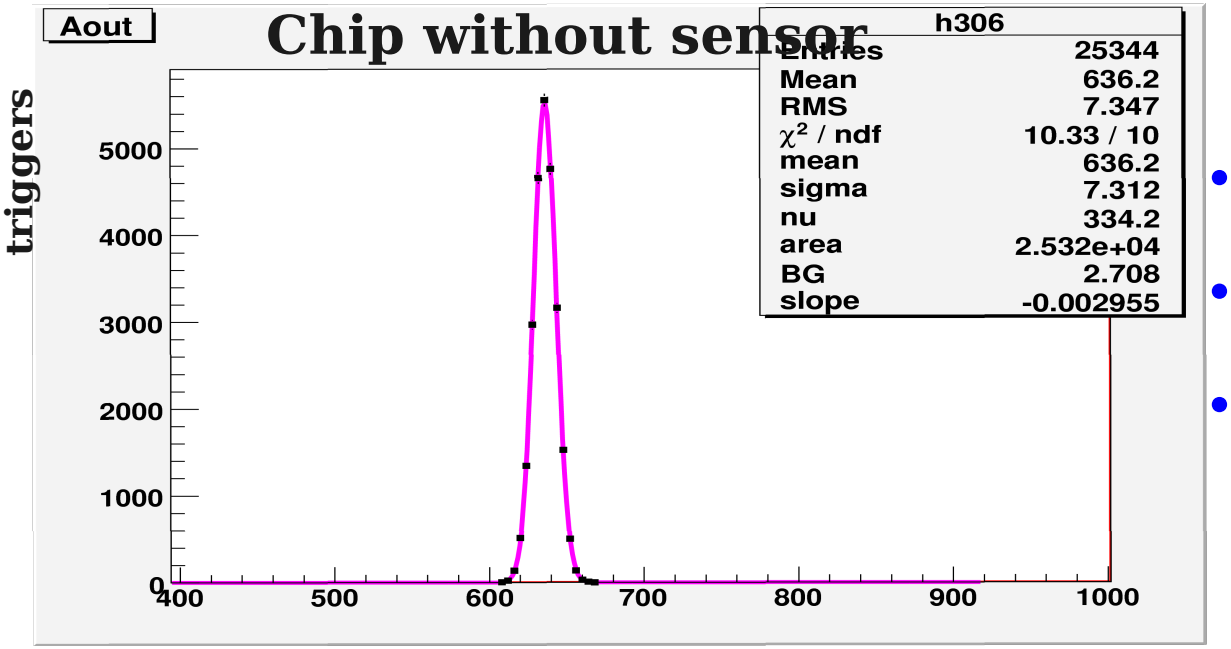
Noise scan

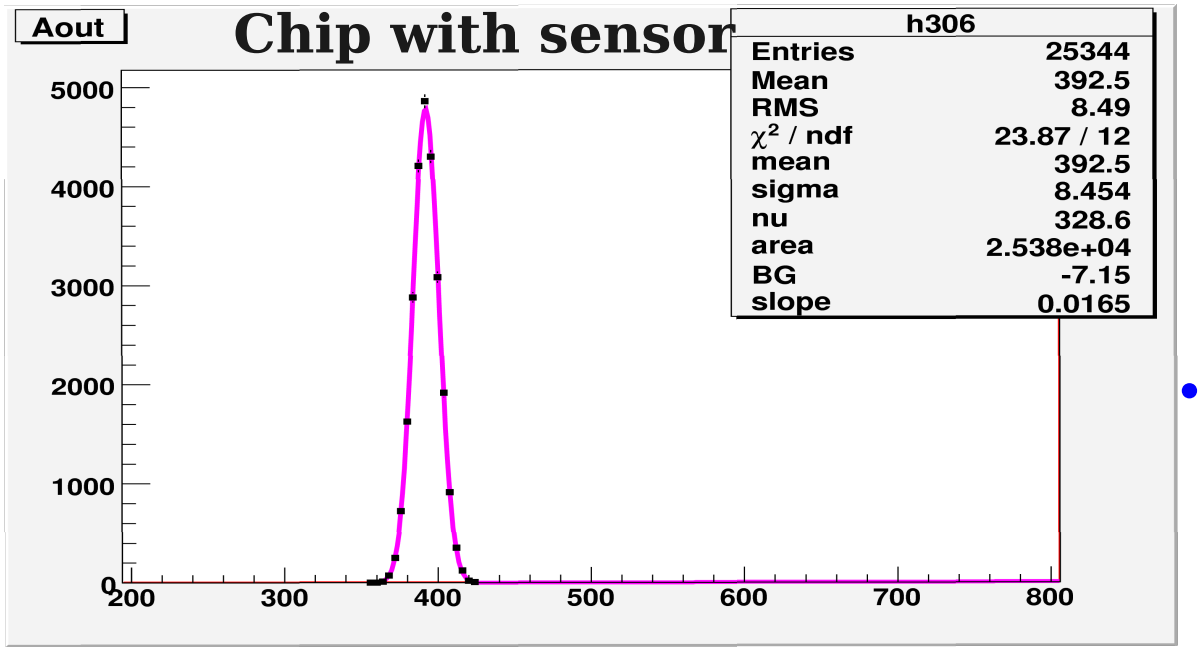
Chip with sensor



- Average noise:
  - no sensor – 111 e^-
  - Sensor – 224 e^-
  - PSI ~ 190 e^- (C. Eggel)
- Difference (max) in noise levels:
  - between measurements in one pixel:
    - no sensor – 10 e^-
    - sensor – 21 e^-
  - from pixel to pixel:
    - no sensor – 19 e^-
    - sensor – 21 e^-
  - from chip to chip:
    - no sensor – 16 e^-
    - sensor - 58 e^-
- PSI precision – 13-20 e^- (P. Trüb)

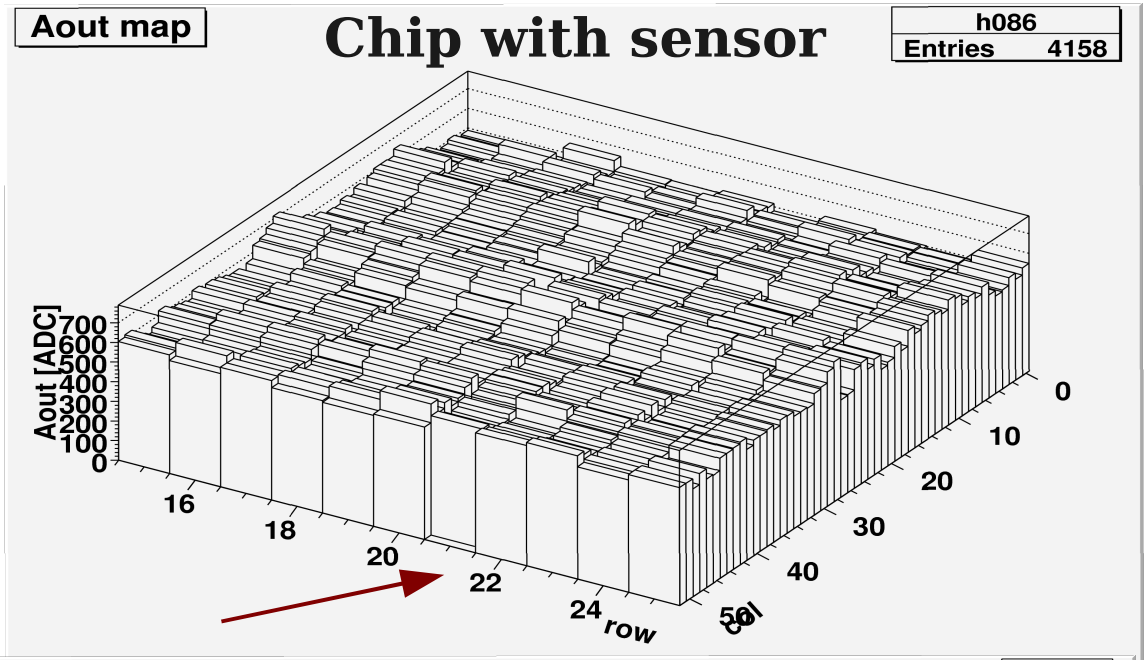
Pixel with test pulse

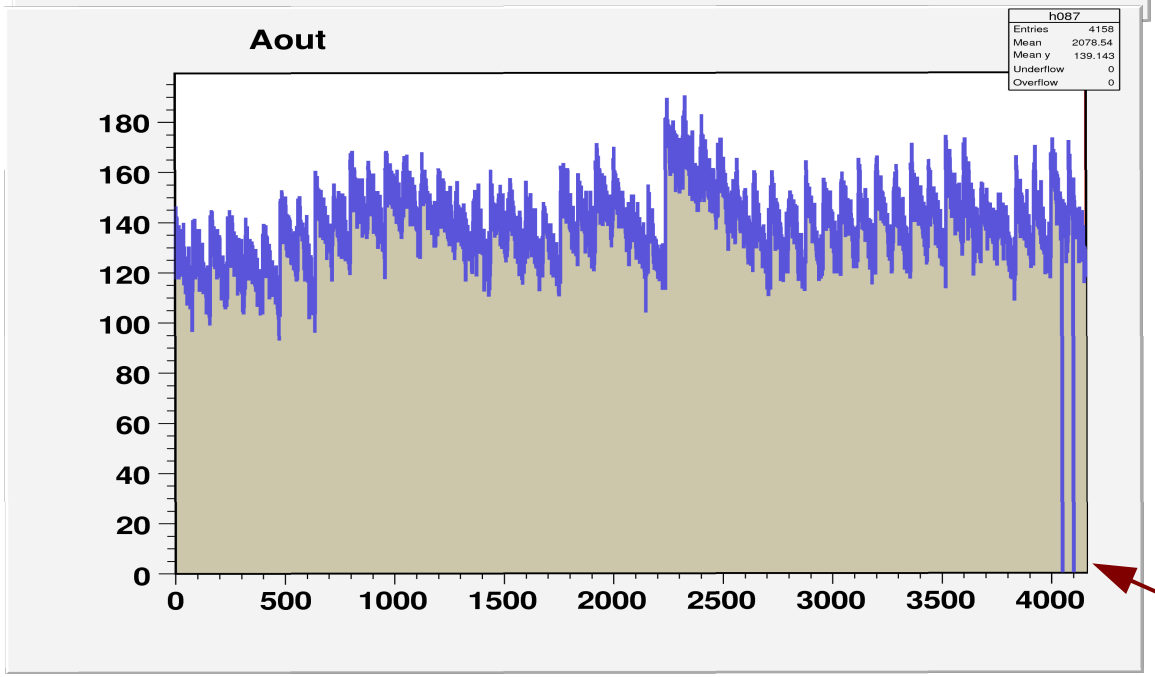




- One pixel active
- № of triggers vs analog PH
- Width = 7-8 ADC counts:
  - noise=65xσ[Aout]xVcal/Aout
  - noise=149 e (no sensor)
  - noise=298 e (sensor)
  - thermal noise,
  - perfect Gaussians
- Noise level is a little bit higher than in noise scan

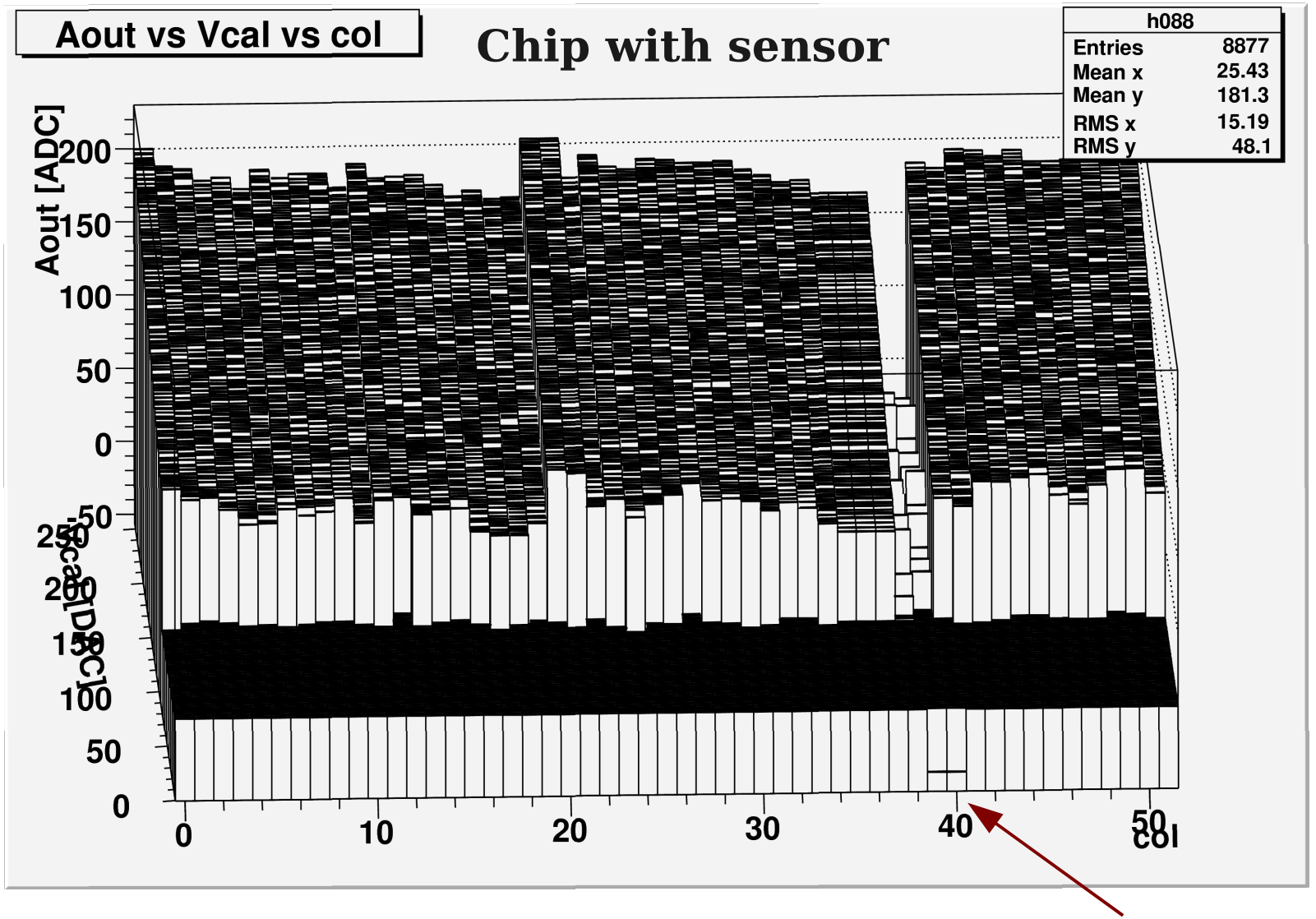
Pixel map





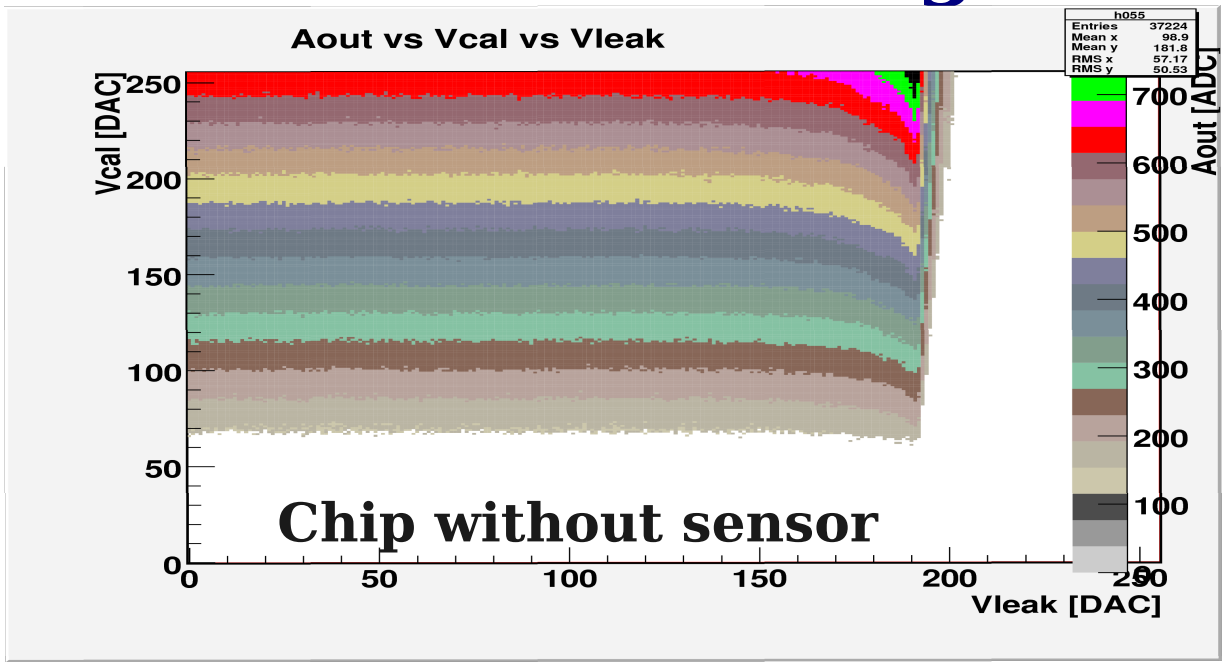
- 52 × 80 = 4160 pixels per chip.
- Vcal = 215 DAC
- VthrComp = 110
- Pixels with low gain are found

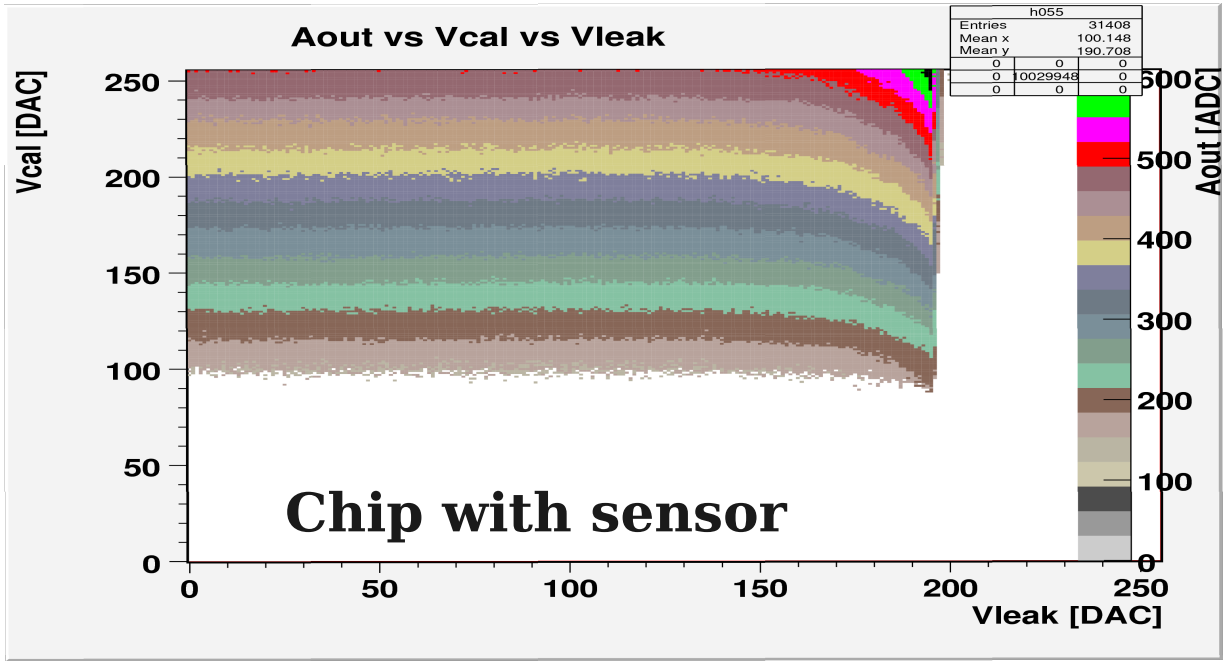
Pixel column map



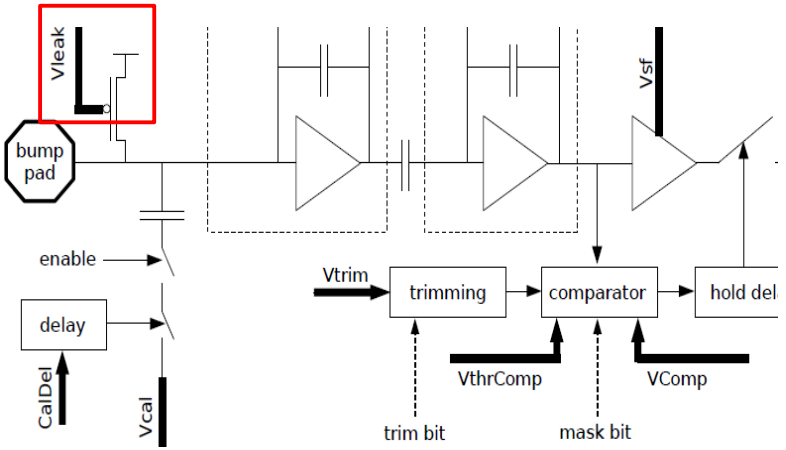
Analog PH vs calibrate amplitude and columns: 2 columns with low gain

Leakage current





- PH vs calibrate amplitude and Leakage current compensation.
- Vleak DAC controls a circuit, which can compensate for leakage current in sensor during irradiation.
- Comparable values of Vleak are observed.



Summary

- Chip test procedure is continued
- Progress in understanding the psi46 readout chip with sensor:
  - operation range explored: timing, thresholds, voltages.
  - several results are similar to PSI measurements.
  - working point established, may need fine tuning.
- Variations from chip to chip (different DAC settings, different noise)
  - Started with automated procedures for finding a working point.
- Problems: one chip with sensor has no address separation – under investigation.
- Further:
  - Visit to PSI, June 8-10

Back up