Updates on Spatial & Temporal Resolution of dSiPM

Exploring the Potential of CMOS SPAD Arrays

Inge Diehl, Finn Feindt, Ingrid-Maria Gregor, Karsten Hansen, Stephan Lachnit, Daniil Rastorguev, Simon Spannagel, Tomas Vanat, **Gianpiero Vignola**

SiDet R&D Meeting, 23 April 2024

Outline

- **Introduction**
- **DESY dSiPM**
- **DESY II Testbeam Setup**
- **Spatial and Timing performance of bare prototypes**
- **Spatial and Timing performance of dSiPM + thin LYSO**
- **What next and Summary**

References:

SiDet 13-09-2022: G. Vignola Laboratory & test beam results of the DESY digital-SiPM prototype

SiDet 18-07-2023: I. Diehl, Time-to-digital converter (TDC) in CMOS technology - overview and design example

I. Diehl et al, Monolithic MHz-frame rate digital SiPM-IC with sub-100 ps precision and 70 µm pixel pitch

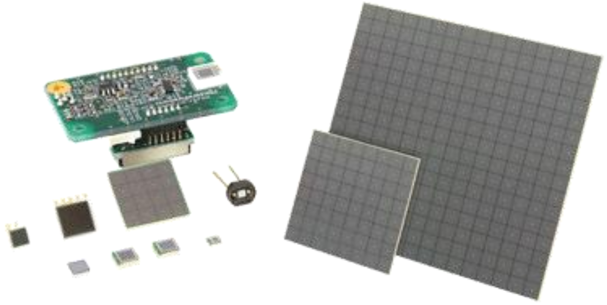
S.Lachnit, Time Resolution of a Fully-Integrated Digital Silicon Photo-Multiplier

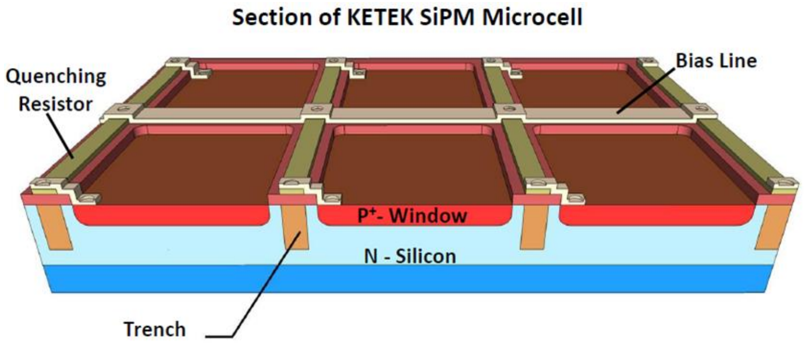
F.Feindt et al, The DESY digital silicon photomultiplier: Device characteristics and first test-beam results

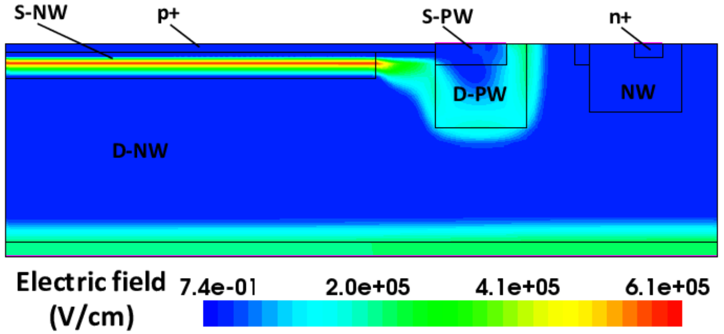
What is a Silicon photomultiplier

State of art in Single Photon detection

- Array of SPAD with pitches in the range **10-100 µm**
- **High Internal Gain** thanks to High doped amplification region
- Signal proportional to **number of photons** that hit the sensor
- **High quantum efficency**
- **Low power comsumption**
- **Insensitive to magnetic fields**







http://dx.doi.org/10.1109/JSEN.2019.2916424

Why CMOS SiPM-IC?

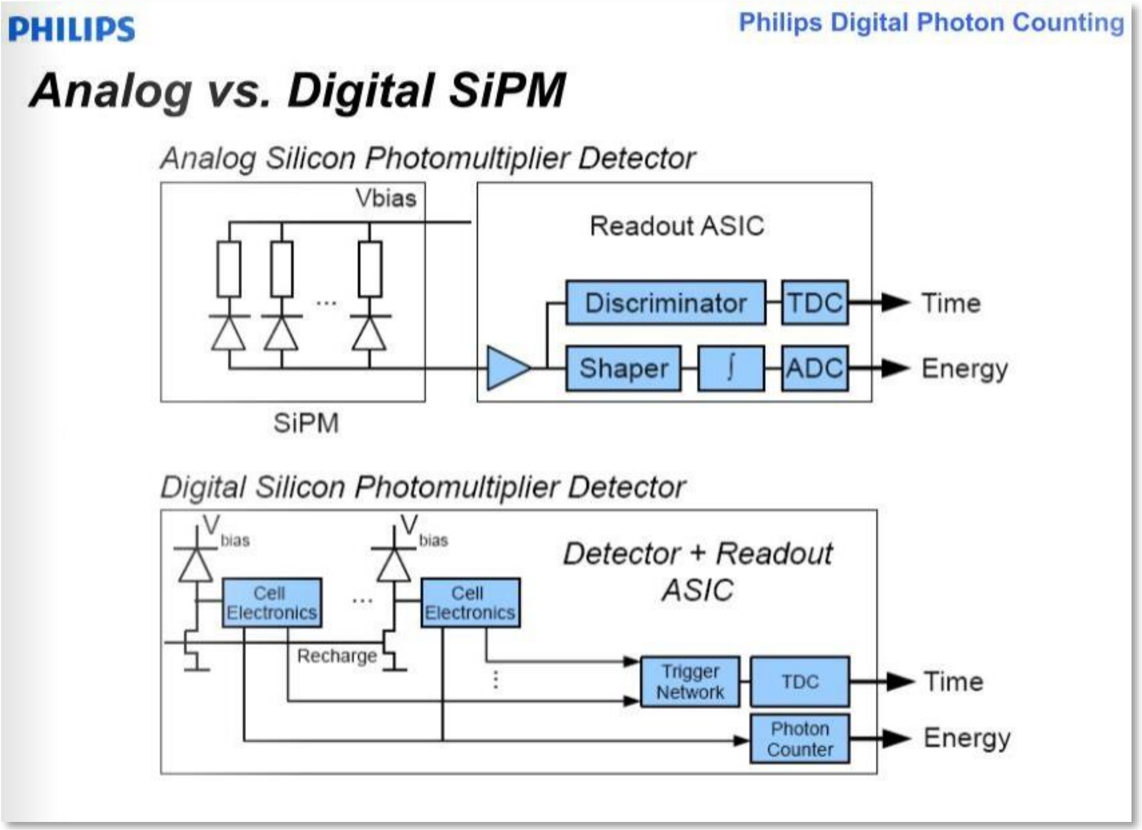
Vantages of Integrated Electronics

As an alternative to analog SiPM

- Reduce complexity of DAQ chain with CMOS electronics
- New in-chip features:
  - Noise suppression
  - Full hitmap readout
  - Photocounting
  - Trigger logic
  - Parameters tuning (e.g. quenching)
- Customized cost-effective solution

As candidate for new applications in HEP

- Multi optical-fiber readout
- 4D-Tracking of MIPs



https://www.yumpu.com/en/document/view/2279838/philips-digital-photon-counting-precision-muon-physics

DESY dSiPM Specifications

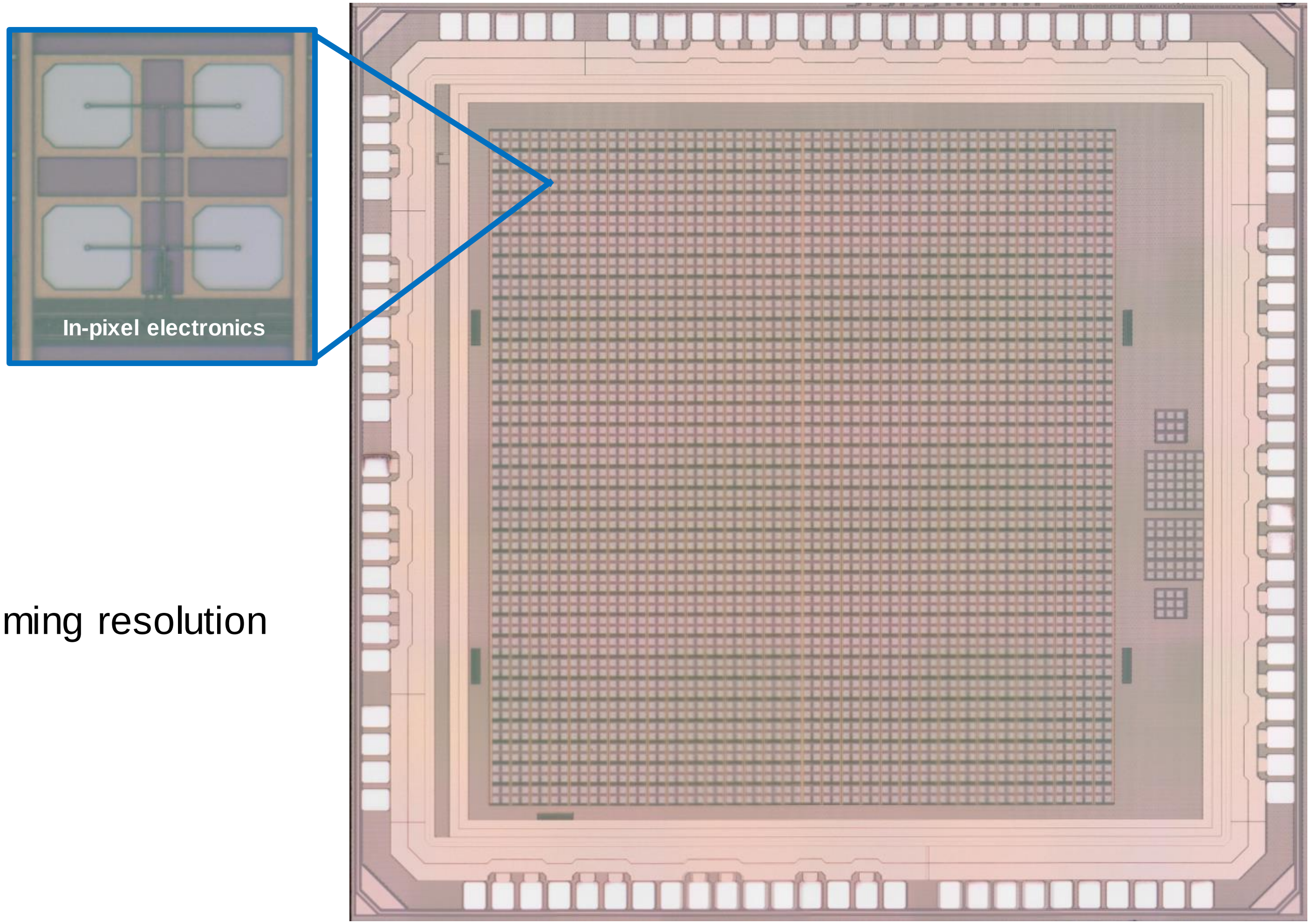
ASIC in LF 150 nm CMOS

Layout

- In LFoundry 150 nm CMOS technology
- Main matrix: 32 x 32 pixels (4 SPADs per pixel)
- Sensor area: 2.2 x 2.4 mm^2
- Test structures in the chip periphery

Features

- Full hit matrix readout and timing measurements
- 4 x 12-bit Time to Digital Converters with ~95 ps timing resolution
- Pixel masking
- In chip trigger logic
- 2-bit in-pixel hit counting
- Readout is frame based (3 MHz frame rate)

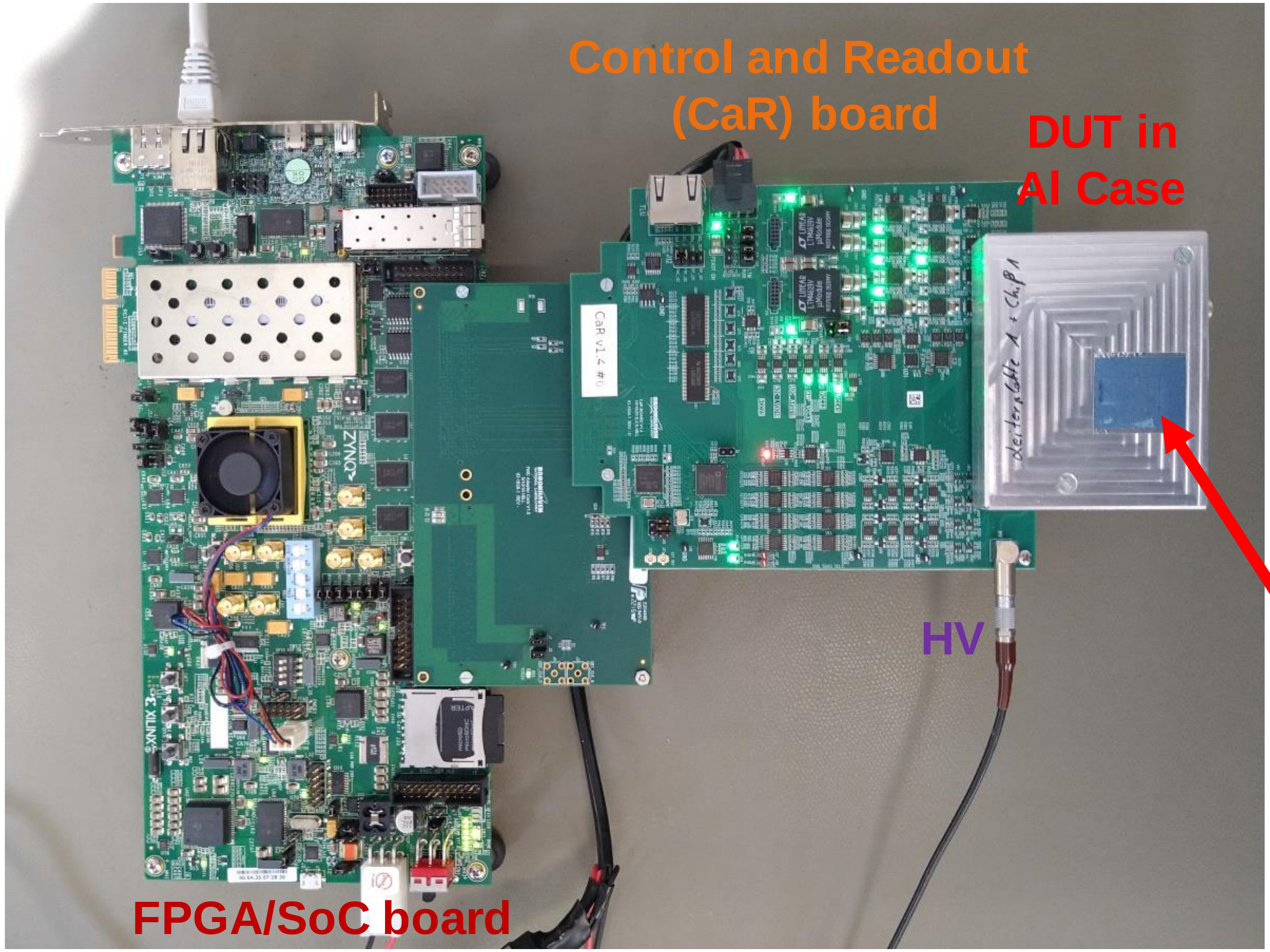


DESY dSiPM

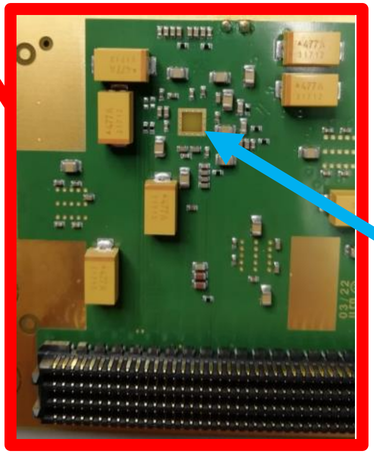
For details on ASIC see: [I. Diehl et al 2024 JINST 19 P01020]

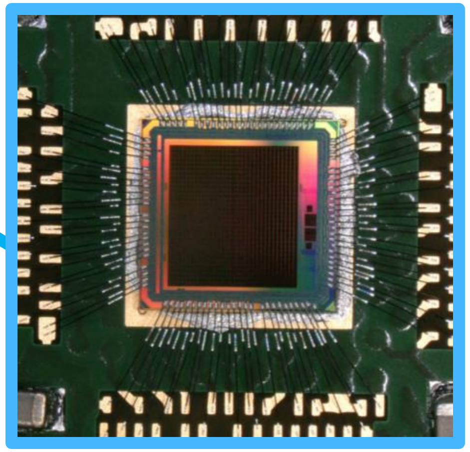
DAQ system

Caribou based



- DESY dSiPM uses the versatile **Caribou DAQ system**
- **Firmware & software** developed entirely at DESY
- The DUT is **glued & bonded** on the dedicated PCB
- The **Aluminium case** acts as a **heat sink** and protects the SiPM from external light sources
- **Holes and windows** have been designed to reduce the material budget (TB studies)

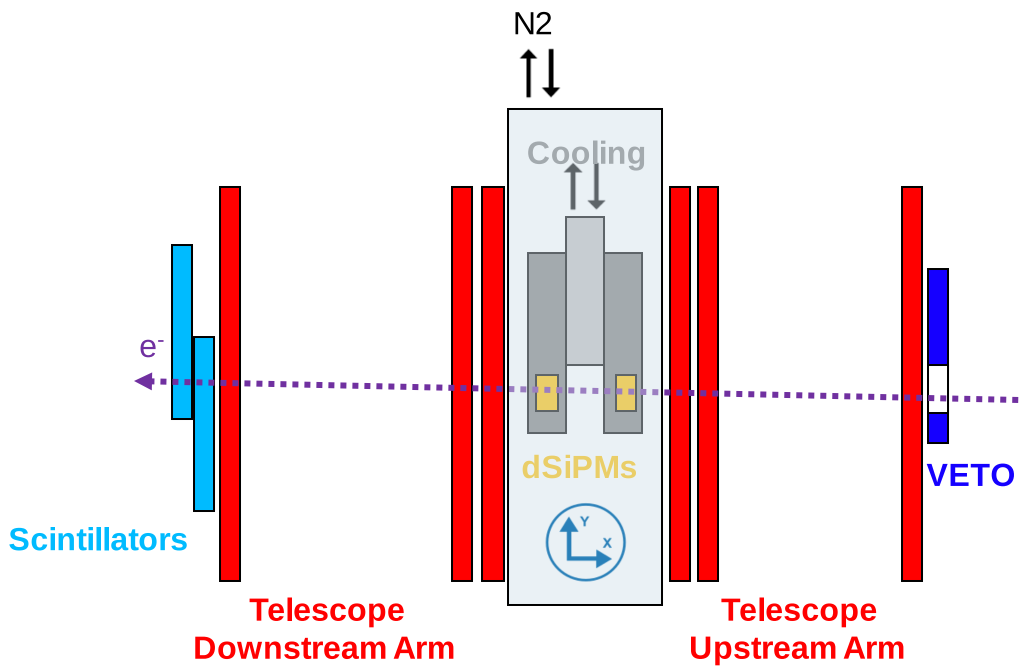




DSiPM in MIP detection

DESY II Test Beam Setup

March 2023 & February 2024



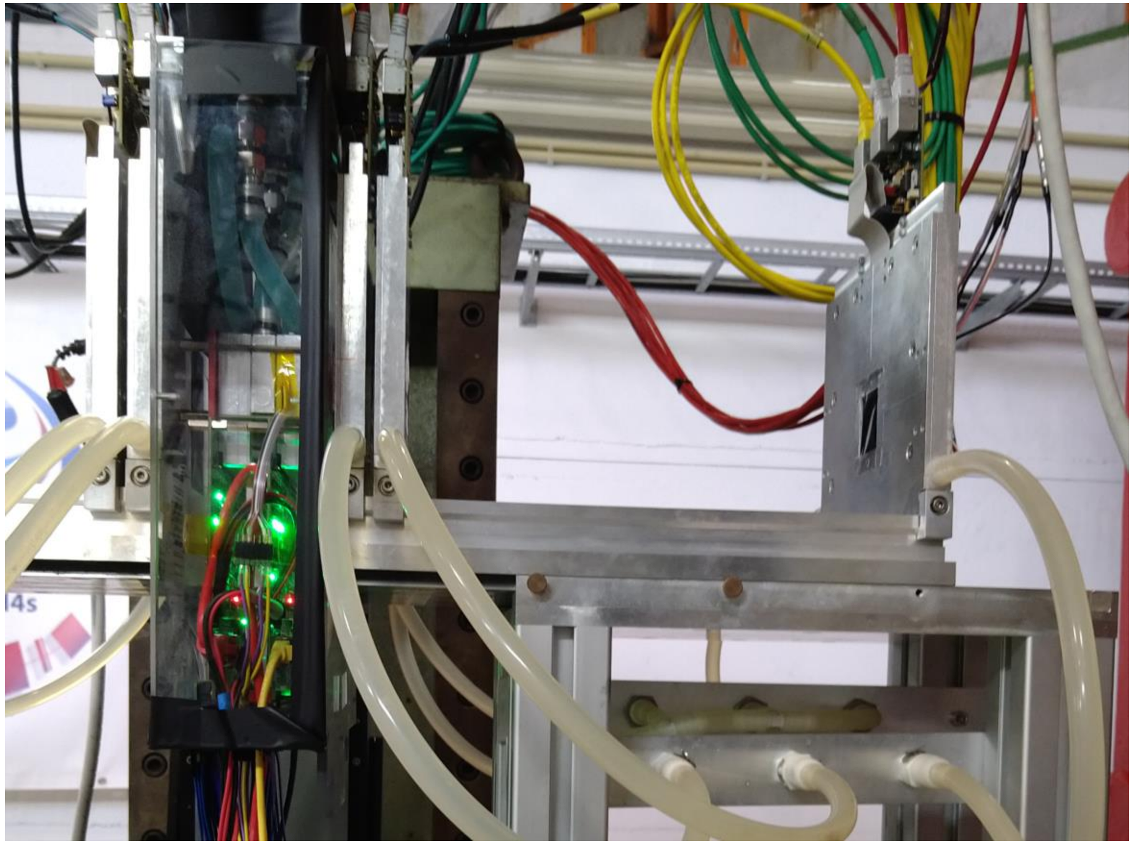
Beam momentum used: ~ 2-5 GeV/c

Synchronization: Trigger Logic Unit (TLU) and EUDAQ2

Active cooling: Stable DUT temperature down to 0 °C

Beam telescopes:

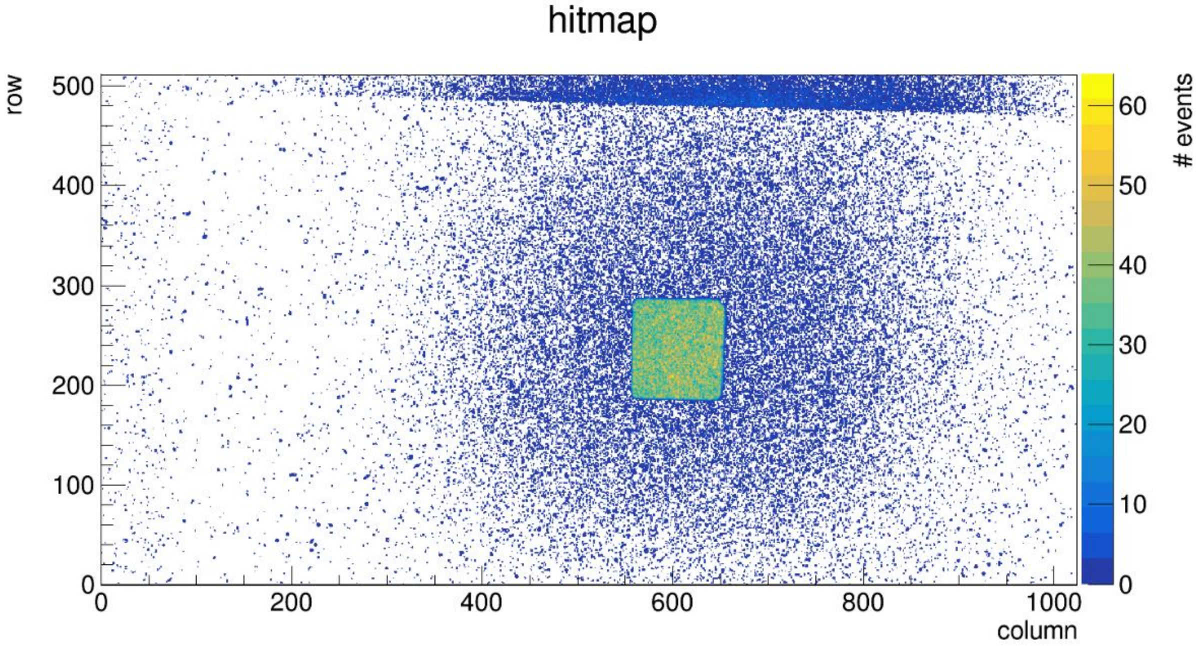
March 2023: EUDET type telescope with Mimosa26
February 2024: ADENIUM telescope with ALPIDE

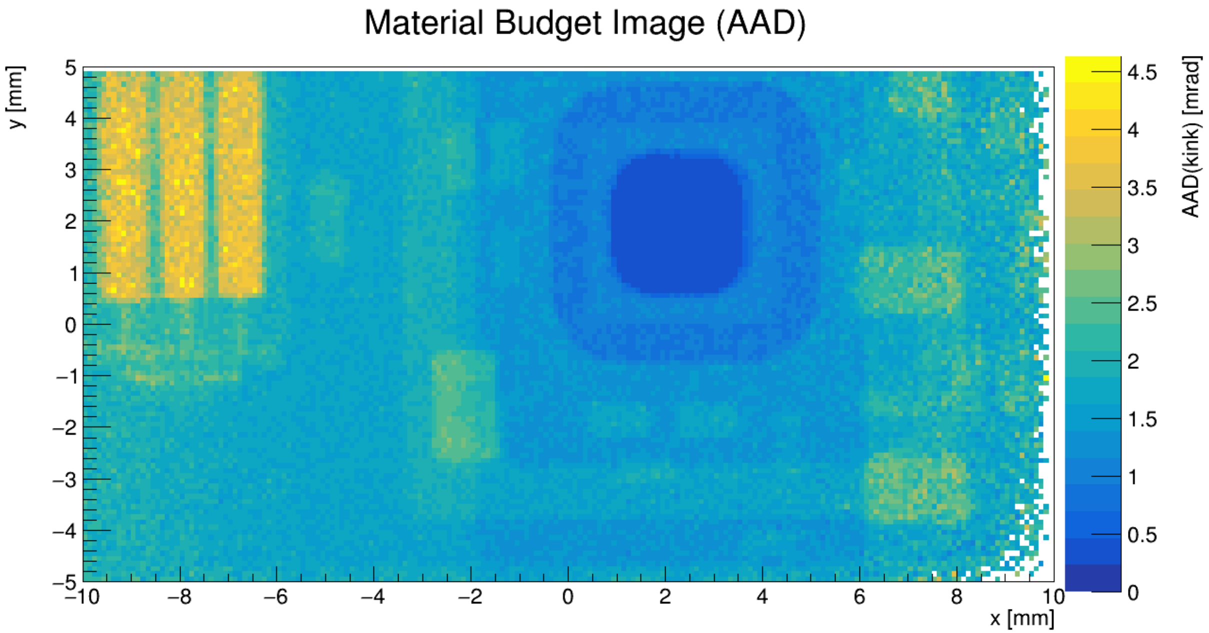


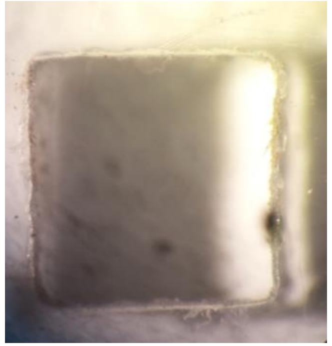
dSiPM testbeam setup March 2023

DESY II Test Beam Setup

MBI for Alignment to the VETO Area

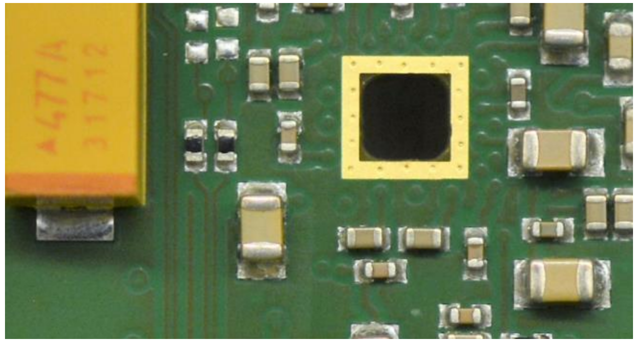






Plastic scintillator with a hole used as VETO for Trigger

- Anticoincidence with other scintillators
- Trigger only in a ROI slightly larger than DUT
- Allows to save disk space and maximize yeld



Material budget image for DUT alignment

Corryvreckan modules:

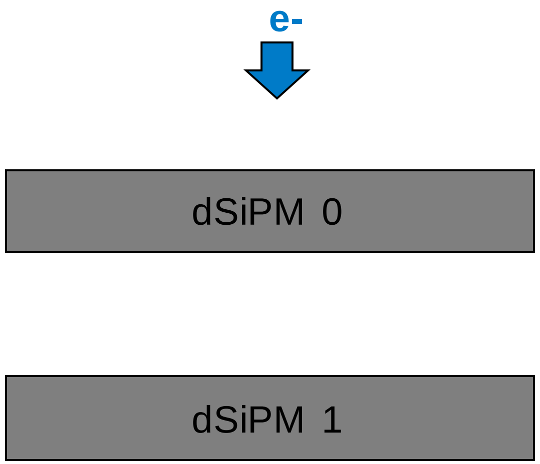
[TrackingMultiplets]

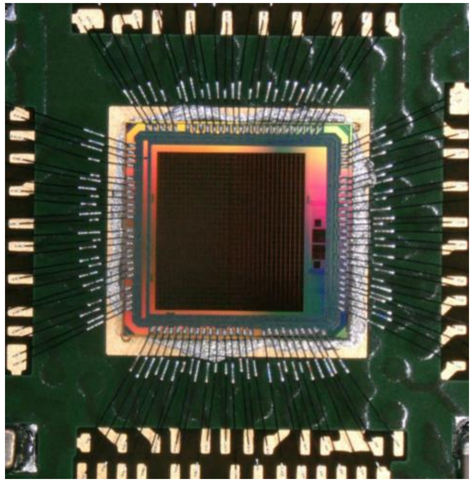
[AnalysisMaterialBudget]

Device Under Test

Bare Prototypes and Coupling with Thin LYSO

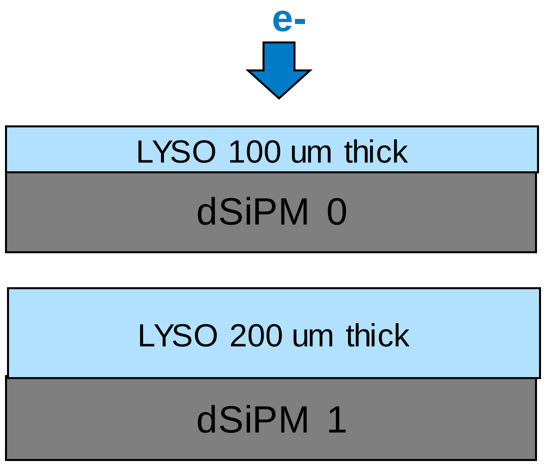
Testbeam March 2023

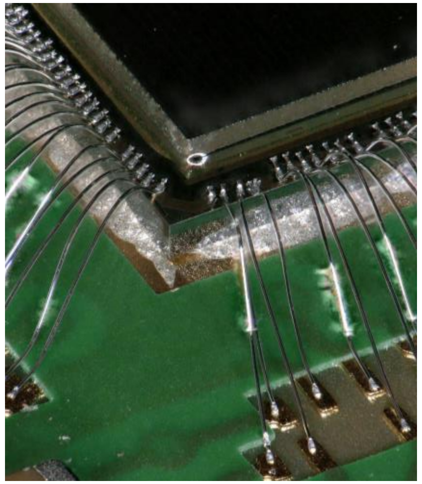




- 2DUT aligned with the trigger area
- **Only bare silicon** exposed (light shielded)
- Device treated as a MIP detector

Testbeam February 2024





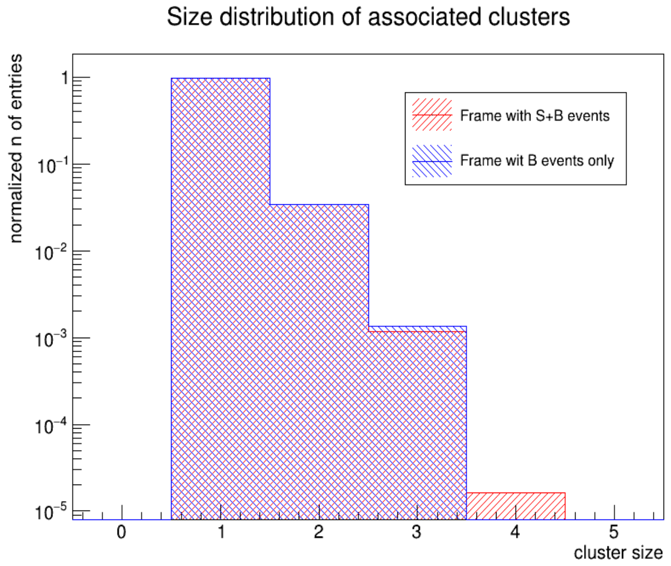
- 2DUT aligned with the trigger area
- **DSiPM coupled with thin LYSOs** (100 & 200 µm thick)
- Device treated as a MIP detector

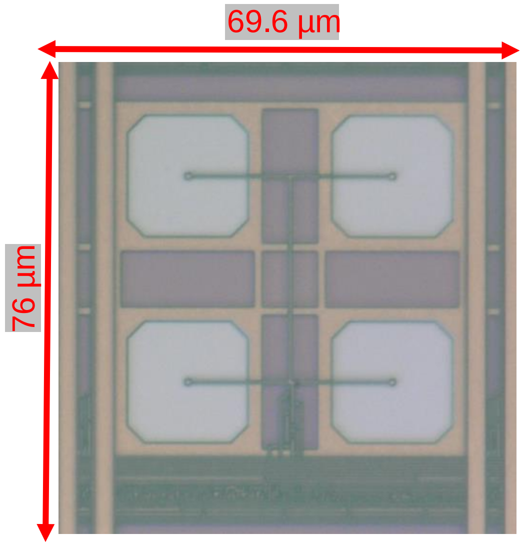
DESY dSiPM Spatial Resolution

In MIP Detection Using Bare Prototypes

Associated cluster size

- Mainly one, no visible charge sharing
- Large gap between pixels to avoid crosstalk
- Cluster size of MIP and noise event compatible

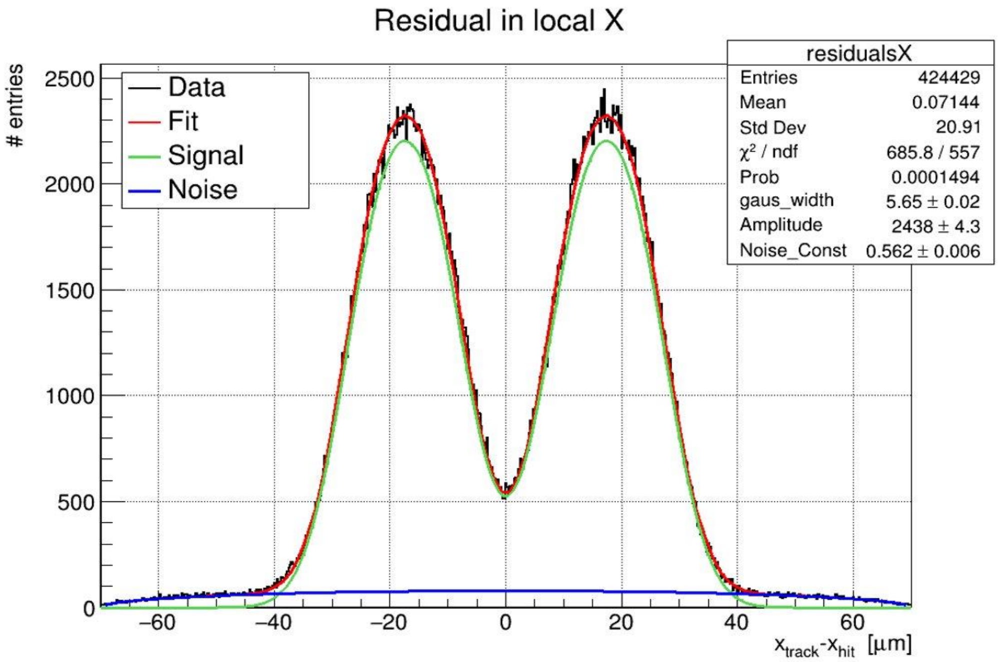




dSiPM pixel picture

Spatial residuals

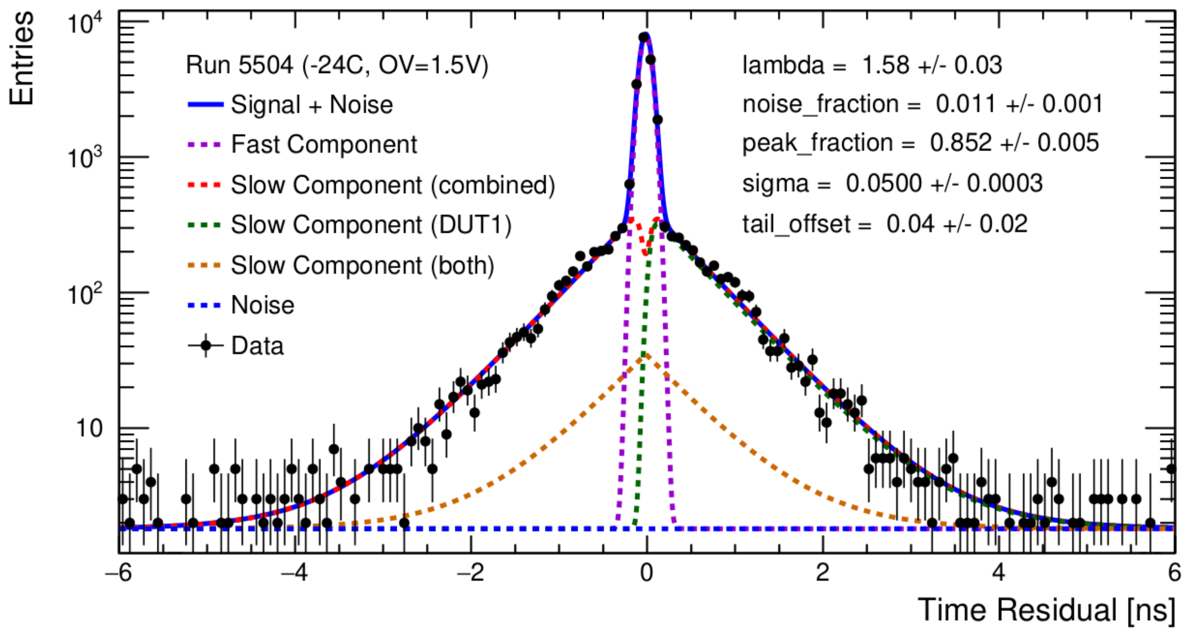
- Defined as the difference between cluster position in DUT and interpolated track in the same z-position
- Double peak structure (inefficiency in the pixel centre)
- Small noise contribution (in blue)
- Std Dev of signal **~20 µm** in x and y (dominated by DUT resolution)
- Spatial resolution compatible with pitch/sqrt(12) (~20 – 22 µm)



DESY dSiPM Timing Performances

In MIP Detection Using Bare Prototypes

@ Stephan L.

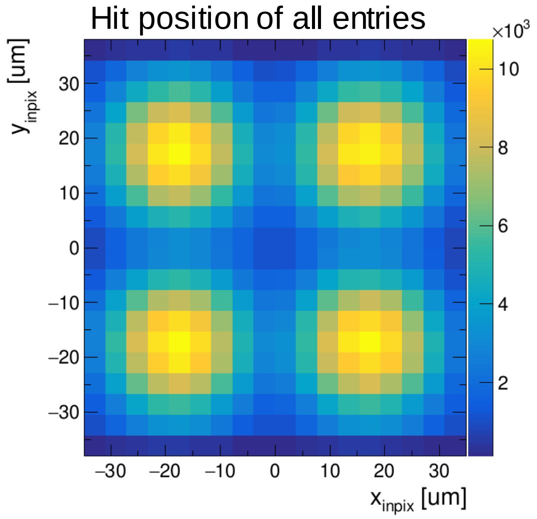


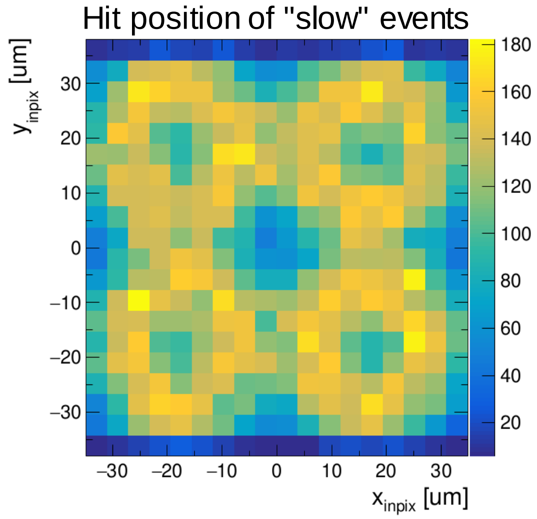
Time residuals

- Defined here as the difference between the DUTs timestamps (dSiPM1 – dSiPM2)
- Can be used to determine dSiPM + TDC time res.
- Time resolution measured: **46 ± 5 ps** (Fast Component)
- Limited mainly by TDC resolution (~95 ps)

Slow component

- Slower component only in the 15 % of the entries
- Visible as ns tails in time residuals
- Slow component correlated to SPAD periphery
- Probably due to MIP interaction in low E-field regions





DESY dSiPM Efficiency

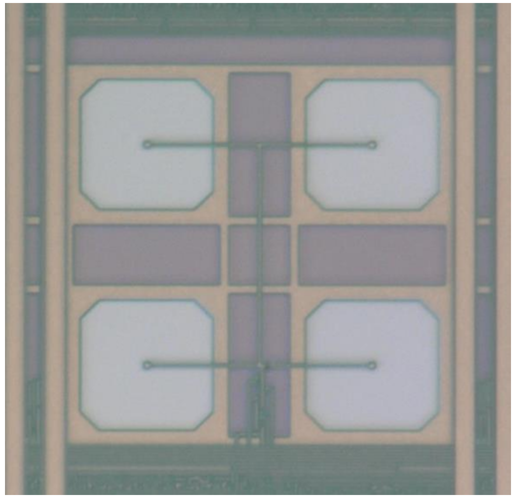
In MIP Detection Using Bare Prototypes

Direct MIP detection

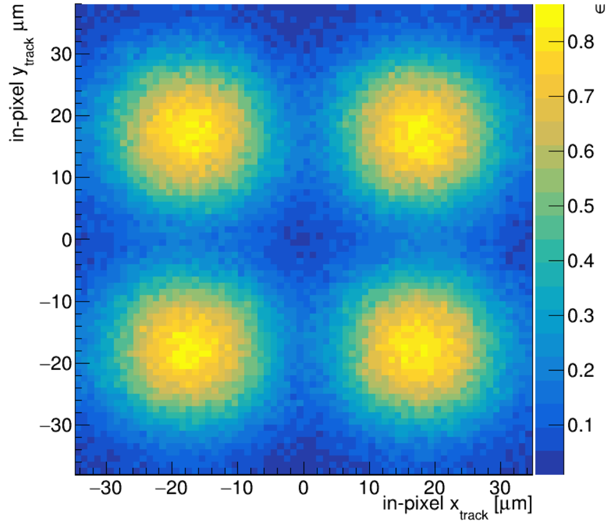
- Main limit is the fill factor (~30%)
- Maximum efficiency in the SPAD centre
- Track resolution O(4 µm)
- Measured value is slightly larger than the fill factor
- Small OV dependence
- No temperature/sample dependence observed

Overcome efficiency limits

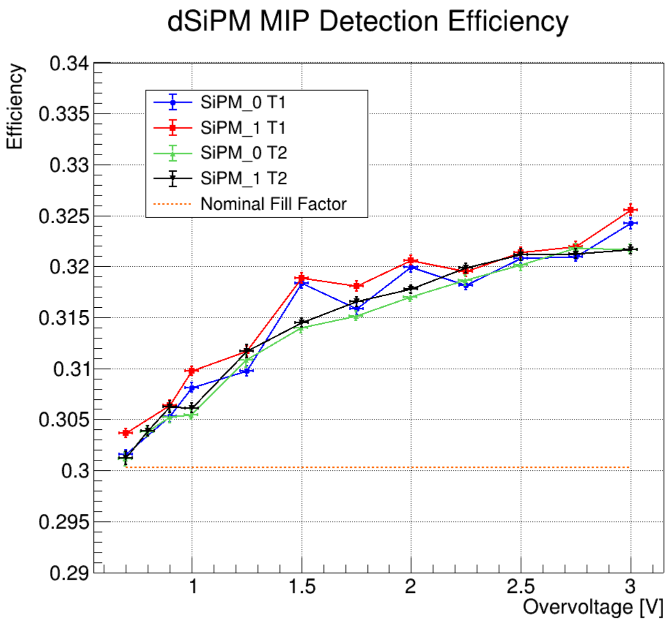
- Along with the DCR represents the main limit for 4D-Tracking
- Use larger SPADs (and not 4 x small)
- Use design/processes with slimmer SPAD isolation
- Explore the coupling with thin radiators (next slides)



DSiPM pixel picture



DSiPM In-pixel efficiency map



DSiPM + Thin LYSOs

Preliminary results from Feb-24 TB

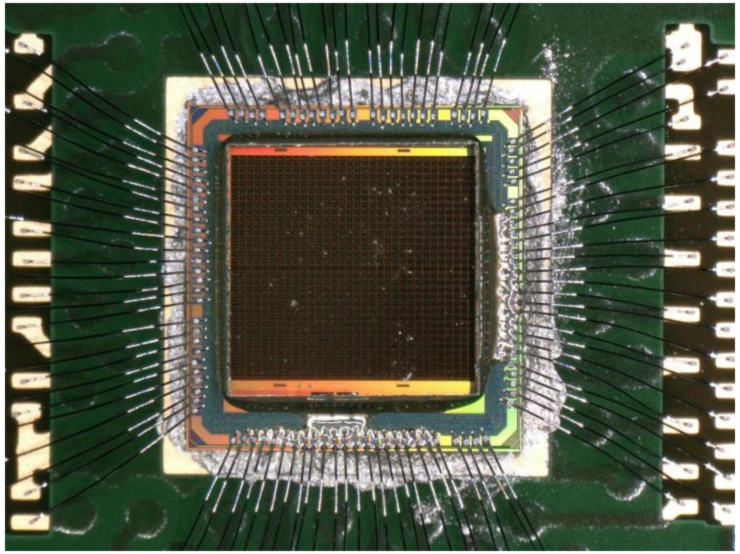
Thin Radiator Concept for DESY dSiPM

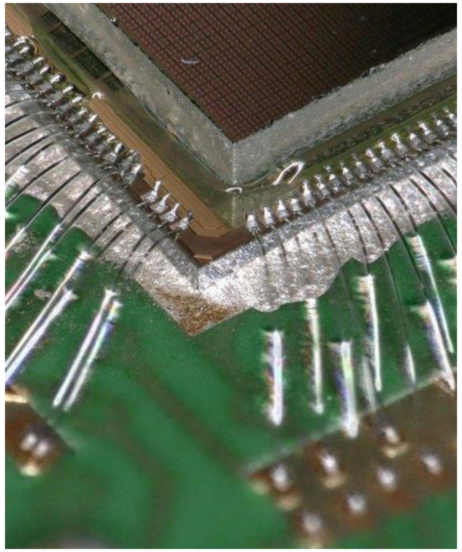
Increase Efficiency and "Reduce" Noise, Towards 4D-Tracking

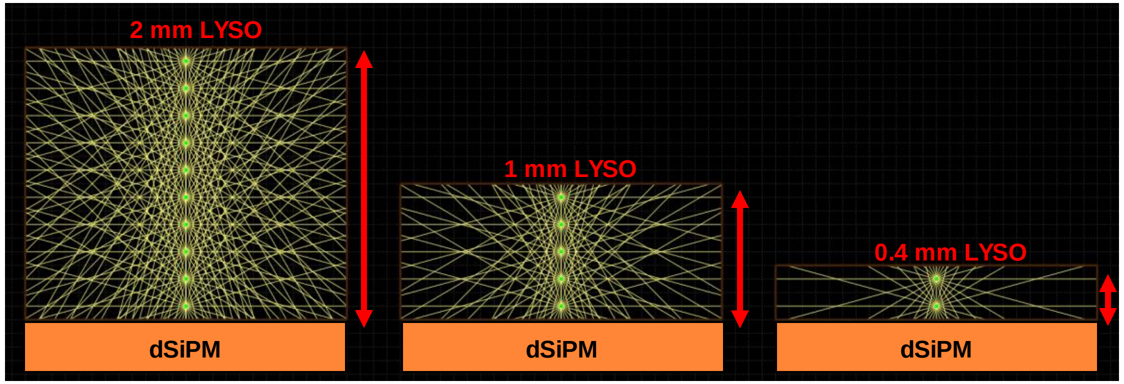
Following the thin radiator coupling concept already explored with SiPM in MIP detection [1] [2] [3]

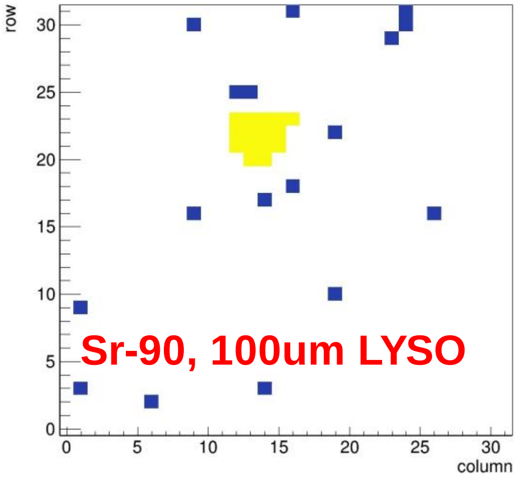
DESY dSiPM + thin LYSO scintillators:

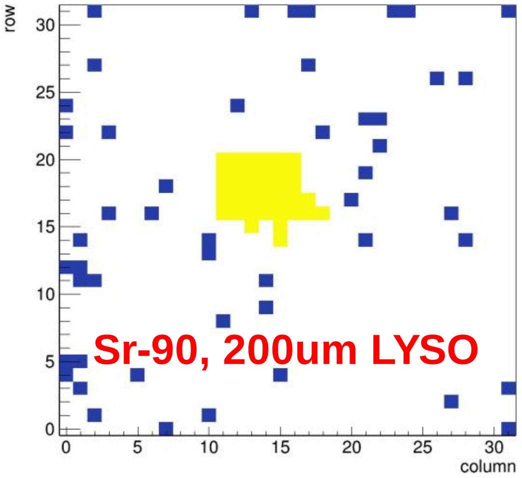
- Higher number of photons/µm produced
- Thinner converter -> cluster of photons
  - Preserve spatial resolution on DUT
  - Strongly suppress DCR noise (>> 1 SPAD firing)





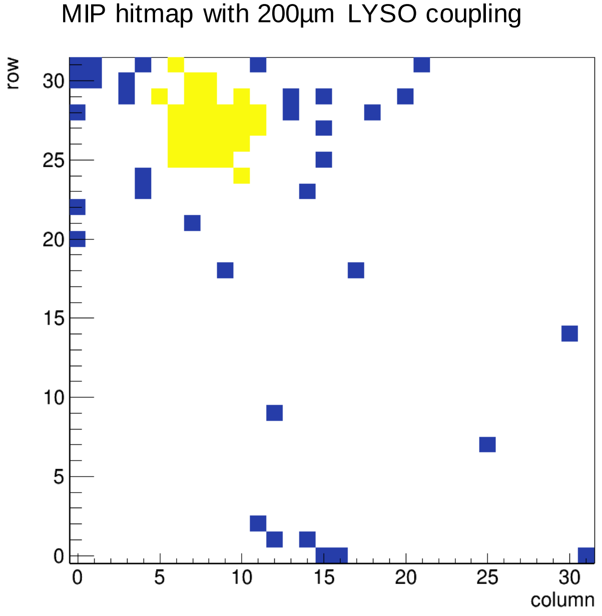


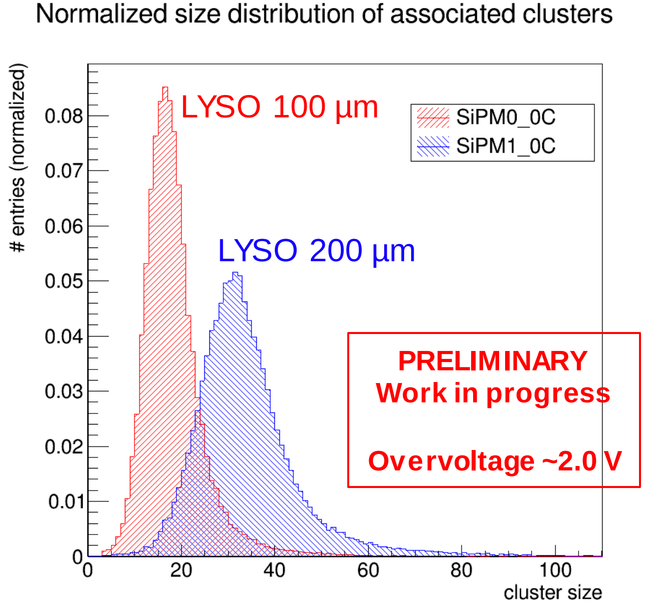


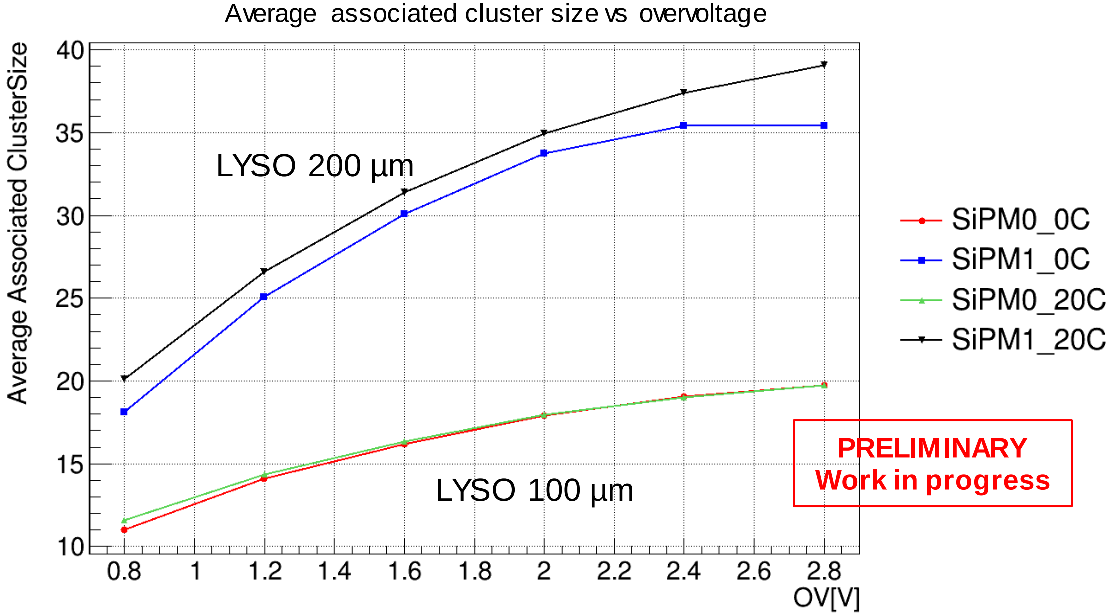


dSiPM + LYSO Cluster Size

In MIP Detection







Associated cluster size

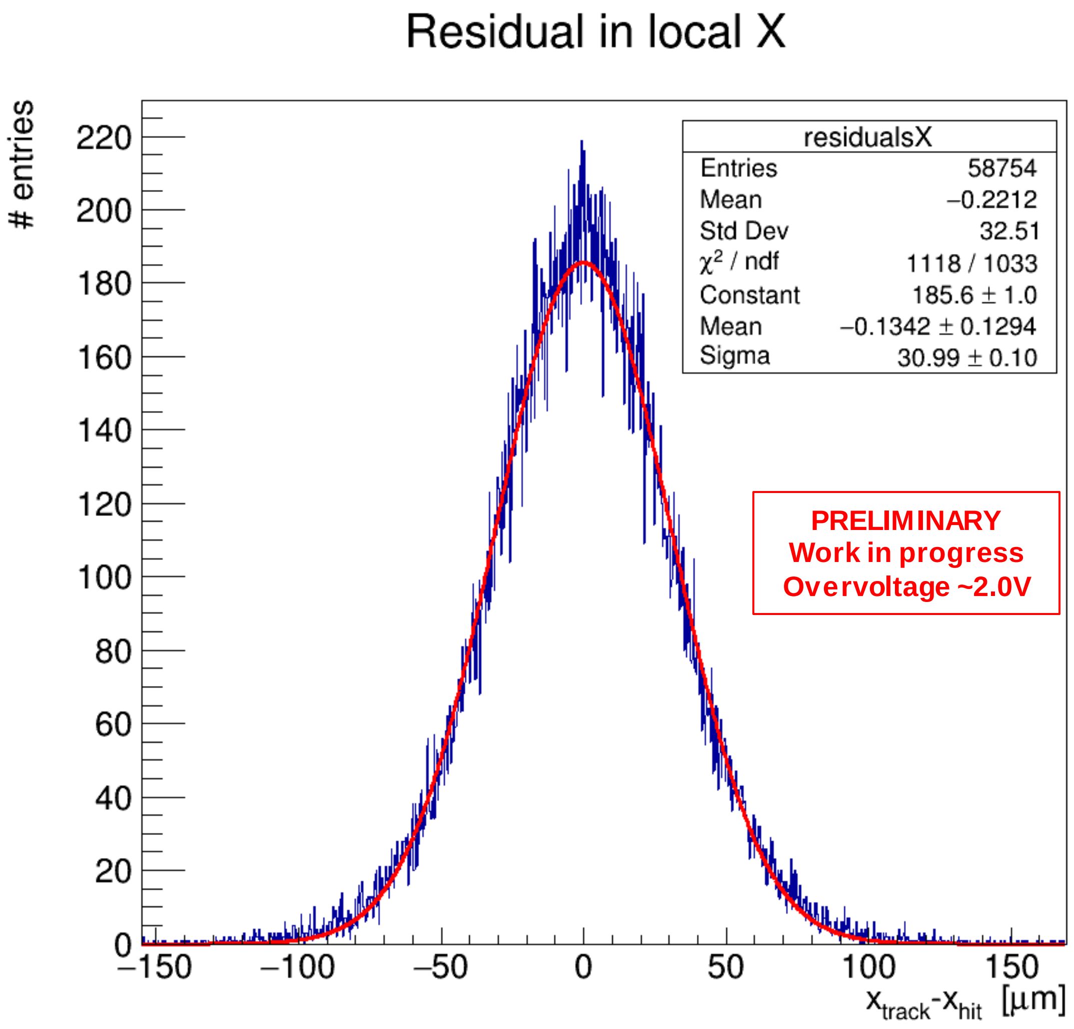
- Large clusters (high number of scintillation photons)
- Signal clusters can be distinguished from noise (usually 1-2 SPADs)
- Strong noise suppression cutting on cluster size

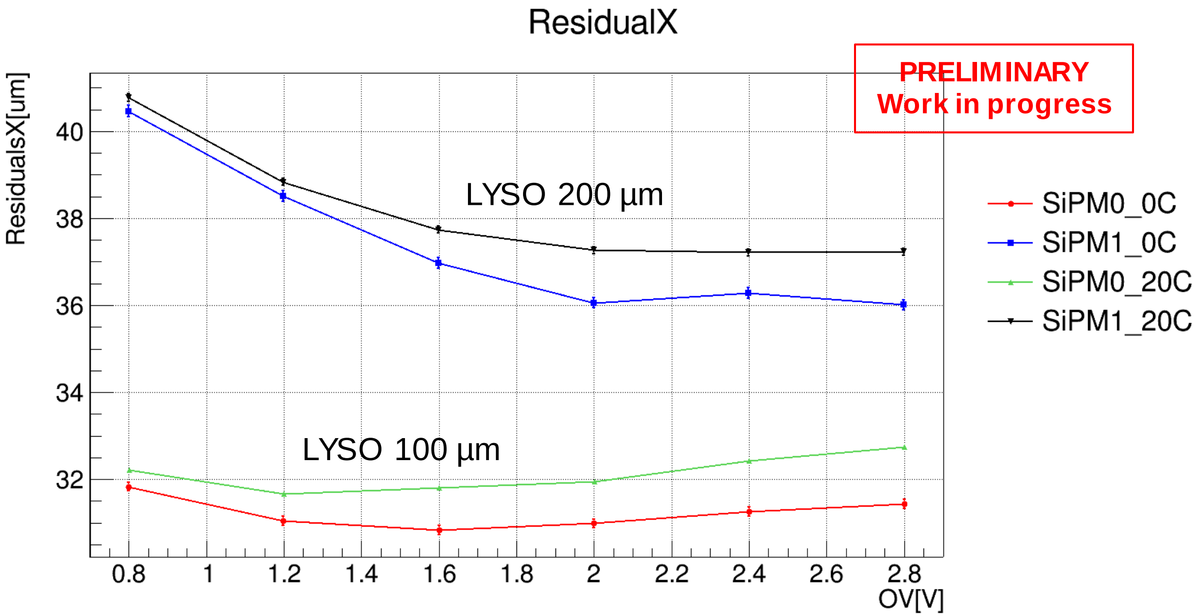
Cluster Size Comparison

- Cluster size increases with overvoltage (SPAD PDE increase)
- Thicker the LYSO larger the cluster size (number of photons)
- Small increase of clustersize with temperature (higher DCR)

dSiPM + LYSO Spatial Resolution

In MIP Detection



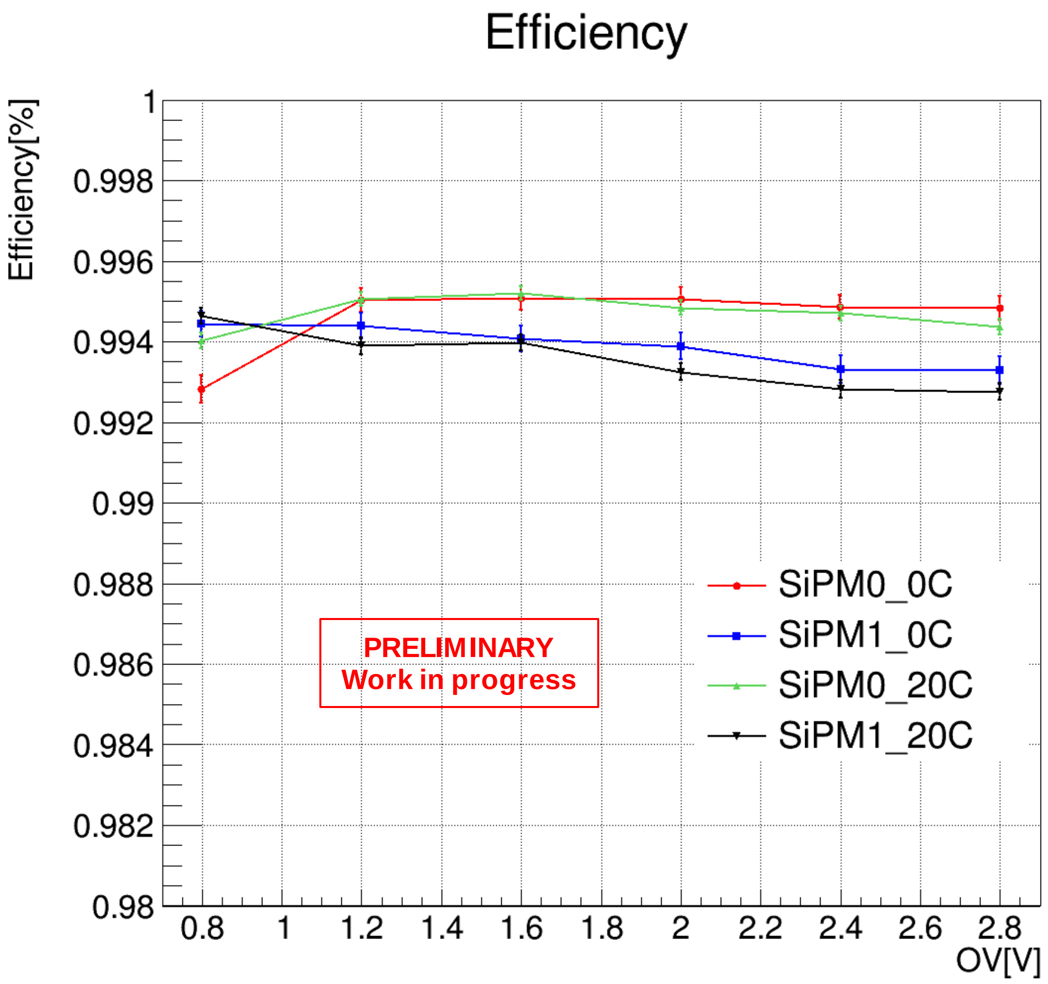


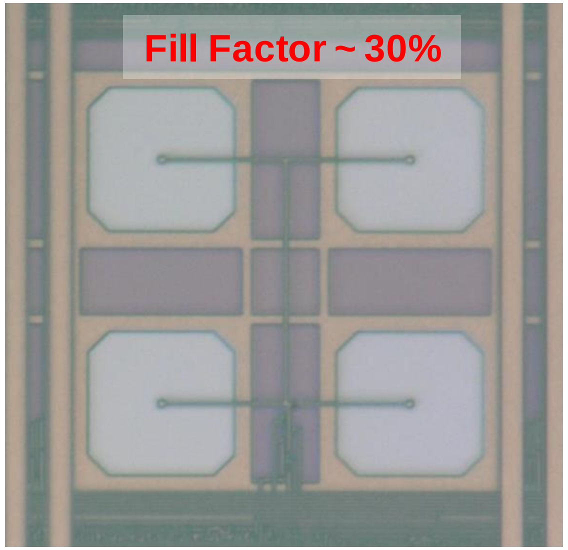
Spatial residuals

- Defined as the difference between cluster center in DUT and interpolated track in the same z-position
- Gaussian distribution (double peak structure no longer visible)
- Sigma ~33 µm (100µm LYSO) and ~38 µm (200µm LYSO)
- Spatial resolution compatible with ~pitch/2
- Residuals VS OV trends under investigation

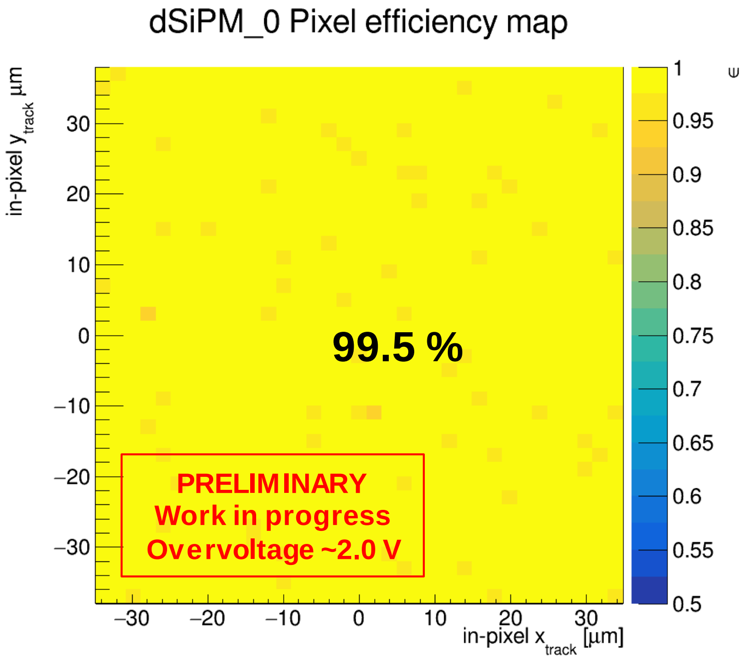
dSiPM + LYSO Efficiency

In MIP Detection





DSiPM pixel picture



DSiPM In-pixel efficiency map

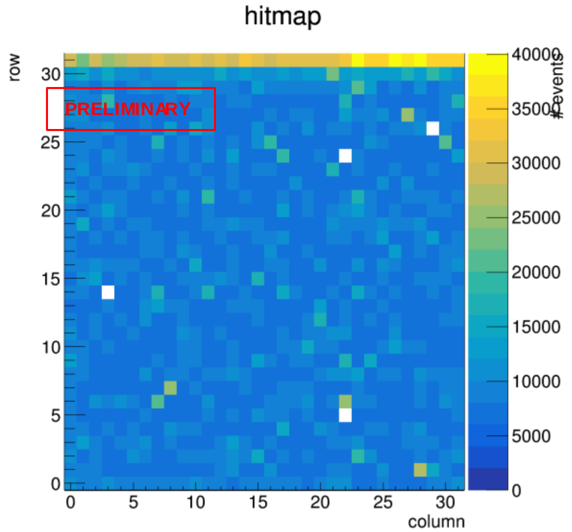
Efficiency using thin radiator

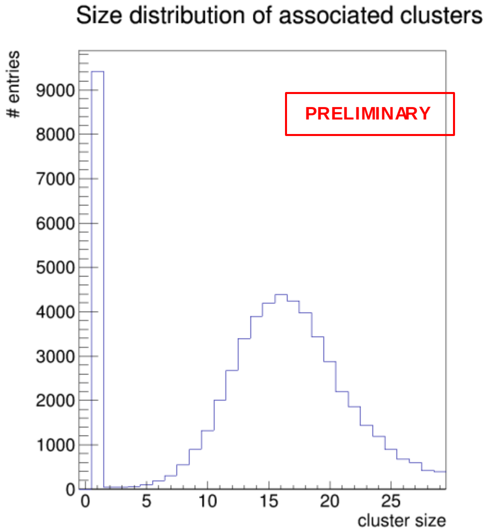
- Unifor in-pixel efficiency (SPADs position no longer visible)
- From ~33% (bare silicon) to ~99% using Thin LYSO
- No particular OV or temperature/sample dependence observed

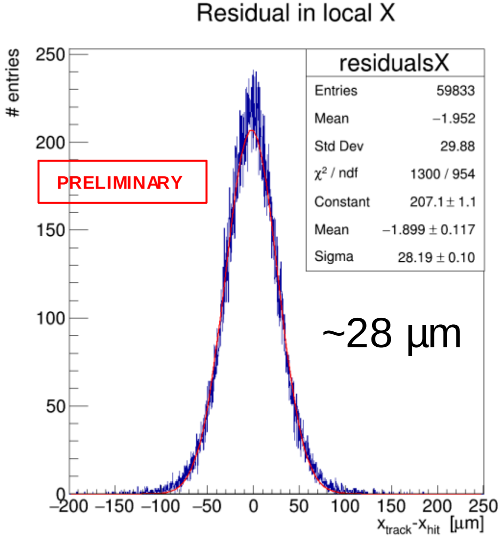
Let's Play Chess

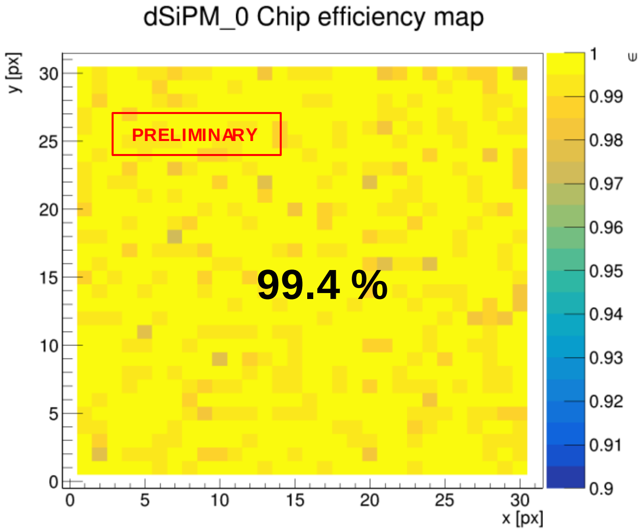
Similar Performances Whith Half Active Area!

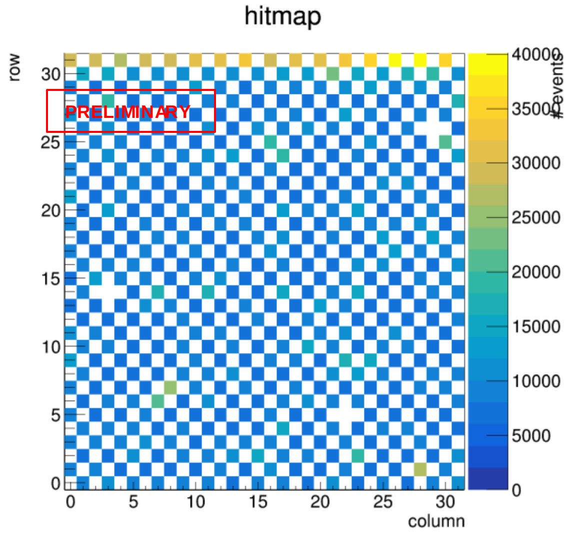
Using Cluster Center,
May improve using nearest pixel

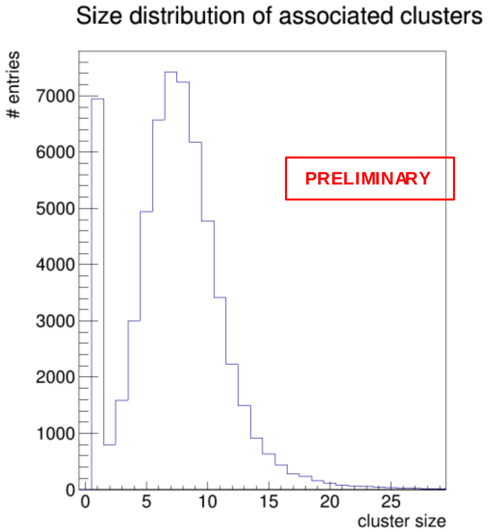


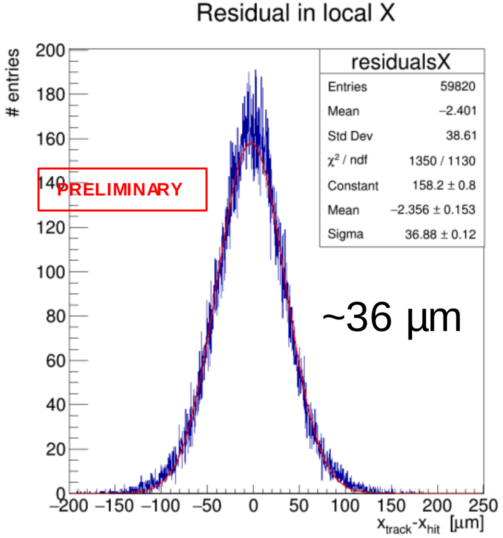


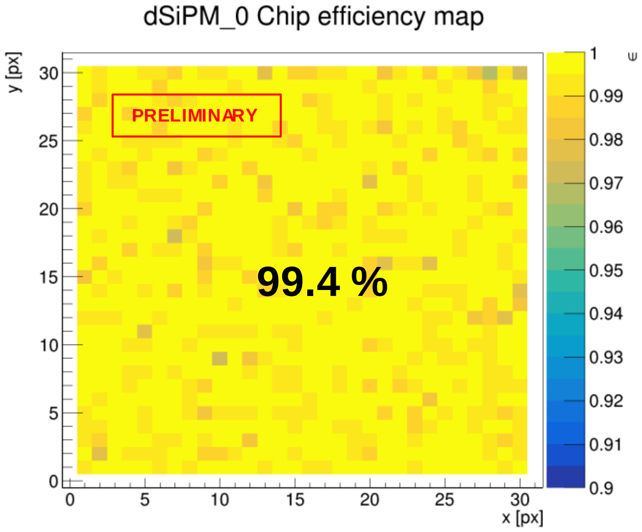








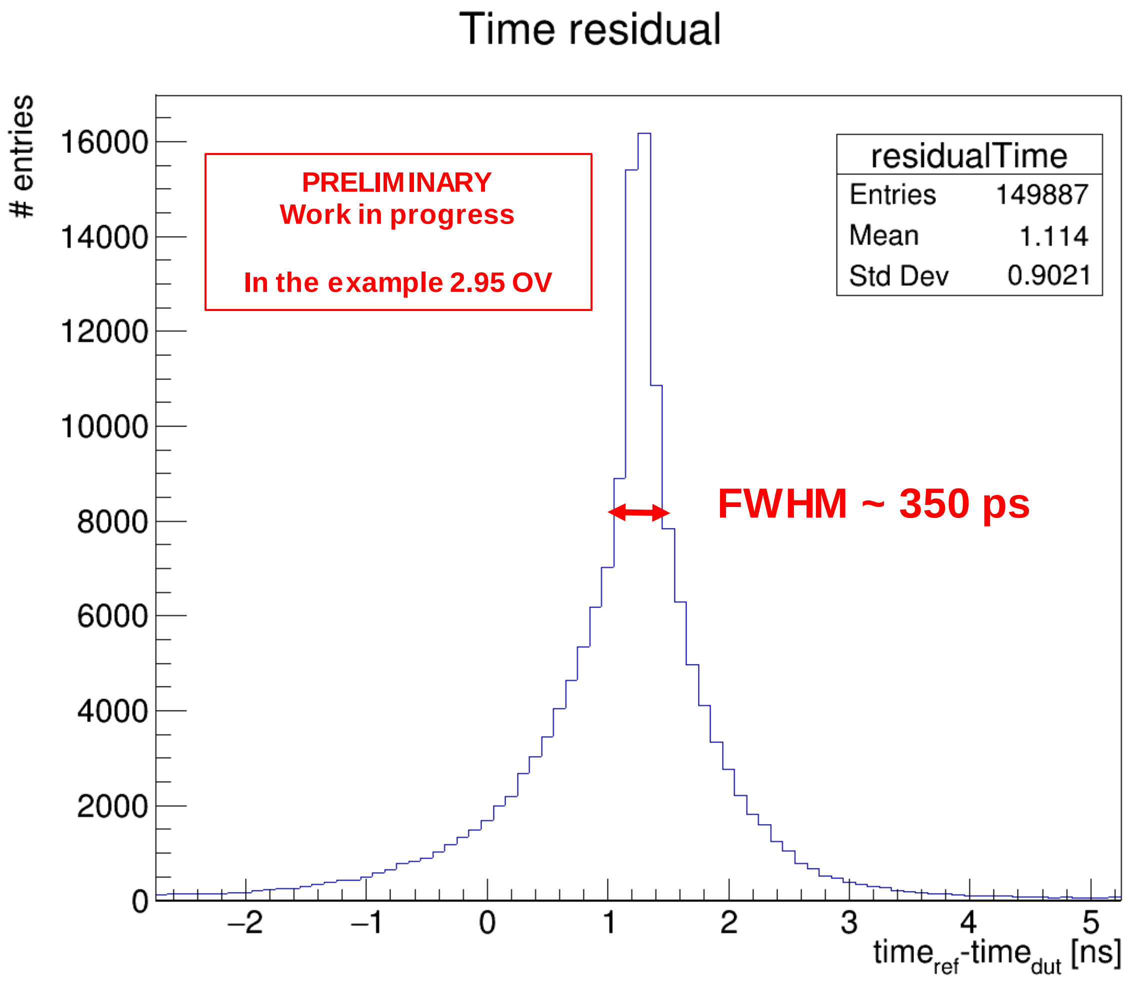




Run 1826, 2 OV chip10-100um LYSO

dSiPM + LYSO Timing

In MIP Detection



Time residuals

- Defined here as the difference between the DUTs timestamps
- Can be used to determine dSiPM + circuit time res.
- Core has a FWHM ~ 350 ps
- Overvoltage dependence currently under investigation

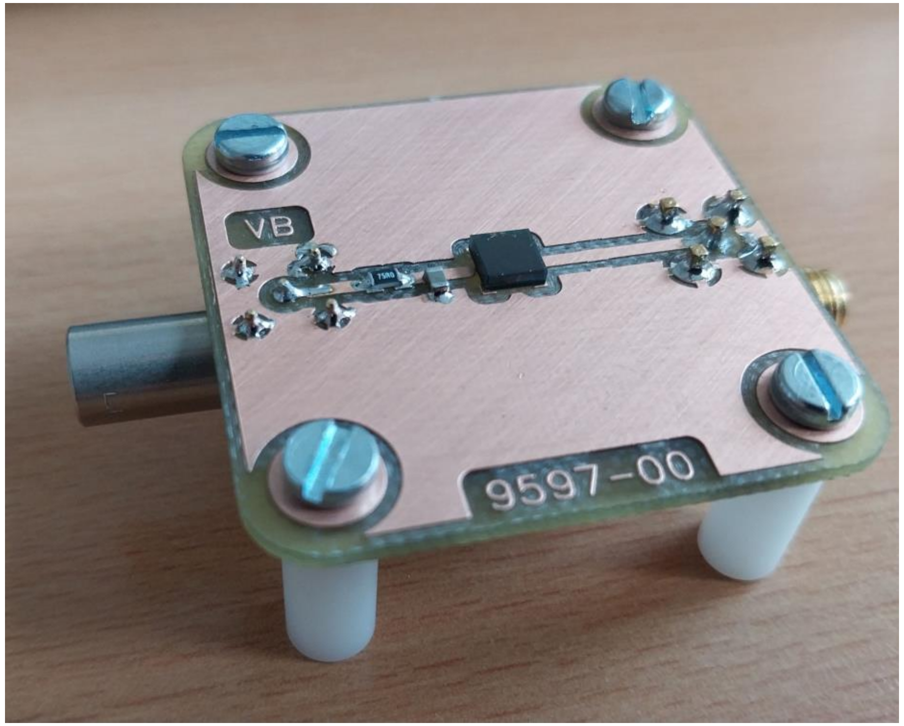
Important slow component

- A considerable fraction of the events has a time resolution in the O(1ns), long tails in time residuals
- Asymmetry related to the different LYSO thickness
- Probably related to slow LYSO component and small PDE
- Strategies to reduce the slow component under investigation

What Next?

Finilise results and writing

- Investigation of intrinsic LYSO timing using analog SiPMs
  - Using SiPM with high PDE + charge amplifiers
  - Sampling with high sample rate and bandwidth scope
- Laboratory crosstalk measurements with IR camera (summer student project)
- Testbeam end of May (analog + digital samples)
- 2 Paper in the coming months
- Pisa Meeting oral presentation + proceedings
- Always open for idea on possible application of the technology



Summary

DESY digital SiPM

CMOS SiPMs R&D

- dSiPMs can be an interesting alternative to analog SiPM
- Combination of SPAD and CMOS electronics in the same silicon die opens new application possibilities & reduces complexity

DESY dSiPM & MIP 4D Tracking

- DSiPMs may represent a possible candidate technology for 4D-tracking
- DESY dSIPM used in a test beam setup as particle detector

Bare Silicon:

- Spatial resolution of the O(20 µm)
- Efficiency comparable to the fill factor (~ 33%)
- Time resolution O(50 ps) sigma

DSiPM + Thin LYSO

- Spatial resolution of the O(35 µm)
- Efficiency >99% with strong noise suppression
- Time resolution <1 ns

	dSiPM	dSiPM+LYSO
Signal Cluster Size	~ 1	10 – 40
Spatial Resolution	~ 20 µm	~ 35 µm
Efficiency in MIP detection	~ 33 %	> 99 %
Dark Counts (Noise)	O(MHz)	O(Hz)*
Time Resolution	~ 50 ps	< 1ns *

*currently under investigation

Thank you.

Gianpiero Vignola
gianpiero.vignola@desy.de

Deutsches Elektronen-Synchrotron DESY
Notkestraße 85, 22607 Hamburg
1C, O1.331, ATLAS

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

DSiPM TB4 Timing

Not exactly as expected, work in progress

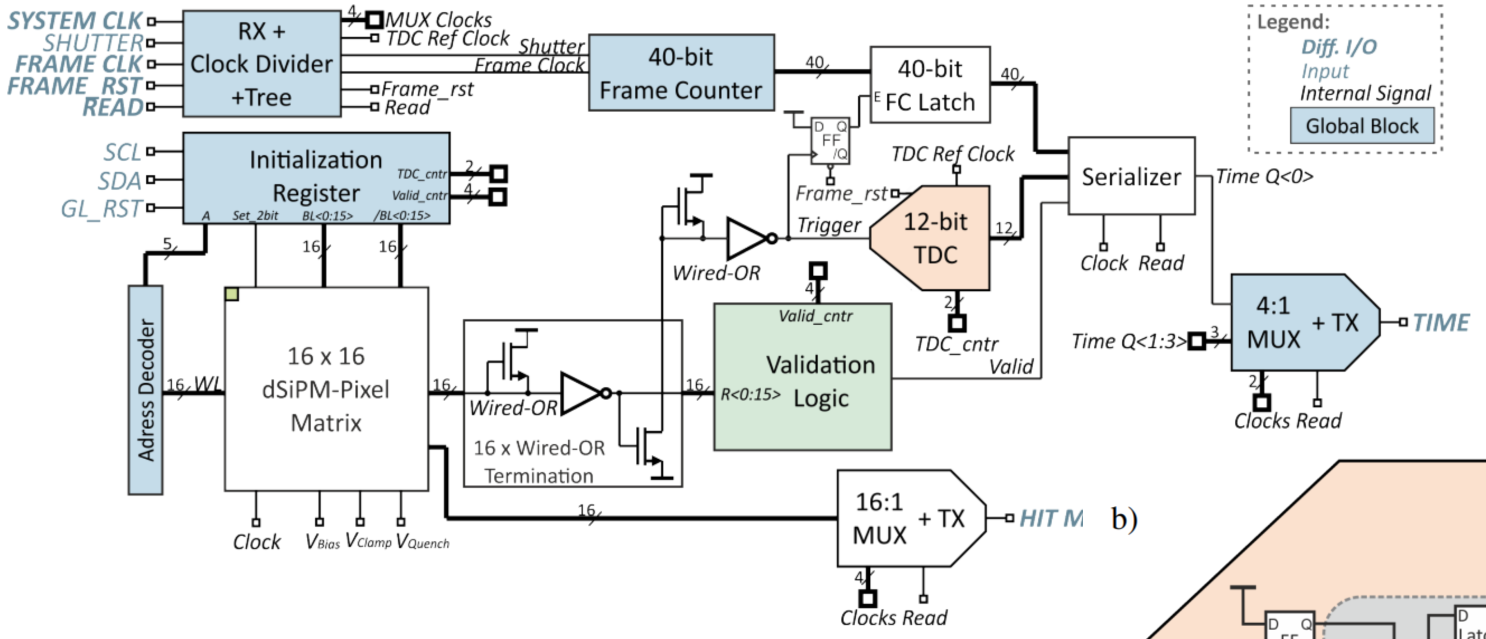
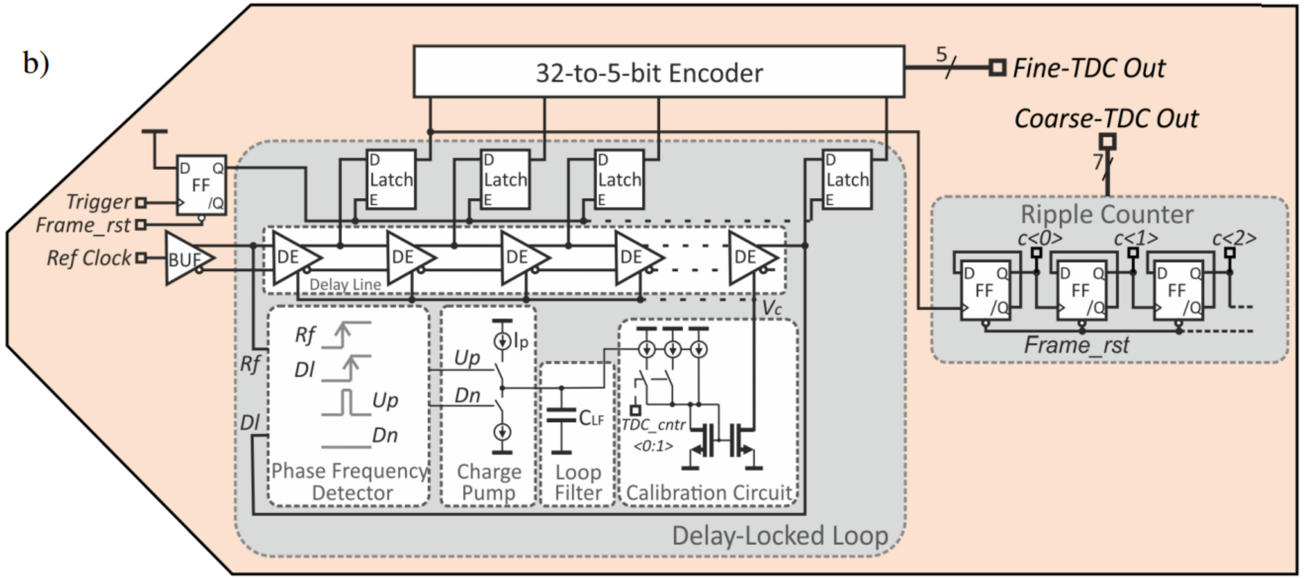


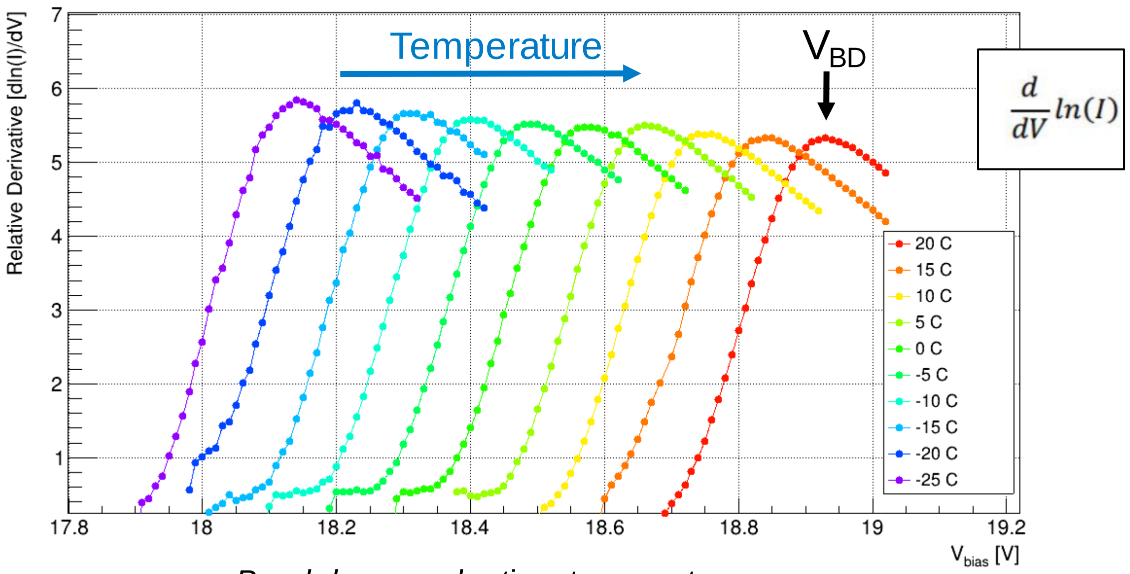
Figure 2. Quadrant block diagram.



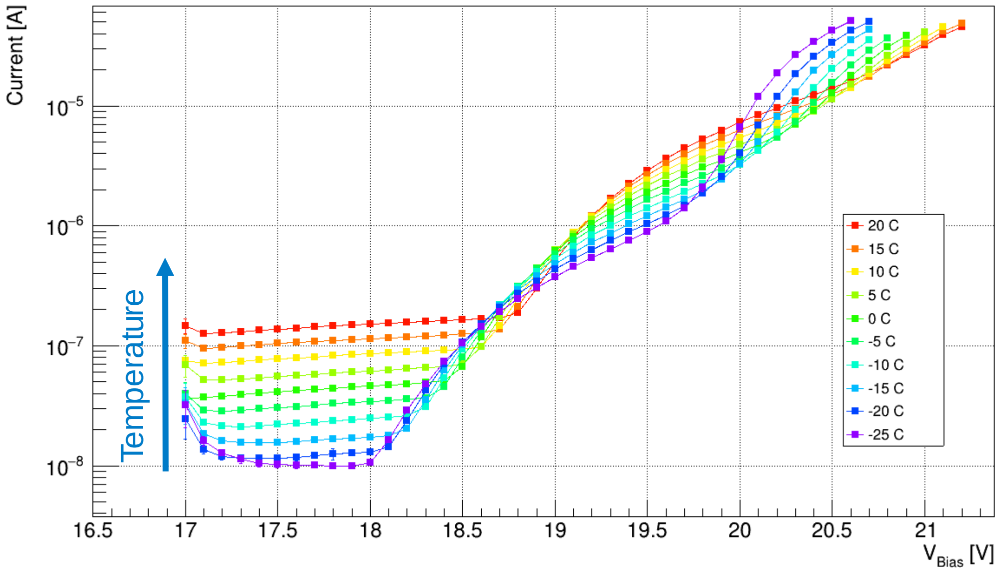
IV Curves & Dark Count Rate

Basic Chip Characterization

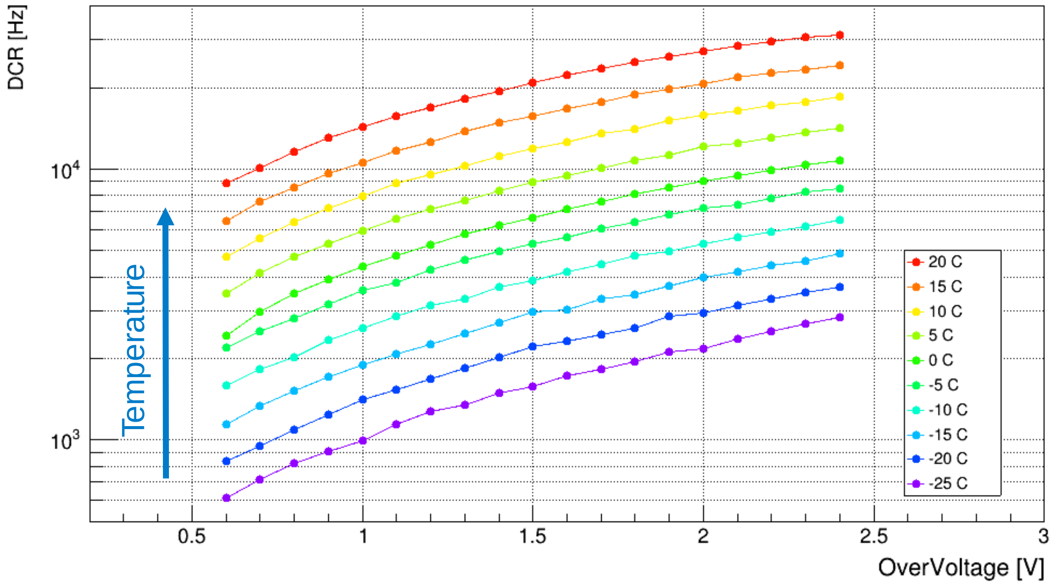
- Detailed characterization performed on several samples (Chip4 shown in figures)
- IV & Dark Count Rate studies performed with controlled **temperature** (from -25 to 20 °C) and **humidity** (~ 0 %) in a dark environment
- Measurements compatible with expectations



Breakdown evaluation, temperature scan



IV curves (full matrix), temperature scan



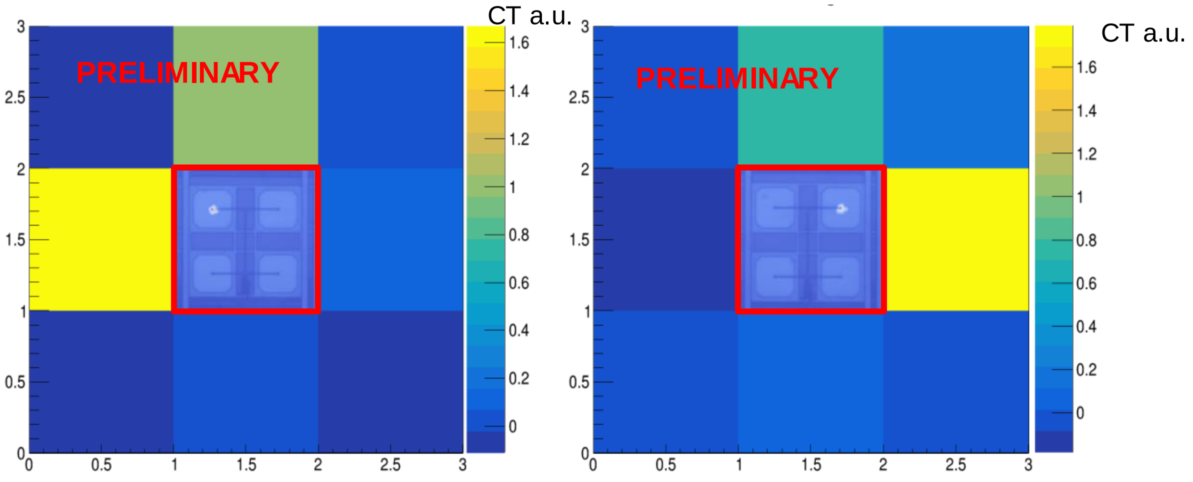
Dark Count Rate (per pixel), temperature scan

DESY dSiPM Characterisations

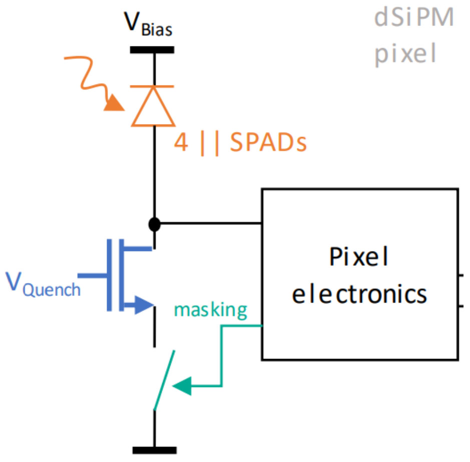
Exploring the Potential of Digital SPADs

Studies possible thanks to digital features

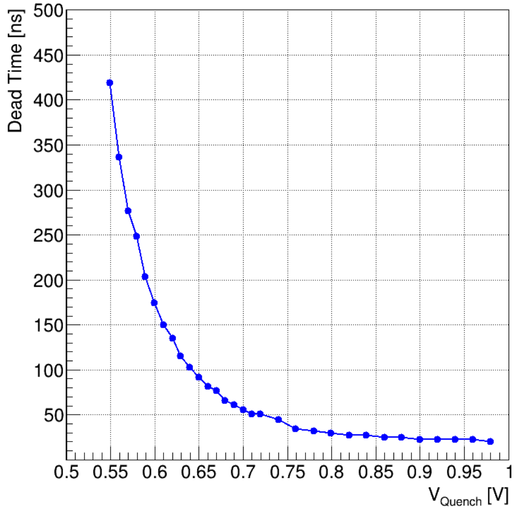
- Effect of quenching transistor tuning in senor response
- Pixel masking: effect on IV and DCR reduction
- Pixel crosstalk characterisation: studying the correlation between avalanche position and CT probability in neighbours



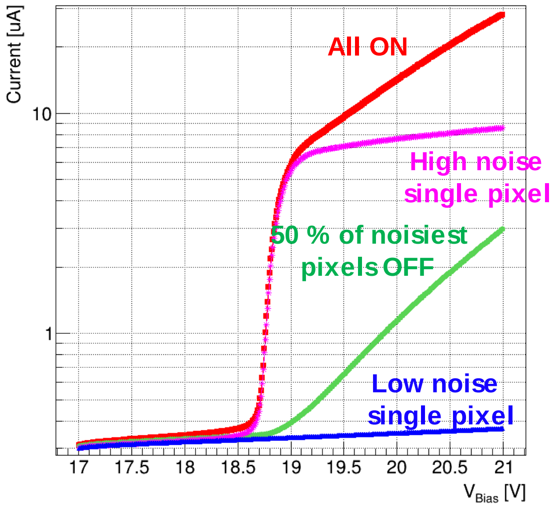
Crosstalk studies as function of avalanche position



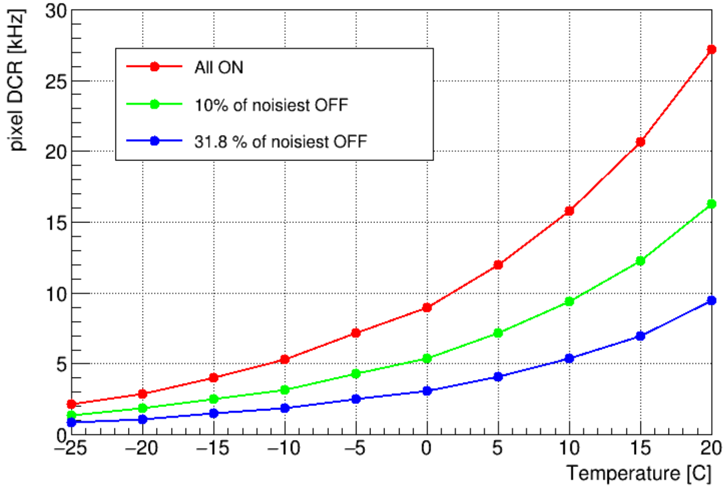
Pixel circuit



Dead time vs V_{Quench}



IVs with different masks



DCR with different masks (2 OverVoltage)

Pixel Design & Readout

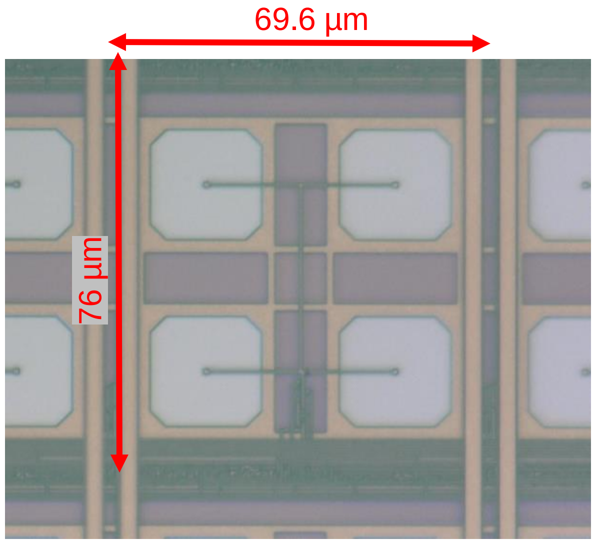
4 SPAD Layout

Pixel Layout & electronics

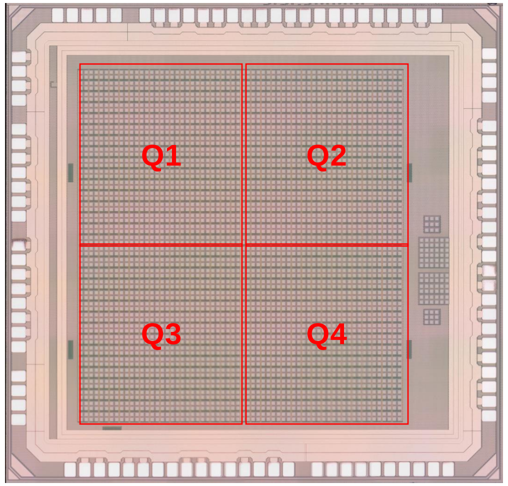
- 4 SPADs sharing one Frontend and additional readout electronics
- Fill factor ~30% (limited by SPAD dimension available)
- Quenching Transistor (V_{Quench})
- Masking Circuitry
- In-pixel Hit counter

Readout concept

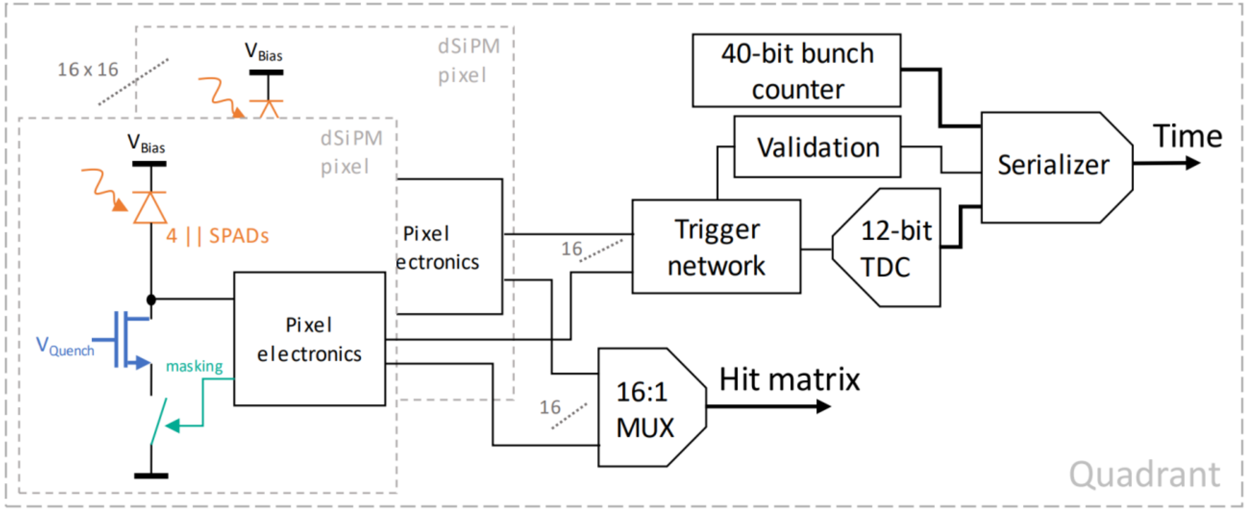
- The ASIC is divided into four identical quadrants (16 x 16 pixel units)
- Outputs of all pixels are combined in a wired-OR
- The fastest pixel signal triggers a running 12-bit TDC
- Validation logic to discard undesirable events
- The Hit matrix is readout via a 16-to-1 multiplexer



Microscope picture of a pixel



Microscope picture of the Chip



Readout concept of a 16-by-16 pixel unit (Quadrant)

Additional characterizations

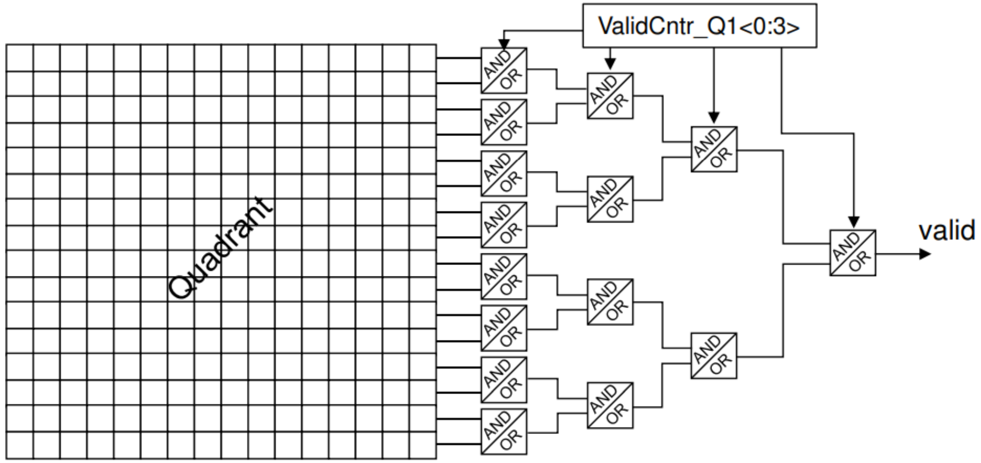
Validation Logic & Dead Time

Validation logic

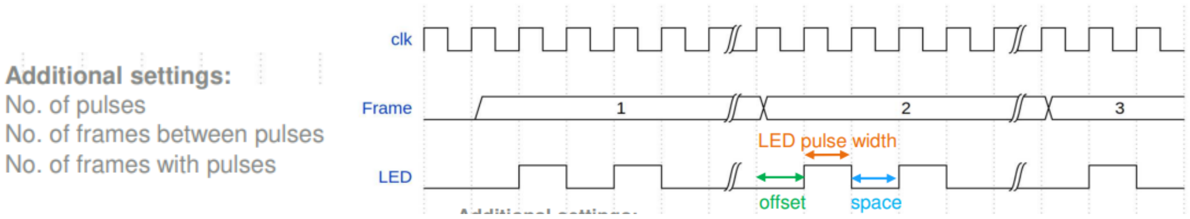
- A 4-step validation logic is implemented in every quadrant
- Every step can be configured to be an AND or OR gate
- A flag bit is generated for event validation within 2 ns
- Successfully validated using laser pulses and masking

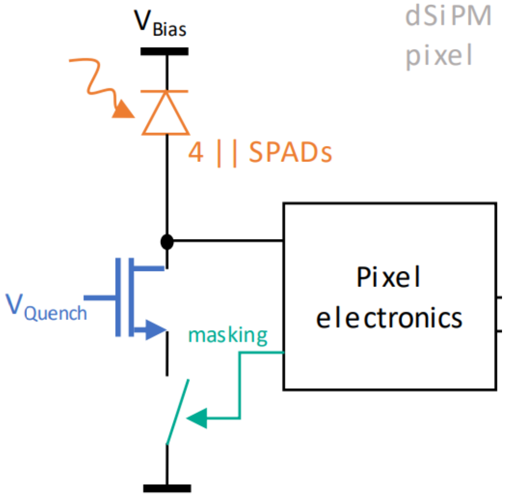
Quenching & Dead Time

- In 2-bit mode is it possible to count laser pulses within the frame
- Consecutive pulses can be distinguished only if the discriminator threshold is crossed (non-overlapping pulses)
- Pulse length can be tuned by acting on Vquench Transistor (Global Setting)

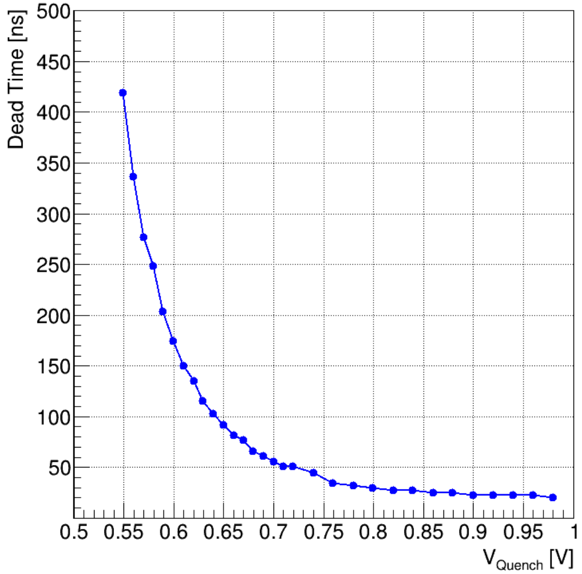


Schematic representation of the Validation Logic





Pixel Circuit



Dead Time vs V_{Quench} (chip4)

DAQ System in Test Beam

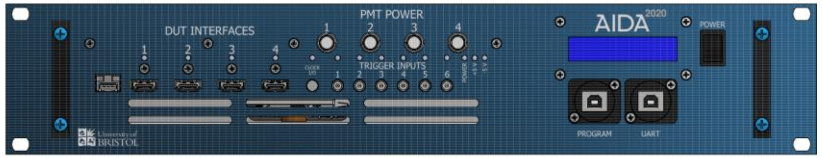
AIDA TLU Core

https://doi.org/10.1140/epjti/s40485-016-0033-2

Scintillators & PMTs

NIM Logic

Trigger IN



https://doi.org/10.1088/1748-0221/14/09/P09019

EUDET TELESCOPE
(6 x Mimosa 26)

BUSY

Trigger ID

AIDA Trigger Logic Unit
"Aida Mode"

Clock, t0

Trigger OUT

BUSY

Caribou DAQ

Clock

LVDS

dSiPM

http://dx.doi.org/10.22323/1.370.0100

Telescope Hitmap

Event Timestamp & Trigger ID

dSiPM Hitmap & Timestamp

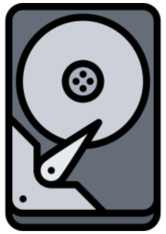
EUDAQ

https://github.com/eudaq

https://gitlab.cern.ch/corryvreckan/corryvreckan

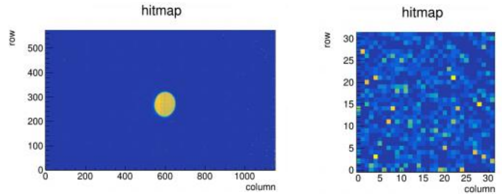
Analysis Chain

Using Corryvreckan



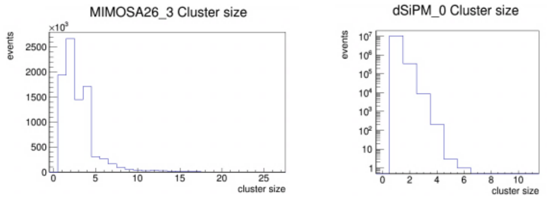
Data Decoding

Raw Telescope & dSiPM **data** are **decoded** into an accessible format



Clustering

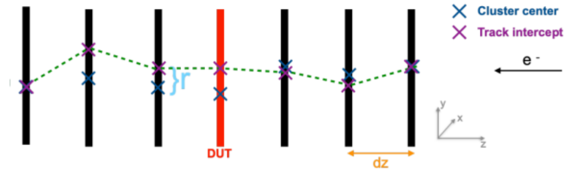
Clusters of hits in the reference telescope and DUT are identified



Tracking

*

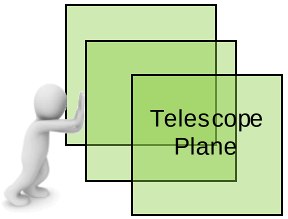
Tracks are reconstructed using telescope clusters + spatial & temporal cuts

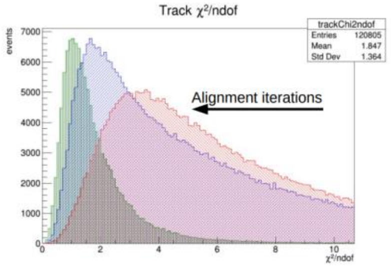


*

Telescope Alignment

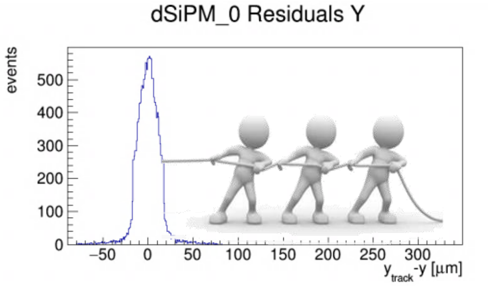
Software **translations and rotations** of the **telescope planes** are performed





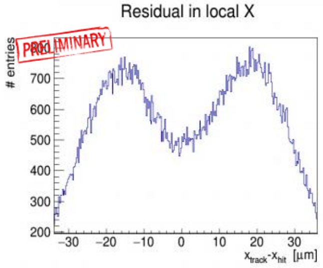
dSiPM Alignment

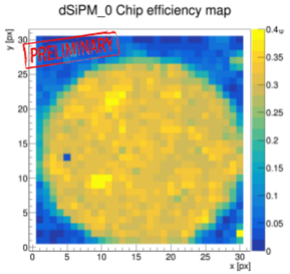
Translations and rotations of the **DUT** are performed to minimize unbiased residuals



DUT Association & analysis

DUT clusters are associated with tracks & its **MIP detection response** is analyzed

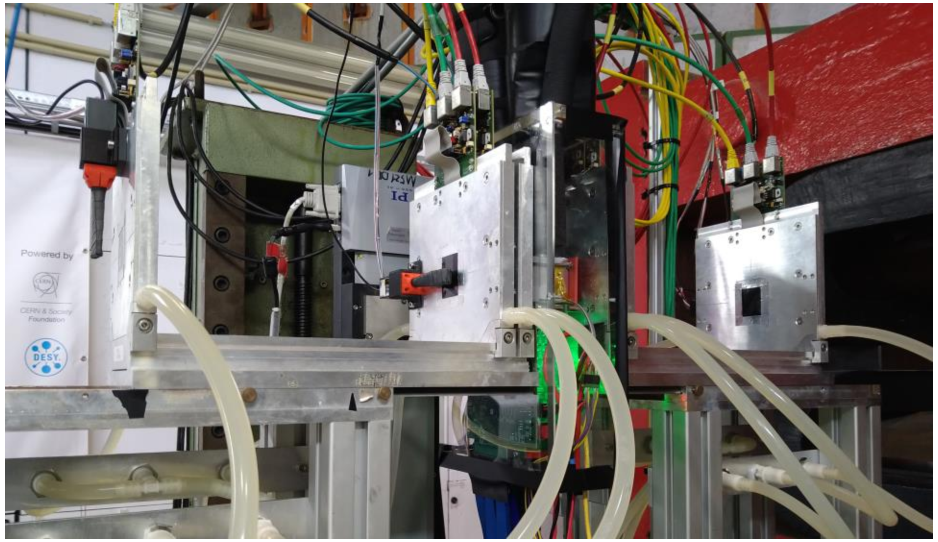


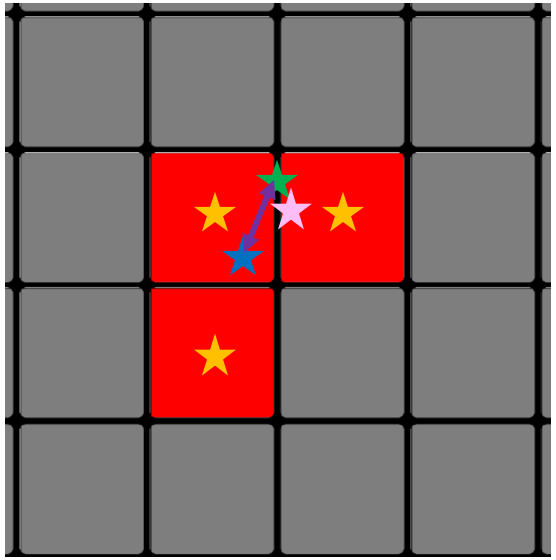


TestBeam data reconstruction

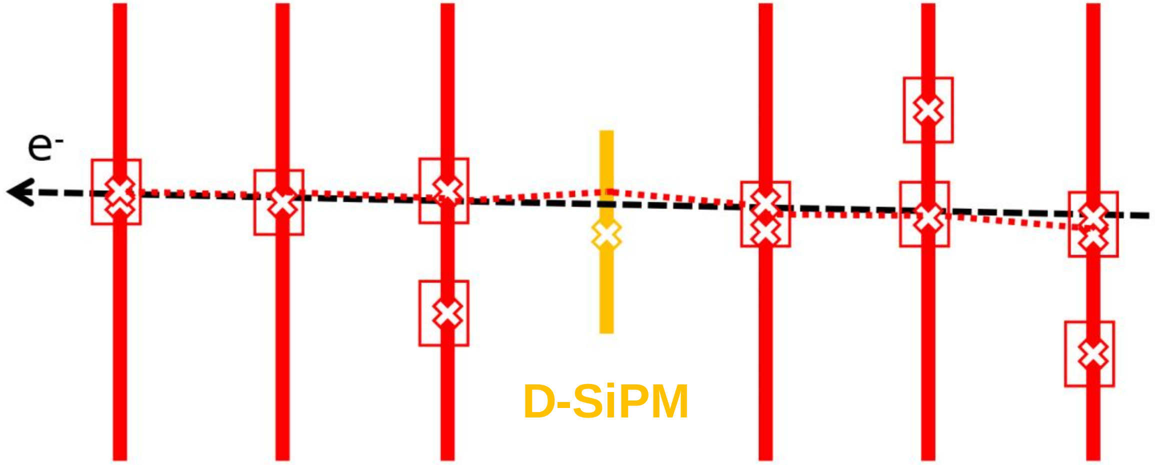
Using Corryvreckan Framework

- Corryvreckan use hit (pixels above threshold) and Clusters (groups of adjacent hits) to reconstruct particle trajectories.
- DUT response is then investigated on associated events





- Real Track
- Hit
- Cluster
- Cluster center
- Reconstructed Track
- Residuals



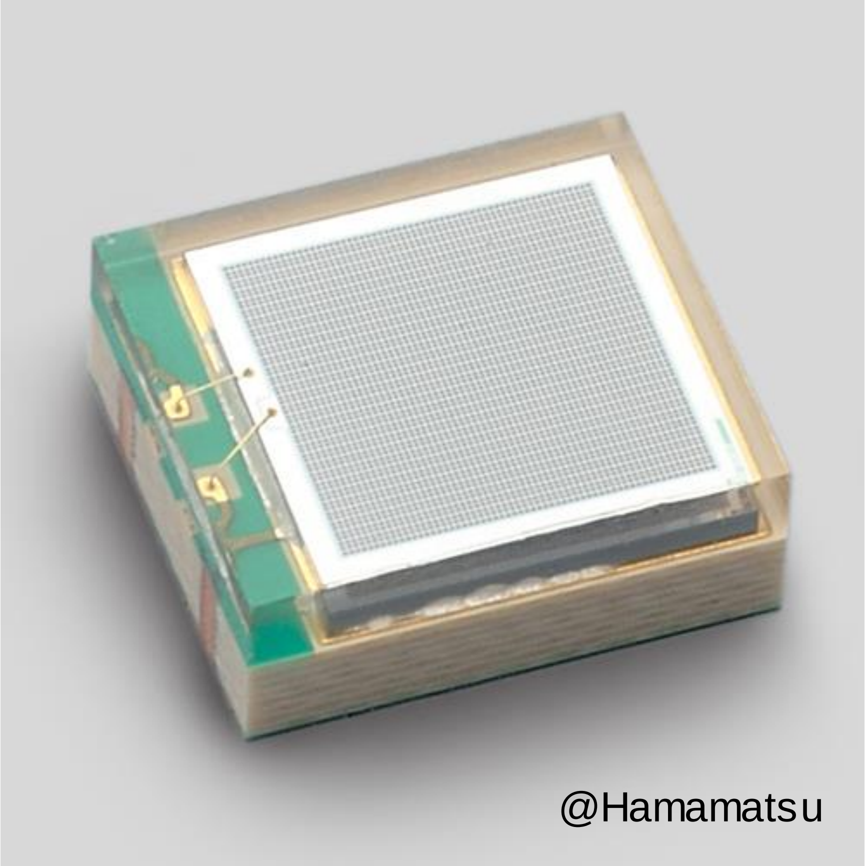
http://cern.ch/corryvreckan

Possible Solution to Increase Efficiency

And "Reduce" DCR Noise

MIP detection with analogue SiPMs

- High detection efficiency observed while detecting MIP
- High number of SPADs firing
- Correlation between MIP response and SiPM packaging
- Effects attributed to Cherenkov light produced in commercial SiPMs protection materials (~0.6-1.5 mm Epoxy resin or Silicone)
- Benefits:
  - High efficiency of SiPM in direct MIP detection
  - Low DCR contamination (high threshold)
  - Multipurpose detector (single photon and MIP)



References

F.Carnesecchi, G.Vignola et al. *Direct detection of charged particles with SiPMs*, 2022

F.Carnesecchi, G.Vignola et al. *Understanding the direct detection of charged particles with SiPMs*, 2023

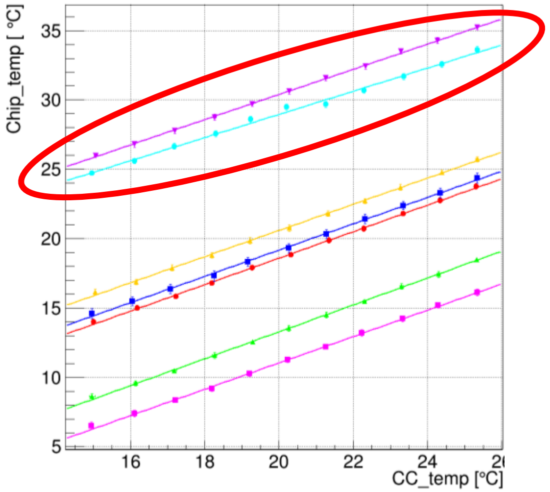
F.Carnesecchi, B.Sabiu et al. *Measurements of the Cherenkov effect in direct detection of charged particles with SiPMs*, 2023

Which samples?

I'll go for Chip10 & Chip11 (LYSO 100 & 200)

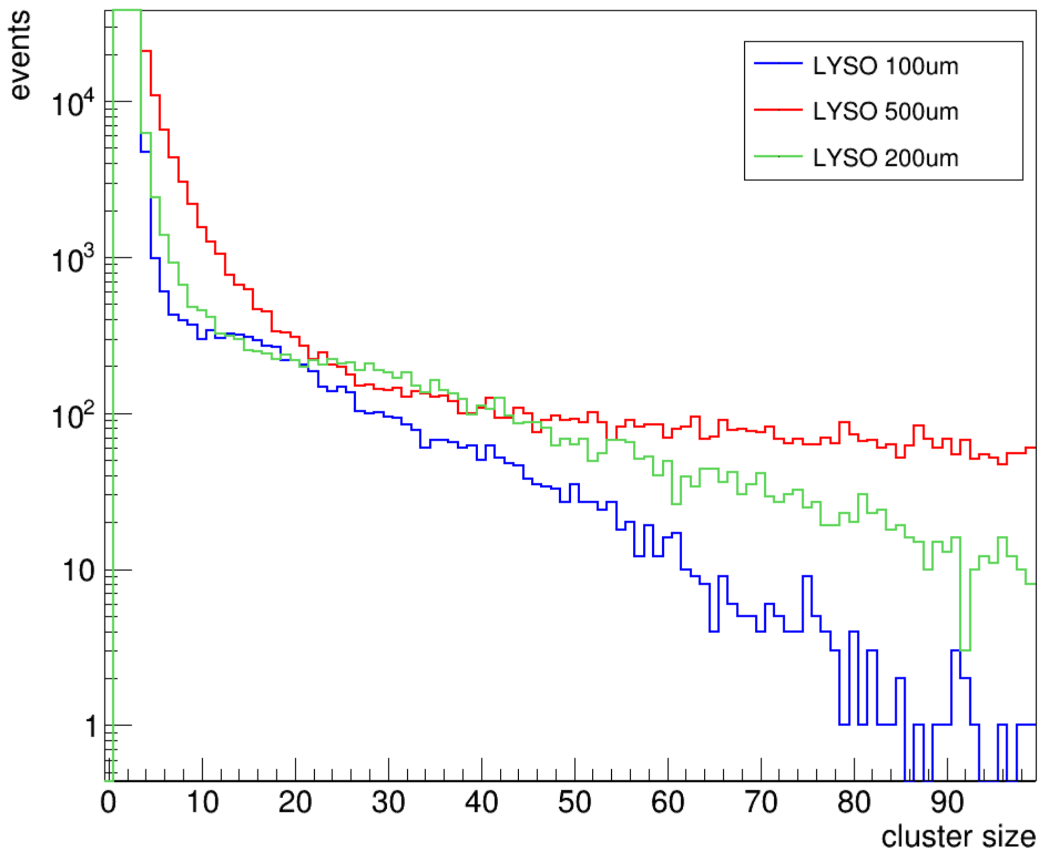
Sr-90 in ELAB4

- 2 days campaign with Sr-90 in ELAB4 last week 2024
- Using Eudaq for data taking & Corry For analysis
- Geant4 simulation trend confirmed:
  - 100 & 200 LYSO similar
  - 500 LYSO clusters too big (poor spatial performances)



Logbook

dSiPM_0 Cluster size



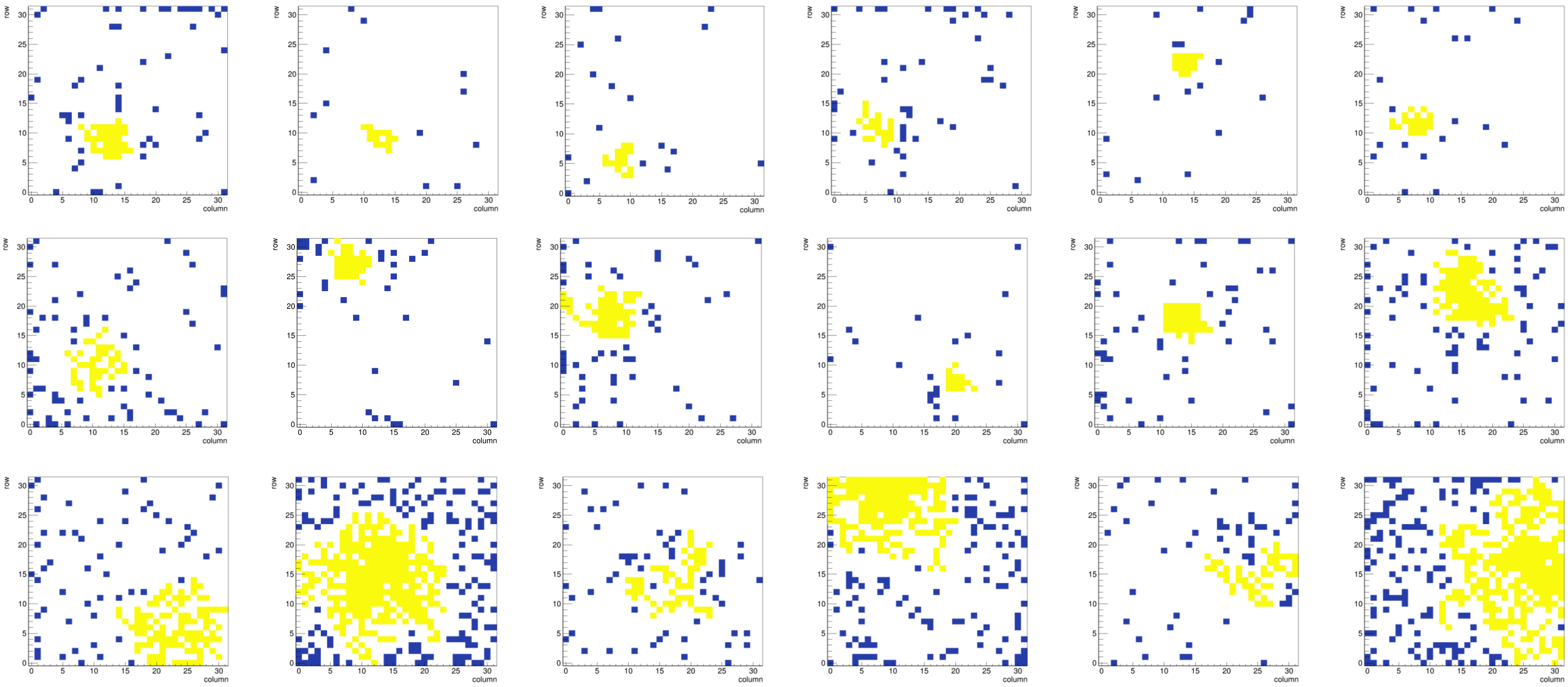
Overvoltage ~1.5
Temperature on Chip ~25C

Which samples?

Cluster sizes, random selection (100, 200, 500 from the top)

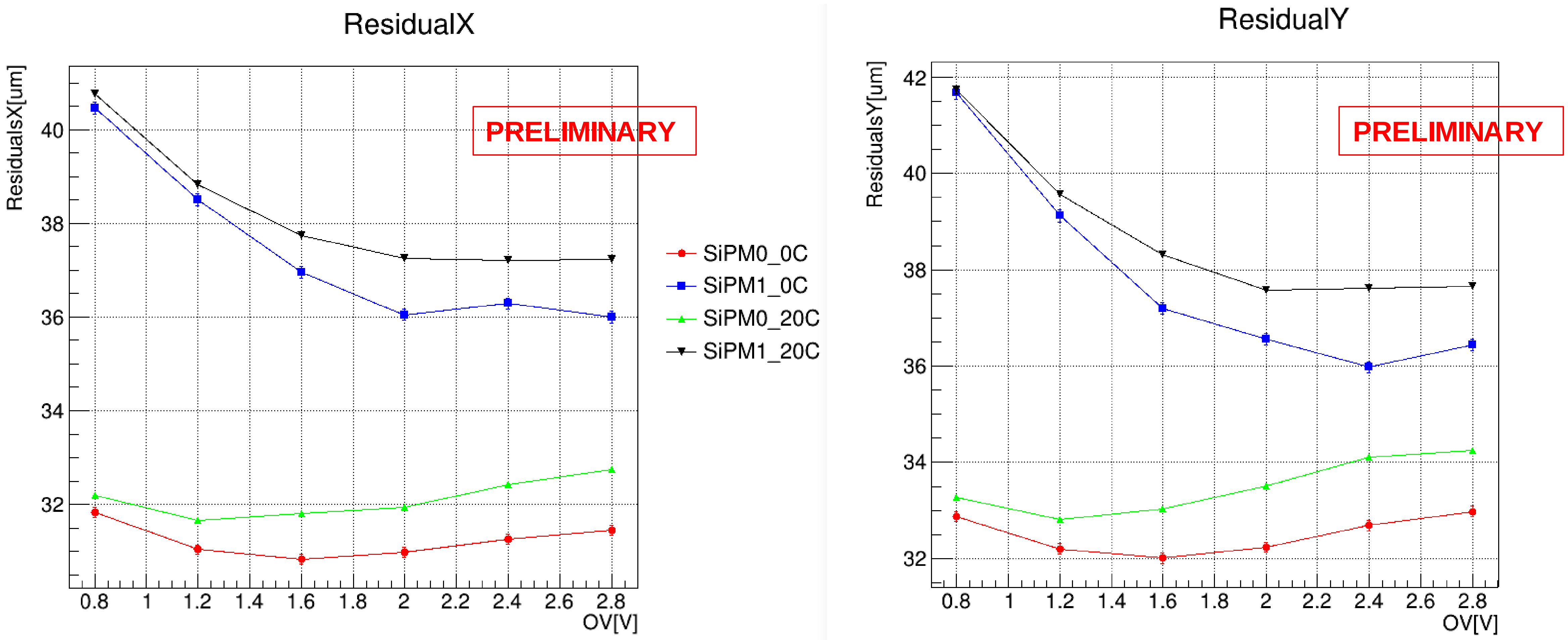
Overvoltage ~1.5

Temperature on Chip ~25C



Residuals vs OV

As Funtion of Overvoltage



Time Residuals

Correction Applied

Selection & corrections

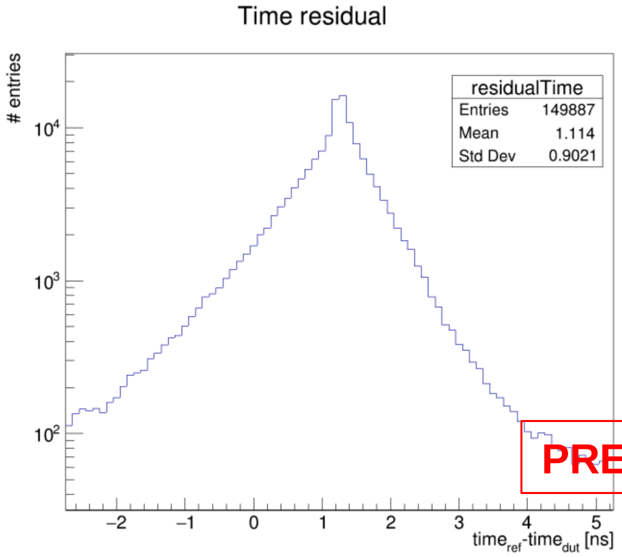
- Only 1 Frame decoded
- ROI quadrant center
- DNL correction
- Delay correction*
- Timestamps from Cluster center

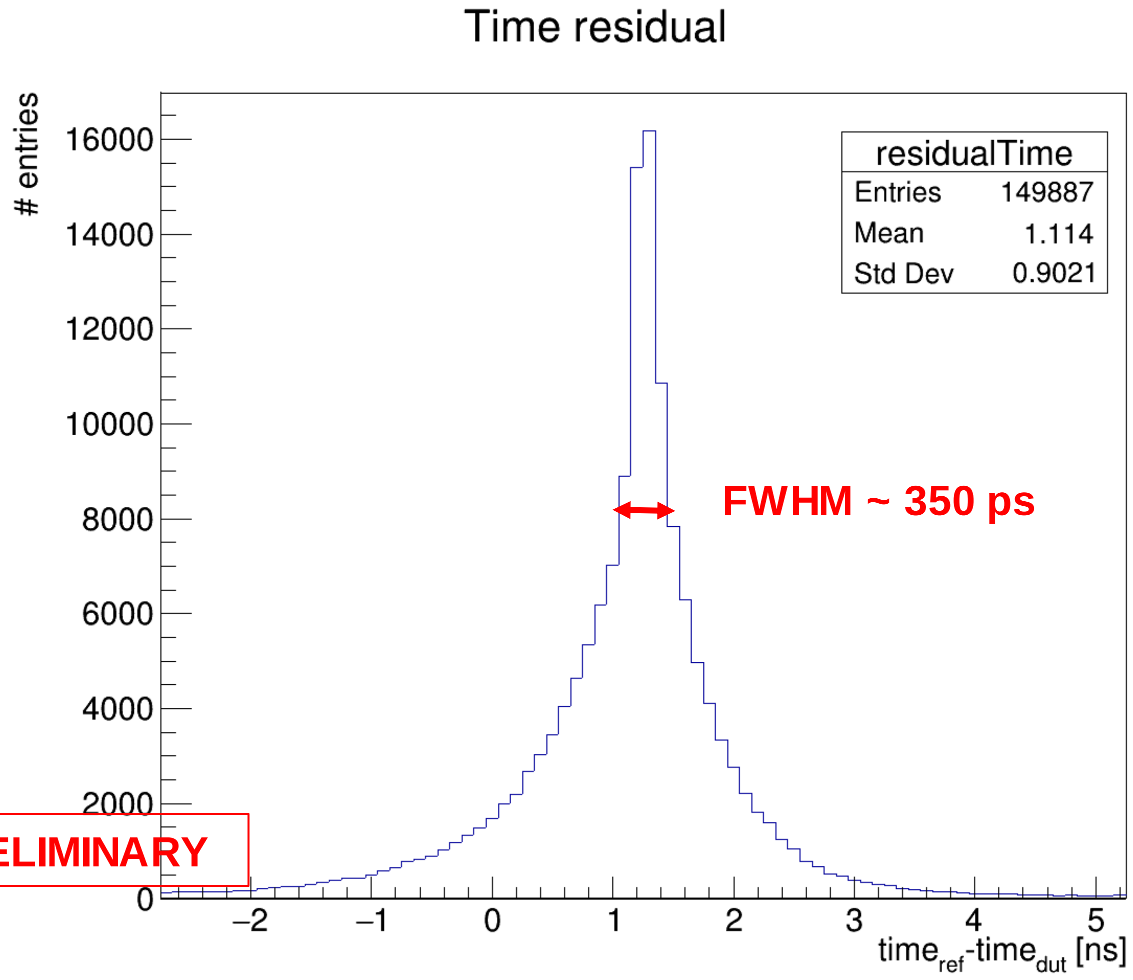
Run 1821

(2.95 OV, 0C)

dSiPM1-dSiPM0

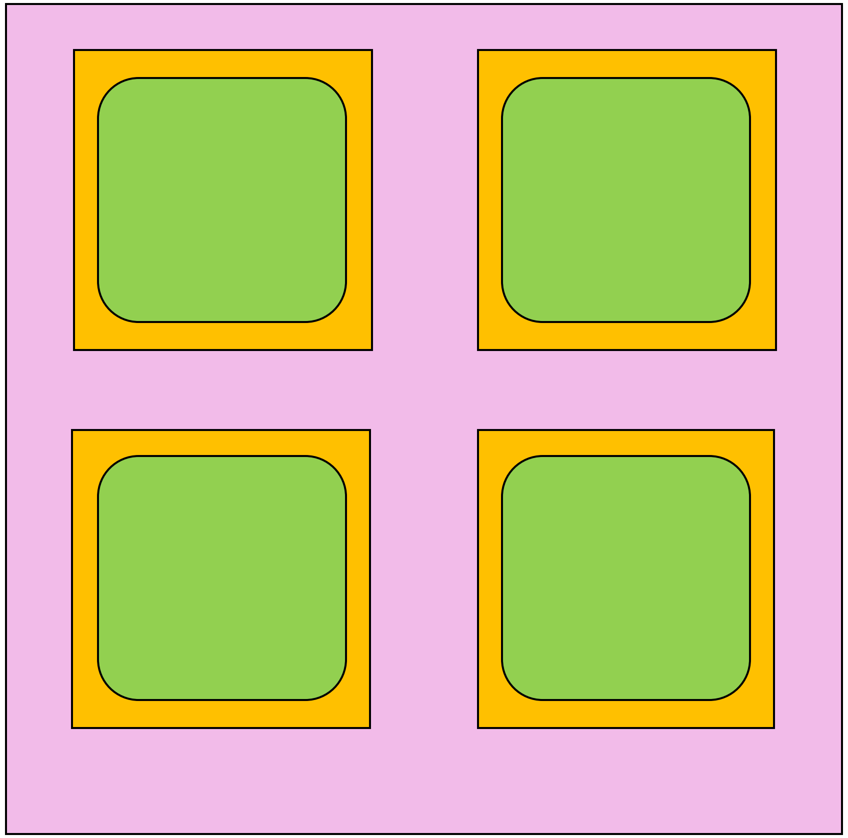
LYSO200 – LYSO100



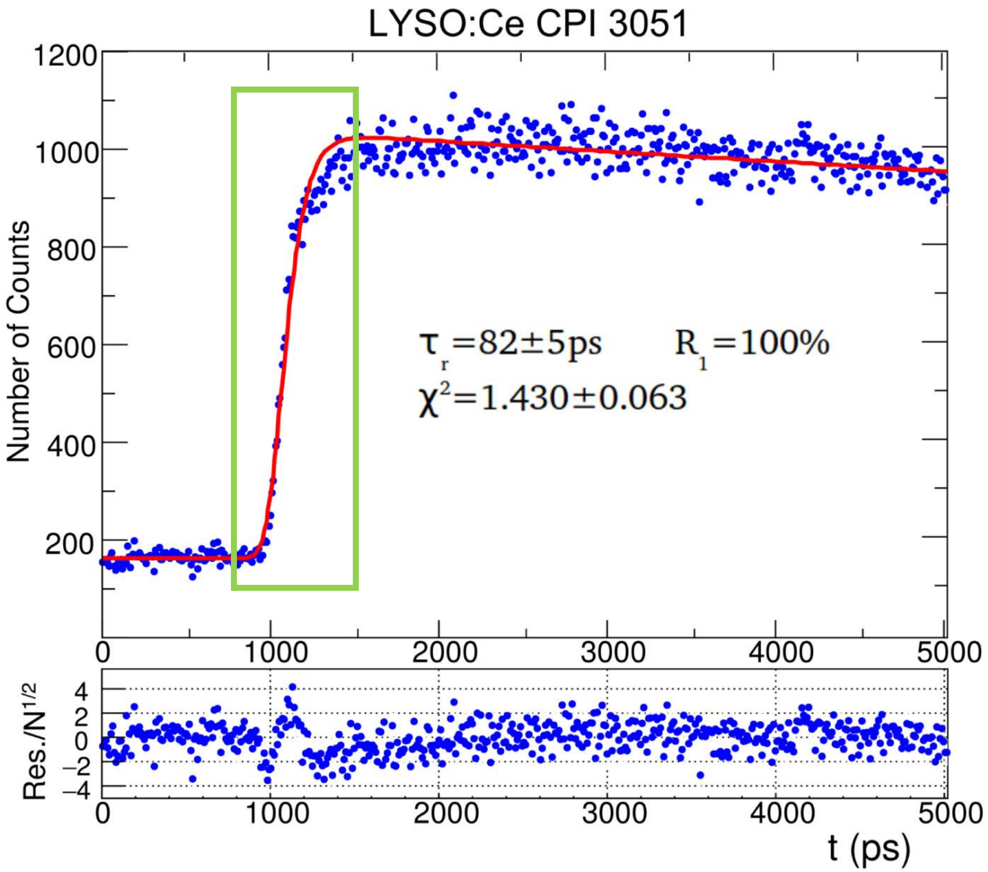


Timing considerations

Time Residuals components



https://www.sciencedirect.com/science/article/pii/S0168900218302286



dSiPM Timestamp: Fast, Slow, None

LYSO Timestamp: Fast if we catch one prompt ph

Updated Version of Time Residuals

PRELIMINARY

Interesting outcome