Concept and Design

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Technology – GlobalFoundries ($90nm \rightarrow 45nm$)

	CMS90WG	45SPCLO
NMOS, PMOS f _T (Hz)	150G / 80G	280G / 230G
Supply Voltage (V)	1.2 / 3.3	1 / 1.8
Data Rates	≤ 50Gbps	≤ 100 Gbps
Electronics	RVT, LVT, DG, Coils	RVT, LVT, UVT, DG, Coils
Photonics (O-band)	MZM, WG, PD, IOSMF	MZM, Rings, WG, IOSMF
Packaging	C4 Bumps	C4, 2.5 / 3D stacking, TSV's



✓ state-of-the-art electro-optical Co-Design environment including photonic models



Concept & Design



- In any process, channel bandwidth is limited by electronics (50Gbps @ 1bit / UI for 45SPCLO)
- One can increase the data rates by advanced modulation scheme PAM-4 (2bits / UI)
 - MZM Concept 1
- An alternative approach to enable high transceiver bandwidth is Wavelength Division Multiplexing without increasing optical fibers
 - **Ring Modulators** Concept 2

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Monolithic Electronic-Photonic IC for Data Transmission Concept 1 - (Global foundries – 90nm SOI CMOS)





25 Gbaud PAM-4
7 pJ / bit



- 25 Gbaud PAM-4
- 0.8 pJ / bit
- PAM-4 can be realized either electrically or optically
- Optical is chosen to keep the design complexity to low
- Large voltage swings, High power consumption
- Large footprints, Large device capacitance,

Concept & Design – Micro Ring Modulator (MRM)



- Because only a selected wavelengths will be at resonance within the loop, RM functions as a filter.
- Small footprint (7.5u x 40u), low device capacitance and low power consumption
- Very sensitive to temperature variations, thermal tuning is needed

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Concept & Design – Concept 2 - Dense Wavelength-Division-Multiplexing (DWDM)



- Attractive approach to realize high data rates up to 50 Gbps per single fiber
- Spacing between the channels \rightarrow 2.1nm
- highly efficient integrated heating elements to tune their resonant wavelengths to the desired WDM channels

Concept & Design – Serializer, Driver



• 10:1 Serializer

- Flipflops, Latches are custom made
- Data rates up to 12.5 Gbps



• Asymmetric differential driver



Concept & Design – Serializer, Driver, Layout



- Serializer + Driver: 62u x 11u
- Serializer + Driver: 240 fJ / bit
- Heater power: ~ 400 fJ / bit
- Control circuit: ~ 140 fJ / bit

@ 50Gbps

Power (pJ / Bit)	Concept 1	Concept 2
Driver	7	3.12



Concept & Design - Submission

• Test chip would be an optical transceiver (concept 2) targeting data rates up to 50 Gbps



- Design work is in progress Desy
- Process (Photonics devices) is still in development (6 PDK's) GF
- Planned to submit in 02/2025