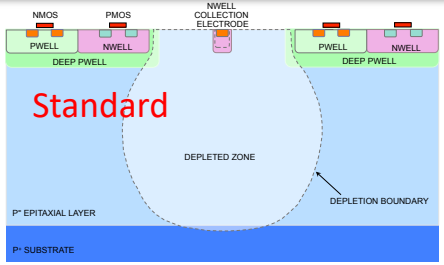
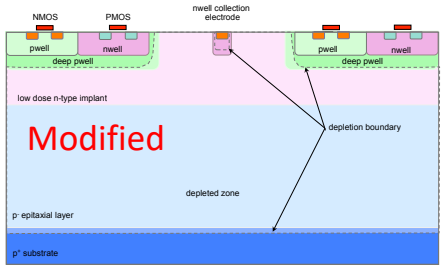
CE65 Measurements and Results

- Introduction
- CE65-v1
  - Pixel pitch impact
  - Process impact
- CE65-v2:
  - Pixel pitch impact
  - Process impact
- Digitization

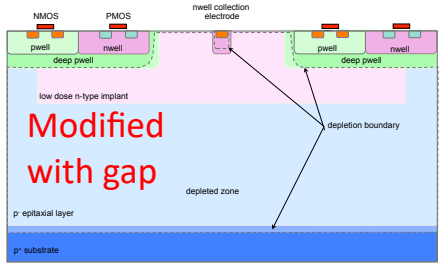
TPSCO 65 nm : BENEFITS AND SPECIFITIES

- Benefits : 65 nm vs 180 nm
  - Better spatial resolution due to smaller feature size
  - Larger wafers : 300 mm vs 200 mm => final sensor : 27x9 cm^2
  - Lower power supply : 1.2 V vs 1.8 V => Low power consumption
  - Lower material budget : thinner sensitive layer (~ $10\mu m$)
- Provides 2D stitching
- 7 metal layers
- Process modifications for full depletion:
  - Standard (no modifications)
  - Modified (low dose n-type implant)
  - Modified with gap (low dose n-type implant with gaps)





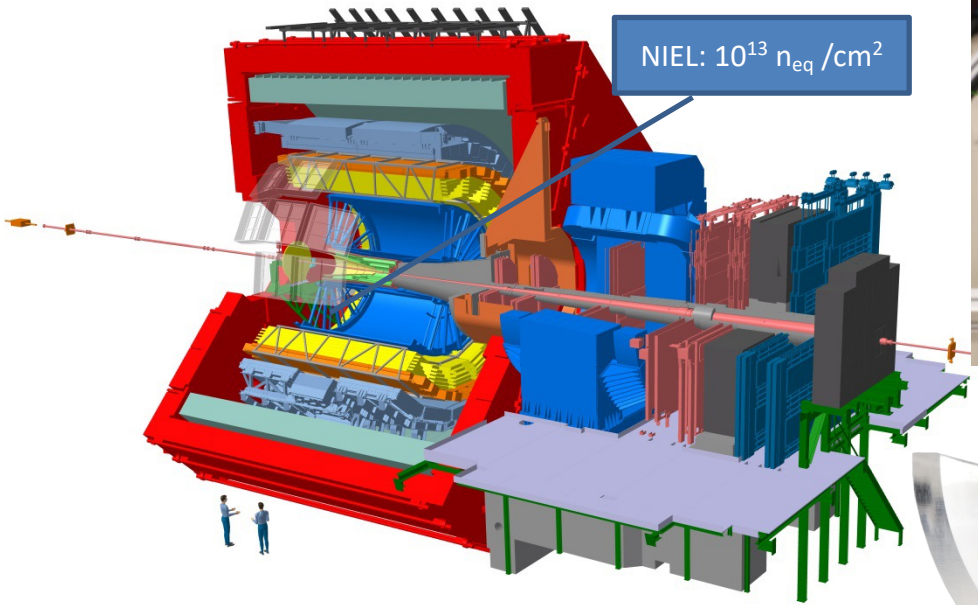
https://doi.org/10.1016/j.nima.2017.07.046

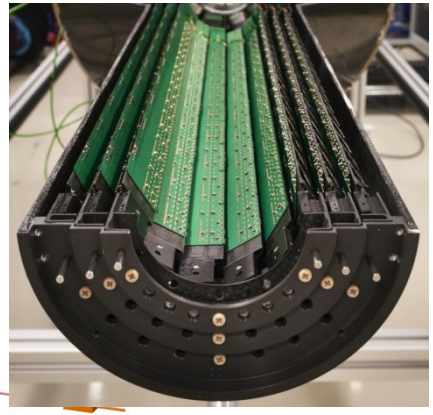


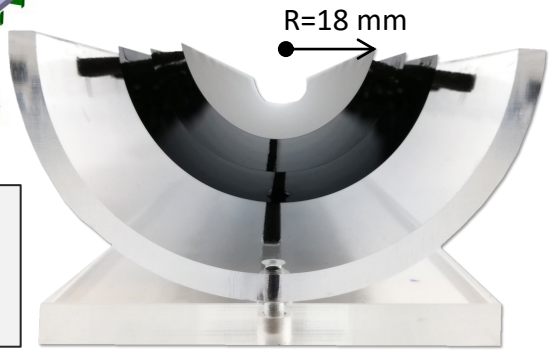
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

ALICE DETECTOR LS3 UPGRADE: ITS2 (180 nm) → ITS3 (65 nm)

R. Ricci, PSD 2023







ALICE – general purpose detector at LHC:
- Tracking (100 MeV/c – 100 GeV/c)
- Particle identification: π, K, p, e (0.1 – 50 GeV/c)

ITS2:

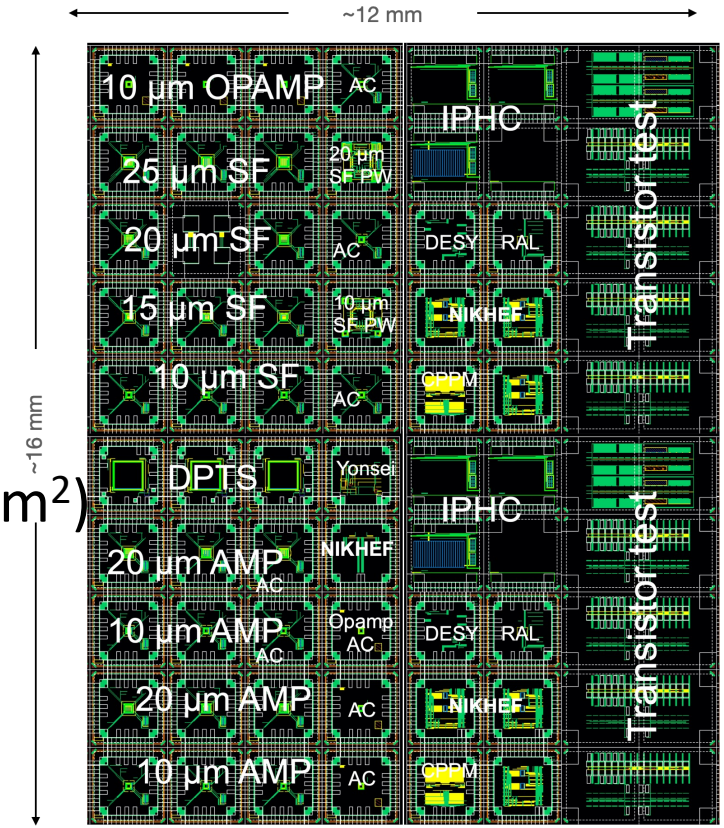
(S.Beolé, iWoRiD 2022)
- 7 layers of MAPS
- TJ 180 nm CMOS
- 12.5 Giga pixels
- Pixel size: 27×29 µm^2
- Water cooling
- **0.3 % X_0 / inner layer**

ITS3

(M. Šuljić, iWoRiD 2023)
- 4 outer layers of ITS2
- 3 new fully cylindrical inner layers
  - Sensor size up to 27×9 cm
  - Thickness <= 50 µm
  - No FPCs
  - Air cooling in active area
- **0.05 % X_0 / inner layer**

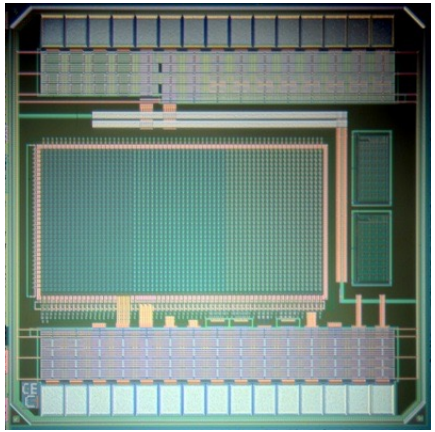
First test submission : MLR1

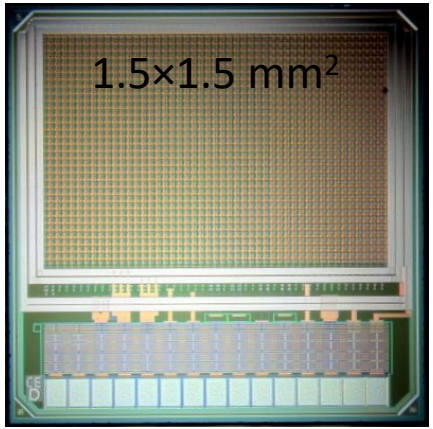
- Submitted in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle (12×16 mm²):
  - 10 transistor test structures (3×1.5 mm²)
  - 60 chips (1.5×1.5 mm²)
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**



CE65 : Circuit Exploratoire 65 nm

- 2 matrix sizes
  - 64×32 with 15 µm pitch
  - 48×32 matrix with 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - **Standard process 15 µm pitch**
  - Modified process 15 µm pitch
  - **Modified process with gaps 15 µm pitch**
  - Standard process 25 µm pitch
- Fabrication in September 2021
- Presented results from CERN PS beam test : May 2022





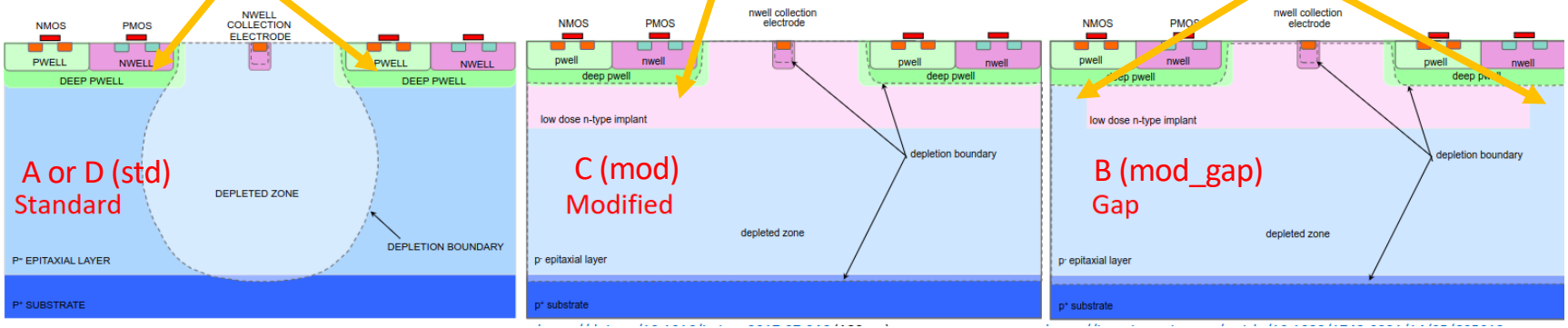
CE-65 nm VARIANTS: PIXEL PITCH AND PROCESS

Variant	Process	Pitch	Matrix	Sub-matrix
CE65-A	std	15μm	64×32	AC/21, DC/21, SF/22
CE65-B	mod_gap	15μm	64×32	AC/21, DC/21, SF/22
CE65-C	mod	15μm	64×32	AC/21, DC/21, SF/22
CE65-D	std	25μm	48×32	AC/16, DC/16, SF/16

Prevent circuitry's nwells from collecting charge

To obtain a full depletion

To overcome the weak electric field near the edges



Beam test setup

Telescope:

Reference Arms : 4 ALPIDE planes for track reconstruction

DUT : CE65

TRG : DPTS

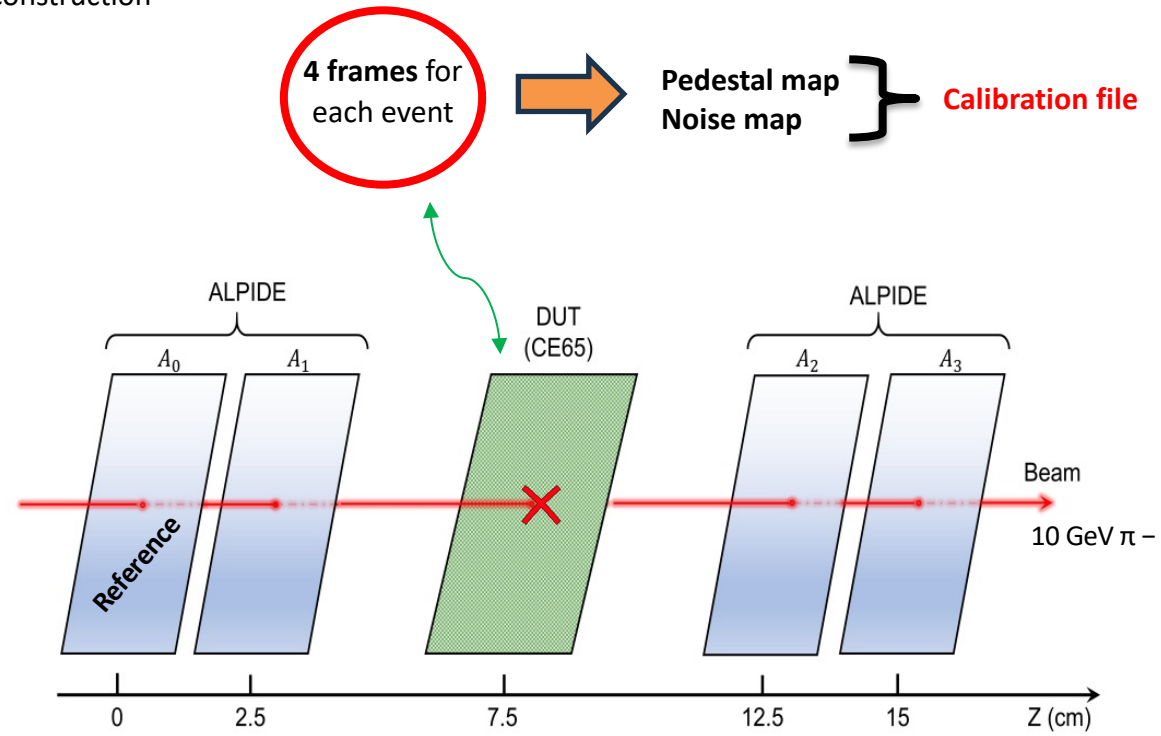
Test beam:

May 2022 at CERN-PS

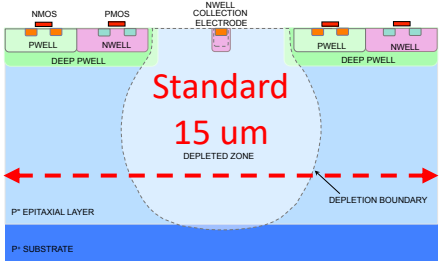
Data acquisition:
EUDAQ2
Event reconstruction algorithm and data analysis framework:
Corryvreckan

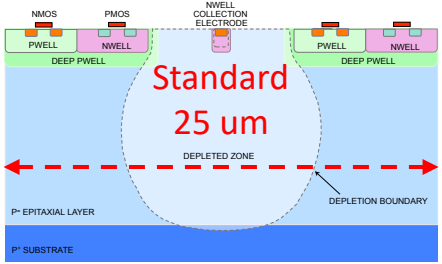
Noise run-**Beam** run:
correlated double sampling method (**CDS**)

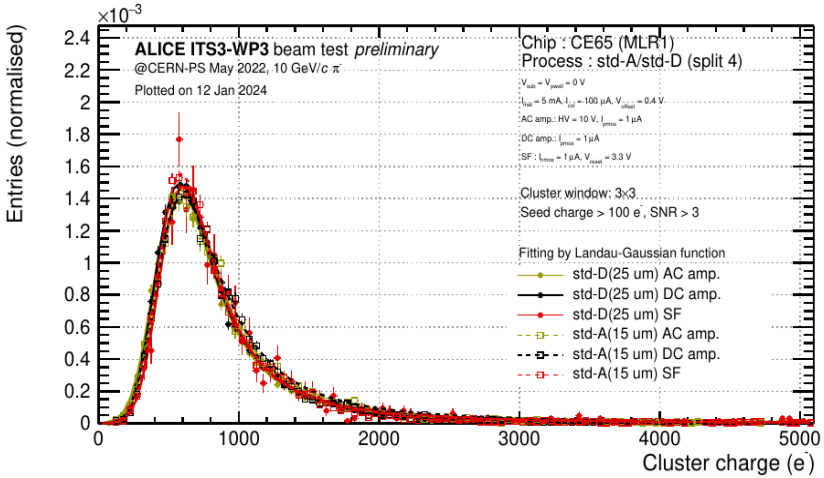
Support provided by Alice Collaboration

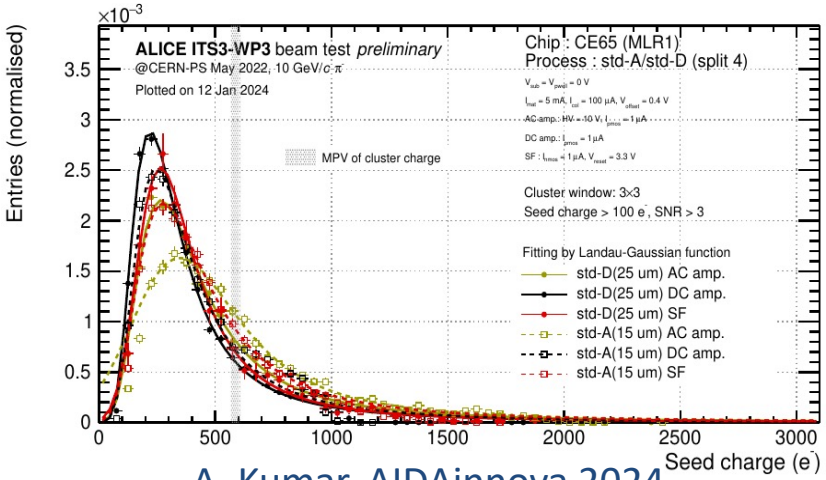


PIXEL SIZE IMPACT



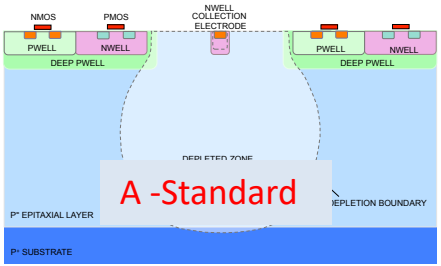


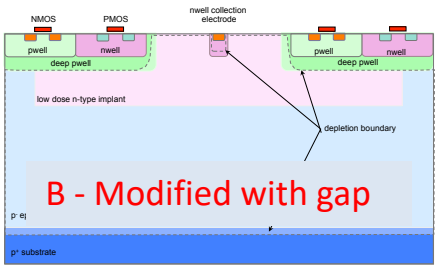


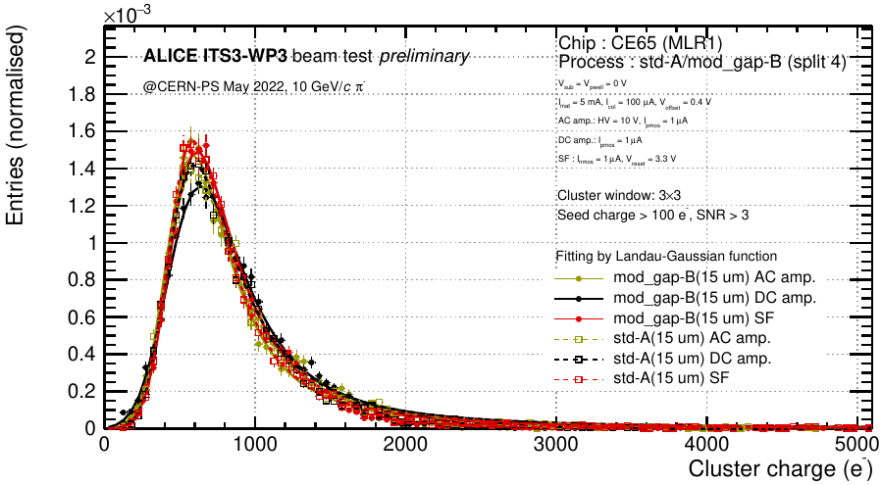


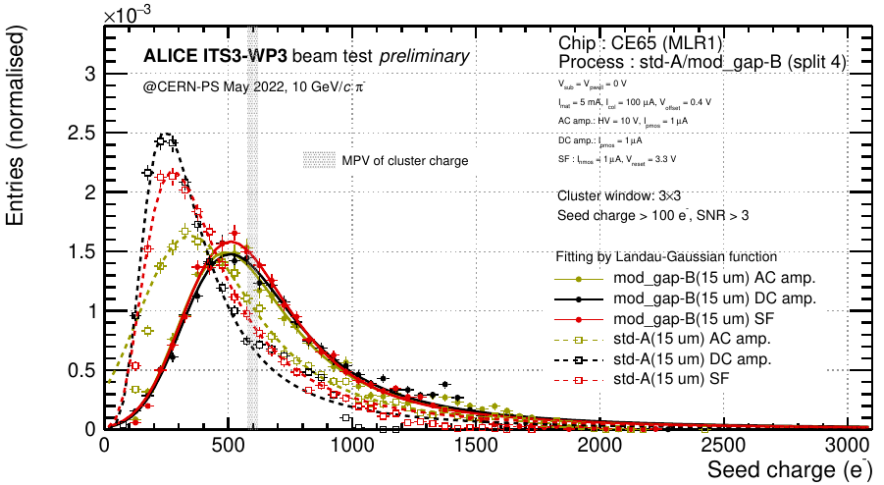
A. Kumar, AIDAinnova 2024

PROCESS MODIFICATION IMPACT

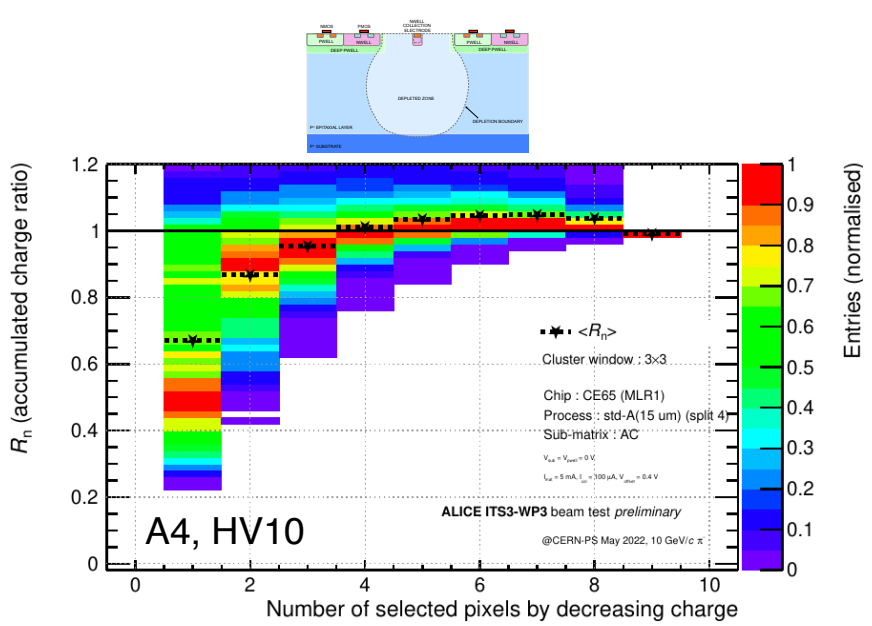


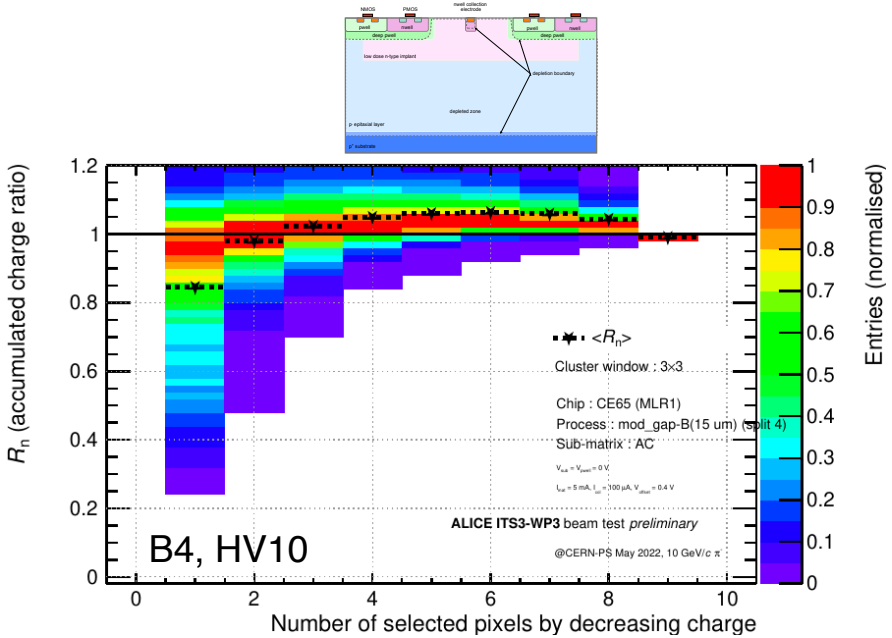






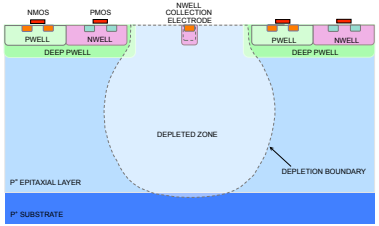
PROCESS MODIFICATION : CHARGE SHARING

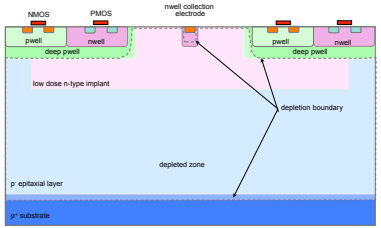


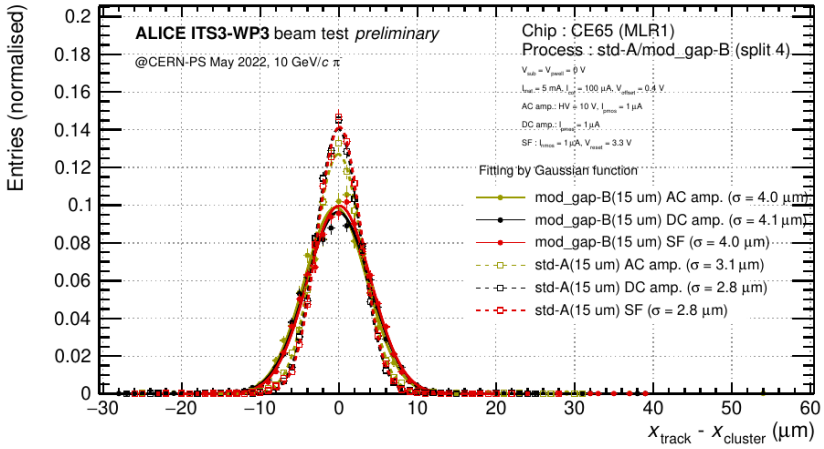


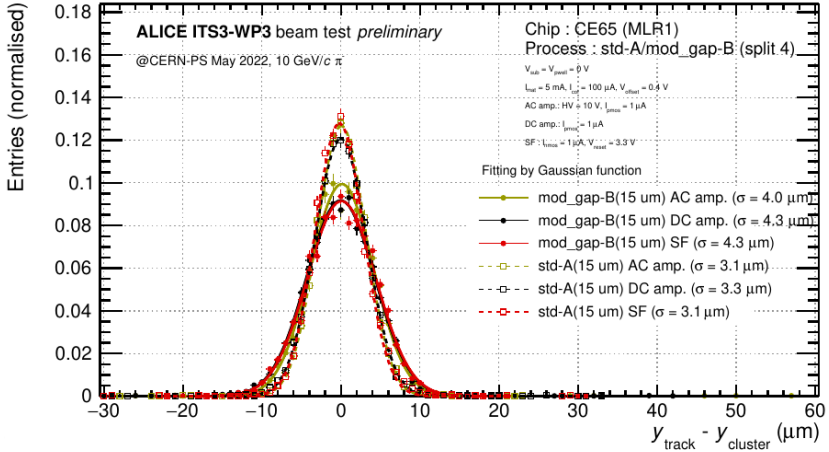
Charge sharing (std) > Charge sharing (mod)

PROCESS MODIFICATION : SPATIAL RESOLUTION





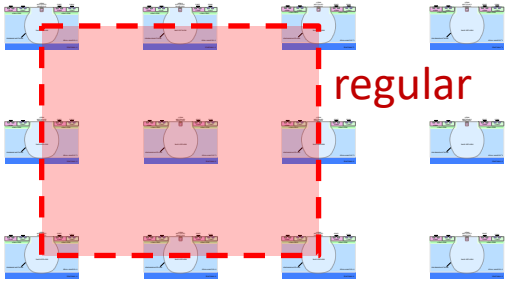


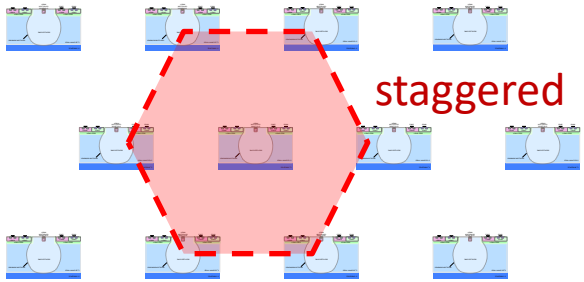


Residual (std) < Residual (mod)

NEXT … CE65 (v2)

- AC-coupled only
- Three processes (STD, GAP, BLANKET)
- Three pixel pitch values (15 um, 18 um, 22.5 um)
- Pixel arrangement





- An option for window readout
- Beam tests done @ SPS (April 2024) & ongoing @ DESY

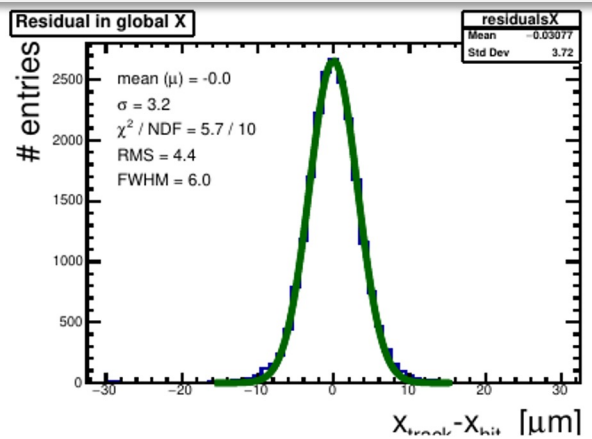
Objective : Mesure the spatial resolution as a function of the pixel's pitch and geometry

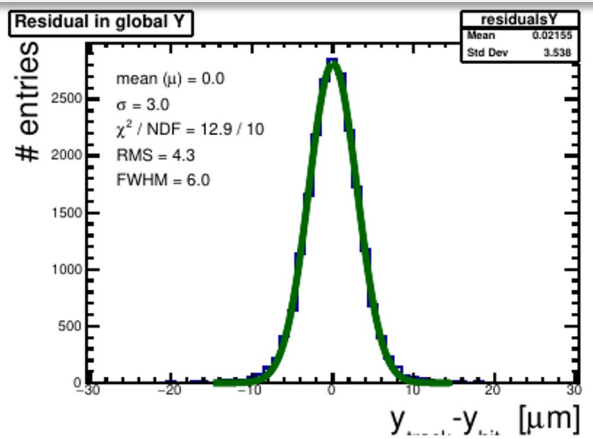
Chips that were tested (HV: 4 V & 10 V)

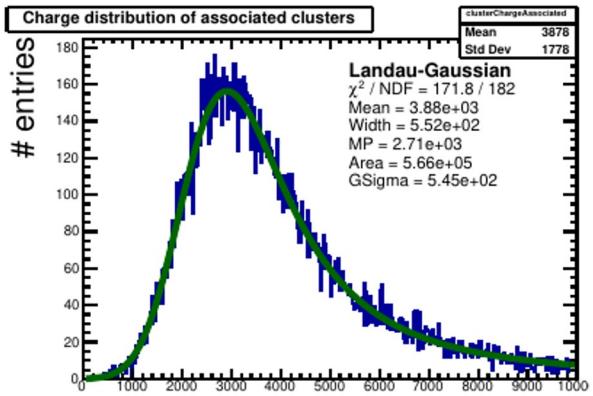
- 22.5 GAP SQ - PCB7 (Prague)
- 22.5 STD SQ - PCB18 (Zurich)
- 18 GAP SQ - PCB2 (Strasbourg)
- 18 STD SQ - PCB23 (Prague)
- 15 GAP SQ - PCB19 (Zurich)
- 15 STD SQ - PCB6 (Zurich)
- 22.5 GAP HSQ - PCB5 (Strasbourg)
- 22.5 STD HSQ - PCB4 (Strasbourg)
- 18 GAP HSQ - PCB3 (Strasbourg)
- 18 STD HSQ - PCB24 (Strasbourg)

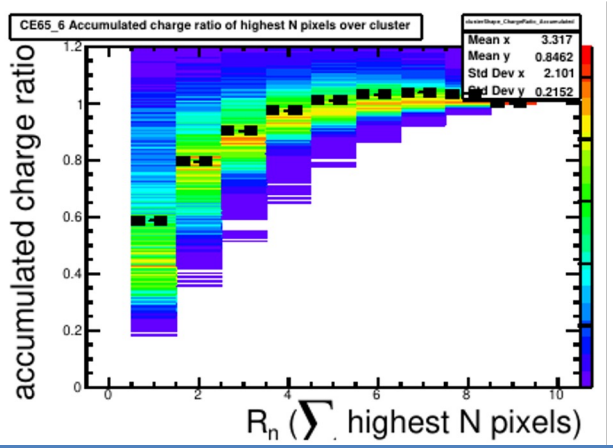
Bonus: additional runs were performed with a high number of events to study in-pixel resolution

PCB18, 22.5 µm, STD, SQ

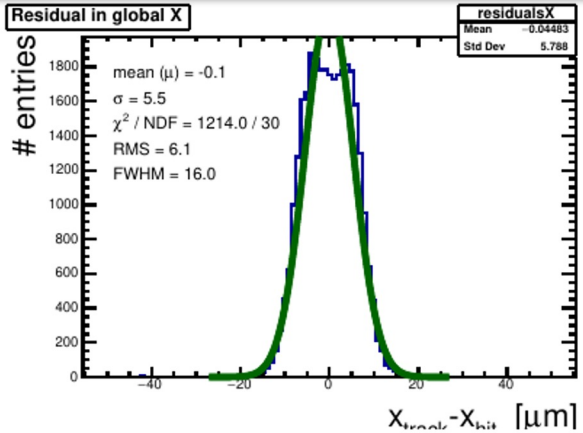


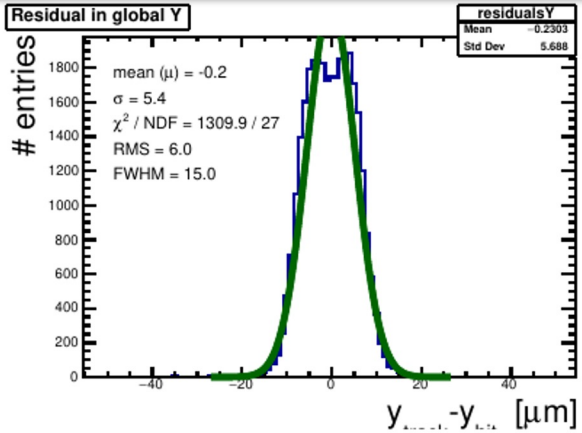


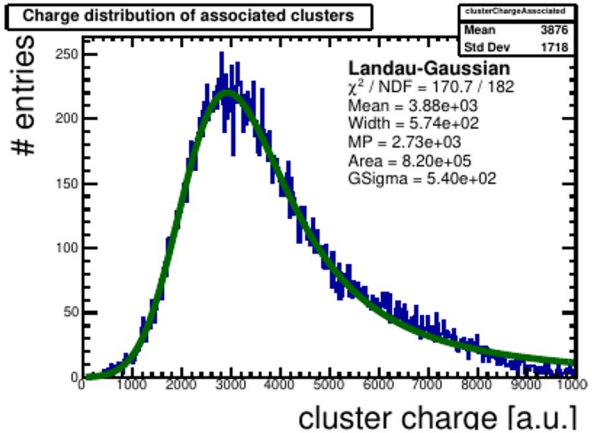


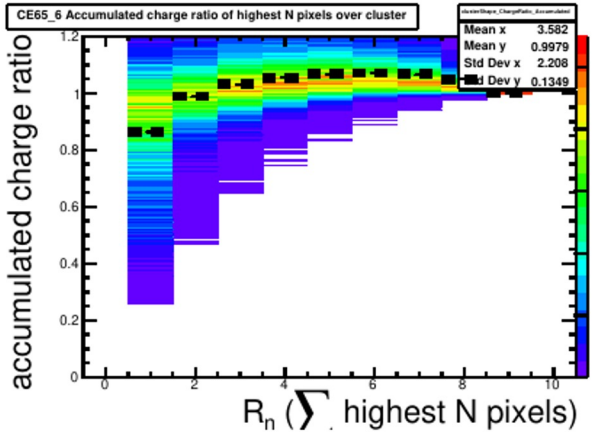


PCB10, 22.5 µm, GAP, SQ









Spatial resolution summary

PCB	Geo	Process	Pitch(um)	HV(V)	Sp. Res.(um) (telescope resolution subtracted)
10	SQ	GAP	22.5	10	~5.1
02	SQ	GAP	18	10	~4.1
19	SQ	GAP	15	10	~3.2
18	SQ	STD	22.5	10	~2.4
23	SQ	STD	18	10	~1.8
06	SQ	STD	15	10	~1.3

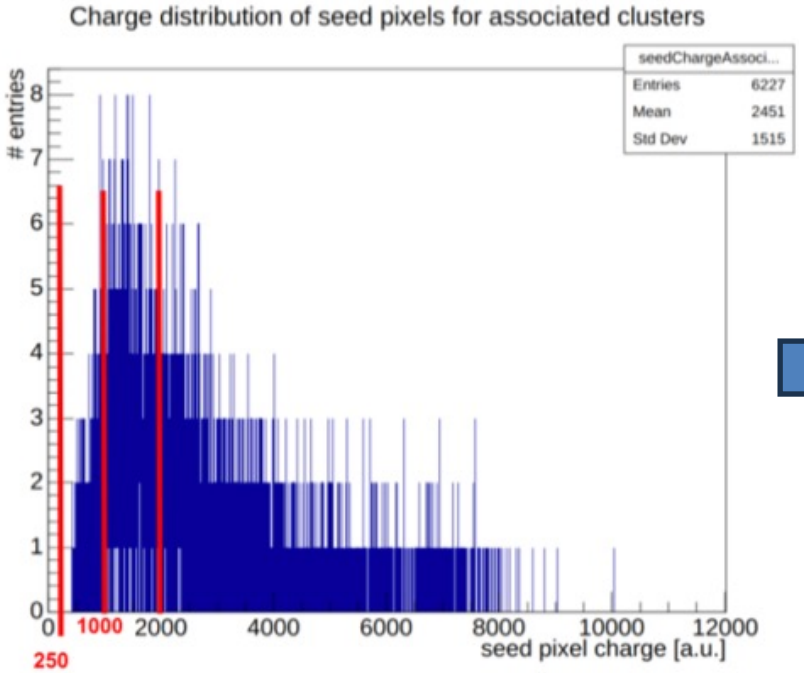
Telescope resolution: **~2.1um** (Calculated from https://mmager.web.cern.ch/telescope/tracking.html)

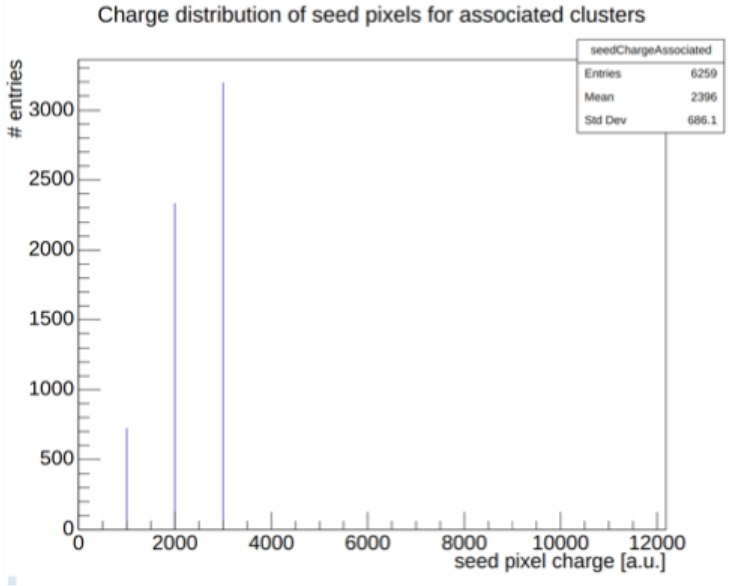
What is required from a sensor?

- Fast Readout → Digital Readout
- Low spatial resolution → Analog Output
- Radiation tolerance…
- etc ….

Is there any trade-off that we preserve the spatial resolution without sacrificing the readout speed?
What if we use two bits for digitization, three or maybe four instead of 1 bit?

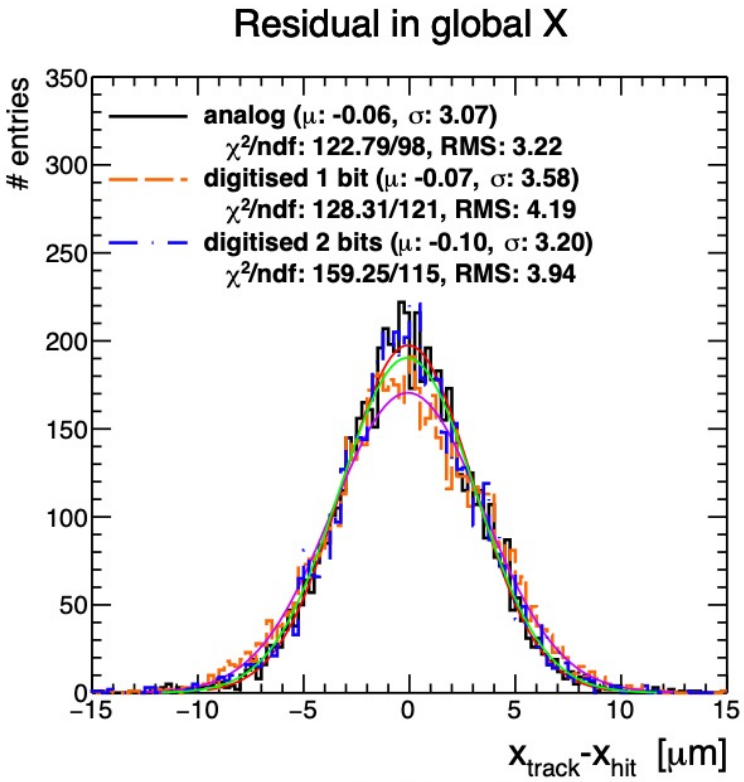
DIGITIZATION* : SEED PIXEL SIGNAL – 2 BITS EXAMPLES

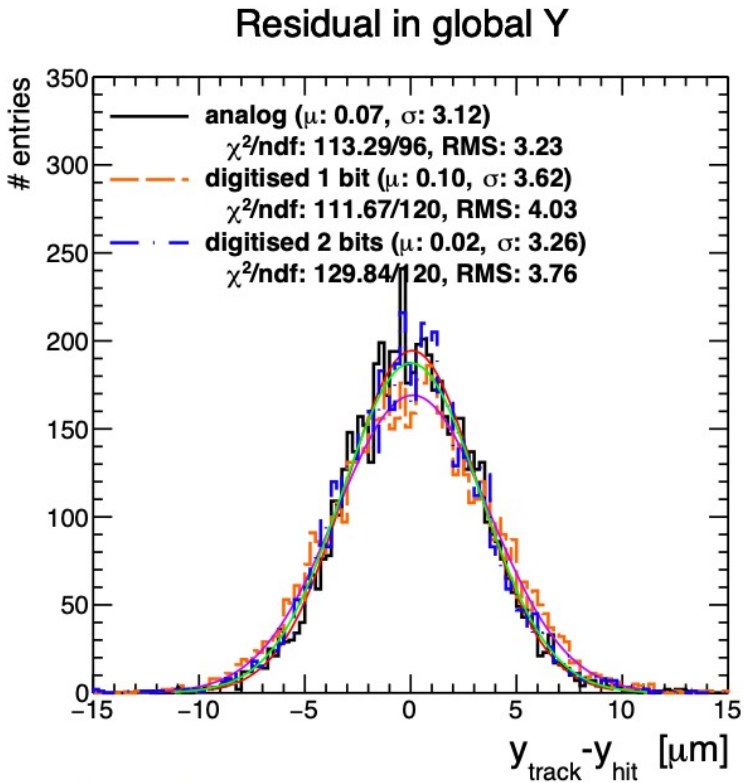




*PhD Gaëlle SADOWSKI

Digitization*: the impact of the number of bits on the position residuals

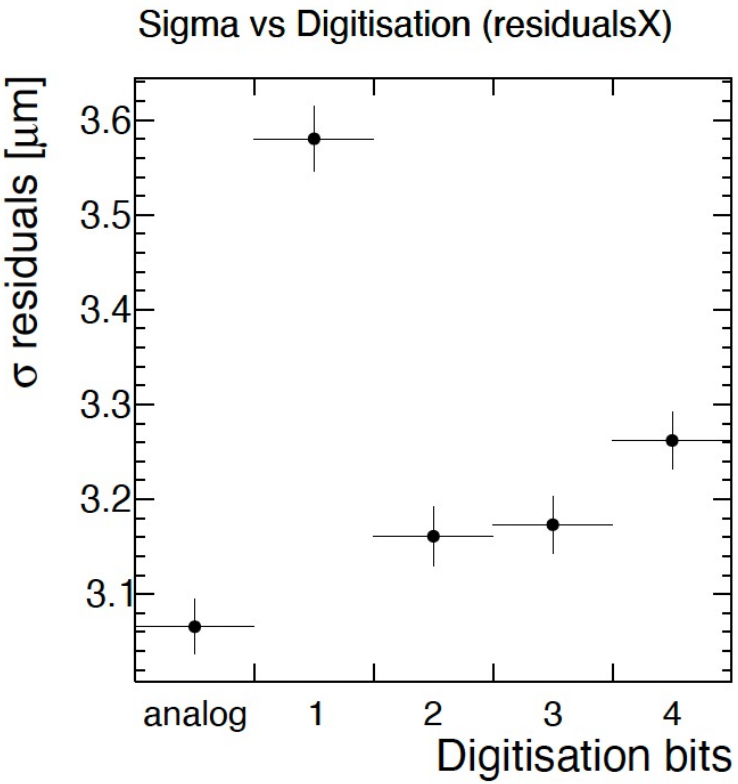


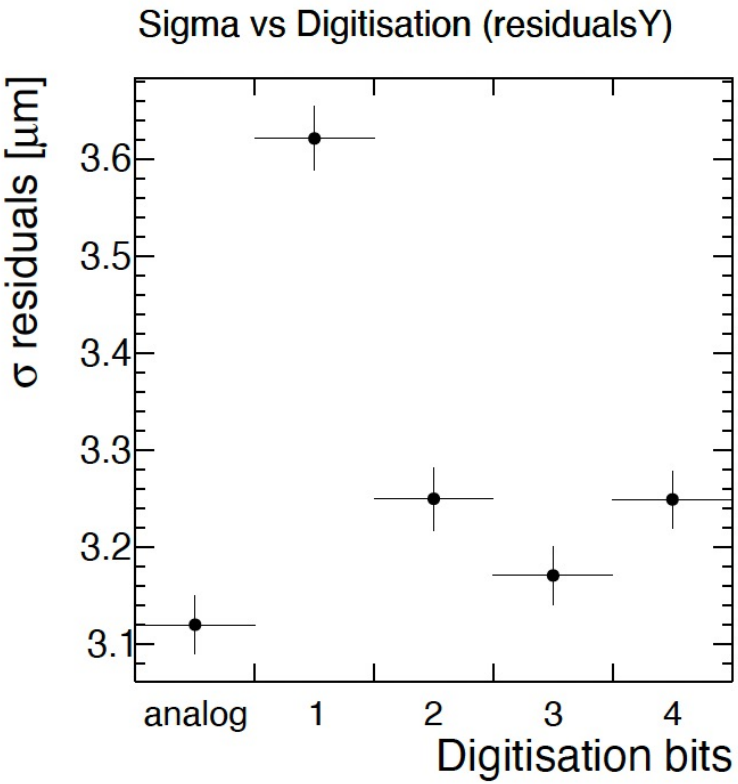


analog → red fit, 1 bit → purple fit, 2 bit → green fit

*PhD Gaëlle SADOWSKI

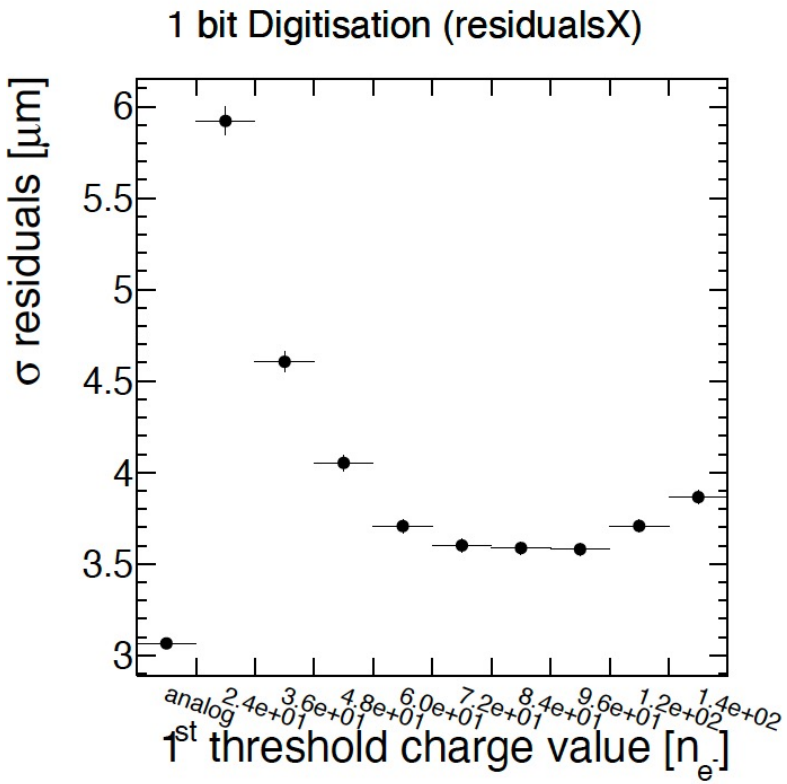
DIGITIZATION*: EFFECT OF N_{BITS}

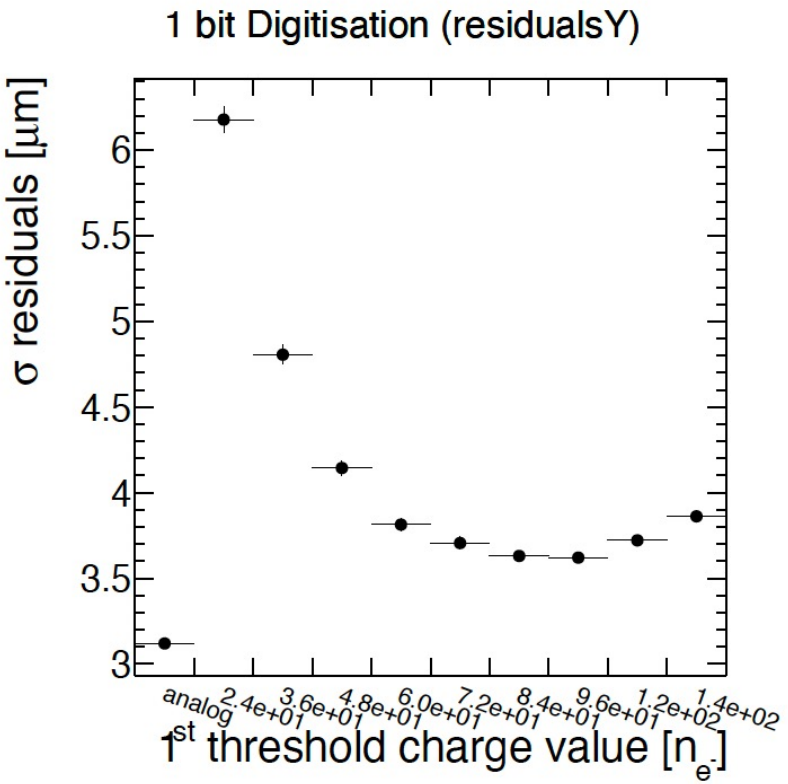




*PhD Gaëlle SADOWSKI

Digitization: Effect of threshold value on the position residuals





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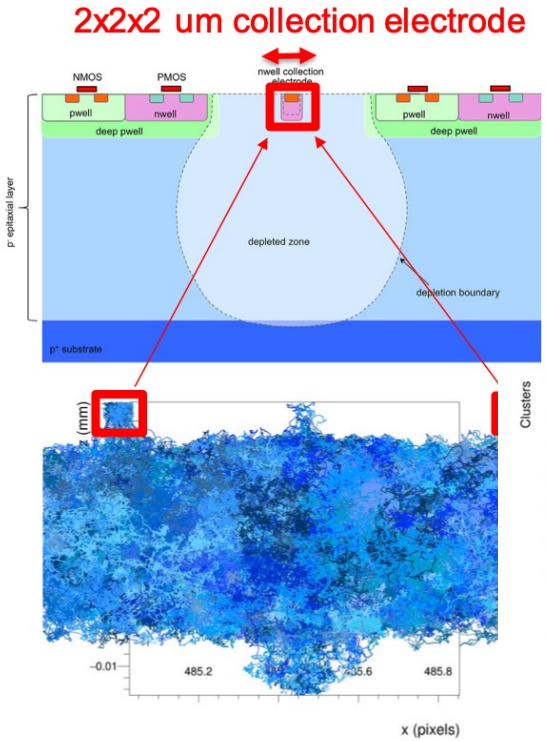
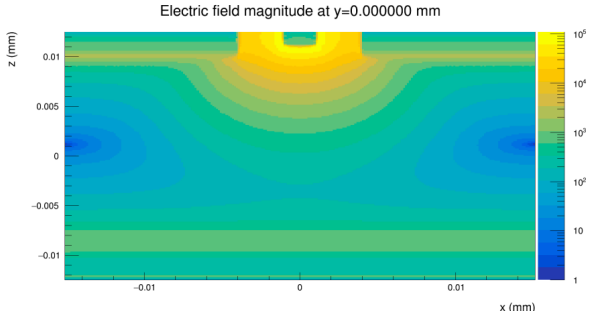
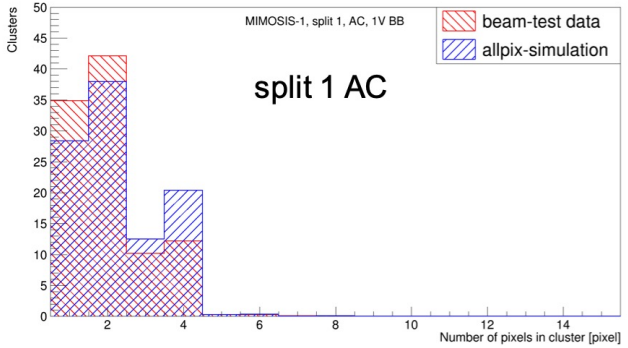
TCAD AND ALLPIX² SIMULATIONS : A WORKING GROUP IN DRD3

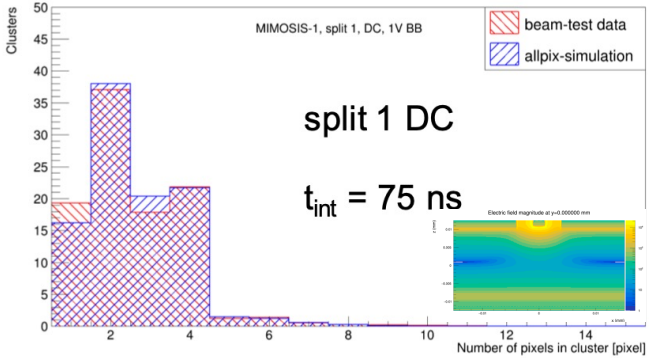
Hasan Darwish, DPG 2024

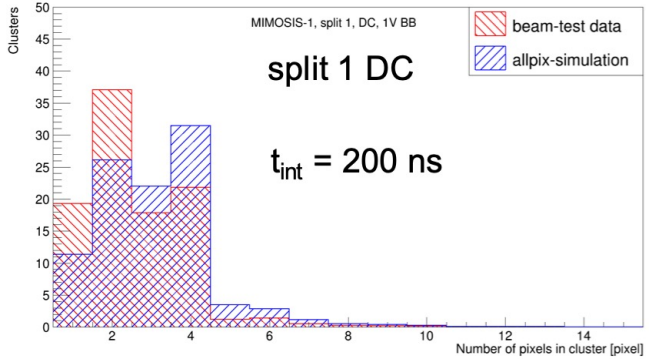
@ IPHC











TCAD AND ALLPIX² SIMULATIONS : A WORKING GROUP IN DRD3

https://arxiv.org/pdf/2303.18153.pdf

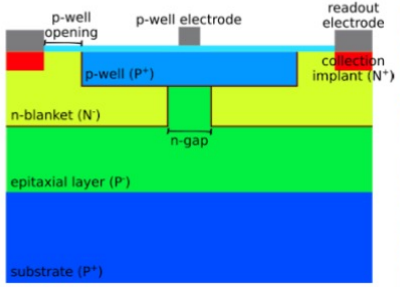


Fig. 1: *n*-gap layout example of the Tangerine sensor.

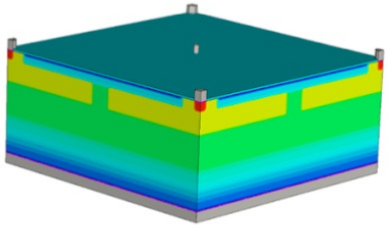
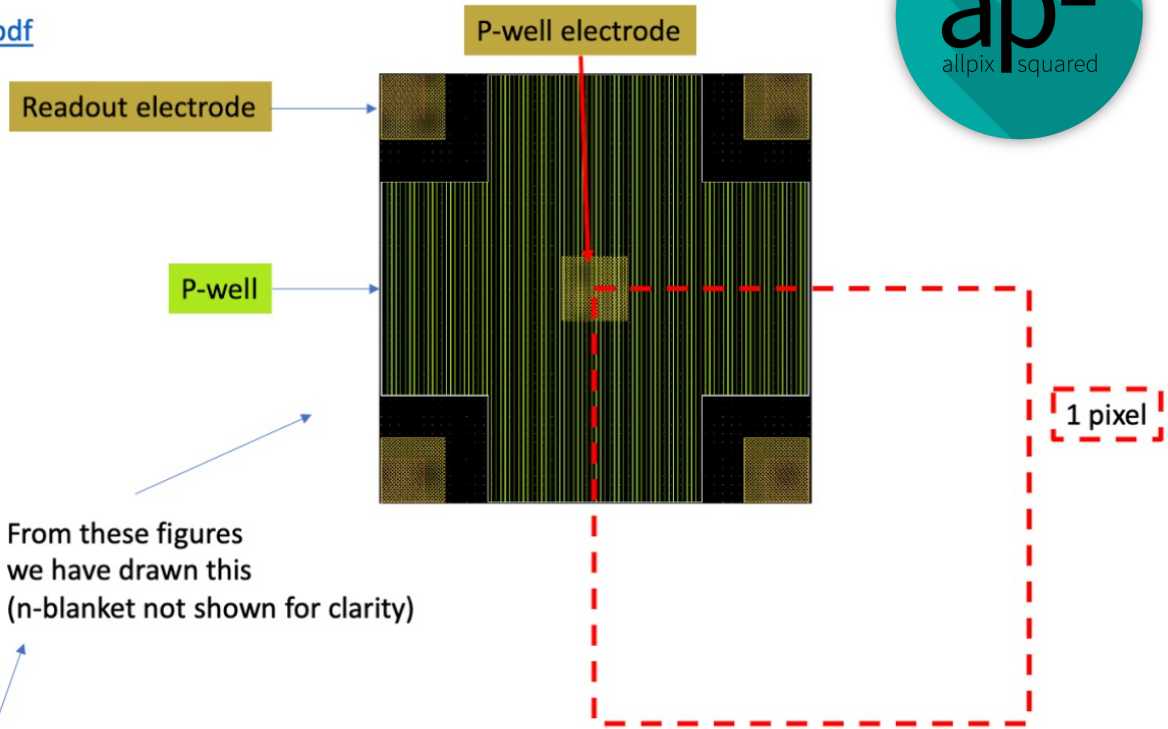


Fig. 2: Generic 3D TCAD simulation of the *n*-gap layout.



From these figures
we have drawn this
(n-blanket not shown for clarity)

@ APC & UPC
M. Bomben @ F. Voisin

Credits to Fabrice for the layout file

TCAD AND ALLPIX² SIMULATIONS : A WORKING GROUP IN DRD3

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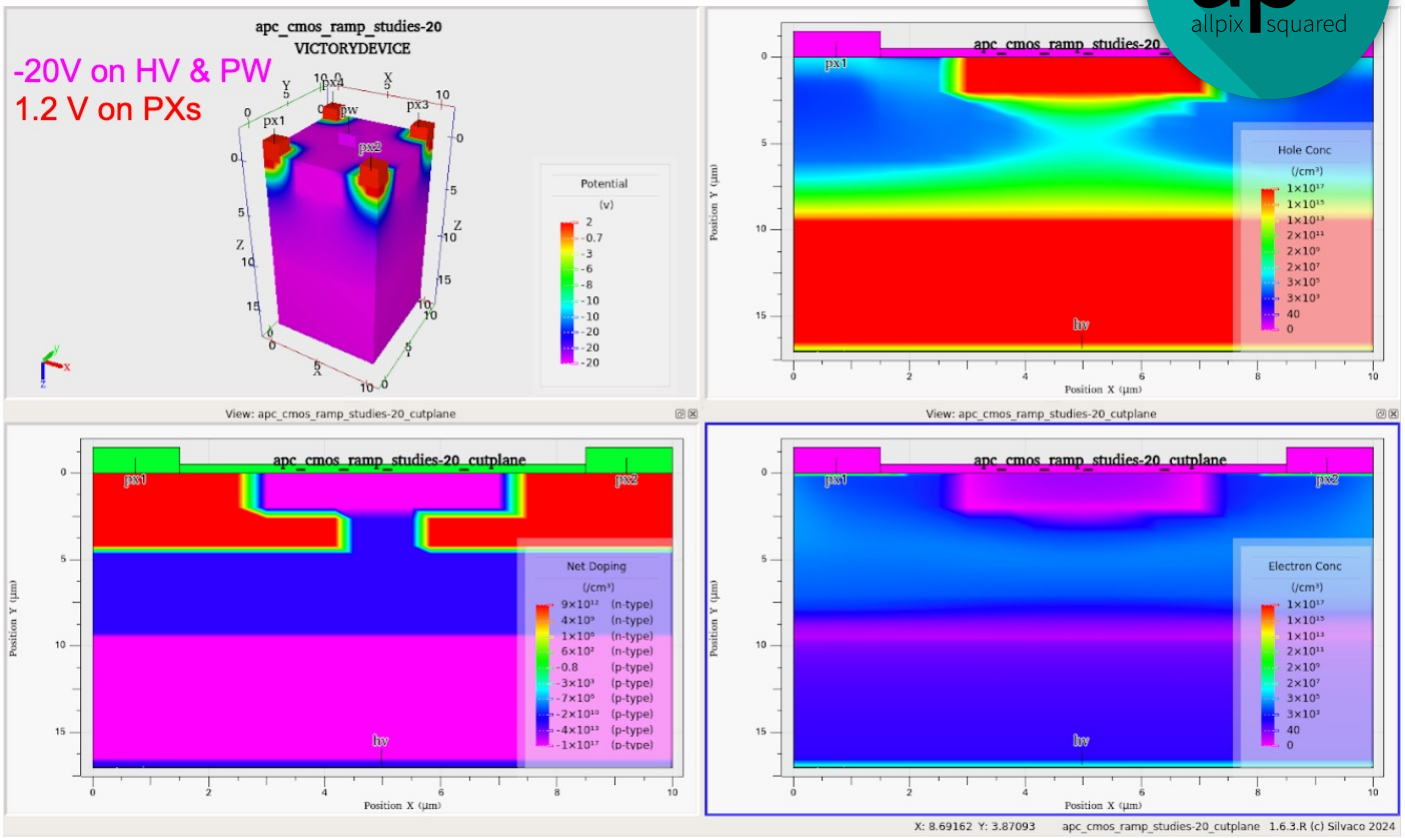
M. Bomben @ F. Voisin



- 65 nm Technology is being scrutinized
  - ✓ Impact of pixel pitch
  - ✓ Impact of the process (std, gap, …)
  - ✓ Impact of pixel geometry

- Digitization is on progress

- TCAD and Allpix^2 simulation frameworks have reached an advanced level and are important tools to improve the understanding of mechanisms involved in the charge collection process which will impact the spatial resolution as well as other performances.