IPHC Brainstorming for vertexing

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From brainstorming sessions with many Strasbourg colleagues

Context

- Serie of brainstorming meetings @ IPHC around TPSCo 65 nm
- Started in February and still under going
  - ~ one meeting per month
- C4PI engineers and MAPS user physicists from IPHC are involved
- 2 main tracks
  - Tracking (ALICE3 OT / LHCb UT / FCCee tracker)
  - Vertexing (ALICE3 VD, FCCee vertex)
- Main challenge in vertexing is to reach a ~3 µm spatial resolution

Key data

Specifications: numbers!

	CBM MVD	ALICE ITS3	Belle-II VXD	ALICE3 VTX	ALICE3 tacker	EIC tracker	LHCb UT	FCCee VTX	FCCee tracker
Sensor readiness	2026	2026	2026?	2030?	2027	2027?	2027	~2040	~2035
Total area (m^2)		10	1	0.15	5/57	?	4.5	~1	~50
Techno (nm)	TJ 180	TPSCo 65	TJ 180	TPSCo 65	TPSCo 65	TPSCo 65			
Spatial res. (µm)	**~5**	**~5**	< 10	**2.5**	10/10		O(10 µm)	**3**	~10
Pitch (µm)	27x29	22x22	<40x40	**10x10***	50x50		50x50	**15x15***	50x50
Mat. budget (%X0)	~0,3	**0.05**	**0.15**	**0.1**	1/1	0.05-0.55	<1	**0.15**	**<<1 ?**
Hit rate (MHz/cm^2)	**15-70**	9	**100** triggered	**94**	1.7/0.06	?	**160** 20Gb/s	O(20)	<10
Time figure (ns)	5.10^3	5.10^3	~100	100	100/100	100 (?)	**O(1)**	10^2-10^3	10^2-10^3
Trigger rate (kHz)	-	-	30	-	-	500	-	-	-
Power (mW/cm^2)	<100	**20 (matrix)**	200	70	**20/20**		100-300	**20**	50?
Rad.hard. (kGy) (n_{eq}/cm^2)	30 /year $< 10^{14}$ /y.	3 $3x10^{12}$	100 $5x10^{13}$	3000 **$1.5x10^{15}$** /year	50/2 10^{14}/5.6x 10^{12}	- 10^{15}	**2400** **$3x10^{15}$**	20 $5x10^{11}$	20 $5x10^{11}$
nb of layers			5-6	3	4/4	5 + 5d	3-4	3x2	
bunchX (ns)		25	4			10			

* Assuming binary output

How to reach ~3 µm: Binary outputs and pitch around 10 µm

- Excellent for charge collection efficiency
  - Increase radiation hardness
- Integration is difficult
  - Compact front-end
  - Compact pixel readout
- Power consumption is high
  - Ultra low-power front-end needed
  - Increase collecting diode gain
    - By reducing capacitance while maintaining the same collection efficiency
    - With linear avalanche (First steps in R&D)
    - Close relation with foundry needed
  - Efficient pixel readout needed since number of bits increase (pixel density)
- ALICE3 is looking in this direction for a unique sensor for vertexing and tracking
  - A study group is set up

How to reach ~3 µm: Mutli-bits outputs and pitch around 22 µm

- See Ziad's presentation
- Limited by charge sharing
- Integration is less difficult
  - More room for front-end and readout
  - Need to add multi-bit outputs and readout
- Power consumption is lower
  - More power available for time-accurate front-end
  - Efficient pixel readout needed since number of bits increase (pixel digitisation)
- Optimisation between pitch and number of bits is needed
- Direction in which C4PI moves for vertexing

Front-end consideration

- Large impact on power, detection efficiency and time resolution
- Could be based on DPTS
  - Wide range of biasing for power and time resolution optimisation
  - For 20 mW/cm2 and 22 µm pitch: ~50 nW is available for each front-end
    - No margin for 100 ns time resolution due to timewalk
    - Higher pixel-to-pixel variation with less power
- Another front-end can be developed

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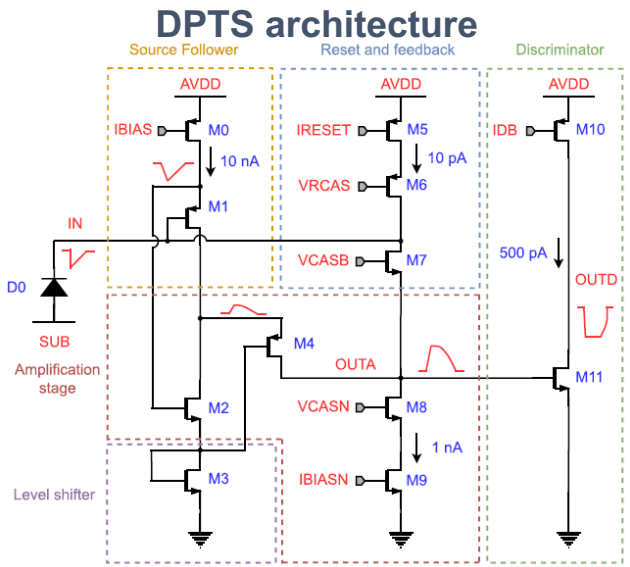

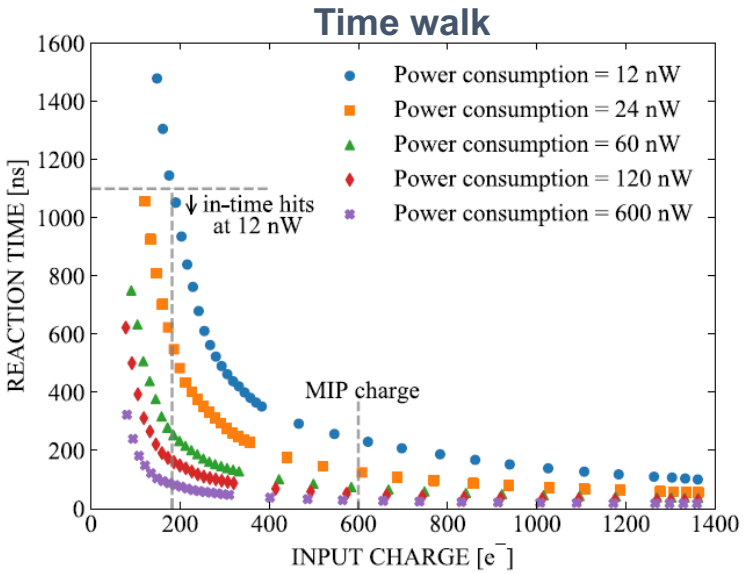

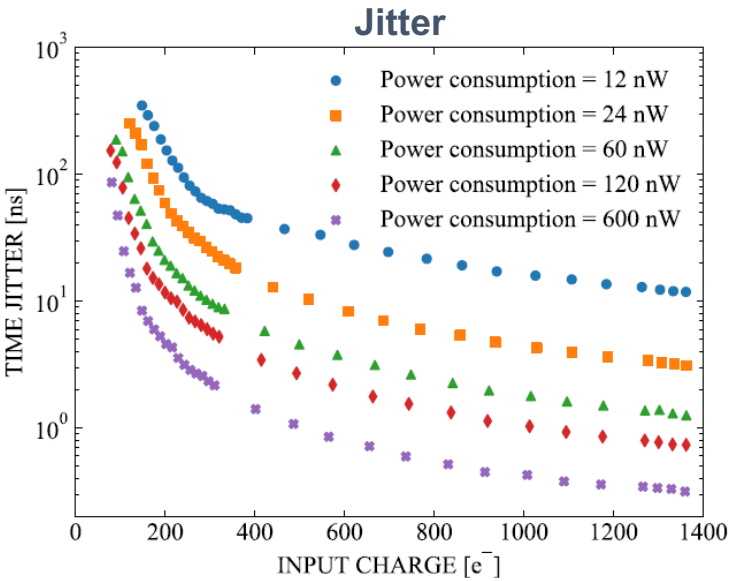

Multi-bits conversion

- ADC
  - Difficult to integrate for high number of bits
  - See Ziad's talk
- Two thresholds (1.5 bits ADC)
  - Easy to integrate
    - Duplicate discriminator branch in ALPIDE like FE
  - Low threshold for charge sharing / High threshold for seed pixel identification
  - Limited performances on spatial resolution
    - Dedicated study needed
    - Timewalk can be used to encode charge value
- Time over threshold
  - Easy to correct timewalk
  - Difficult for in-pixel integration in small pitch
    - Shared VCO
  - Can be done at column level if the readout is asynchronous and fast enough

Pixel Readout consideration

- Data driven readout have the best power/bandwidth ratio
  - Possible hit-rate (>>100 MHz/cm²) surpasses periphery bottleneck
  - This high speed could be used to make rough timestamping
- Column-drain: FEI-3, MONOPIX/OBELIX
  - In-pixel gray-counter + column-hitOR for more precision
  - High power consumption
- Priority encoder: ALPIDE, MIMOSIS, MOSS
  - Timestamp = frame duration (~µs)
  - Compact and low power
- Asynchronous bus: MALTA, MOST
  - Timestamp from digital pulses
- Asynchronous arbiter: (under-development) SPARC
  - Free timestamping of few ns

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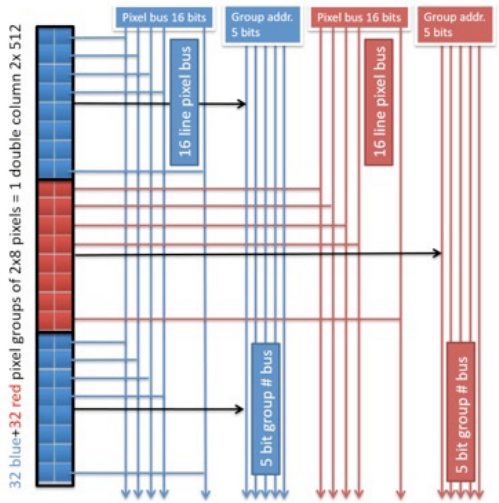
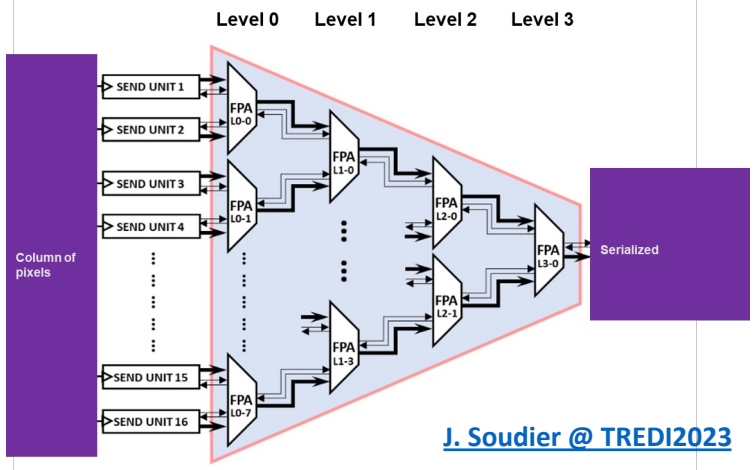
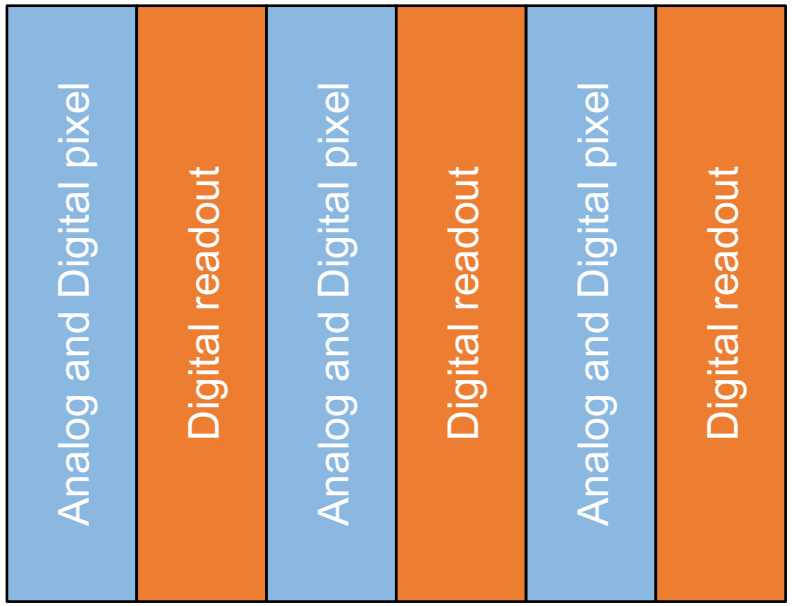


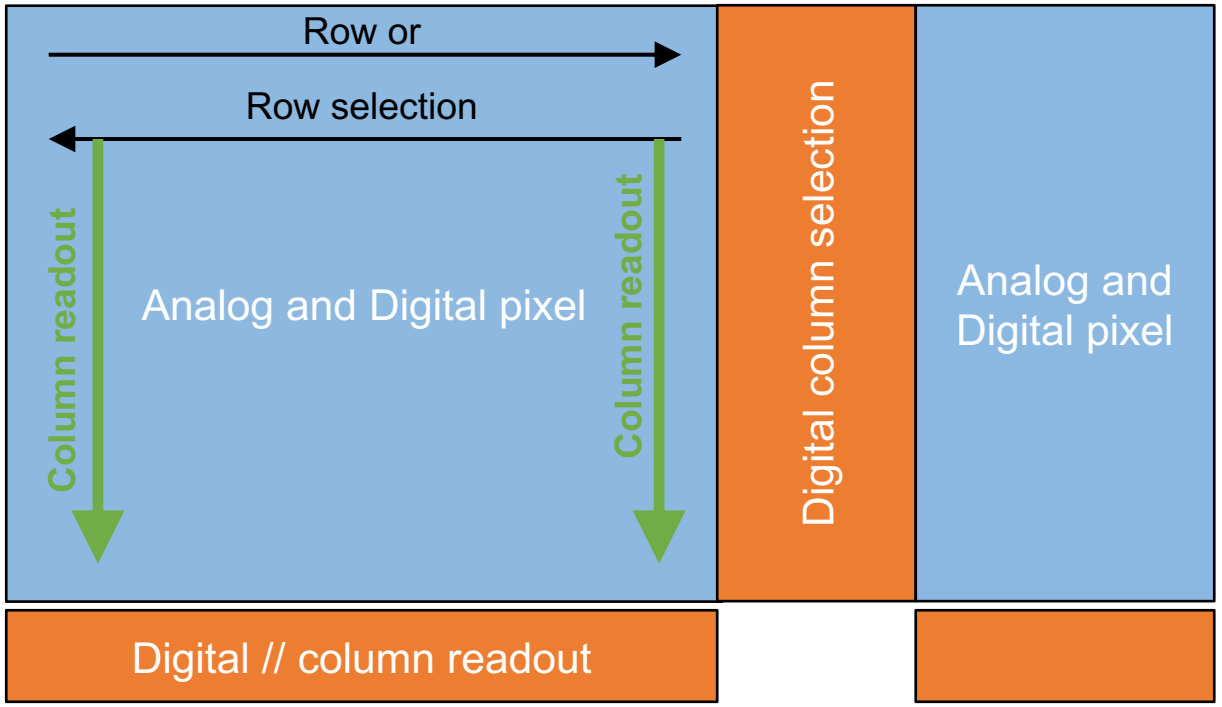


J. Soudier @ TREDI2023

Column or Matrix level readout

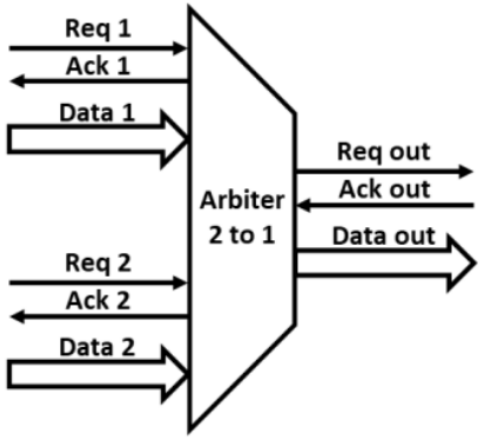
- To reduce the pitch the column readout can be done at matrix level
  - Sacrifice one pixel column to add a digital column selection for sub-matrix
    - Need to add simple digital logic to the matrix (buffering, selection and or logic)
  - Limited hit rate compare to column-level readout
  - MOSS has a pitch of ~18 µm with a yield close to the ~22 µm

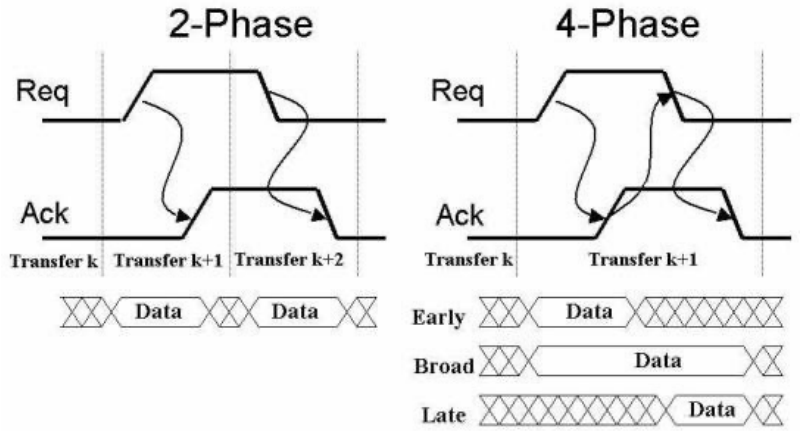


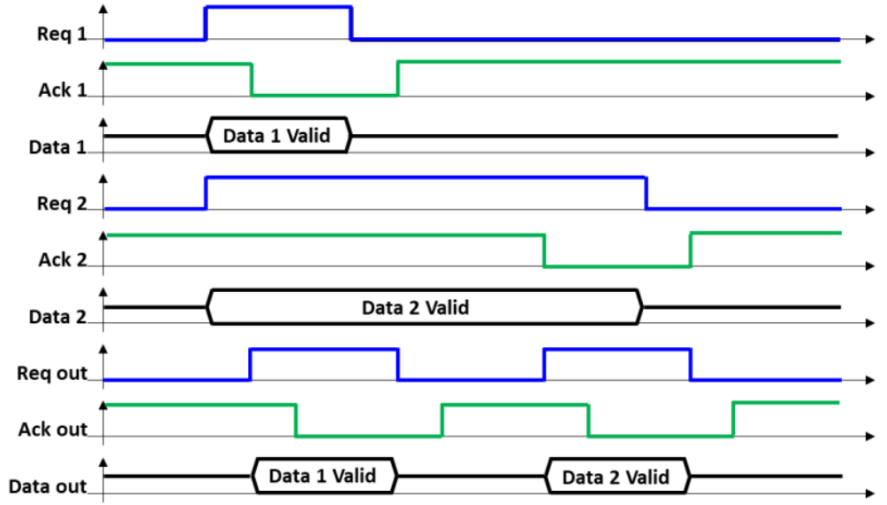


Asynchronous readout: principle

- Based on 4-phase Request / Acknowledge transactions
- Asynchronous arbiter tree builds the address
  - The first event locks the arbiter until it is processed
  - Priority is used in case of simultaneous event
- The event is sent at the matrix periphery as soon as is available
  - Free event timestamping of few ns

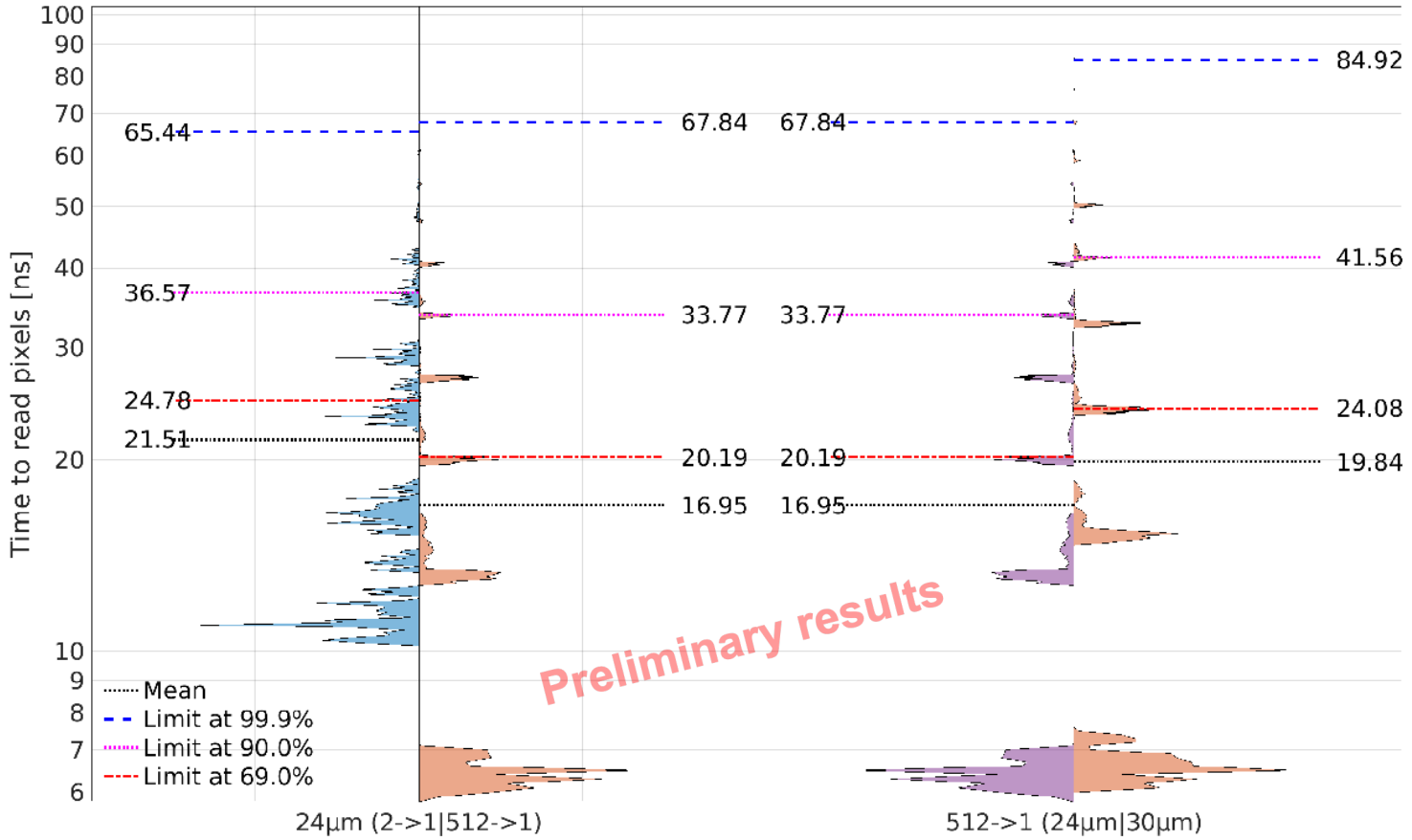






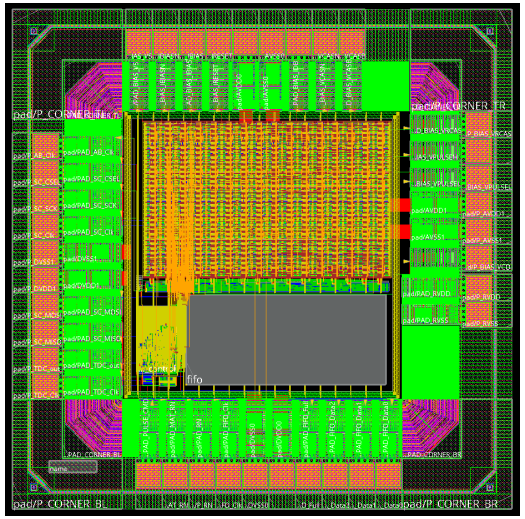
Asynchronous readout: some post-layout simulations

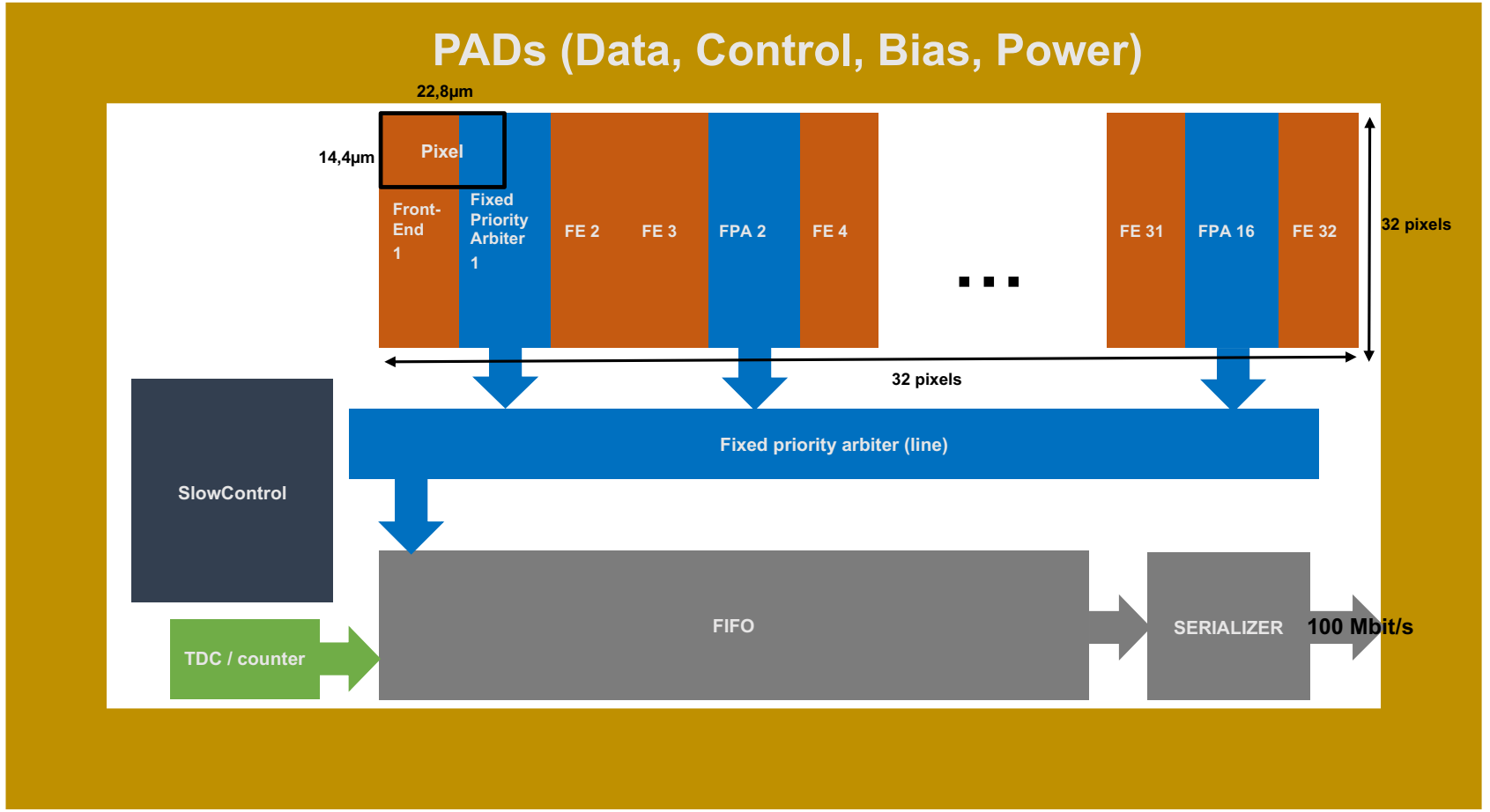
- J. Soudier poster for PISA 2024
- Time to read an event for different physical events
  - 2 different topologies
    - 2->1 and 512->1
  - Large number of events are read in less than 7 ns



SPARC: Quick overview

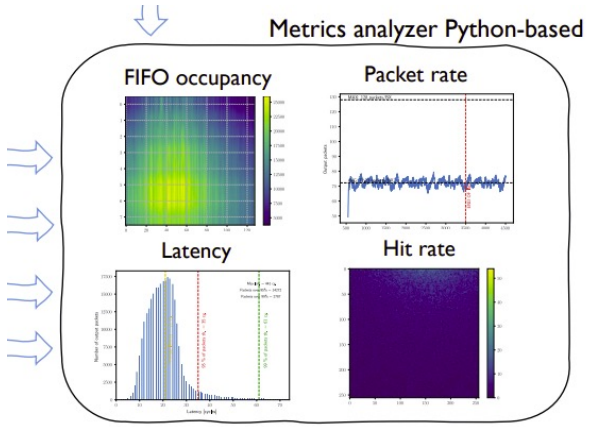
- Chiplet of the ER2 run for ALICE ITS3
- 1.5 mm x 1.5 mm
- 32 x 32 pixels
- 14.4 µm x 22.8 µm
- PhD thesis of Jean Soudier
- Collaboration
  - IPHC, ICUBE and IRFU





Periphery readout

- Crucial part of the sensor specific for each experiment
  - Data bandwidth, trigger, …
- Large power dissipation contributor ~50%
  - Data output is large contributor
    - From few mW to few tens of mW depending of the number of links
    - Not really dependent from data
    - Buffer memories to average data throughput
  - On-chip power regulators could be needed for system integration
- Data output and buffer sizing impact on performance
  - DRD 7.2.c: Virtual electronic system prototyping with PixESL
    - SystemC framework to help to dimensioning periphery
    - Need to be updated for asynchronous pixel readout



D. Ceresa @ TWEPP 2023

Conclusion

- Many aspects need to be validated before converging on an architecture
- Need to build a team to address these challenges
- Synergies with other projects in TPSCo 65 nm are desirable
  - Reuse of IP blocks like bandgap, high speed link, …