ÖAW AUSTRIAN ACADEMY OF SCIENCES

HEPHY INSTITUTE OF HIGH ENERGY PHYSICS

RD50 CMOS activities and Belle II VTX Upgrade

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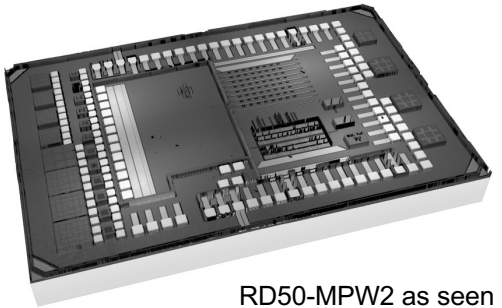
7 May 2024, DESY

CMOS Projects at HEPHY

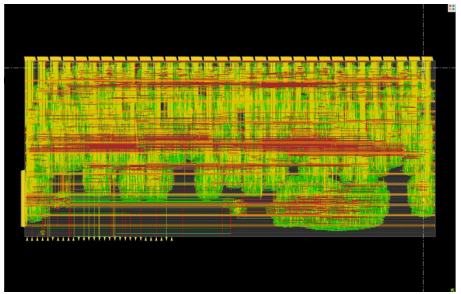
Available foundries/processes:

- Lfoundry 150 nm (LF15A)
  - Used by **RD50 MPW chips**
  - "Large collection electrode"

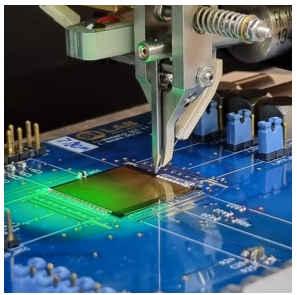


RD50-MPW2 as seen through confocal 3D microscope

Periphery of RD50-MPW3



- Towerjazz 180 nm CMOS Imaging Process
  - Used for **Belle-II VTX** upgrade
  - "Small collection electrode"
  - Process modified to improve lateral depletion and thus radiation hardness (10.1016/j.nima.2017.07.046)



- Generic analog ASIC projects (only in backup slides):
  - Efabless Openlane/Openroad Skywater 130 nm node
    - Open-source PDK
  - Fraunhofer IISB SiC-CMOS
    - Silicon Carbide Substrate very attractive synergy with our research on SiC

efabless.com

Sponsored by Google

RD50 CMOS developments

RD50 is/was (until end of 2023) CERNs R&D collaboration on "Radiation hard semiconductor devices for very high luminosity colliders"

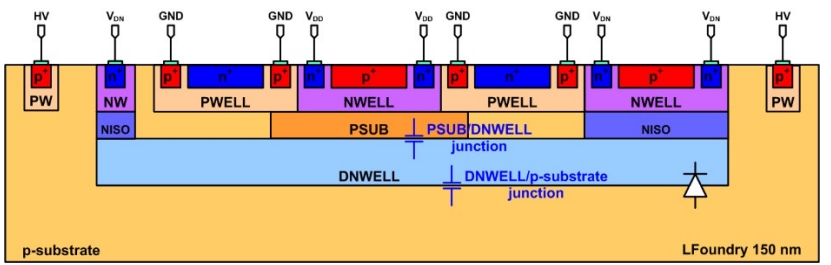
- HEPHY joined RD50 in 2017 when CMOS activities starting in RD50
- Previously, HEPHY did not have access to CMOS R&D activities
  - CERN focused on ALPIDE chip for ALICE
  - Big efforts within ATLAS groups, but nothing within CMS

RD50 CMOS working group:
14 institutes, ~40 people

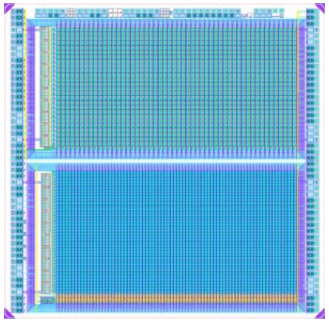
RD50 CMOS activities include

- ASIC design
- TCAD simulations
- DAQ development
- Performance evaluation

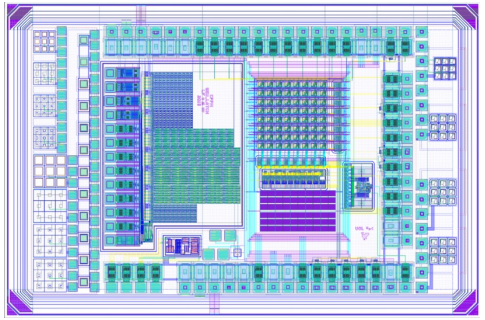
and is/was a (very) small portion of RD50 activities



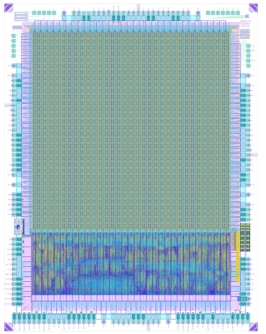
RD50 DMAPS Timeline



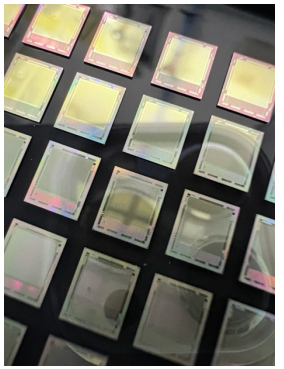
RD50-MPW1
(5mm x 5mm)



RD50-MPW2
(3.211mm x 2.120mm)



RD50-MPW3
5.1mm x 6.6mm



RD50-MPW4

Submission and delivery date

2017 2018 2019 2020 2021 2022 2023 2024

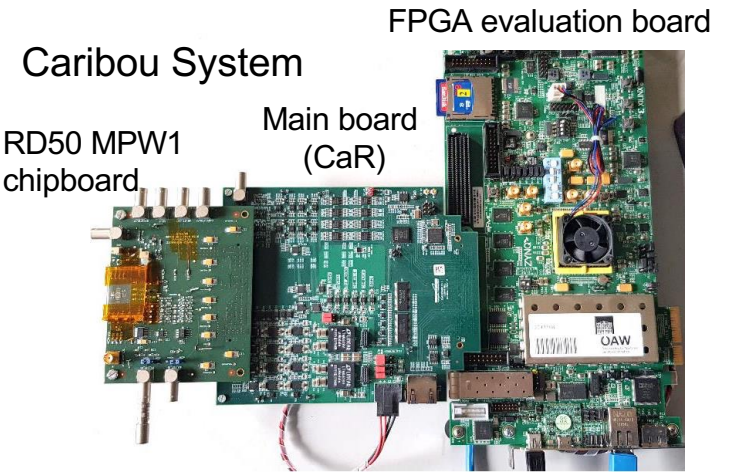
HEPHY involvement started here

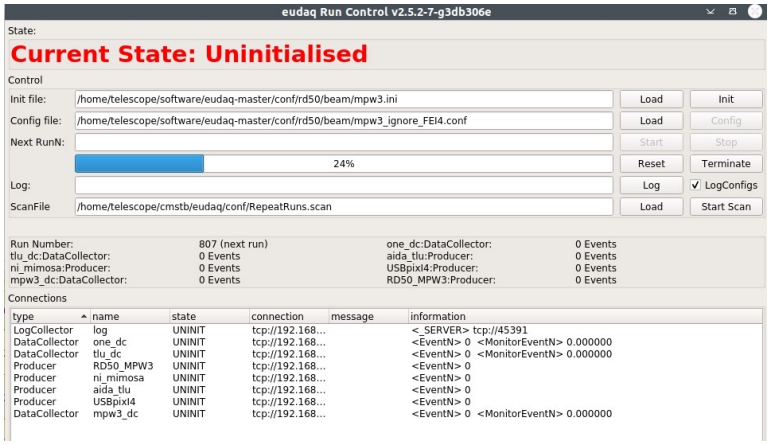
- RD50-MPW1: DAQ System developments at HEPHY
- RD50-MPW2: lab measurements, performed beam tests
- RD50-MPW3 & 4: involved in (digital) chip design, Caribou firmware

DAQ Systems for DMAPS

- DAQ systems: Our starting point with DMAPS sensors
- HEPHY tried to seek synergies and proposed to use the Caribou system for the readout of MPW1
  - Firmware development and EUDAQ integration done at HEPHY
  - RD50-MPW chipboard designed and manufactured by Valencia

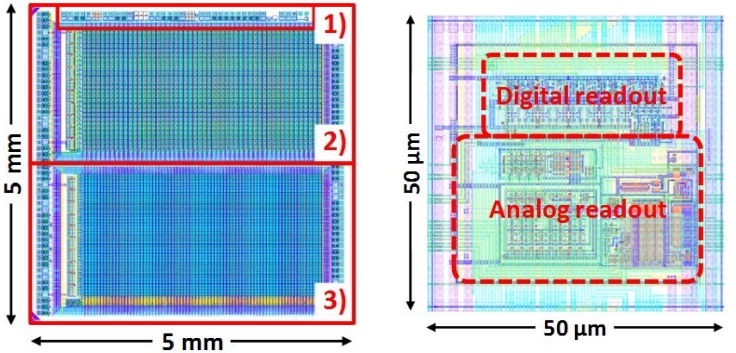
- Our Caribou experience:
  - Robust in operation
  - short-circuit-proof voltage regulators; current and voltage measurements
  - Jitter cleaner is important and available
  - The ADCs only have a maximum sampling rate of 60 MHz, but we don't use that anyway.

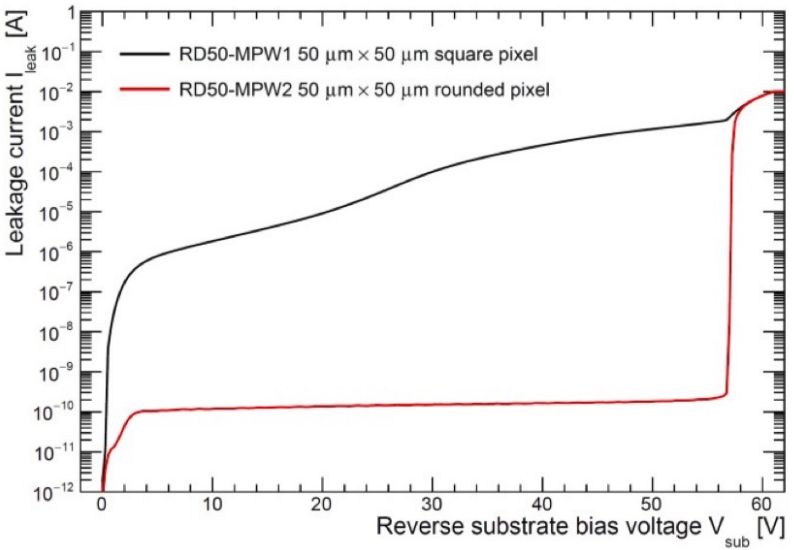




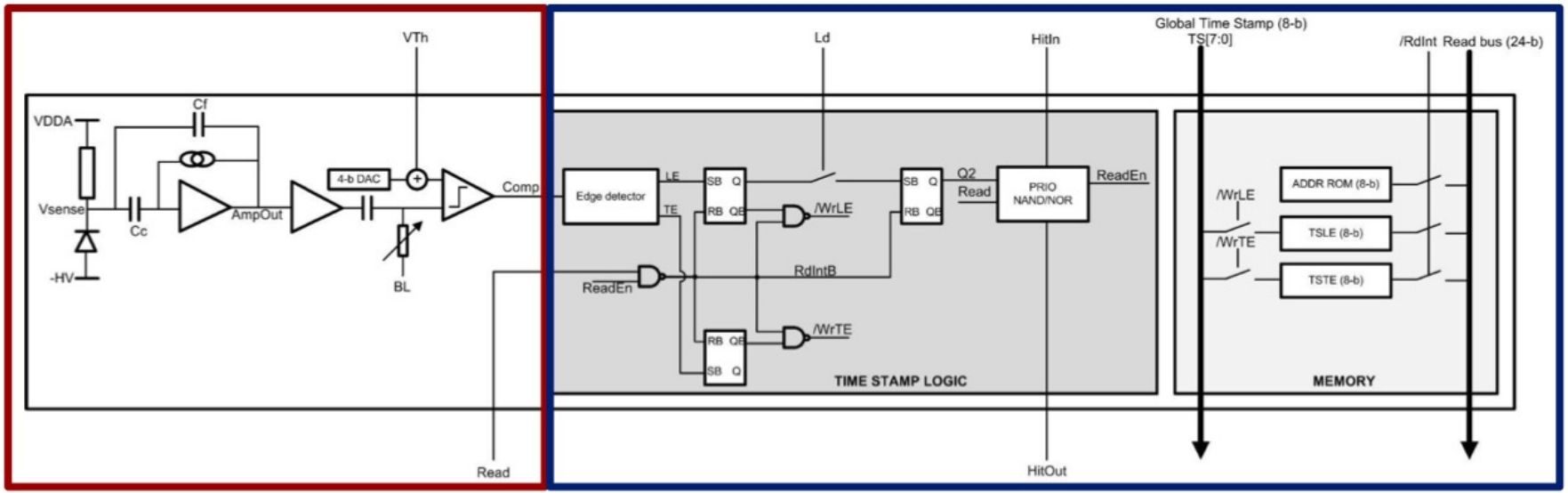
RD50 MPW1

- First try almost from scratch (with some ATLAS heritage)
- “analog on top” design
- Large matrix of DMAPS pixels
- Fabricated using 2 different substrate resistivities: 500-1100 Ω·m (600 measured) and 1900 Ω·cm (1100 measured)
- Suffering from very high dark current
  - I-V measurements done on one 50 µm × 50 µm pixel with 10 mA compliance



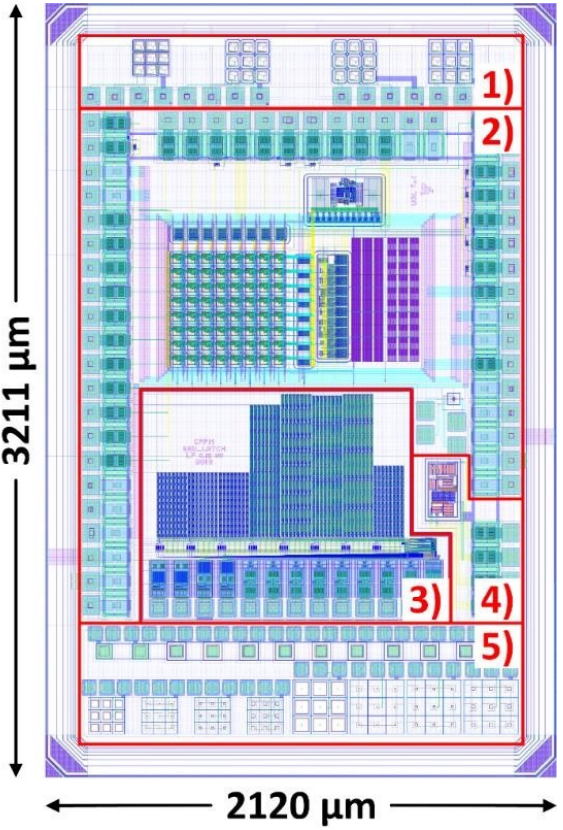


RD50 MPW1



- Analog readout
  - Sensor biasing circuit, CSA, RC-CR filters and CMOS comparator
  - CSA with programmable discharging current
  - CMOS comparator with global V Th and local 4-bit DAC for fine tuning
- Digital readout
  - Column drain readout (synchronous, triggerless, hit flag + priority encoding)
  - Global 8-bit Gray encoded time-stamp (40 MHz)
  - For each hit: * Leading edge (LE): 8-bit DRAM memory * Trailing edge (TE): 8-bit DRAM memory
    * Address (ADDR): 6-bit ROM memory ToT=LE-TE (off-chip)

RD50 MPW2

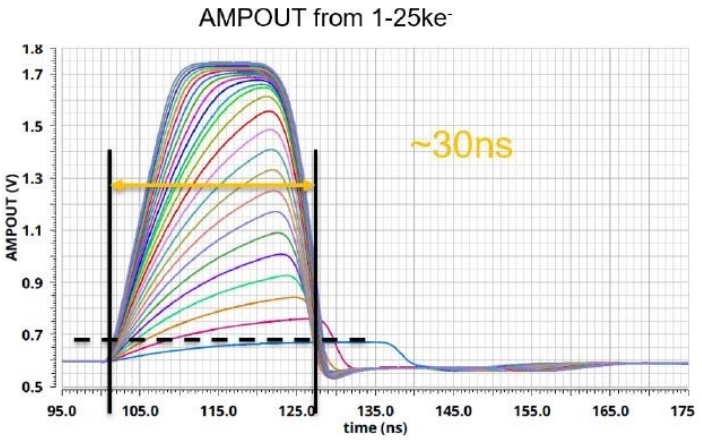


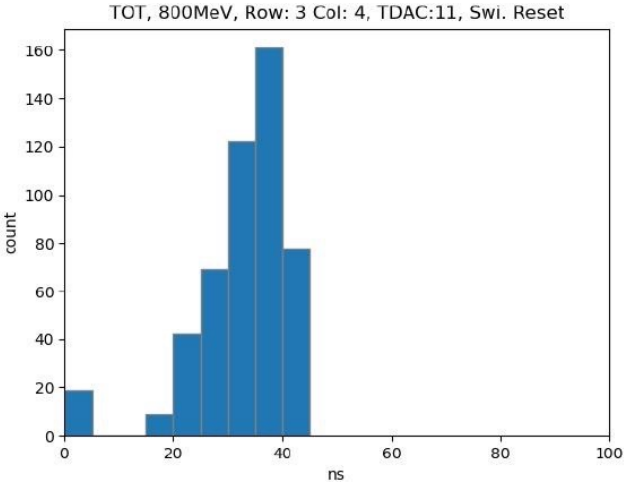
MPW2 scaled down and basically only contains analog part to address the dark current problem:

1) Test structures with depleted CMOS pixels.
2) **Matrix of 8 x 8 depleted CMOS pixels** of 60 µm with embedded analog readout.
3) SEU tolerant array.
4) Bandgap voltage reference.
5) Test structures with SPADs and depleted CMOS pixels.

Beam test at MedAustron using HEPHY Beam telescope: Time over Threshold comparison for one pixel design flavor (switched reset)

- Simulation (all energies) : ToT ~30ns
- Measurements (800 MeV protons) --> ToT ~20-40ns --> in good agreement with simulation

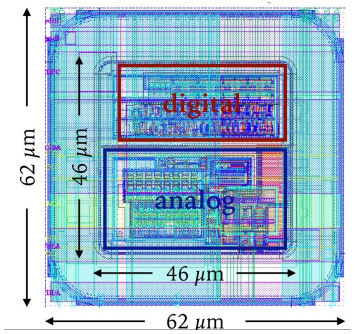


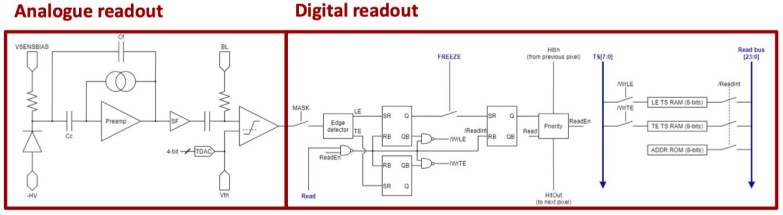


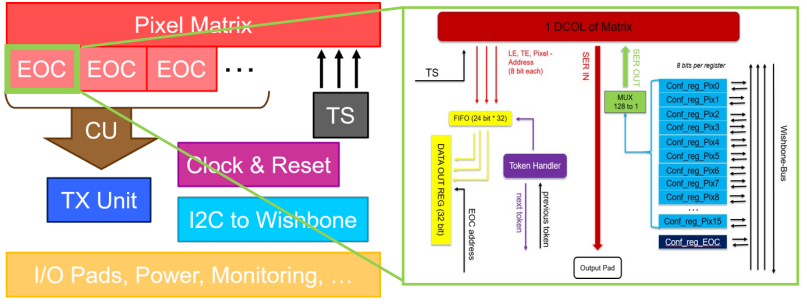
RD50-MPW3 Design

Larger and more advanced matrix to further study HV-CMOS sensors:

- 64 x 64 pixels, each 62x62 µm
- Analog readout: from RD50-MPW2
- Digital readout: highly improved
  - One End-of-Column (EOC) per double column
  - Control Unit (CU) to push data from EOCs to readout bus via rolling shutter
  - Transmission unit (TX Unit): De- randomization of EOC data, framing, encoding and serialization
  - Configuration bus (I²C/Wishbone) to configure 16 registers per pixel, one for EOC configuration



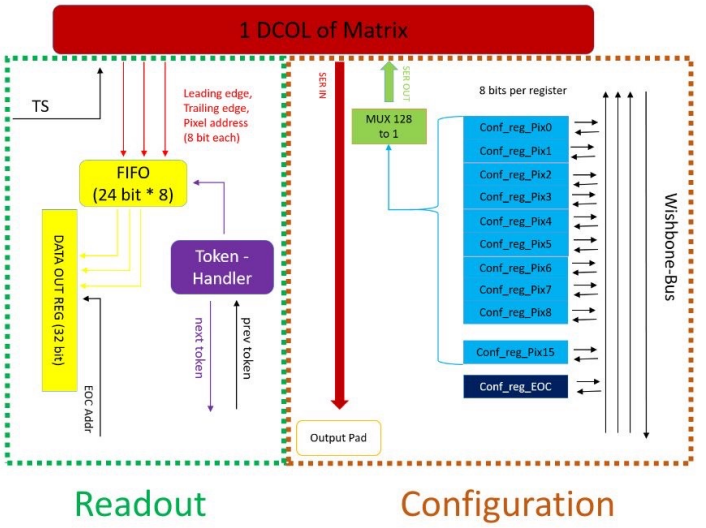




RD50-MPW3 Digital part

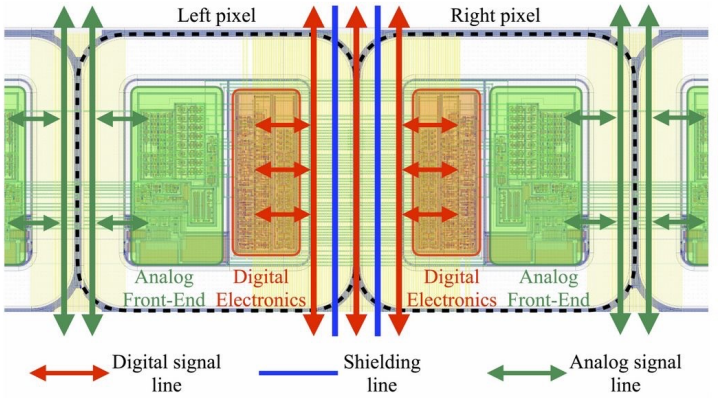
End-of-column (EOC) logic

- 16 registers of 8 bit for configuration
- Rolling shutter: combinatorial token-handler with highest address read out first
- A 24-bit wide FIFO for pixel data de-randomization
- Time stamps and pixel address are collected in EOC
- Serial readout of 32-bit EOC registers at 640 Mbps



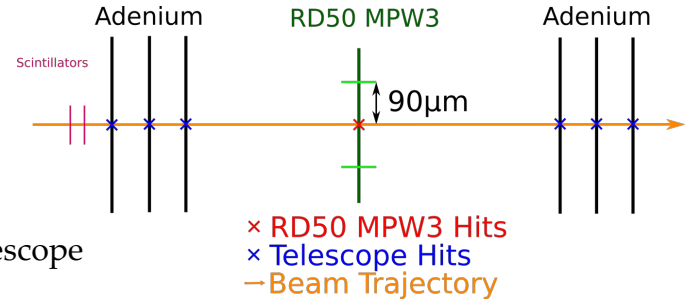
Crosstalk mitigation

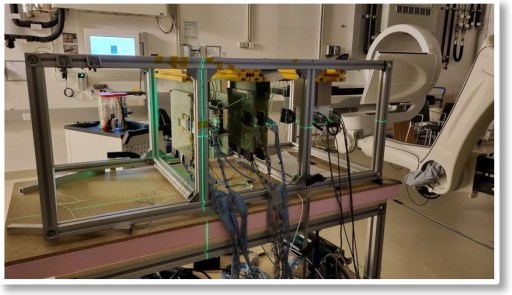
- Digital signal lines are placed in the middle of each double column
- Analog lines between double columns
- Grounded shielding lines between digital signal
- Power grid to minimise voltage drop

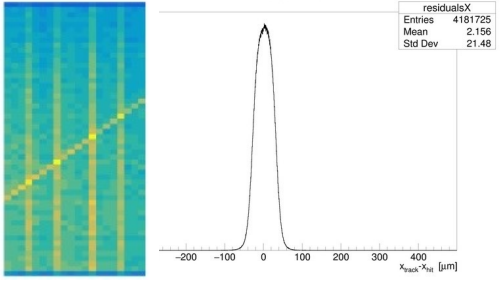


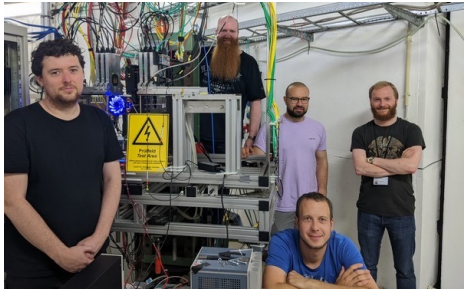
RD50-MPW3 evaluation

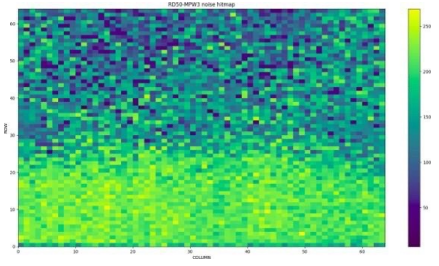
- RD50-MPW3 received from foundry in summer 2022
- Beam tests performed:
  - MedAustron Sept 2022
  - CERN SPS Oct 2022: with AIDA beam telescope
  - MedAustron Jan 2023
  - DESY Jul 2023: Utilizing Adenium telescope (based on ALPIDE pixel chip)
  - MedAustron Sept 2023
- Saw correlations with beam telescopes
  - Time walk ~9 ns
  - ToT ~ 55ns (for 5ke$^-$)
  - ENC ~120 e$^-$
  - Residuals of 21.5 µm
  - Inefficiency (no hits, high noise) in lower chip region



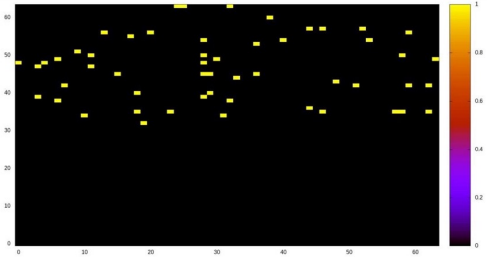








MPW3 noise map

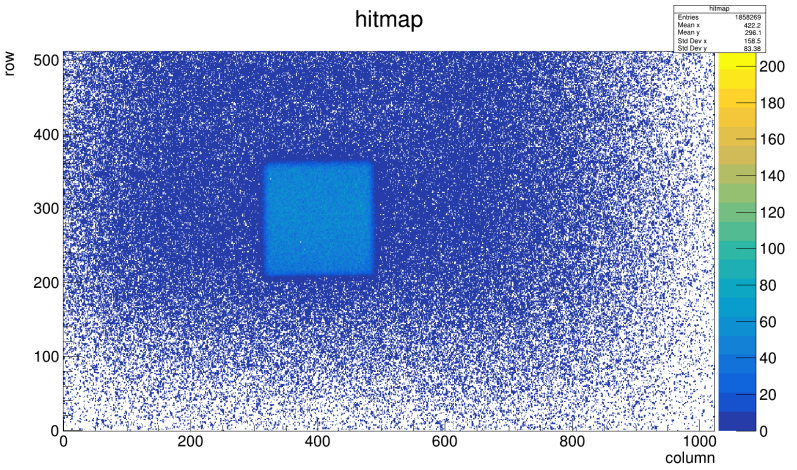


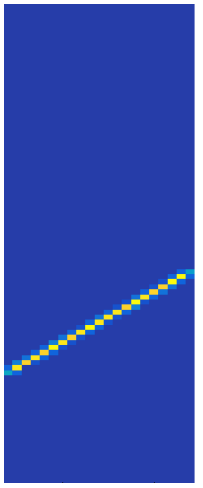
MPW3 hit map

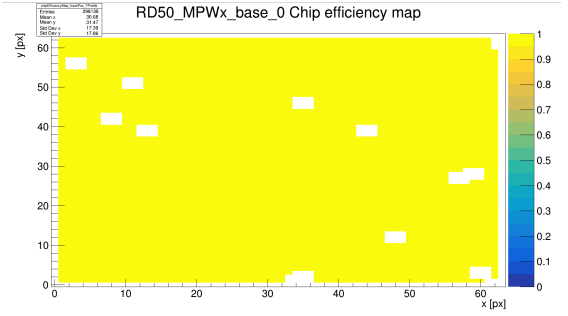
B. Pilsl: Beam test characterization of RD50-MPW3
43rd RD50 meeting Nov 2023
https://indico.cern.ch/event/1334364/contributions/5672048/

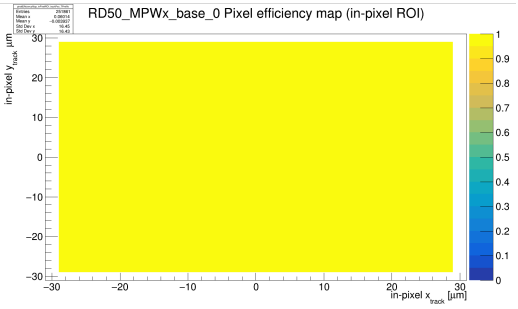
RD50-MPW4

- Submitted in June 2023
  - Improvements w.r.t. MPW3 (crosstalk/noise gradient on pixel matrix,…): full decoupling of analog, digital and periphery power, different routing of power lines
  - Length of the signals between EOC and matrix made adjustable to allow operation at full 640/40 MHz.
  - Received in January 2024
- Recent beam test:
  - MedAustron (March 2024)
  - DESY (April 2024) two weeks ago
- Preliminary results:
  - Works with almost 100% efficiency!
  - 19µm residuals



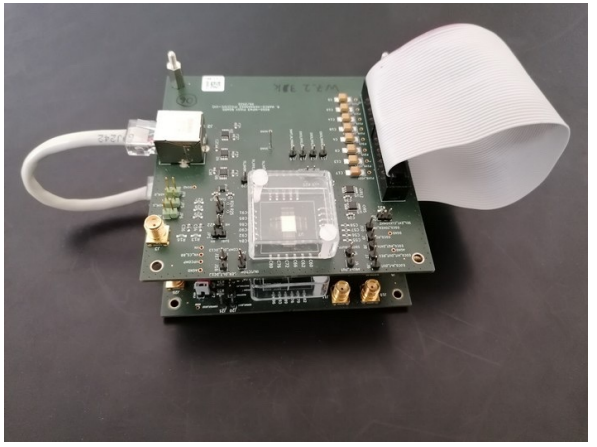






Future of RD50-CMOS in LF15

- Piggy Board
  - Additional PCB allows to operate two RD50-MPW3s with only one Caribou system
  - Applications: for better beam telescope synchronization and to directly compare different sensor flavors (e.g. irradiated vs. unirradiated)
- Another beamtest with irradiated MPW4 chips



- New Run?
  - Larger matrix
  - Include experiment-specific needs (there is the idea of going developing chip futher towards application in LHC-b upgrade)
  - Full engineering run was the initial intention of RD50-CMOS group

- The future is unclear after the shift to DRD3

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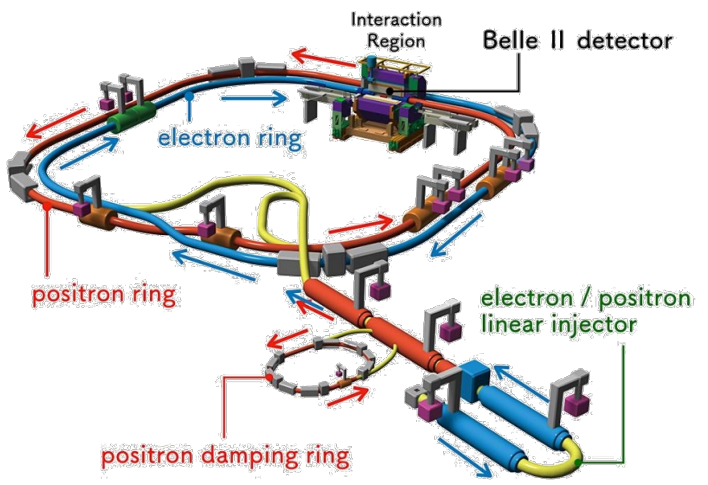
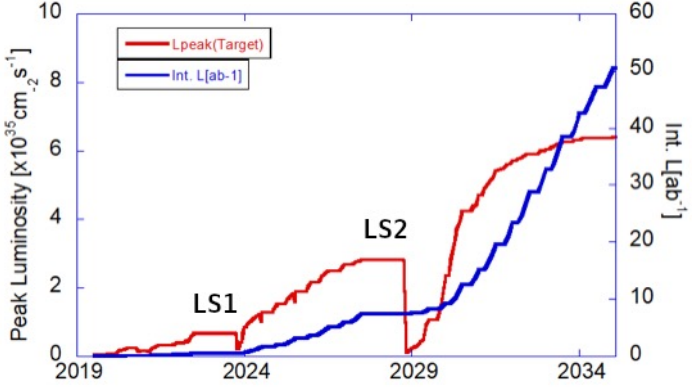
Belle II VTX Upgrade

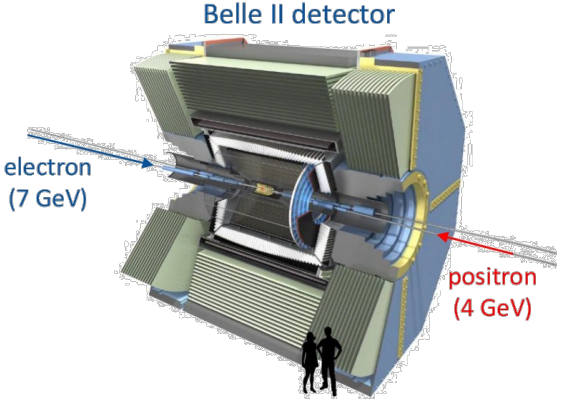
- Tower 180nm process node
- DMAPS called “OBELIX”
- Based on TJ-Monopix2

Belle II Experiment

- Located at the SuperKEKB collider in Tsukuba Japan
- Asymmetric $e^+ - e^-$ collisions
- $\sqrt{s} = M\,\Upsilon(4S) = 10.58$ GeV
- World record peak luminosity: Test-bed for FCC-ee
- Restart early 2024 after LS1



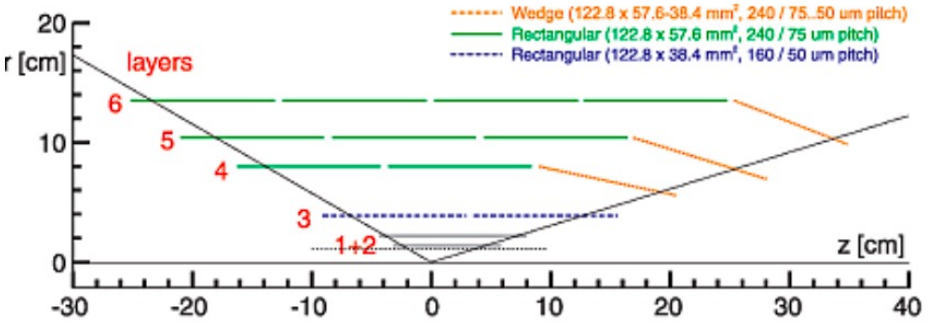




Current Vertex Detector

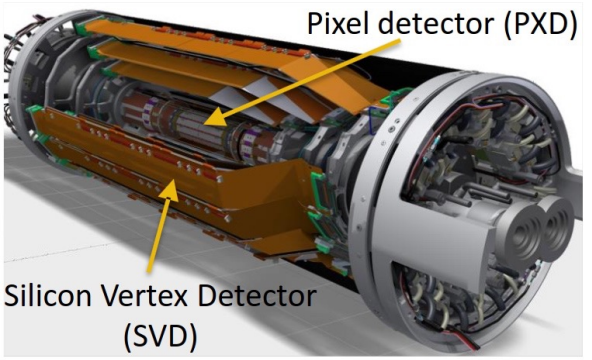
PXD:

- 2 Layers of DEPFET pixel sensor
- ~ 10 μm spatial resolution; 20 μs integration time
- Full installation in LS1 only

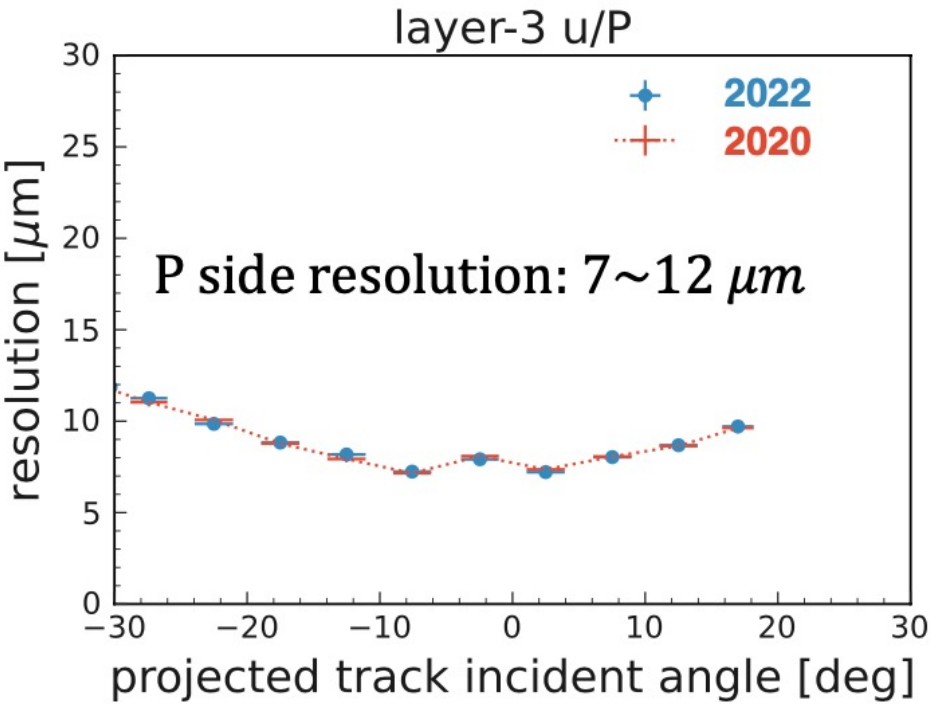


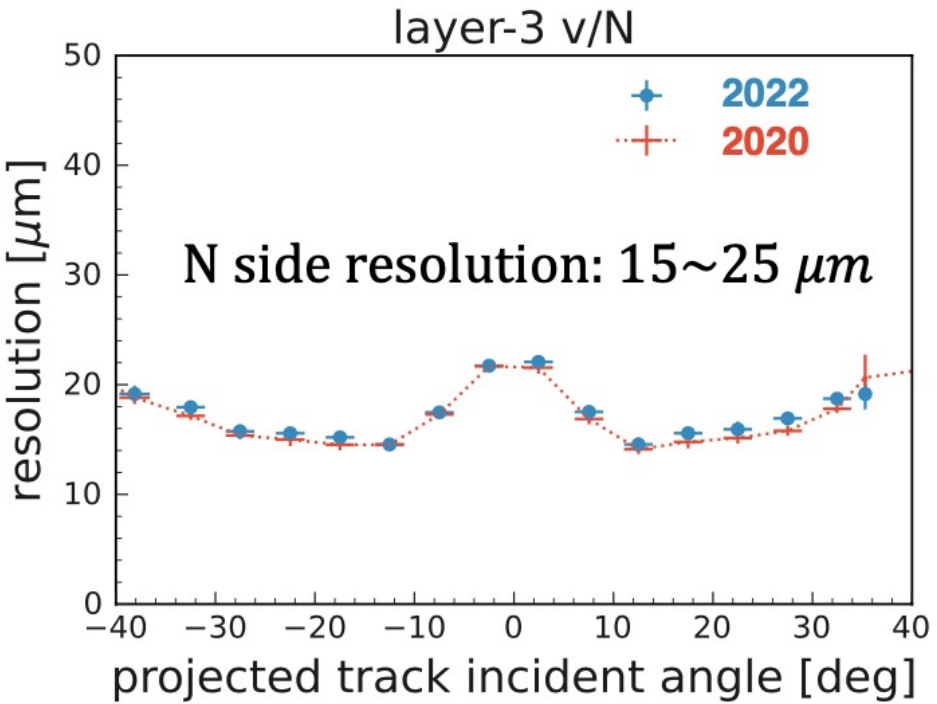
SVD:

- 4 layers of double-sided strip sensor (DSSDs); layer 3 straight and layers 4-6 with slanted forward part (trapezoidal DSSD)
- 172 sensors covering 1.2m^2 and using 224k channels
- Read-out by APV25 chip developed and deployed in CMS
- Material budget 0.7 % X_0/layer
- Estimated radiation levels of 0.35 Mrad/yr (8 × $10^{11} n_{eq}/cm^2/yr$)
- Smooth and stable operation without major issues since 2019
- 3% Occupancy limit (6% with hit-time reconstruction + BG rejection)
- Expected occupancy up to 4.7 % after LS2 (large uncertainty)
  - Little safety margin in occupancy
- Trigger latency limited to 5 μs by SVD readout



SVD position resolution





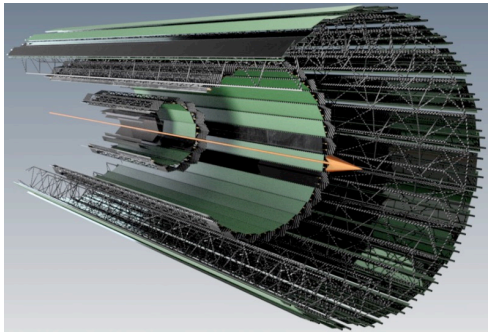
Belle VTX Upgrade

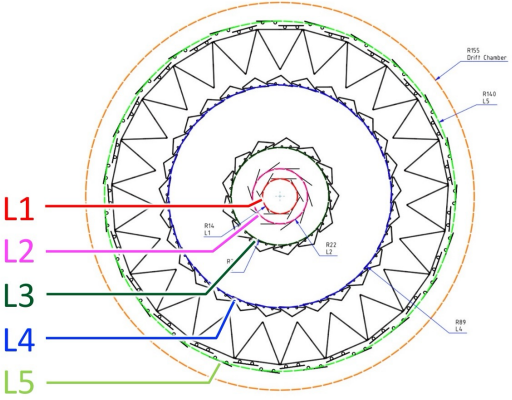
- Same size / volume as current Belle II VXD (PXD+SVD)
  - VTX Upgrade replacing both PXD (DEPFET) and SVD (DSSDs)
  - Planned for LS2 ~2028
  - Different competing ideas (SOI, “conventional” strip sensors) were converging towards MAPS-based system

- Fully pixelated vertex detector
- Five straight layers made from Depleted CMOS MAPS
  - Same chip in all layers
  - 30 - 40 µm pixel pitch
  - 25 - 100 ns timestamp resolution
  - 120 MHz/cm² hit rate

- Radiation tolerance
  - TID: ~ 10 kGy/year
  - NIEL: ~ 5×10^{12} n_{eq}/cm²/year

Possible VTX Layout



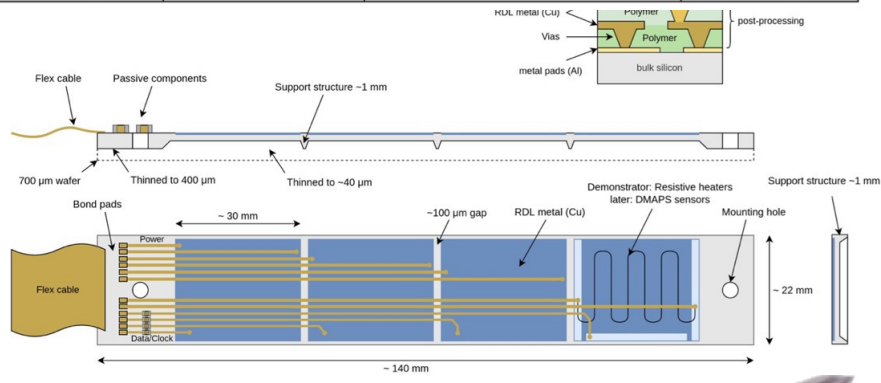


VTX Layer Design

- iVTX = 2 inner layers
  - Radii: 14, 22 mm, Length: ~120 mm
  - All-silicon design, ~0.1 % X0
  - 4 consecutive chips on a wafer are cut out as one self-supporting module
  - Redistribution layer for interconnections
  - Air cooling (less features activated to reduce power dissipation)

- oVTX = 3 outer layers
  - Radius: 40 - 140 mm, Length: up to 700 mm
  - CF truss support frame, ~0.3 – 0.8 % X0
  - Polyimide flex for interconnections
  - Cold plate with liquid cooling

	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	8	18	26	
# Sensors	4	4	8	16	48	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.1	0.1	0.3	0.5	0.8	% X_0

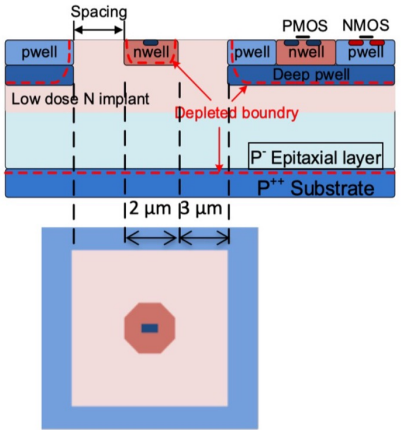


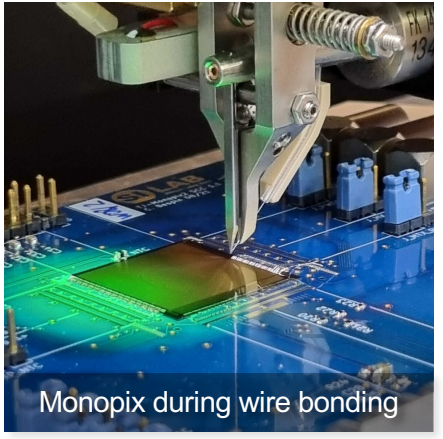
TJ-Monopix2

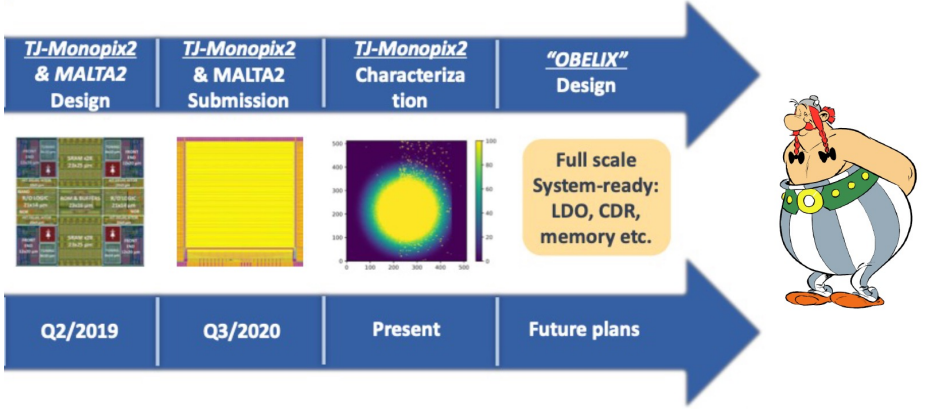
- DMAPS in TowerJazz 180 nm process
- Originally designed for ATLAS
- Now being used as basis for Belle-II VTX DMAPS chip called OBELIX (Optimized BELle II pIXel sensor)

- Small collection electrode
  - small capacitance
  - low power and noise
- High-resistivity epi layer: 1-8 kΩ cm
- Chip size: 20 × 20 mm²
- Pixel size: 33 × 33 μm²
- 512 × 512 pixels
- Column drain readout -> triggerless

- Testing and characterization ongoing







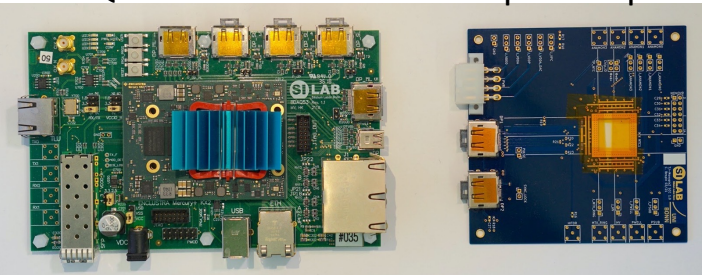
DAQ Hardware

- Setup used for
  - R&D, debugging
  - lab measurements
  - beam tests at testbeam facilities

- TJ-Monopix uses BDAQ53 board
  - initially developed for RD53 chip readout: https://doi.org/10.1016/j.nima.2020.164721
  - Simple connection between chipboard and readout board by Displayport cable

BDAQ readout board

Monopix2 chipboard

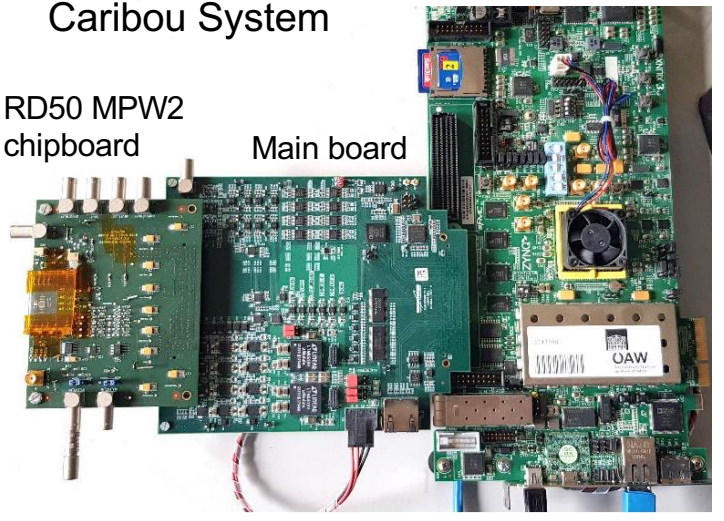


FPGA evaluation board

Caribou System

RD50 MPW2 chipboard

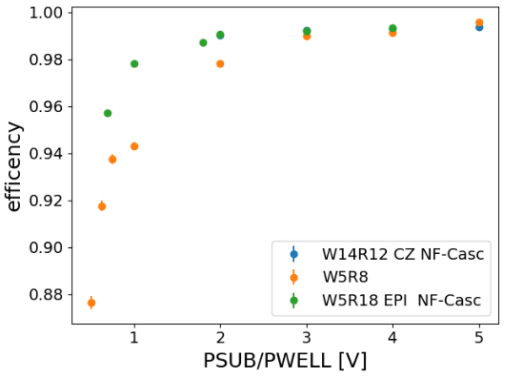
Main board



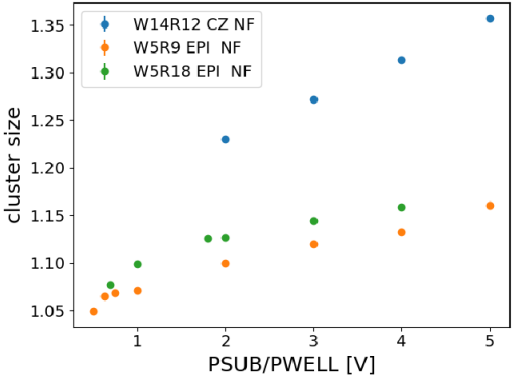
TJ-Monopix2 Testbeam 2022

- Testbeam at DESY in July 2022
  - performed by Belle-II collaboration with significant contribution by HEPHY
  - focusing on requirements of VTX
  - 4 GeV electrons
  - Readout integrated into EUDAQ2
- High efficiency > 99%
  - For Vbias ≥ 2V (PSUB/PWELL)
- Good spatial resolution < 10µm
  - Charge sharing allows improved resolution
- Chip was operating with high threshold
  - Measured at 500 e-, lowering to 200 e- possible
  - Measurements at lower threshold are planned for next test beam in July 2023
  - Should have impact on resolution due to larger clusters

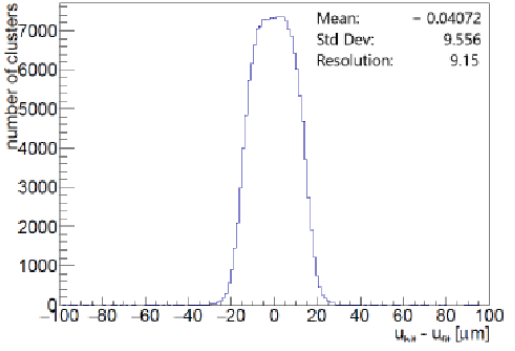
Efficiency vs. Bias Voltage



Cluster Size vs. Bias Voltage

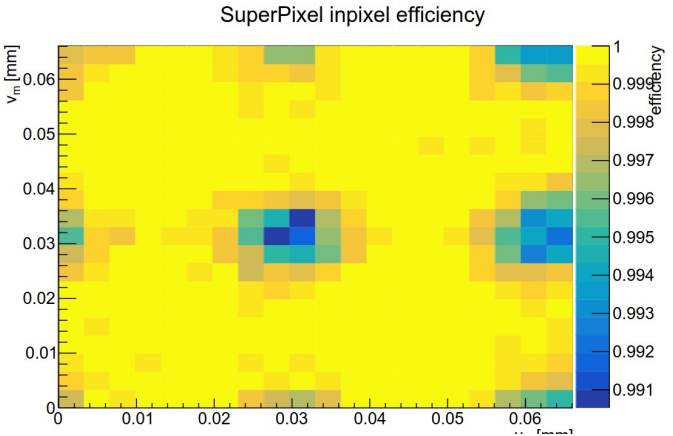


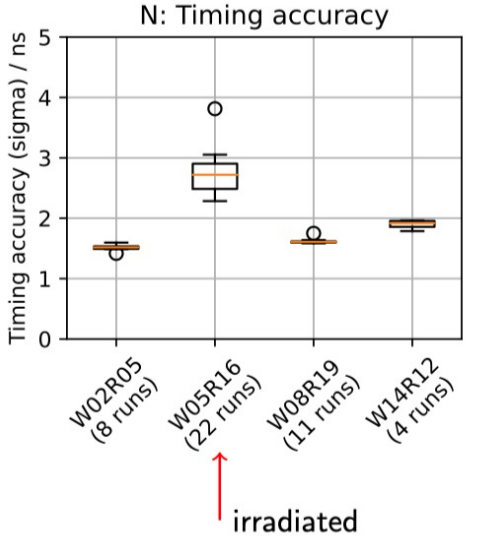
Residuals for all clusters



TJ-Monopix2 Testbeam 2023

- First week: Regular measurements with Duranta telescope (efficiency and angular scans for depletion)
  - Spatial Resolution < 10 μm for all measured chips
- Second week: Timing measurements, (parasitic to RD50 MPW3)
  - TDC module of BDAQ53 firmware measures delay between scintillator and Hitor
  - Ambiguities since whole chip has one Hitor line only → ±25 ns cut applied
  - 2ns (3ns for irradiated chip)



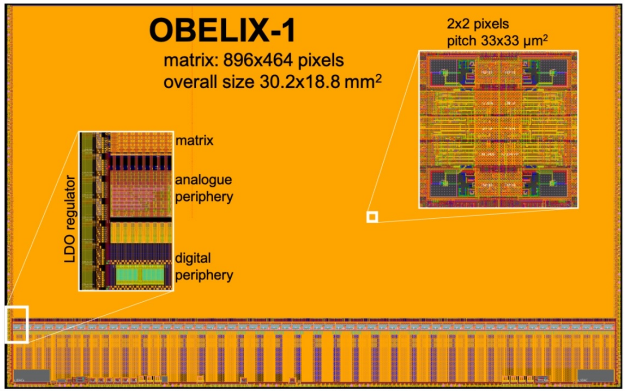


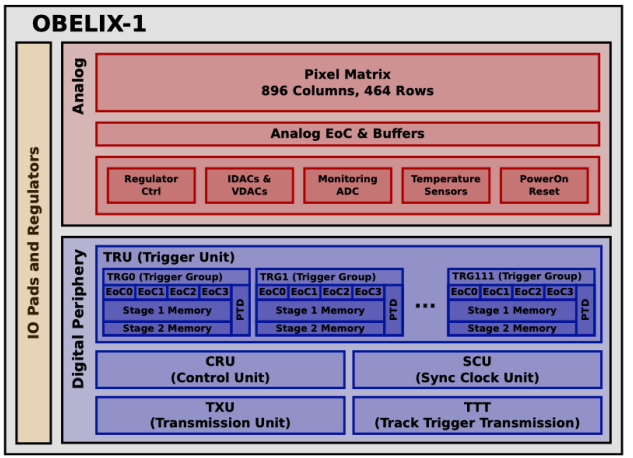
Belle II VTX Key Requirements

- High hit efficiency at demanding hit rates with sufficient timestamping
  - Matrix inherited from TJ-Monopix2
- Handling trigger latency of the Belle II experiment (up to 10 µs)
  - New implementation of digital periphery
  - Simulation to validate performance
- Power dissipation (air cooling of inner layers; liquid cooling outside):
  - Optimized digital logic with optional features (turn on/off)
  - On-chip voltage regulators
- *Increased timing resolution (layer 3-5 feature)*
  - *Precision timing module in the periphery (PTD)*
- *Contribution to Belle II Trigger (layer 3-5 feature)*
  - *Independent fast data path*

OBELIX Chip

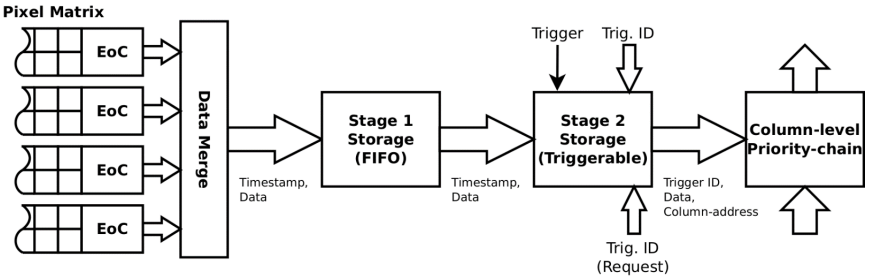
- Optimized BELle II pIXel sensor
  - Matrix and column-drain architecture inherited from TJ-Monopix2, size adjusted
  - Chip size: 30 x 19 mm²
  - Pixel: 33 x 33 µm²
  - 464 rows, 896 columns
  - power: <200 mW/cm² with internal LDO regulators
  - Up to ~10 µs trigger latency
  - NIEL tolerance: $5 \times 10^{14}\ n_{eq}/cm^2$
  - Hitrates up to 120 MHz/cm²



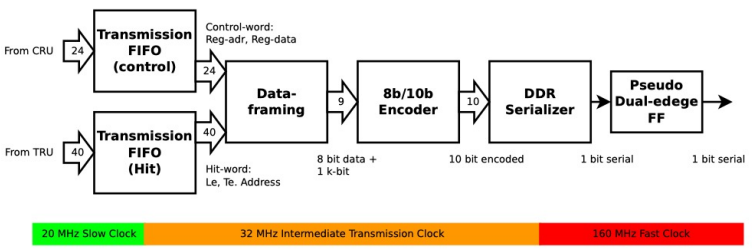


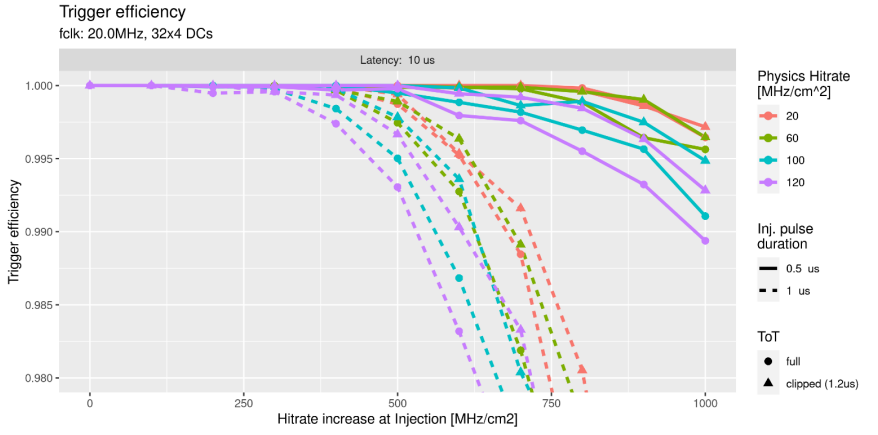
OBELIX Digital Periphery (1)

- Triggering system
  - Optimized for low power consumption and 10µs latency
  - Dual-stage memory design
    - Stage 1: Pre-trigger buffer SRAM, low power
    - Stage 2: Associative memory to match trigger (power-hungry)
  - Large simulation effort for performance evaluation
  - Trigger memory: 112 Tigger Groups, for 8 columns each



- Transmission unit
  - 160MHz Double-Data-Rate LVDS
  - Most TXU components run at 32 MHz (160 MHz / 5) intermediate clock
  - Serializer needs one byte (10 bit encoded, DDR) per 32 MHz clock cycle

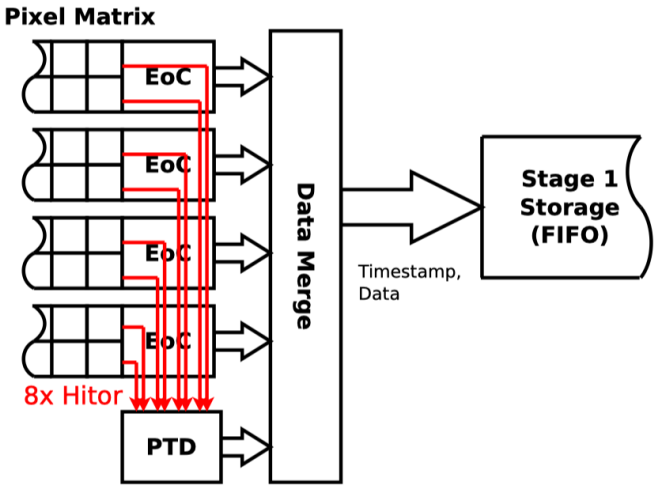


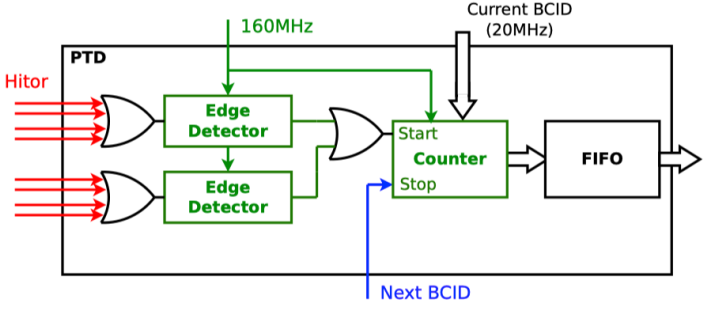


determination of FIFO buffer size

OBELIX Digital Periphery (2)

- Precision timing
  - Hitor: all comparator outputs of one column in an OR-chain (as y nchronous)
  - PTD: precision timing better than Timestamp (50 ns)
    - Sampling : 2.95 ns period (169.7 MHz DDR)
    - Single-digit ns timing precision per layer expected
  - Power hungry feature: disabled in iVTX
    - oVTX layers with more power budget can enable this feature
  - Little overhead when disabled (Little die space, clock can be turned off)
  - Resolution limited by timewalk and process corners (process, voltage, temperature variation)



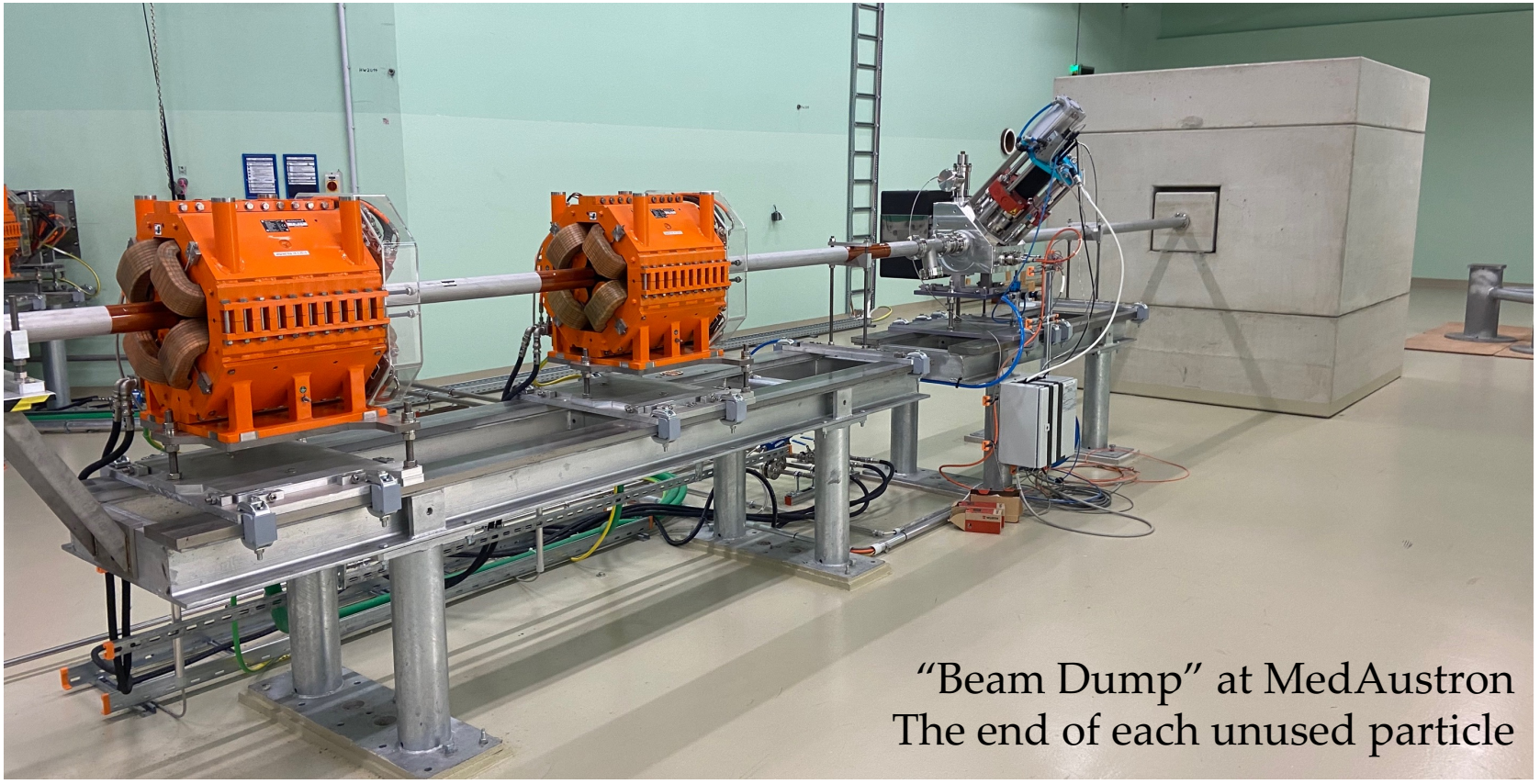


More Details: M. Babeluk: **The DMAPS Upgrade of the Belle II Vertex Detector**
13th "Hiroshima" Symposium (HSTD13), Vancouver, Canada (Dec. 2023)
https://indico.cern.ch/event/1184921/contributions/5574834/

Summary

- RD50 CMOS project was a good start in CMOS activities for us at HEPHY
  - Developed digital periphery
  - Developed to Caribou firmware
  - Future unclear
- Belle II VTX upgrade is a natural application of CMOS technology given the expertise and SVD history
  - Uses well-established Tower 180 nm node and TJ-Monopix2 expertise
  - Realization depending on luminosity increase of SuperKEKB accelerator and occupancy in current VTX
  - Perfect test-bed for FCC-ee DMAPS chip

The End.

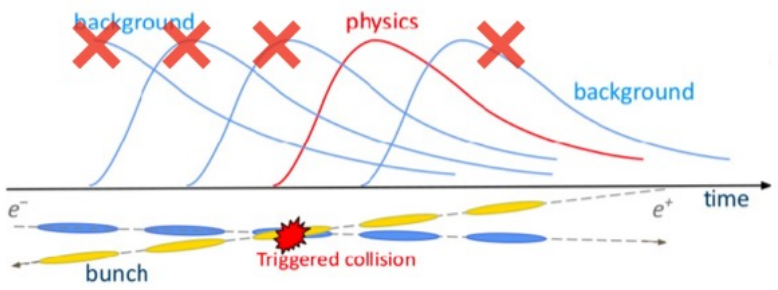


SVD hit-time finding

Hit-time selection: excellent hit-time performance (resolution <3ns) allows efficient removal of off-time tracks

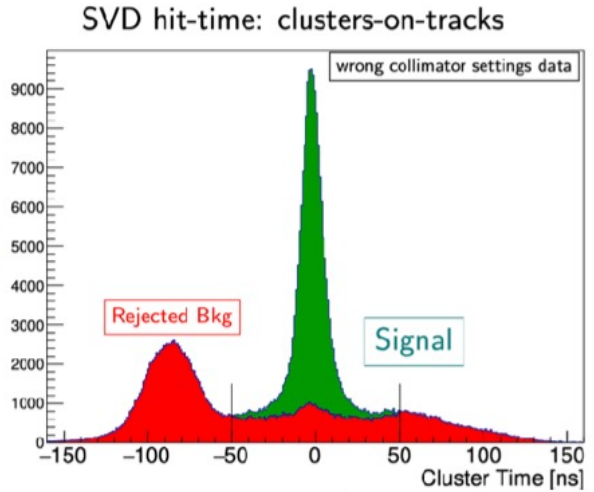
⇒ Efficient to remove 50% off-time hit background , keeping signal efficiency >99%

⇒ Tested but not yet deployed on real data reconstruction since the actual occupancy level is still low



Hit-time selection

$$|t_{u,v}| < 50\,\text{ns}$$
$$|t_u - t_v| < 20\,\text{ns}$$



ÖAW AUSTRIAN ACADEMY OF SCIENCES

HEPHY INSTITUTE OF HIGH ENERGY PHYSICS

Analog ASIC design @ HEPHY

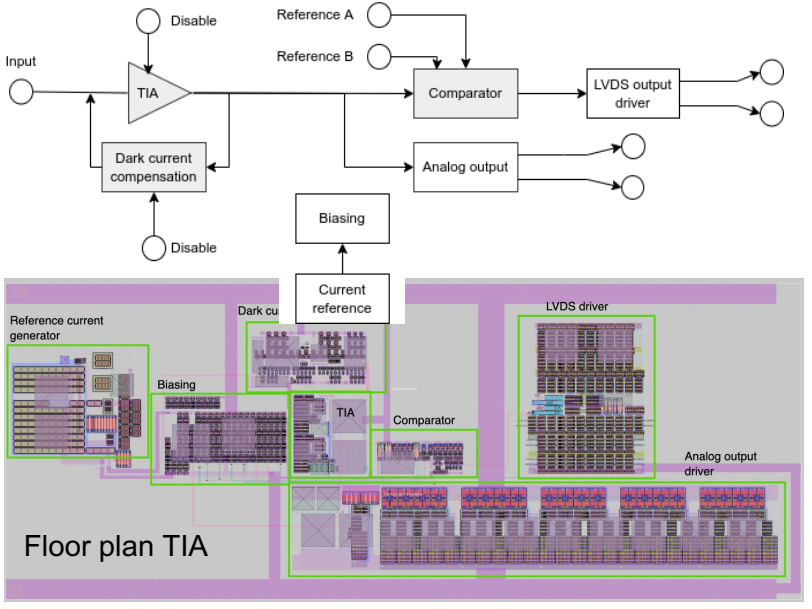
- Open-source chip design
- Silicon Carbon (SiC) particle detectors and CMOS electronics

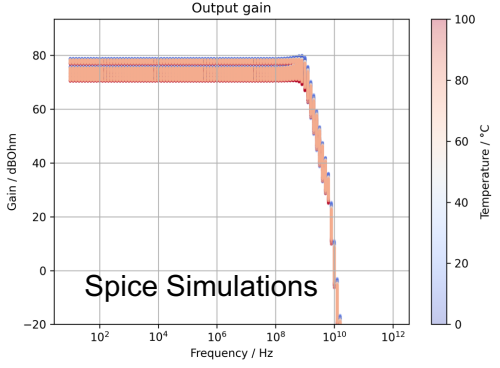
- Aimed for medical Applications (FLASH dosimetry, micro-dosimetry)

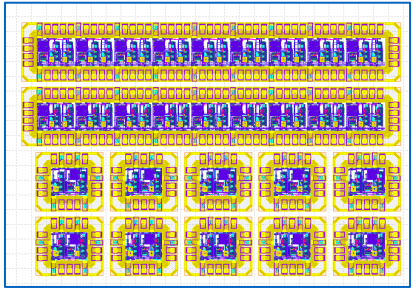
Analog Amplifiers ASIC Design

- Development of front-end ASIC using open-source tools
  - Our licenses of Cadence are restricted to non-commercial use
  - Several funded projects are in collaboration with companies/industry
  - General trend to open-source chip design (release of several PDKs to open-source)

- HEPHY Submissions of Trans-Impedance (broadband) amplifier:
  - Google sponsored MPW5 and MPW7 submission @ Skywater 130nm via efabless.com → **First Silicon received beginning of 2024!**
  - Most sophisticated: NIST-support submission @ Skywater with 18 TIA channels aligned for strip detector readout

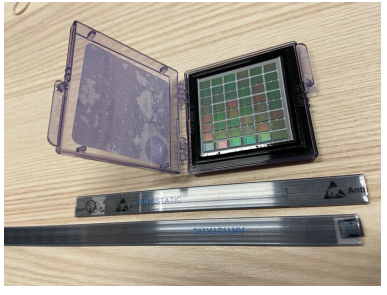






Layout 18 TIA channels for strip sensor readout ("NIST submission")

First Silicon received as bare die and package beginning of 2024 (MPW7):



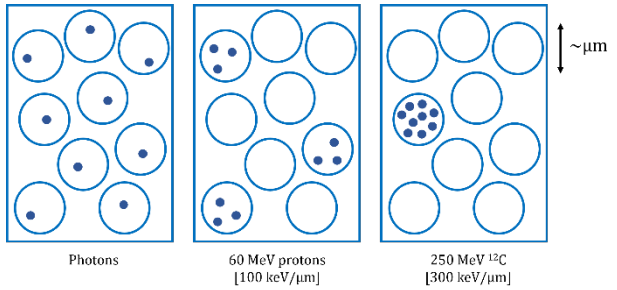
S. Waid: **Detector development for particle physics** (2024)
https://doi.org/10.1007/s00502-023-01201-w

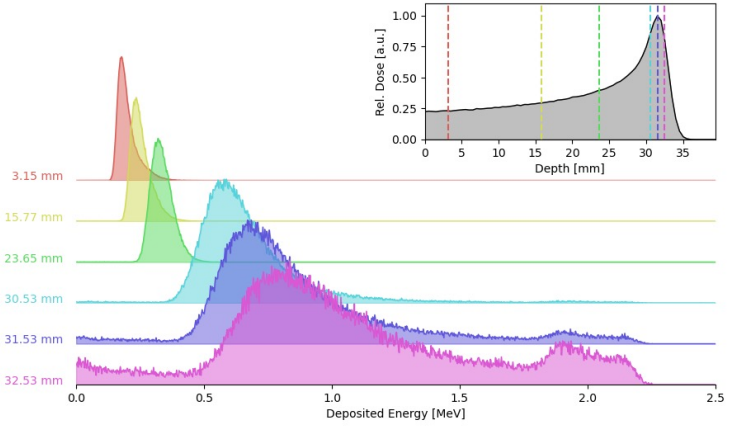
Applications: Microdosimetry

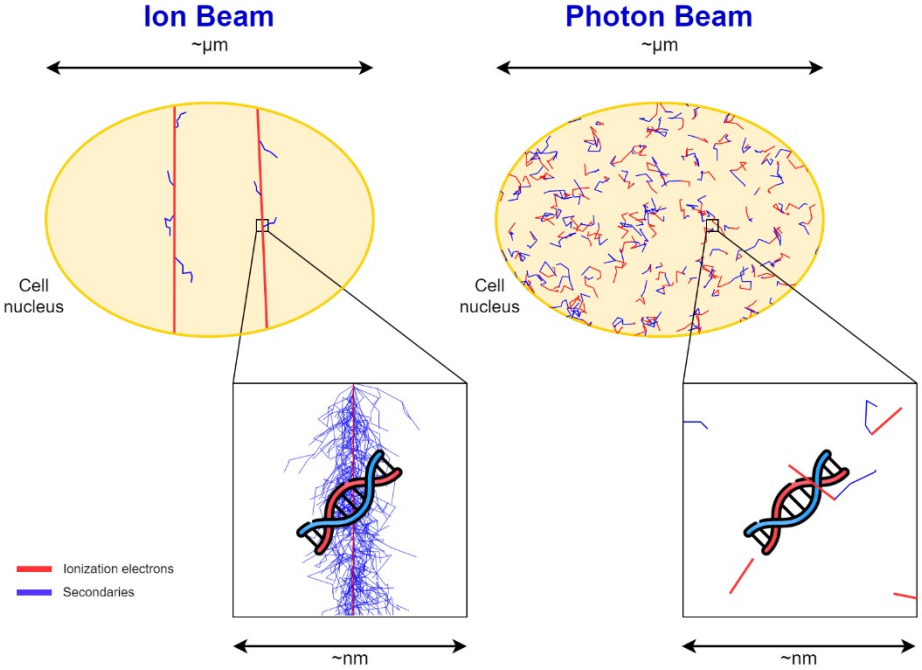
The same dose [J/kg] can be delivered in different qualities
→ Different biological effectiveness

Microdosimetry measures pattern of energy deposition in small (cell nucleus) sized volumes
→ Need small detectors

This can be used for treatment planning in RT



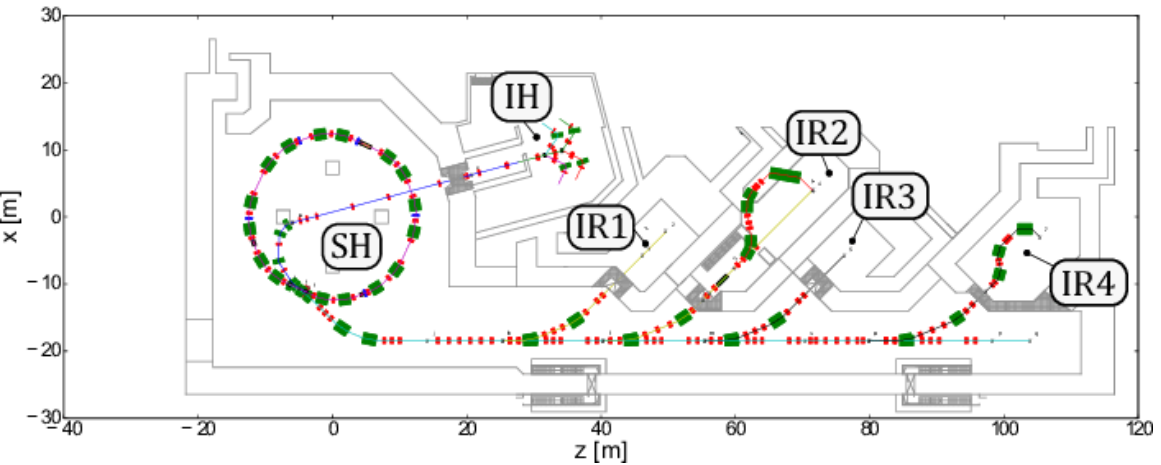


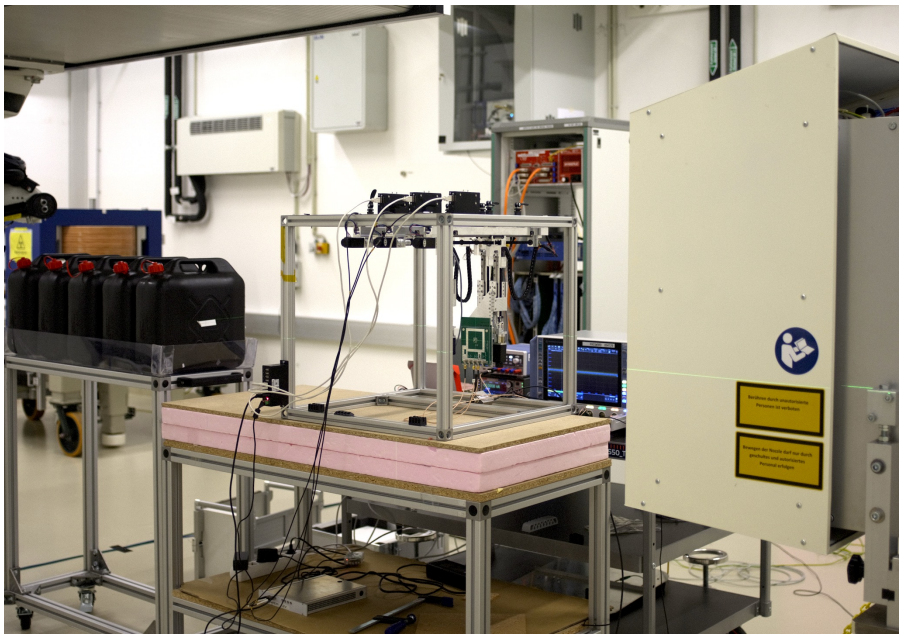


MedAustron Ion Therapy Center

- Synchrotron providing protons, carbon and (soon) helium ions for medical therapy
- 1 dedicated non-clinical research beamline (IR1)
- Energies up to 800 MeV for p^+ (≈ 1.3 MIPs), commissioned together with HEPHY
- Intensities from kHz/cm^2 to 10^{12} /s /cm^2

- Silicon tracker + beam rate monitor built by HEPHY



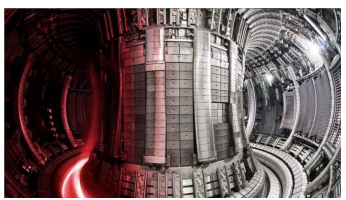


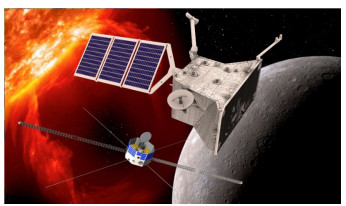
Silicon Carbide Detectors

- Wide bandgap semiconductor (3.26 eV) : Low leakage currents, insensitivity to visible light
- Renewed interest: High quality wafers from power electronics industry

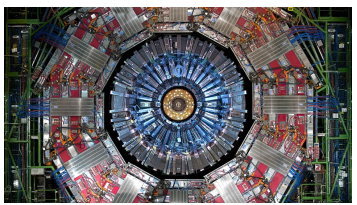
\+ High breakdown field and saturation velocity : timing applications
\+ Potentially higher radiation hardness (displacement energy), no cooling needed after irradiation
\- Higher ionization energy (~30% less signal per µm) [1]
\- Limitations in wafer thickness and resistivity

Dosimetry: µDOS, FLASH [2]

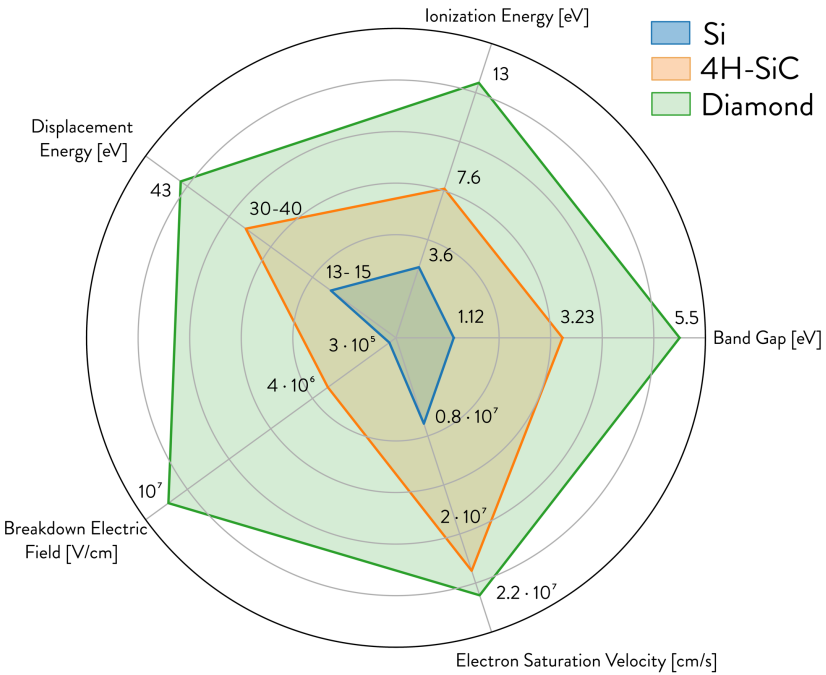




Space, harsh environments (fusion) [3]



Beam monitoring, radiation hard large area detectors [4]



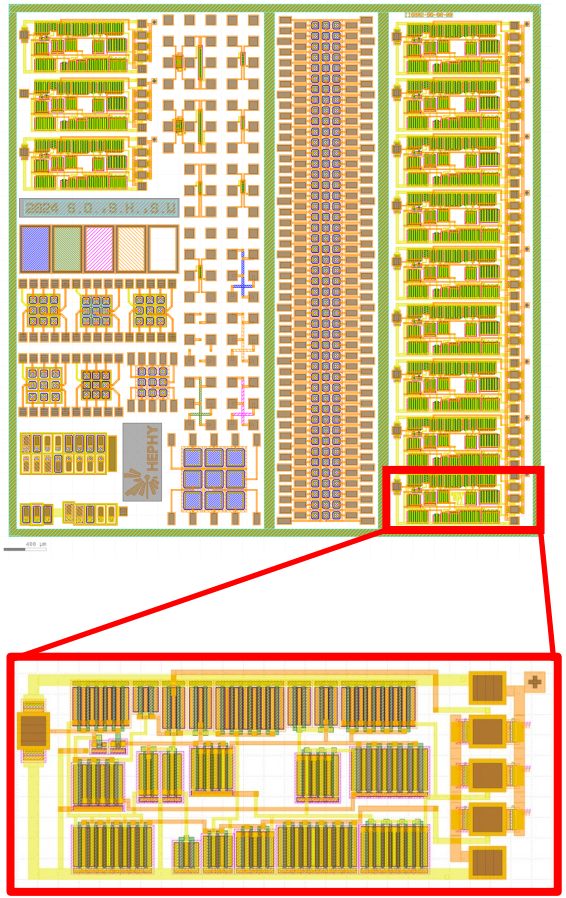
Advantages and disadvantages of 4H-SiC compared to Si

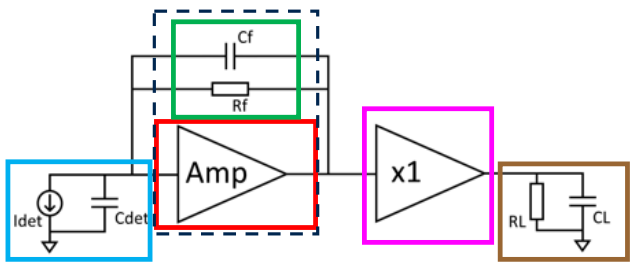
SiC CMOS Run

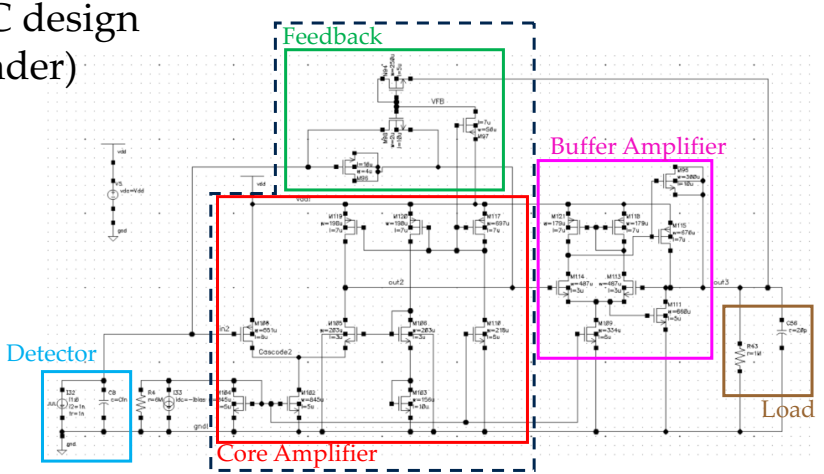
IIBS Fraunhofer offers SiC CMOS process

- CMOS process (very large feature size of 2µm)
- Access via Europractice (5x5 mm² MPW share)
- Submission deadline 9 February 2024
- HEPHY submission contains
  - Pixel detector arrays, Test structures
  - Charge Sensitive Amplifiers (CSA) designed at HEPHY
    - First full-analog ASIC design (Master's thesis S. Onder)

Layout of HPEHY-designed MPW die

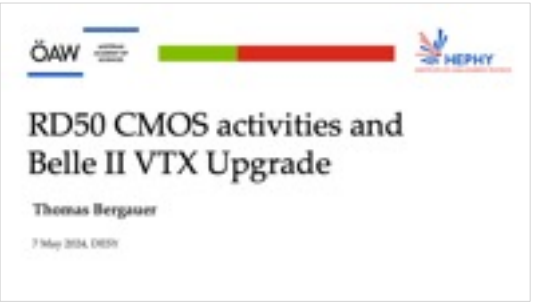




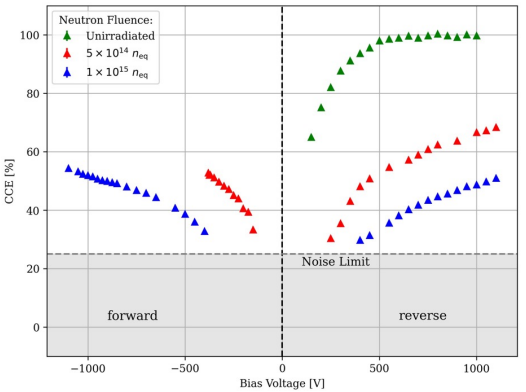


SiC Radiation Hardness

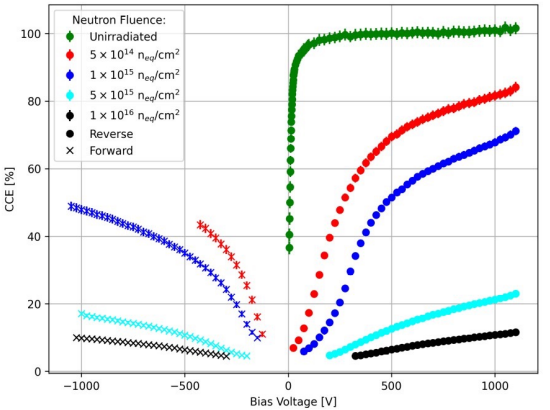
- SiC Samples irradiated with neutrons at ATI Vienna Reactor up to 1e16 n_{eq}/cm^2
- Charge Collection Efficiency (CCE) studied with Alpha particles, Protons@MAUS, UV-TCT
  - Clear decrease of the CCE observed for higher neutron fluences in TCT measurements
  - Forward direction operation (diode behavior lost)
  - Irradiated samples not fully depleted
  - Signal amplification in UV-TCT with very high energy density in forward bias observed
- More work needed to increase radiation hardness of SiC:
  - Annealing
  - Trap level studies
  - Defect Engineering



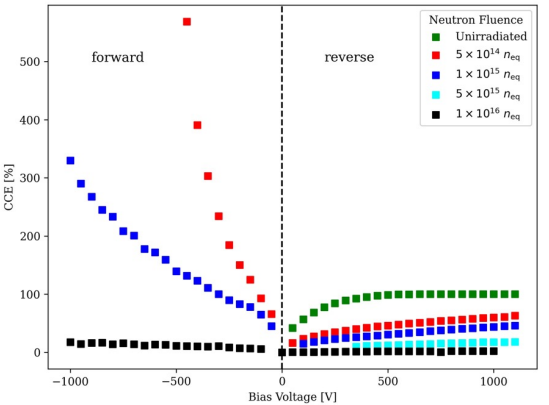
Protons @ MedAustron:



Alpha measurement



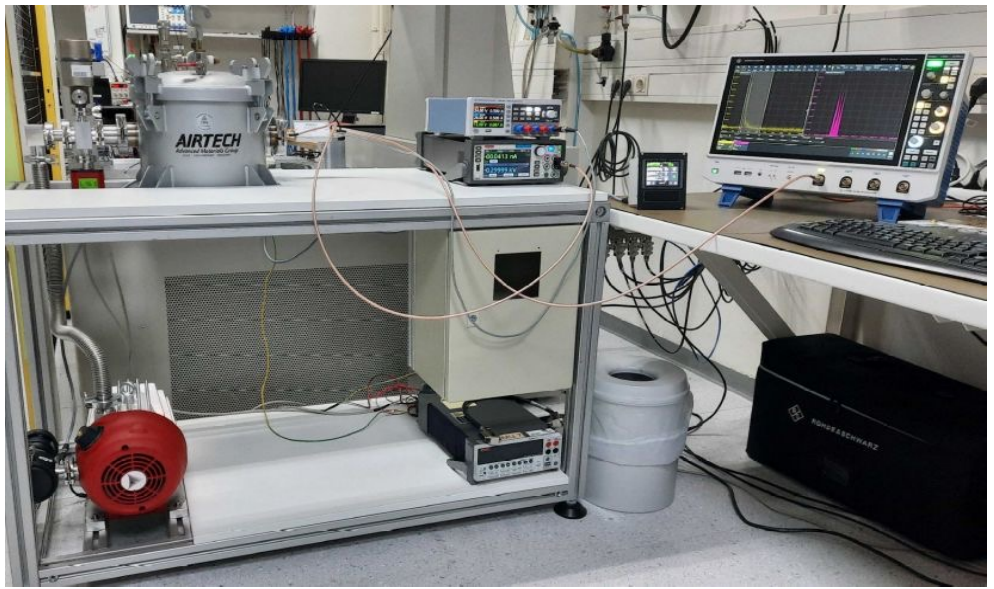
UV-TCT measurement



A. Gsponer: **Investigation of Neutron Radiation Damage in 4H-SiC PiN Diodes**
TIPP 2023 Cape Town Sept. 2023
https://indico.tlabs.ac.za/event/112/contributions/2899/

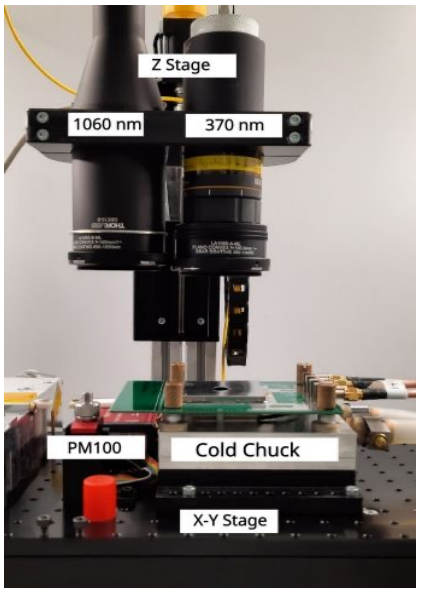
CCE Measurements

- Charge collection efficiency (CCE) is the most relevant metric for detectors
- Room temperature measurements
- Signals collected in forward and reverse bias



Tri-Alpha in Vacuum (^{239}Pu, ^{241}Am, ^{244}Cm)

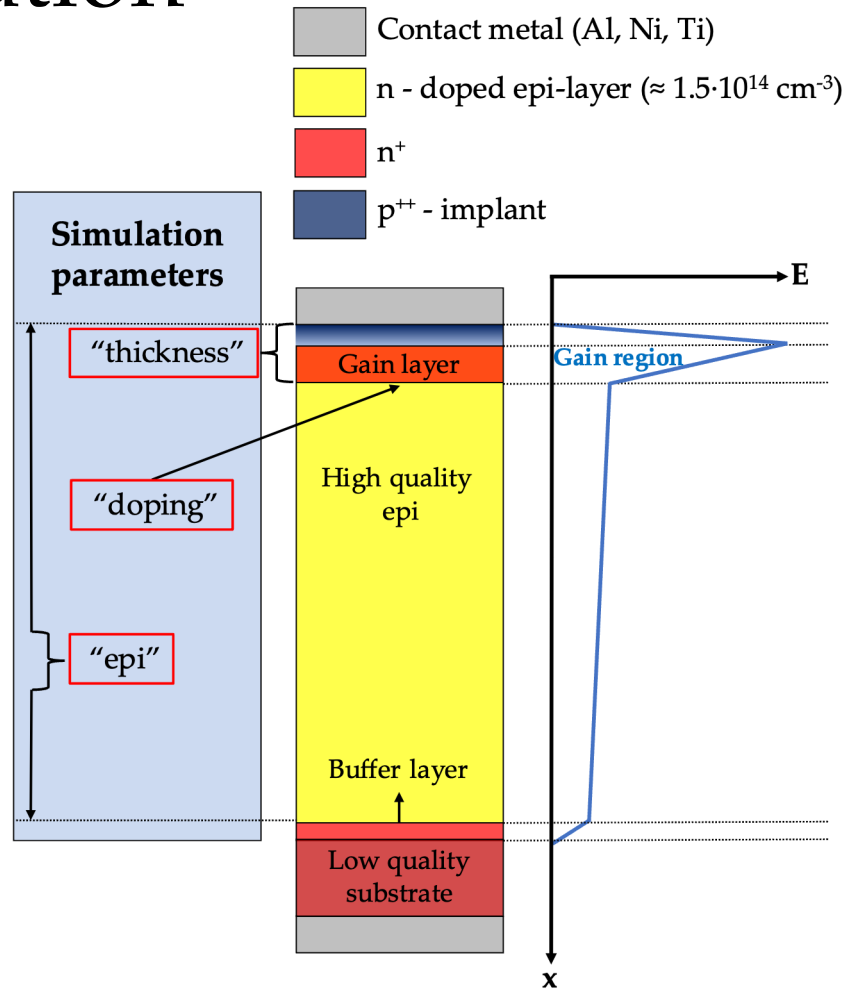
62.4 MeV p^+ at MedAustron (AT)



UV-LASER (370nm)
< 100 ps pulse length

LGAD simulation

- Drawback of 4H-SiC:
  High E_{ion} + small t_{sensor} = small signals
- **L**ow **G**ain **A**valanche **D**iode
- Additional "gain layer" creates high field region
- By tuning the design parameters, the resulting charge multiplication can lead to a controllable signal amplification (gain) instead of device breakdown
- LGADs offer unique timing properties
- Amplification very sensitive to sensor design
  → TCAD simulations to determine optimal design parameters

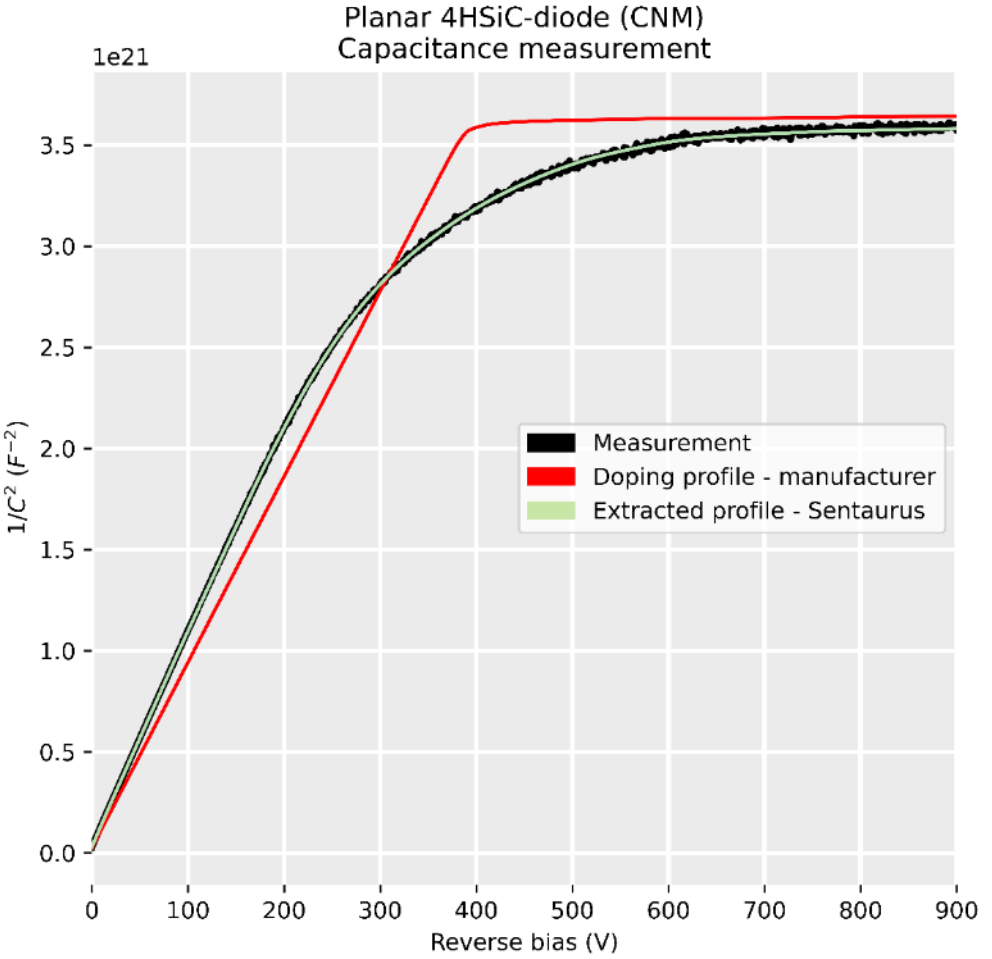


TCAD Simulations

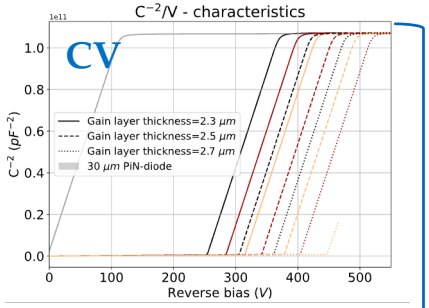
- Doping profile extracted from $1/C^2$ measurements
- 4H-SiC parameters not available per default in most TCAD applications, different polytypes (4H, 6H) of SiC
  → extensive literature review

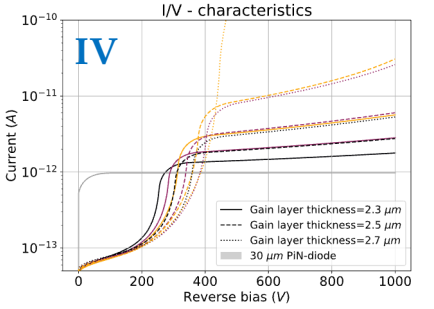
4H-SiC Parameters		
Band structure	**Charge carriers**	**Recombination**

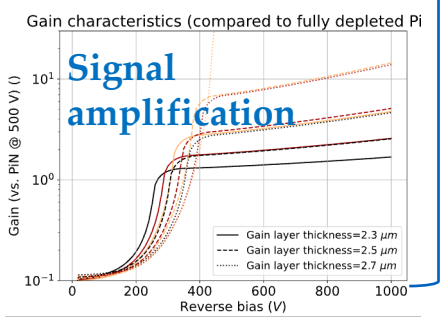
• Permittivity
• BG-narrowing (SB)
• Incomplete ionization Al (p) and N (n) doping
• Split energy levels (N)
	• Mobility:
	  • Temperature dep.
	  • Doping dep.
	  • High field saturation
	• Impact ionization
		• SRH
		• Surface-SRH
		• Auger
		• Traps ($Z_{1/2}$-defect)
		• Radiative



LGAD simulation





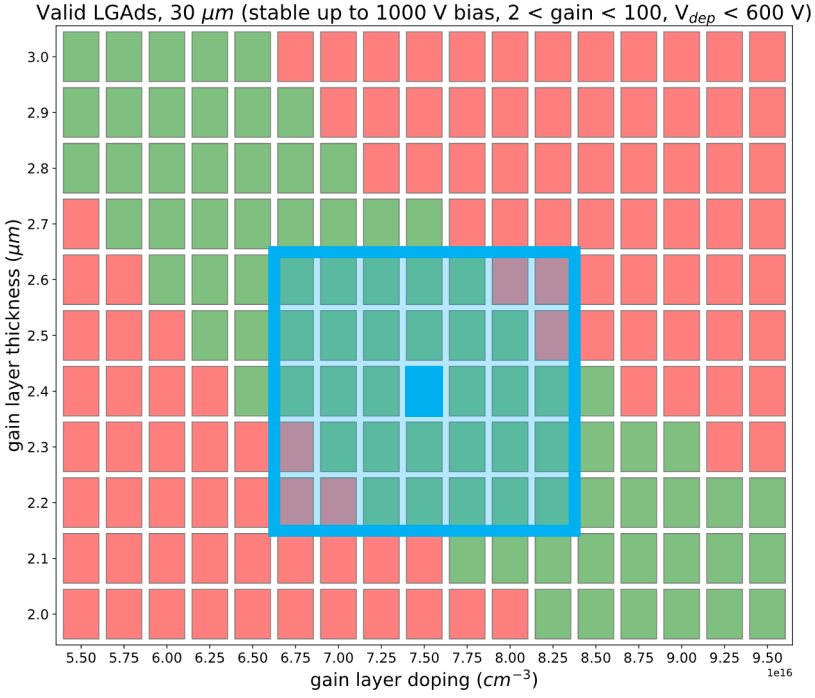


Operational requirements:

- $V_{depletion} < 600$ V
- Breakdown > 1000 V
- 2 < gain < 100

Final design:

- Meeting uncertainties of wafer vendor
- 10 wafers ordered/finished
- CERN-RD50 common project



Design parameter	Target
Sensor thickness	30 µm
Gain layer thickness	2.4 µm
Gain layer doping	$7.5 \cdot 10^{16}$ cm^{-3}

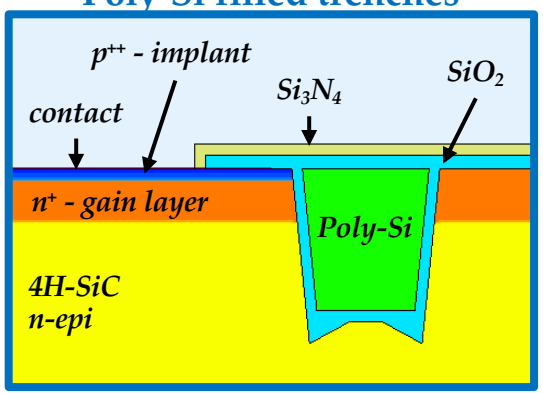
LGAD simulation

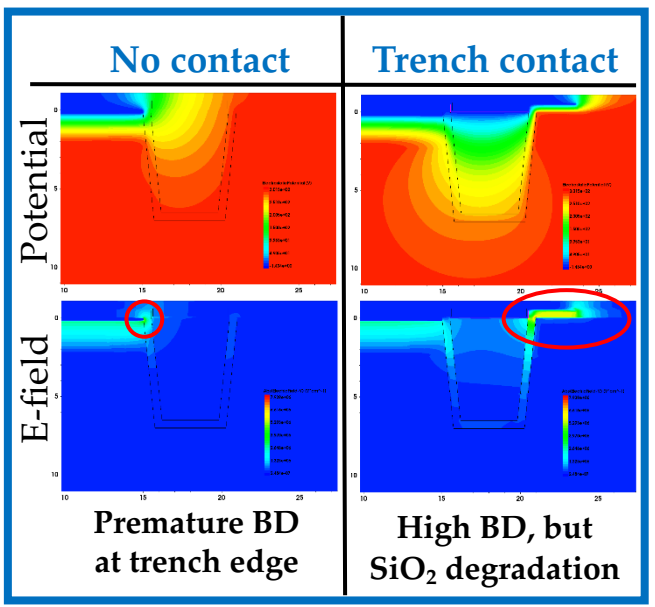
Guard structure design

- Simple implants not possible, since gain layer is grown
- Processing by CNM Barcelona

- Simulations still ongoing
- Combined approach (trenches + JTE) looking promising (> 700 V)

Poly-Si filled trenches





Additional JTE implants