The CLIC Vertex Detector

Vertex Detector Discussion Meeting – DESY (Hamburg)

May 6, 2024

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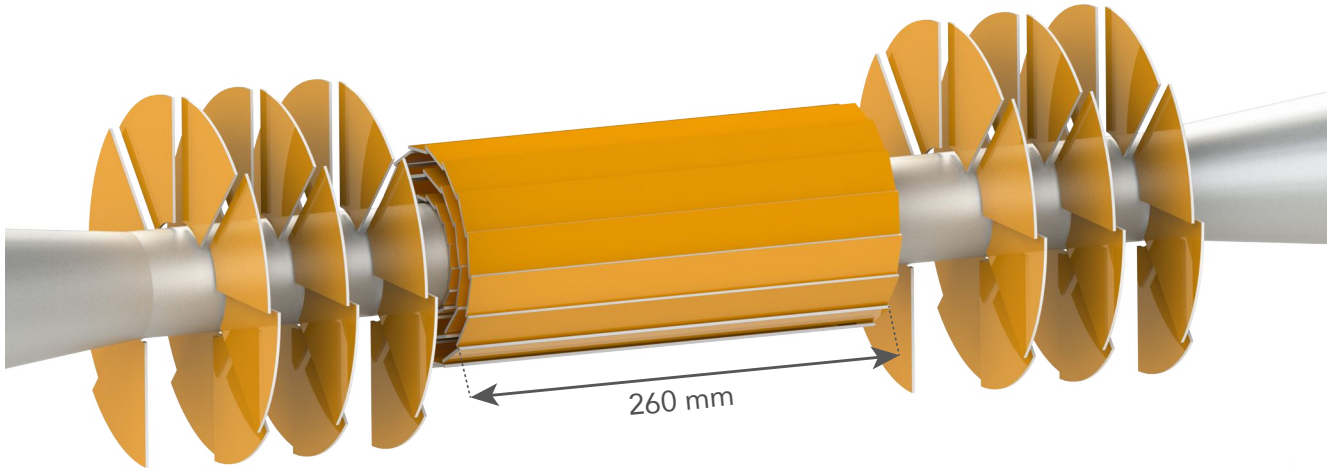
Outline

- CLIC accelerator and experimental conditions
- Vertex-detector requirements and concept
- Technology R&D examples
- Conclusions

- Focus on earlier CLIC-specific studies not covered in other talks
- Many results also applicable for other Lepton Collider proposals

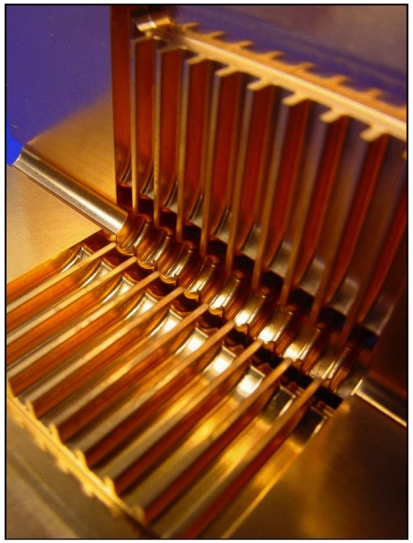


The Compact Linear Collider

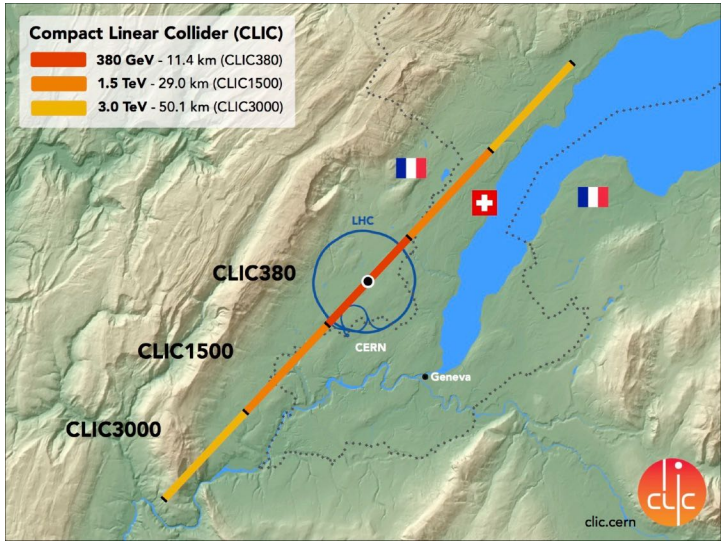
CLIC (Compact LInear Collider): linear e^+e^- collider concept for post HL-LHC phase

- 2-beam acceleration scheme, operated at room temperature
- Gradient: 100 MV/m
- $\sqrt{s}$ up to 3 TeV
- Luminosity: 6×10^{34} $cm^{-2}s^{-1}$ (at 3 TeV)
- Staged construction: $\sqrt{s}$ from few hundred GeV up to 3 TeV
- Physics goals:
  - Precision measurements of SM processes (Higgs, top)
  - Precision measurements of new physics potentially discovered at 14 TeV LHC
  - Search for new physics: unique sensitivity to particles with electroweak charge

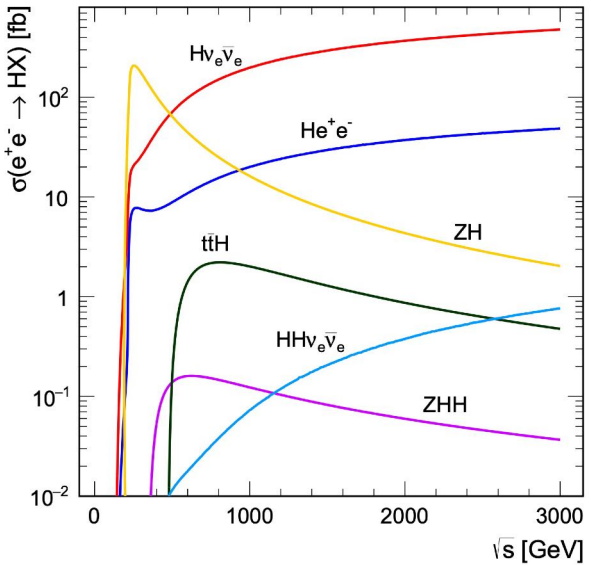
CLIC accelerating structure



CLIC @ CERN



Higgs production processes



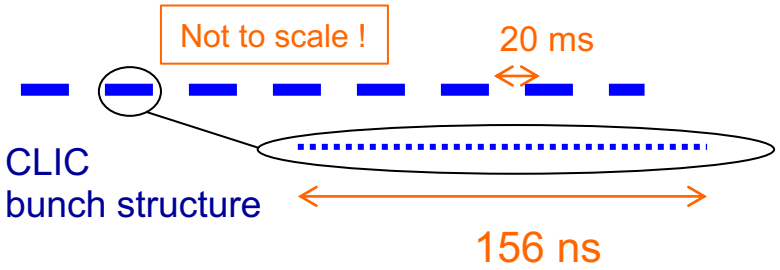
Experimental conditions at CLIC

- CLIC operates with bunch trains, 50 Hz repetition rate

→ Very low duty cycle

→ Trigger-less readout between trains

→ Allows for power-pulsed operation of detector, to reduce average power consumption

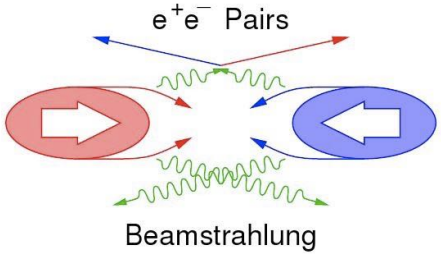


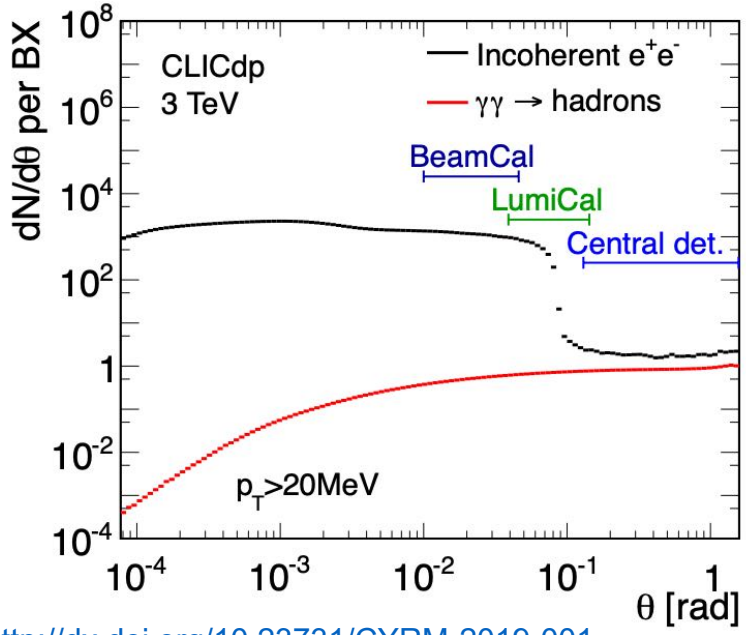
- Collisions within 156 ns bunch trains
- High E-fields lead to Beamstrahlung

→ High rates of beam-induced background particles

→ Drives detector design (layout, granularity, timing)

Very small bunches:
40 nm (x) x 1 nm (y) x 44 μm (z)
(at 3 TeV)





http://dx.doi.org/10.23731/CYRM-2019-001

Main backgrounds in detector

- **Incoherent e+e- pairs**
  - 19k particles / bunch train at 3 TeV
  - Constrains beam pipe radius, granularity
- **γ γ →hadrons events**
  - 17k particles / bunch train at 3 TeV
  - Constrains granularity, layout, impacts physics

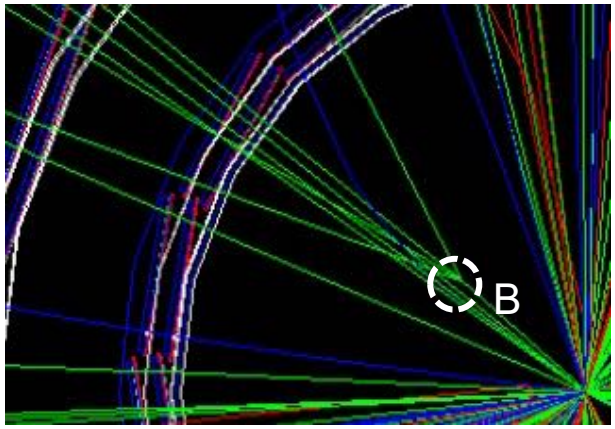
High instantaneous hit rates (up to 6 GHz/cm^2), however: very low readout rate (50 Hz)

CLIC vertex-detector requirements

- efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

a~5 μm, b~15 μm



→ good single point resolution: σ_{SP}~3 μm
→ small pixels ≲ 25x25 μm², analog readout
→ low material budget: X ≲ 0.2% X_0 / layer
→ corresponds to ~200 μm Si, including supports, cables, cooling
→ low-power ASICs (~50 mW/cm²) + air-flow cooling

- 20 ms gaps between bunch trains → trigger-less readout, pulsed powering
- B = 4 T → Lorentz angle becomes important

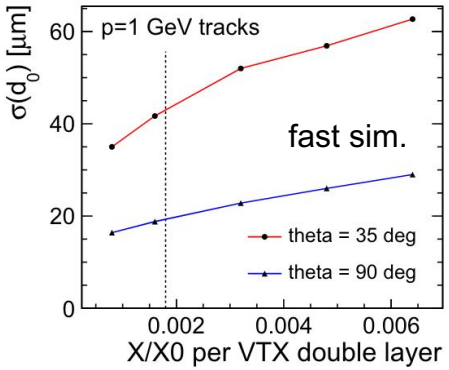
- few % maximum occupancy from beam-induced backgrounds → sets inner radius
- moderate radiation exposure (~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm²/y
  - TID: < 1 kGy / year

- Time stamping with few ns accuracy, to reject background
  → Fast detector signals / frontend

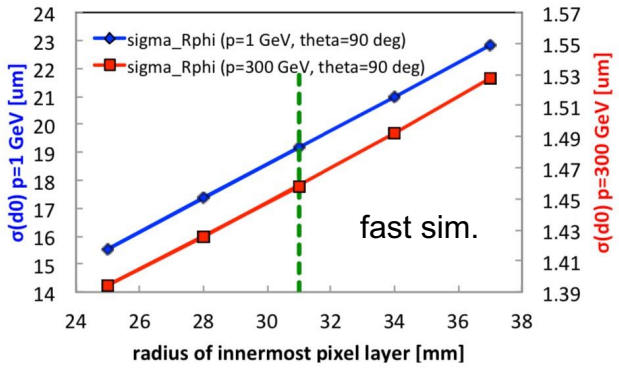
Vertex detector design optimisation

- Study impact of technology parameters (pixel size, material budget) on detector performance
- Optimization of detector geometry (# layers, placement) for given technology assumptions
- Using fast simulations (LiC detector toy) and Geant-4 based full detector simulations including beam-induced backgrounds
- Main benchmark parameters: impact-parameter, flavor-tagging performance, reconstruction efficiency

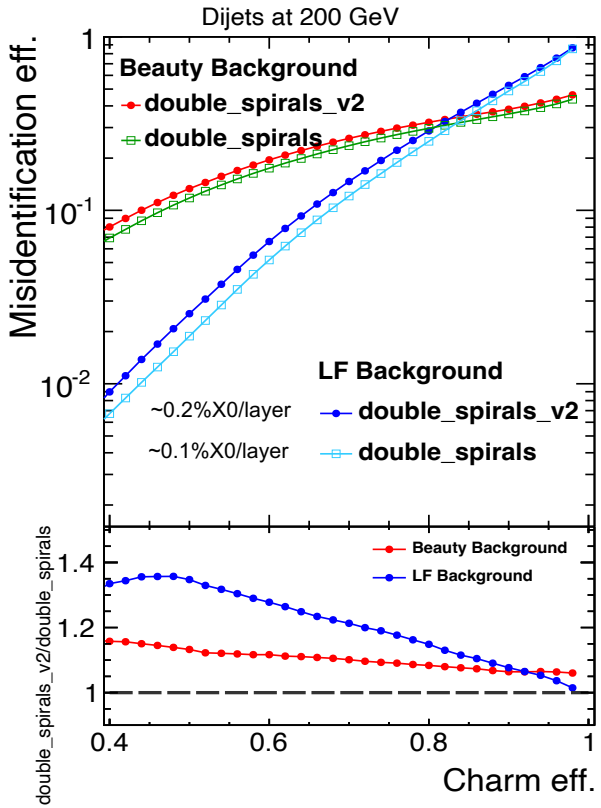
Impact-param. resol. vs. material



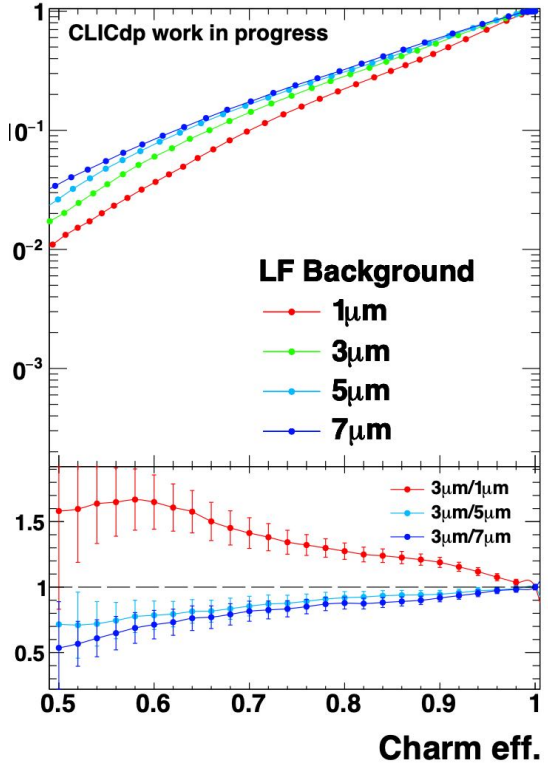
Impact-param. resol. vs. R_{min}



Flavor tagging vs. material budget



Flavor tagging vs. resolution



https://doi.org/10.48550/arXiv.1202.5940

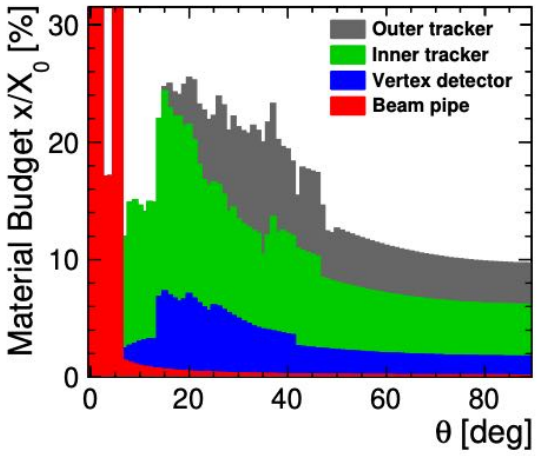
https://cds.cern.ch/record/1742993

CLIC vertex-detector concept

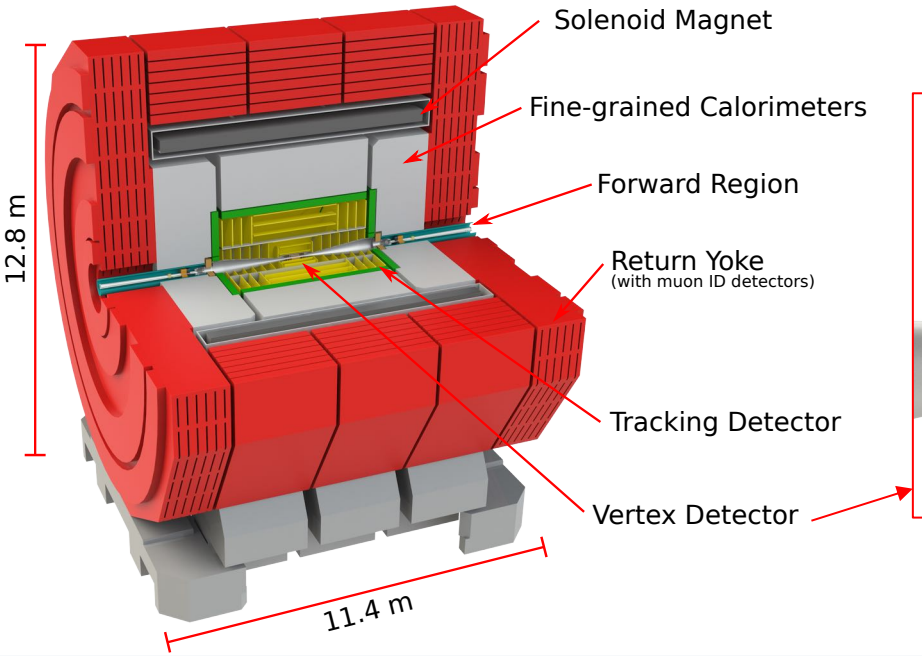
Silicon-pixel vertex detector:

- 3 double layers in barrel and endcap
  (different from barrel-only inner trackers of STAR, Belle-2, ALICE ITS3, Mu3e!)
- Spiral-shaped endcap geometry, to allow for air cooling
- σ_{SP}~3 μm → pixel sizes 25x25 μm^2
- material budget: ≲ 0.2% X_0 / layer
  (equivalent to ~200 μm silicon)

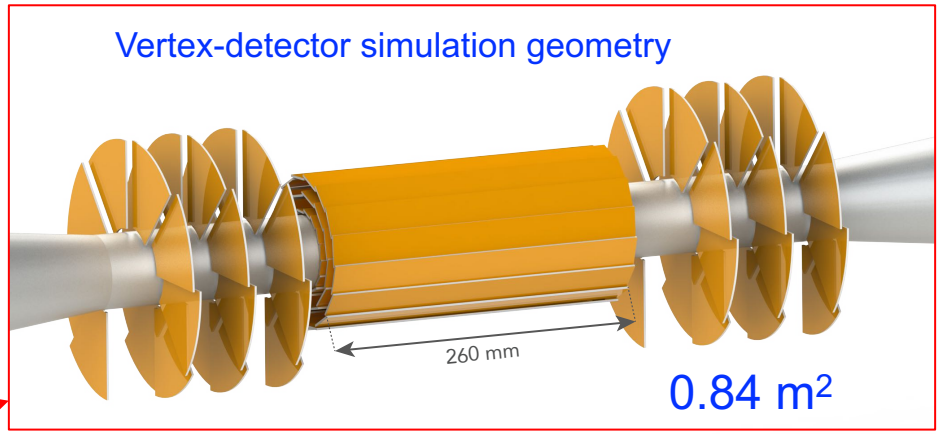
CLIC inner det. mat. budget



CLICdet detector concept



Vertex-detector simulation geometry



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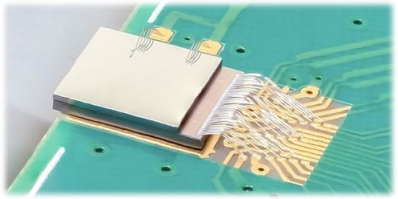
CLIC pixel-detector R&D

Hybrid Assemblies

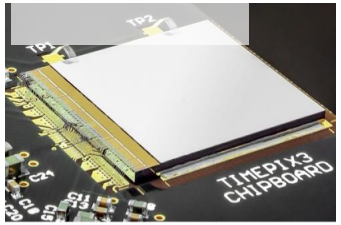
CLICpix2 + planar sensor



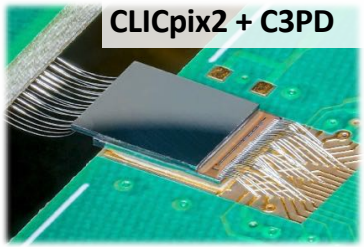
65 nm CMOS

200 nm SOI

Timepix3 ACF-bonding



130 nm CMOS



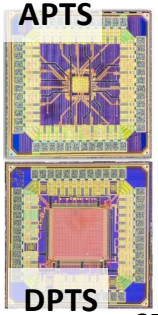
65 nm CMOS
+ 180 nm HV-CMOS

Monolithic Sensors

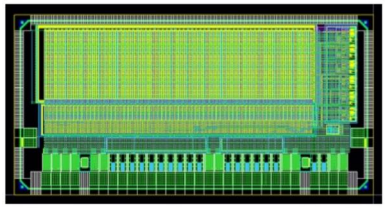
180 nm HV-CMOS

180 nm CMOS

180 nm CMOS



65 nm CMOS

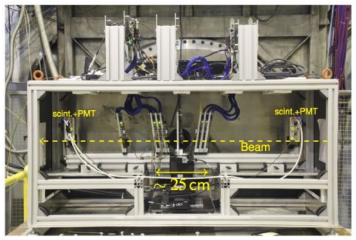


H2M

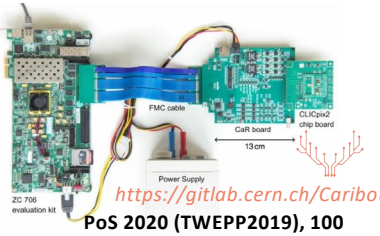
Tools

Detector technologies for CLIC, CERN-YR-2019-001

CLICdp beam telescope



Caribou readout system



https://gitlab.cern.ch/Caribou

PoS 2020 (TWEPP2019), 100

MC Simulation framework: Allpix Squared

https://gitlab.cern.ch/allpix-squared/allpix-squared

NIM A 901 (2018) 164-172

Analysis & reconstruction framework: Corryvreckan

https://gitlab.cern.ch/corryvreckan/corryvreckan

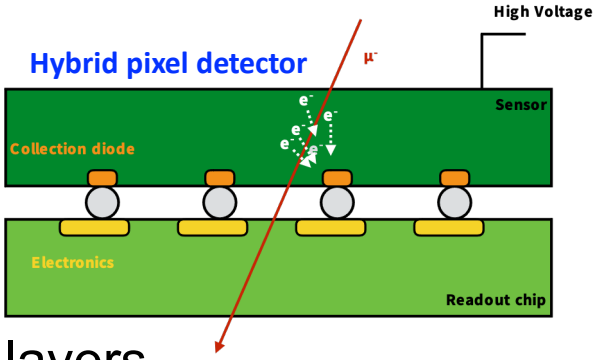
2021 JINST 16 P03008

- Diverse R&D program, focusing on conceptual studies + small technology demonstrators

→ Flexible tools developed, to support the R&D and exploit synergies between the various R&D lines

- R&D performed within various collaborative frameworks (CLICdp, CERN EP R&D, AIDAinnova, Tangerine) and with strong links to other projects (HL-LHC, FCCee, Mu3e, …)

Hybrid pixel detectors



Hybrid pixel detectors

- Target applications: CLIC vertex detector, track-timing layers
- Separate interconnected sensor and readout ASIC layers

→ Factorise R&D on sensors and readout ASICs

- Develop new sensor concepts, e.g.:
  - Thin sensors (50 μm) with large fill factor (active edge)
  - Active / passive CMOS sensors
  - Sensors with enhanced lateral drift (ELAD) for optimal position resolution
  - Sensors with charge amplification (LGAD) for picosecond timing
- Profit from advanced industry technologies for highest ASIC performance (rate, timing)
- Profit from synergy with (HL)-LHC developments, medical imaging, gaseous detector r/o (GridPix)
- Refine and develop new interconnect technologies
- Challenges: material budget, interconnect: cost, minimum pitch

CLICpix2 hybrid pixel detector

- CLICpix2 hybrid readout ASIC
  - 65 nm TSMC process
  - 128 × 128 pixels, 25 µm pitch
  - Simultaneous ToT (5-bit) and ToA (8-bit)
  - Integrated test pulse DACs and band gap

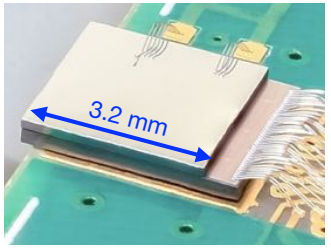
CLICpix2 analog F/E specifications

Parameter	Value
Power dissipation	≤ 12 µW
Area	≤ 12.5x25 µm^2
Input charge, Q_{in}	nominal 4 ke-, max. 40 ke-
Minimum threshold, $Q_{th,min}$	≤ 600 e-
Equivalent input-referred noise, $Q_{n,in}$	≤ 70 e-
ToT dynamic range	≥ 40 ke-
ToA accuracy	≤ 10 ns
Total ionizing dose (for 10 yr)	1 Mrad
Input charge types	e-, h+
Testability	in-pixel test pulse (i.e. Q_{test}) injection

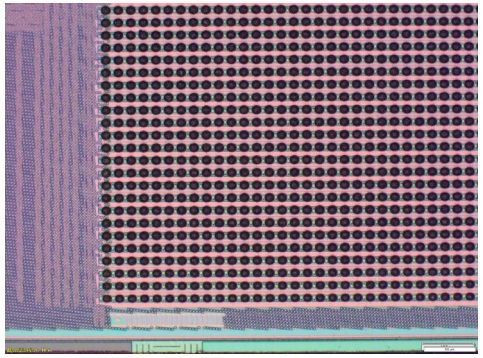
Single-die bump-bonding process developed by IZM:

- pitch 25 µm, sensor thickness down to 50 µm
- Support-wafer processing of ASICs from MPW for UBM and SnAg bump deposition
- Excellent interconnect yield >99.7% observed in laboratory and test-beam

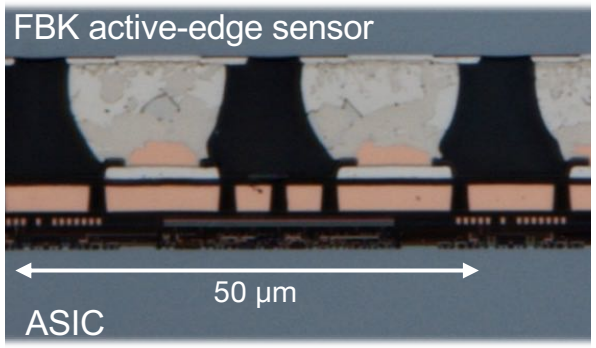
CLICpix2 hybrid assembly



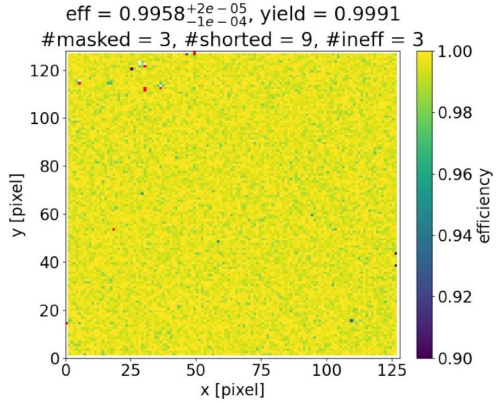
SnAg bumps on CLICpix2 (IZM)



25 µm bump bonding @ IZM



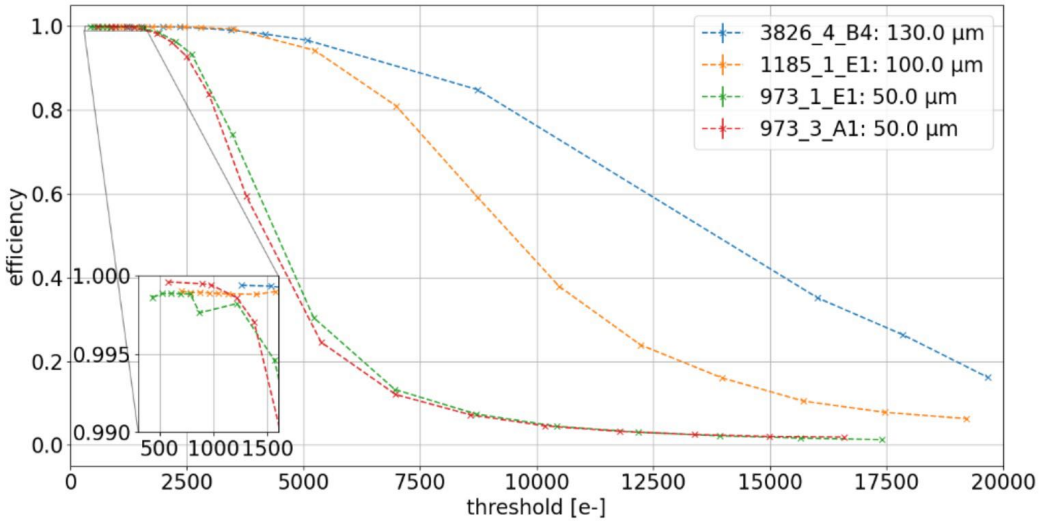
TB pixel efficiency 50 µm CLICpix2 ass.



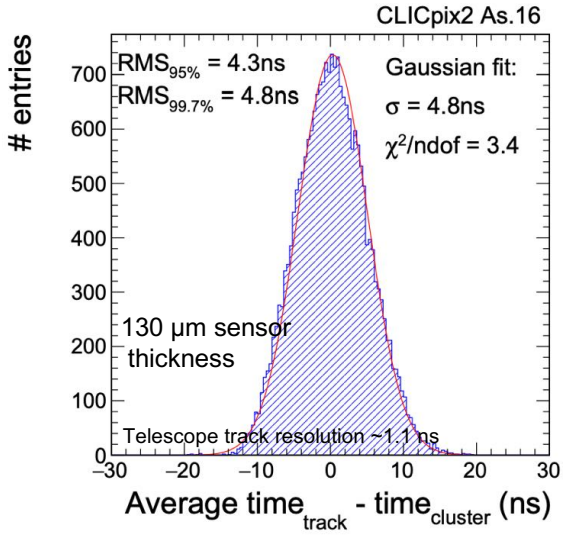
https://doi.org/10.1088/1748-0221/18/03/C03008

CLICpix2 test-beam performance with thin sensors

Efficiency with thin active-edge sensors (25 µm pitch)

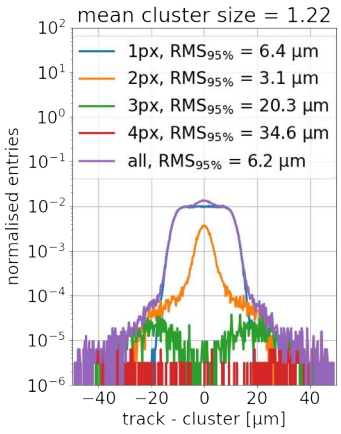


Timing residuals

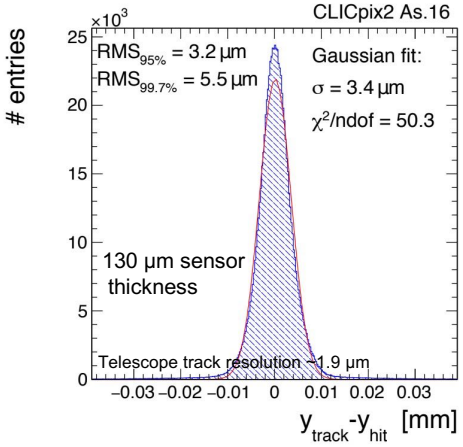


Spatial residuals

50 µm thickness



130 µm thickness



- Efficiency, spatial and timing resolution targets are achieved, but not yet simultaneously with material budget target
  → need advanced sensors with enhanced charge sharing and/or smaller pitch
  (→ 28 nm ASICs)

https://cds.cern.ch/record/2891650

Enhanced Lateral Drift sensors

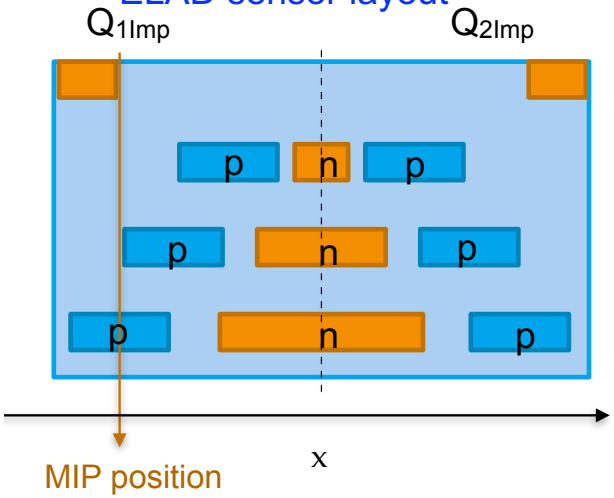
- Position resolution in very thin sensors so far limited to ~pixel pitch / √12 (almost no charge sharing)

→ **E**nhanced **LA**teral **D**rift sensors (ELAD) Patent DE102015116270B4

- Deep implantations to alter the electric field
  → lateral spread of charges during drift, cluster size ~2
  → improved resolution for same pitch (trade-off with efficiency)
- Challenges:
  - Complex production process, adds cost
  - Have to avoid low-field regions (recombination)
- TCAD and MC simulations: Implantation process, Sensor performance for MIPs
  → expect significantly improved position resolution vs. standard sensor
- In production (since 2019): generic test structures, strips and test sensors with Timepix footprint (55 µm pitch) → no recent follow-up
- Electric-field shaping is meanwhile pursued also in monolithic sensors, though with more shallow implants, realized in standard process flow

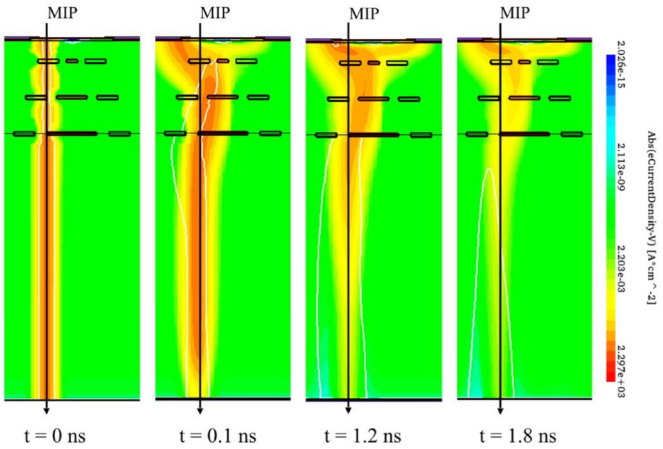
DESY PIER

ELAD sensor layout

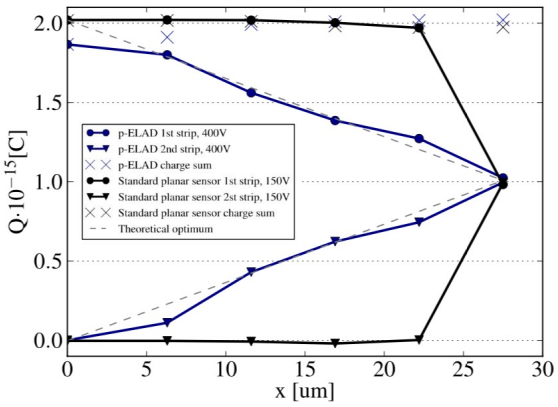


- Attempt to improve single-point resolution for thin sensors;
- Study not yet concluded

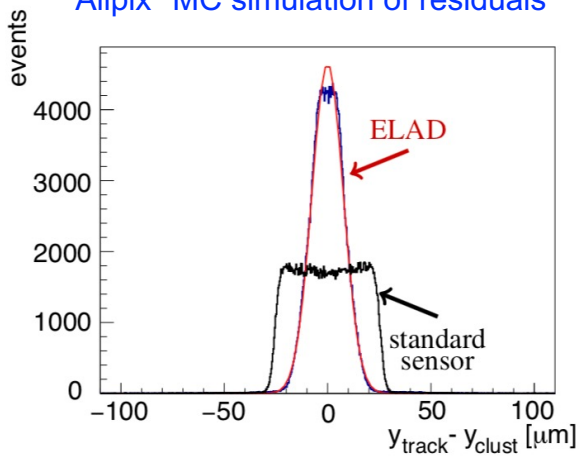
TCAD charge density simulation



Collected charge vs. MIP position



Allpix² MC simulation of residuals

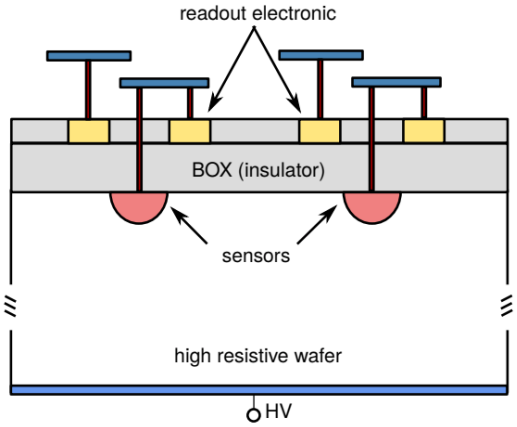


Silicon-on-Insulator (SOI) / 3D integration

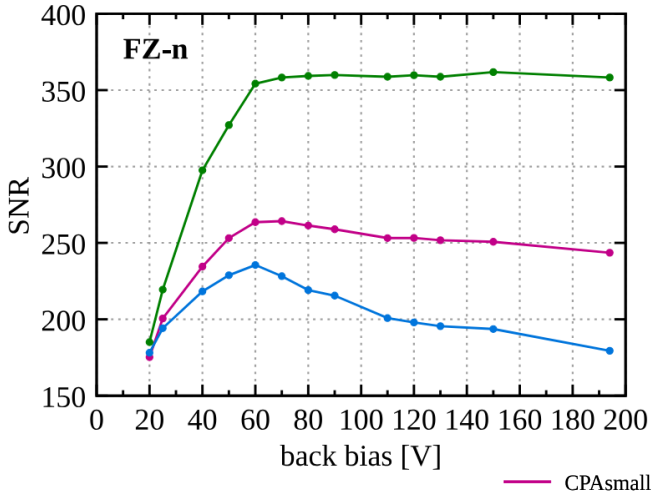
- Silicon-On-Insulator (SOI): r/o electronics on thin low-resistivity electronics wafer, separated from high-resistivity sensor wafer by buried insulation oxide layer
- Considered for CLIC vertex and tracker

- Cracow SOI test chip in 200 nm LAPIS SOI process, with various geometries and technology parameters: >=30x30 μm^2 pitch, single SOI and double SOI, rolling shutter r/o
- Test results for 300, 500 µm thickness, 30x30 μm^2 pitch >99% efficiency, σ_{SP}~1.5 (500 µm) - 3 µm (300 µm)

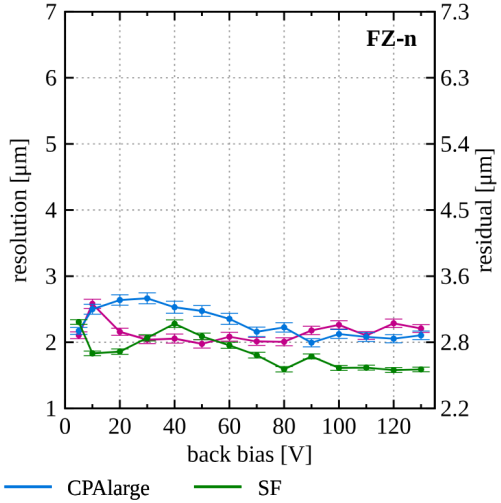
SOI pixel detector



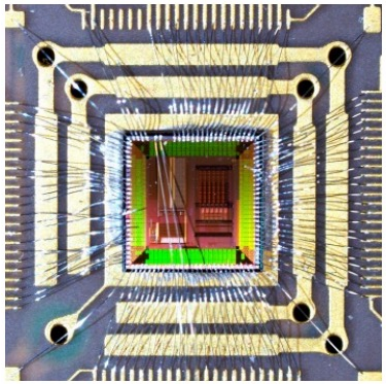
Signal/Noise for 500 µm FZ-n sensor



Resolution 500 µm FZ-n sensor



Cracow SOI test chip



- Developed dedicated reconstruction algorithms for large cluster sizes
- Excellent performance obtained for thick sensors
- Precision timing not yet demonstrated

Nucl. Instrum. Methods Phys. Res., A 988 (2021) 164897

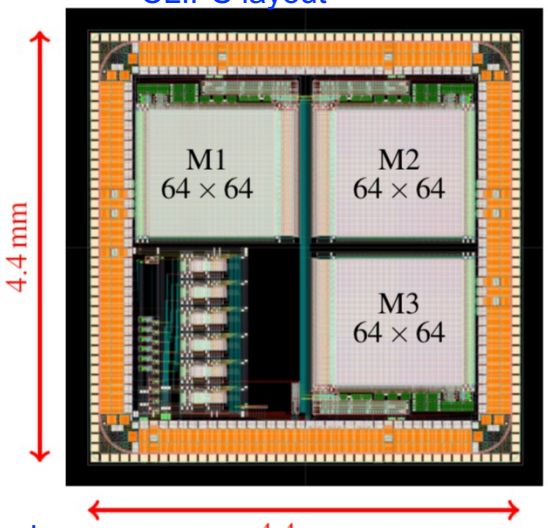
CLIPS SOI sensor

- CLIPS: AGH SOI chip targeted to Linear Collider vertex detectors:
  - 3 test matrices with 64x64 pixels, 20x20 μm² pitch
  - Targets spatial resolution <3 μm, time resolution <10 ns
  - Analog charge and time information in storage capacitors in each pixel
    → no need for fast clock distribution into matrix
  - Snapshot analog readout between bunch trains with external ADC
  - On-chip trigger to reduce the data rate

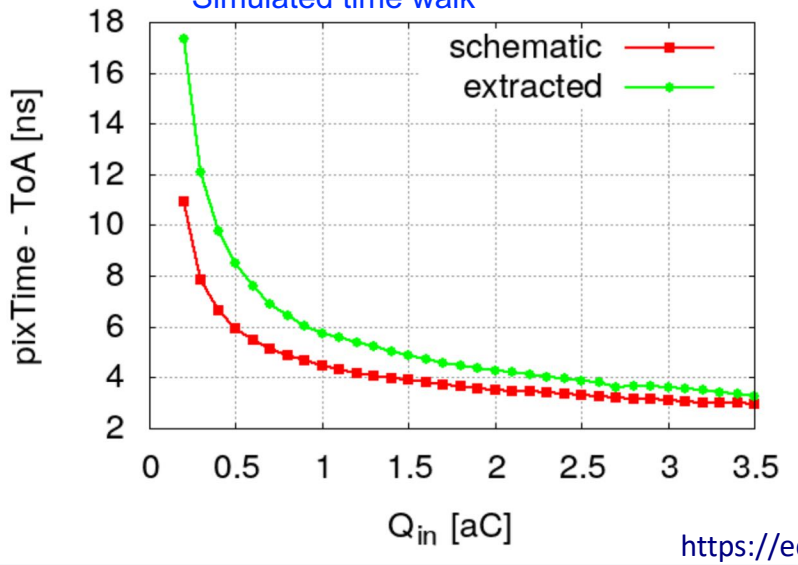
  - Chips fabricated on 500 μm thick FZ-n wafers received in 2019
  - Thinning of selected wafers to 100 μm
  - Test system not finished, project on hold due to lack of resources

r/o design specific to low duty cycle of CLIC machine → not suitable for circular colliders

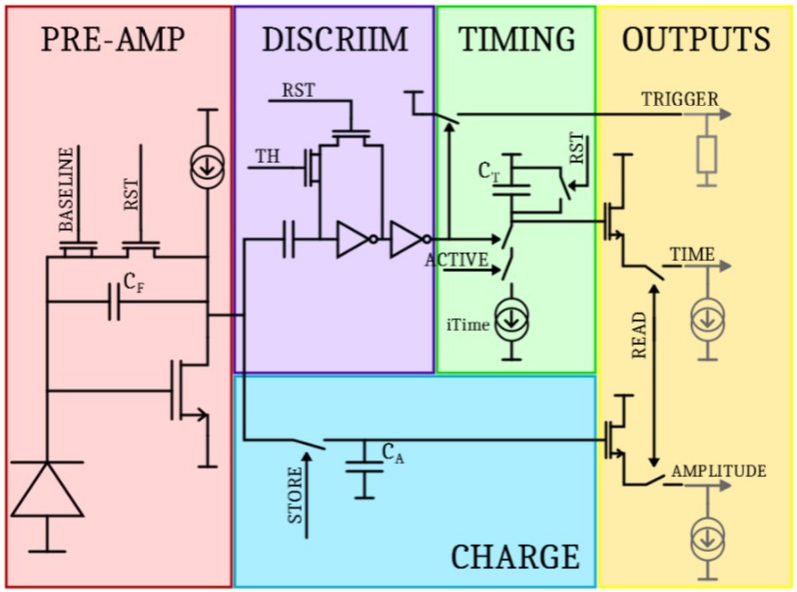
CLIPS layout



Simulated time walk



CLIPS frontend



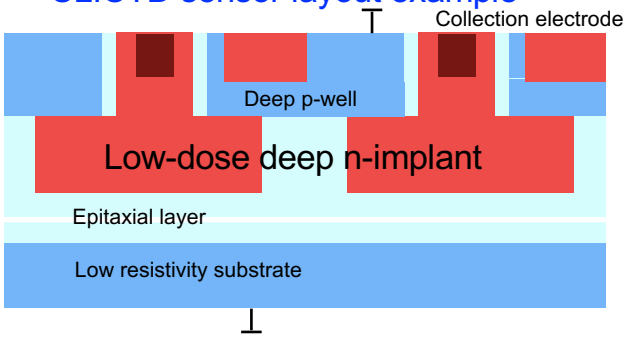
https://edms.cern.ch/document/2087018/1

CLICTD 180 nm CMOS

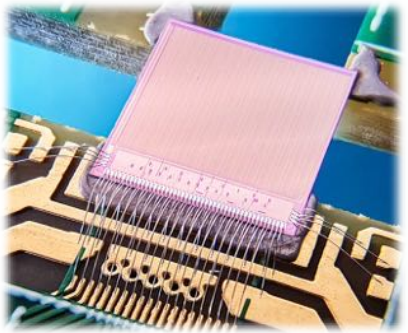
CLICTD 180nm monolithic sensor

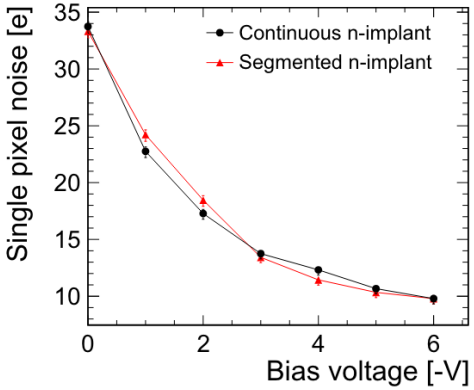
- Modified 180 nm CMOS imaging process with small-collection electrode
- Target application: CLIC tracker
- Innovative sub-pixel segmentation, Channel pitch: (8 x 37.5) µm x 30 µm
- Simultaneous time and energy measurement per channel
- Exploring large parameter space of sensor-design modifications, substrate materials (epitaxial, high-resistivity Czochralski) and thicknesses (40-300 µm), in collaboration with ATLAS MALTA / STREAM
- Detailed TCAD/Geant4-based simulations (Allpix^2), validated with test-beam data

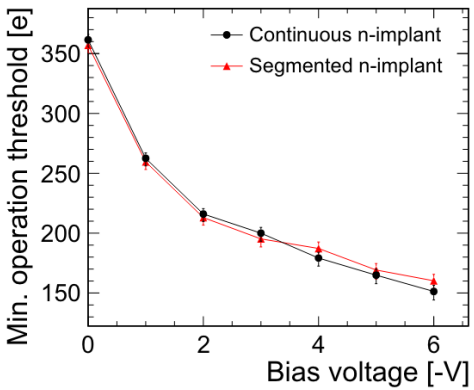
CLICTD sensor layout example



CLICTD on test board







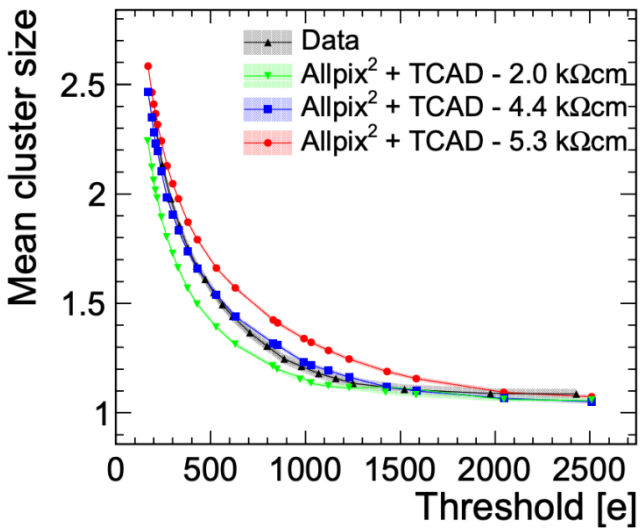
At nominal conditions (-6V):

- noise ~10 e$^-$
- minimum threshold ~150 e$^-$

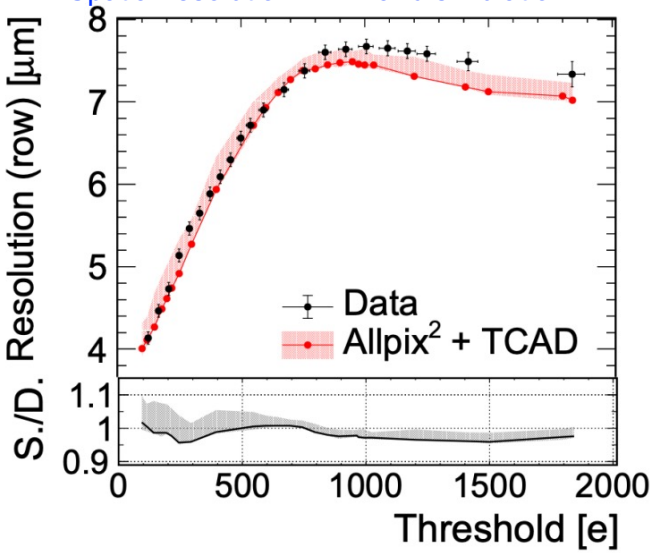
K. Dort, CERN-THESIS-2022-071

CLICTD test-beam results

Cluster size in TB and simulation



Spatial resolution in TB and simulation



IEEE TNS 67.10 (2020): 2263-2272
NIM A 1006 (2021) 0165396
NIM A 1041 (2022) 167413

K. Dort, CERN-THESIS-2022-071

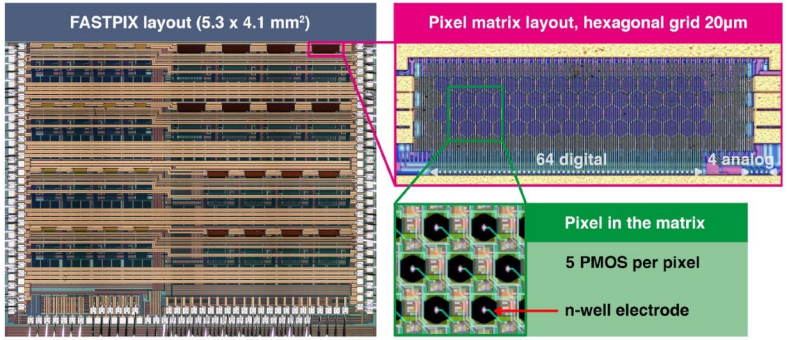
	Required (CLIC tracker)	Epi	Cz*
Spatial resolution (transv.)	< 7 µm	4.6 µm	4.3 µm
Time resolution*	~ 5 ns	5.2 ns*	4.4 ns*
Efficiency	> 99.7 %	> 99.7 %	> 99.7 %
Material content	< 200 µm	40 - 100 µm	100 µm

- Excellent performance observed in test-beam measurements and reproduced by simulations
- Performance gain from Cz wafer with larger depletion → limited by frontend (not optimized for Cz)
- Validated simulations used for parameter extraction
- Results have served as input to sensor optimization, also for 65 nm process

ATTRACT FASTPIX 180 nm monolithic

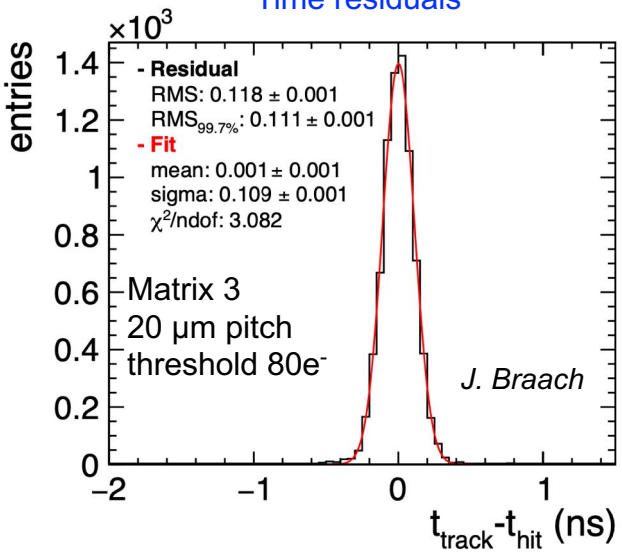
FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process, 25 µm epi, design optimisations for for fast charge collection
- Small hexagonal pixels (8.7 to 20 µm pitch)
- Focus on sensor performance, with limited in-pixel circuitry and not yet optimised for low power
- Time-encoded position and pulse-height readout
- Exploring large parameter space of process and design variations
- Minimum operation threshold ~80 e-
- Time resolution of ~100 ps achieved at >99% efficiency
- Position resolution ~1.3 µm for 8.7 µm pitch

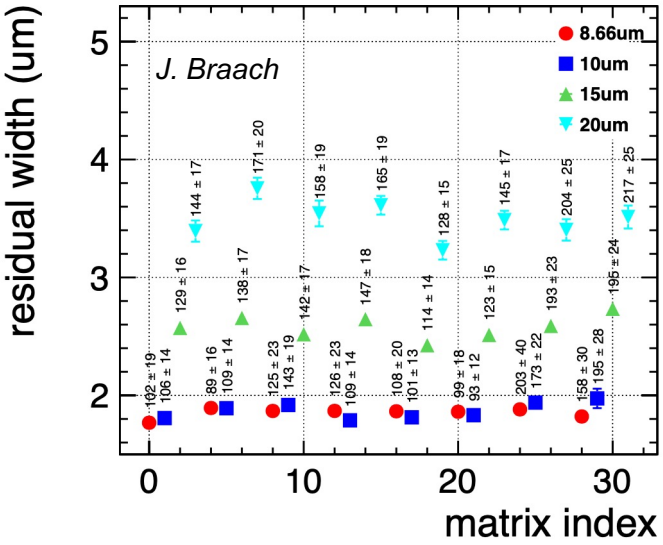


http://dx.doi.org/10.3390/instruments6010013
https://doi.org/10.1016/j.nima.2023.168641

Time residuals



Spatial residuals (x-direction)



- Minimum threshold ~80 e-
- Time resolution of ~100 ps achieved at >99% efficiency
- Position resolution down to ~1.3 µm for 8.7 µm pitch
- ~15-20 µm pitch required for 3 µm resolution

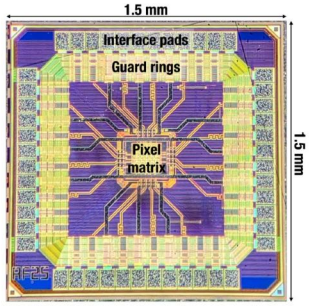
APTS/DPTS 65 nm CMOS

APTS analog test sensor
- Modified 65 nm CMOS imaging process, several design variants, ~10 µm epi layer
- 6x6 matrix, pitch from 10 to 25 µm
- External analog signal readout for 4x4 pixels
- Small signals (~500 e^-) from thin epi
- Threshold ~100 e^-, noise ~25-30 e^-
- Efficiency >99% for thresholds 80-200 e^-
- Small amount of charge sharing

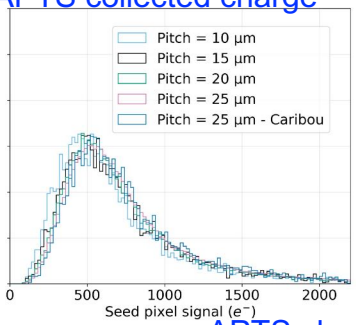
→ Resolution of 3 µm for pitch ~15 µm

DPTS test chip
- Modified 65 nm CMOS imaging process, several design variants, ~10 µm epi layer
- 32x32 matrix, 15 µm pitch
- Time-encoded external ToA and ToT readout (similar to FASTPIX)
- Minimum threshold ~100 e-, noise ~10 e^-
- Pos. resolution >~4 µm, time res. ~6 ns

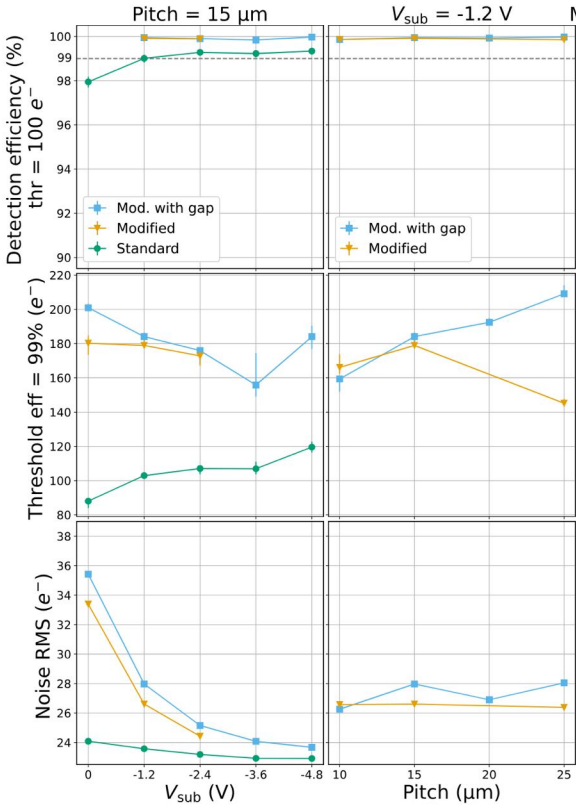
See also the 65 nm presentations by Auguste (MOSS/MOST and others), Manuel (APTS), Ziad (CE65), Christian (DESY ER1) and Sara (H2M)



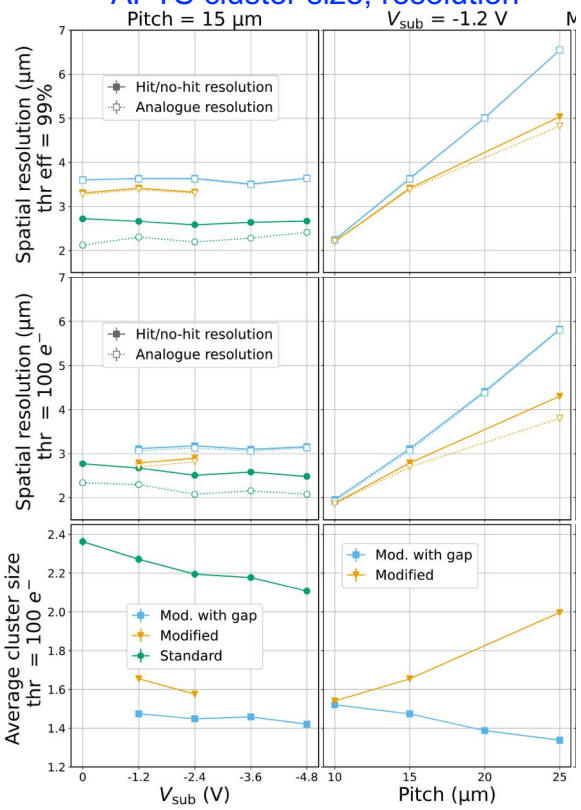
APTS collected charge



APTS noise, efficiency



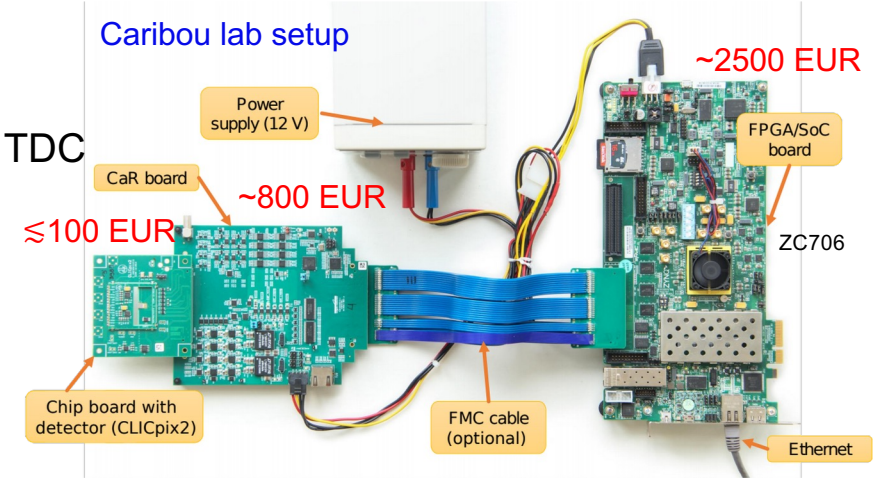
APTS cluster size, resolution



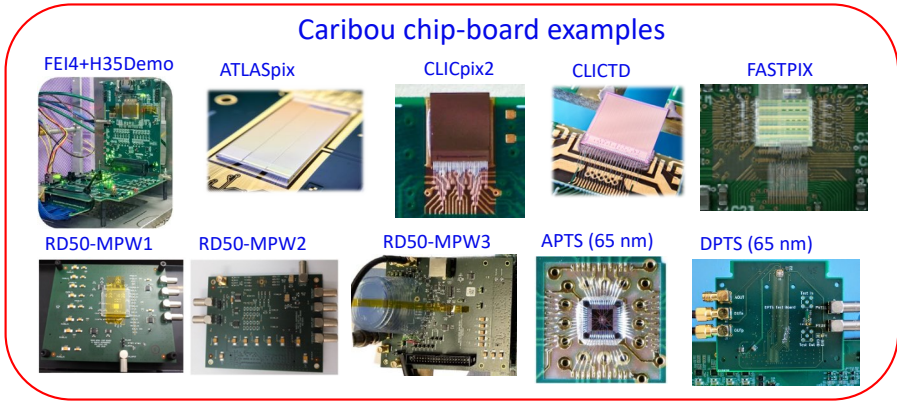
APTS: https://doi.org/10.48550/arXiv.2403.08952
DPTS: https://doi.org/10.1016/j.nima.2023.168589

Caribou DAQ

Caribou versatile open-source DAQ system
- Re-usable hardware, firmware and software
  - System-on-Chip (SoC) board (ZC706)
    - Embedded CPU for Linux operating system, DAQ software (Peary), user interface
    - FPGA for detector control and data processing, TDC
  - Common Carboard interface board
    - Physical interface from SoC board to detector
    - Provides resources (voltage regulators, ADCs, pulse/clock generator)
  - Application-specific chip carrier boards
    - Detector and passive components



Target applications:
- Lab and beam tests of silicon-detectors
- Optimised for R&D support, easy integration of new prototypes
- Not targeting project-specific DAQ in large experiments



Support from RD50 / DRD3:
- Coordinated purchase orders for Carboards
- Financial support through RD50/DRD *common projects*
- Currently preparing order for v1.5 Carboards

https://gitlab.cern.ch/Caribou/

http://dx.doi.org/10.1088/1748-0221/12/01/P01008

http://dx.doi.org/10.22323/1.370.0100

https://doi.org/10.1088/1748-0221/18/02/C02005

Conclusions + Outlook

- Stringent requirements for CLIC vertex detector
  - 3 µm position resolution, <=0.2%X0 / layer, few nanoseconds time resolution
- Optimized detector concept with all-silicon tracker proposed
- Broad silicon-pixel detector R&D exploring different technologies
- Large synergies with approved projects, but no complete overlap of requirements
- Fulfilling all requirements simultaneously remains challenging
- Limitations in 65 nm CMOS
  - Circuit density requires >=35 µm pitch for the desired in-pixel functionality
  - Thin epitaxial layer requires <=15 µm pitch

  → Can we get starting material with thicker epitaxial layer?
- Current + futures projects profit from development of simulation, analysis and DAQ tools

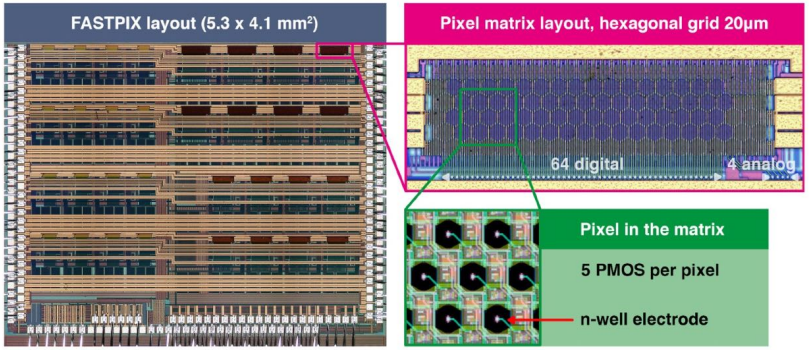
This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under GA no 101004761.
Some of the measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

Additional Material

ATTRACT FASTPIX

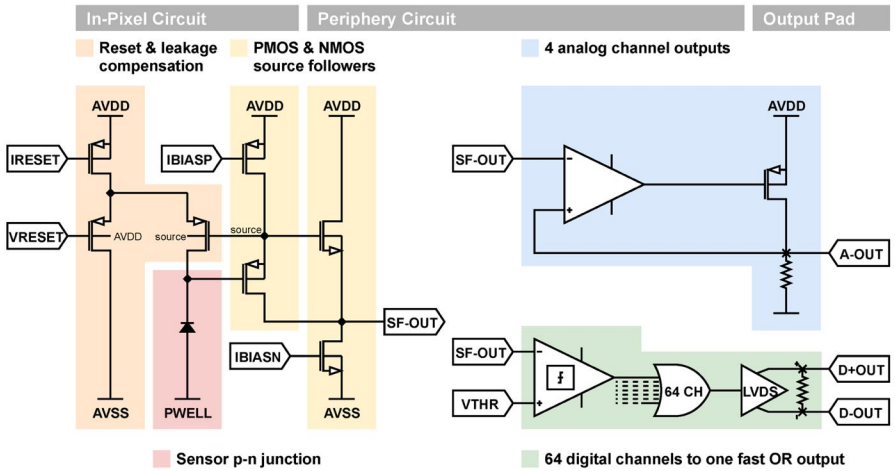
FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process
- 32 mini matrices of hexagonal pixels (8.66 to 20 µm pitch)
- 4 analogue outputs + 4x16 pixels with ToT/ToA
- Various sensor designs and process options
- Position and ToT encoding via delay lines (asynchr. r/o)



On-chip readout circuit

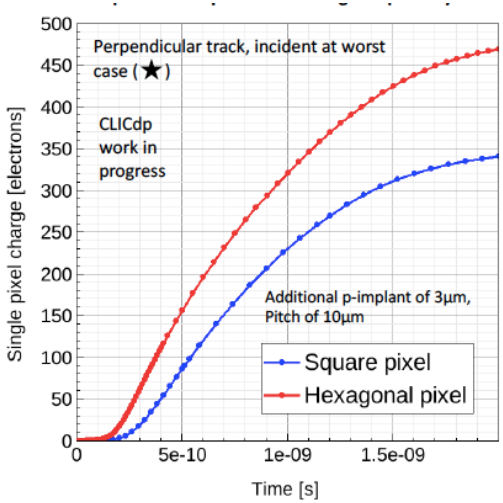
W. Snoeys, T. Kugathasan

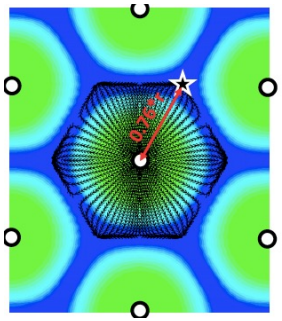


Simulated chip parameters:

Sensor capacitance		1 fF
Equivalent Noise Charge		11 e^-
Jitter (for Q_{in} = 1000 e^-)		20 ps
Power	In pixel source follower	18 µW
	Periphery discriminator	150 µW
	Analog monitoring buffer	20 mW

3D TCAD Simulation





T. Kugathasan et al: Monolithic CMOS sensors for sub-nanosecond timing, Hiroshima 2019

- Optimised for precise sensor timing in 3D TCAD simulation studies
- Hexagonal pixel layout:
  - Improved charge collection at pixel edges
  - Reduced number of neighbouring pixels
    → Less charge sharing