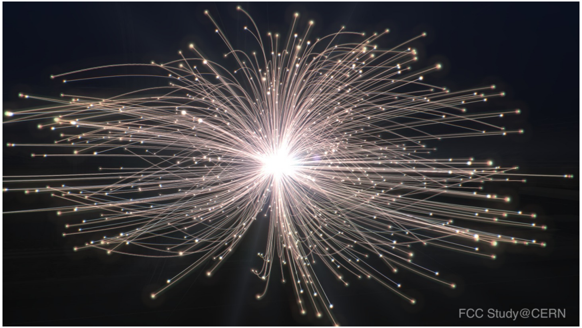
FCC-ee vertex simulations ... and more!

Vertex Detector Discussion Meeting at DESY

Armin Ilg

University of Zürich

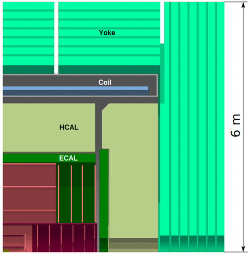
06.05.2024



University of Zurich UZH

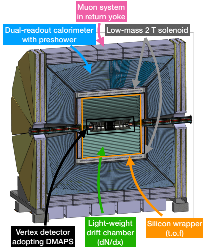
FUTURE CIRCULAR COLLIDER

FCC-ee detector *concepts*



CLD: CLIC-Like Detector [1, 2].

- ILC → CLIC → FCC-ee (→ μCol)
- Si vertexing and tracking
- Highly-granular ECAL and HCAL, CALICE-like
- Solenoid coil outside calorimeter system



IDEA: Innovative Detector for e^+e^- Accelerators [3, 4].

- Si vertexing
- Drift chamber (down to 1.6% X/X0, d$N_{\mathrm{ion.}}$/dx)
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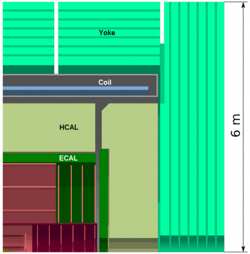
ALLEGRO: A Lepton coLLider Experiment with highly GRanular calorimetry Read-Out (M. Aleksa).

- Si vertexing and drift chamber
- Highly granular noble liquid ECAL, Pb/W+LAr or W+LKr
- ECAL and solenoid coil in same cryostat
- CALICE-like or TileCal-like HCAL

FCC-ee detector *concepts* + variations (RICH, crystal ECAL, ...

University of Zurich[UZH]



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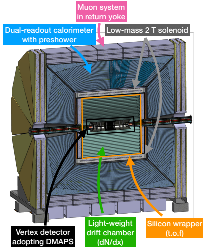

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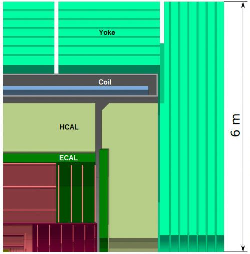

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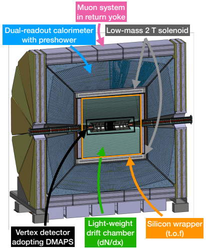

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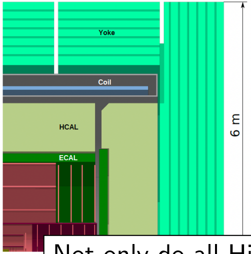

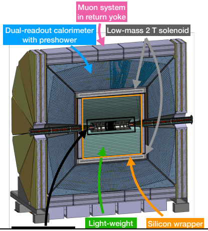

CLD: C

Not only do all Higgs factories foresee silicon pixel sensors for the vertex detectors, they all foresee specifically *Depleted Monolithic Active Pixel Sensors* (DMAPS)

r

ular

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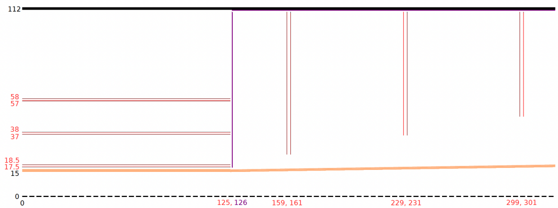
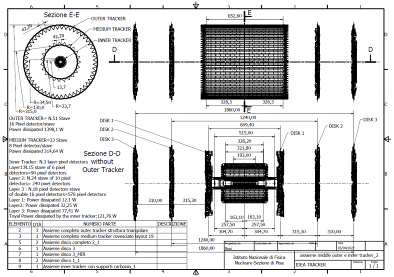
See August's talk tomorrow for detailed discussion on FCC-ee vertex requirements

CLD → Rescaled CLICDet vertex detector



arXiv:1911.12230

IDEA → New vertex detector layout



F. Palla , see talk at FCC US week at BNL

- $r_{\text{min}} = 13\,\text{mm}$, vertex system until $r = 112\,\text{mm}$, $z = 300\,\text{mm}$
- Three double-layer barrel layers and disks
- No engineering studies since CLICDet developments

- $r_{\text{min}} = 13.7\,\text{mm}$, vertex system until $r = 315\,\text{mm}$, $z = 930\,\text{mm}$
- Three single-layer barrel layers
- Two outer barrel layers and three disks
- Engineered design, integrated into MDI

FCC-ee vertex detector layouts

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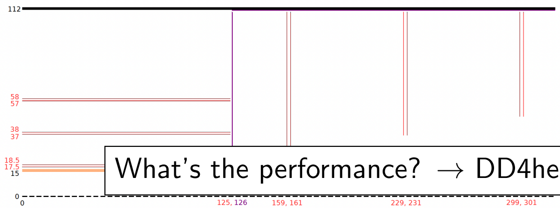

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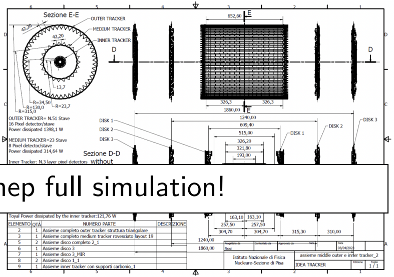

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What's the performance? → DD4hep/Key4hep full simulation!

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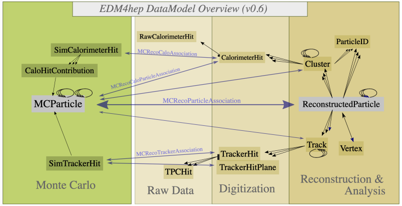
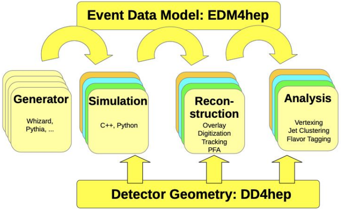
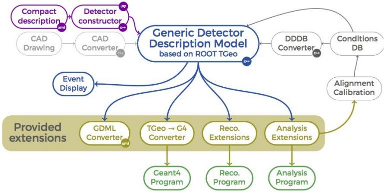
The common software vision: Key4hep

Key4hep is a huge ecosystem of software packages adopted by all future collider projects, complete workflow from generator to analysis

- Event data model: EDM4hep for exchange among framework components
  - Podio as underlying tool, for different collision environments
  - Including truth information
- Data processing framework: Gaudi
- Geometry description: DD4hep, ability to include CAD files
- Package manager: Spack: `source /cvmfs/sw.hsf.org/Key4hep/setup.sh`

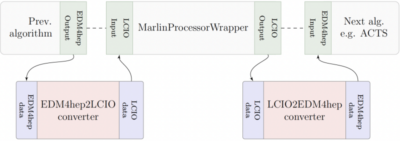




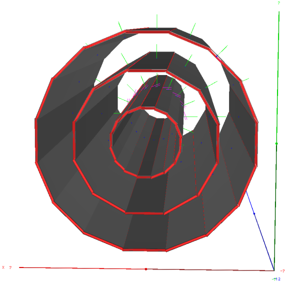


Detector model in k4geo

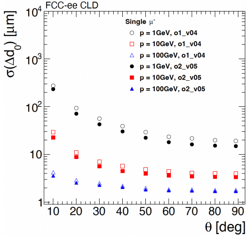
- Linear collider reconstruction (iLCSoft/CLICPerformance)
- Can generate EDM4hep output using k4MarlinWrapper



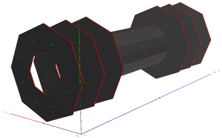
Access to all LC tools: PandoraPFA, LCFI+, etc.



CLD vertex barrel



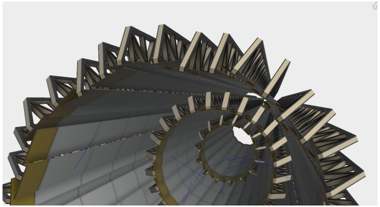
Updated CLD vertex (G. Sadowski, 7th FCC Physics Workshop)

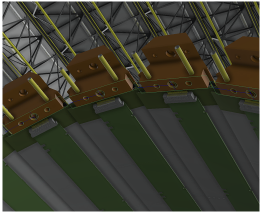


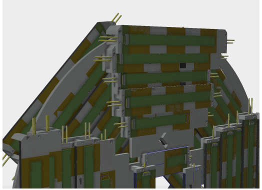
CLD endcap and vertex barrel

IDEA vertex detector: Design

Vertex detector by INFN Pisa (more details in F. Palla's talk at 2nd FCC US Workshop), support tube by INFN-LNF, holding lumical, vertex and beam pipe (more on MDI in M. Boscolo's talk)

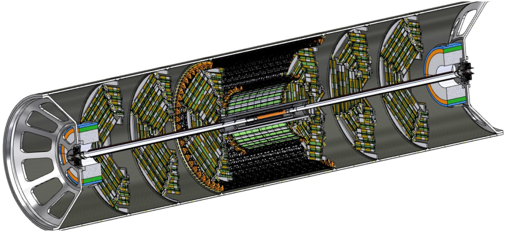






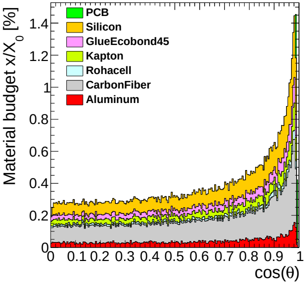
Vertex outer barrel and vertex disks using quad ATLASPix3 DMAPS with $150 \times 50\,\mu m^2$ pixels, water-cooled

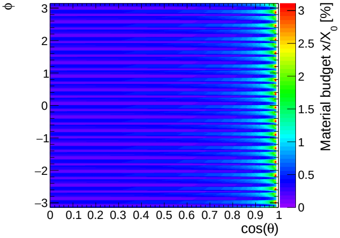
Vertex inner barrel consisting of staves of dual ARCADIA DMAPS, with pixels of $25{\times}25\,\mu m^2$ ($\sim 3\,\mu m$ single point resolution), air-cooled



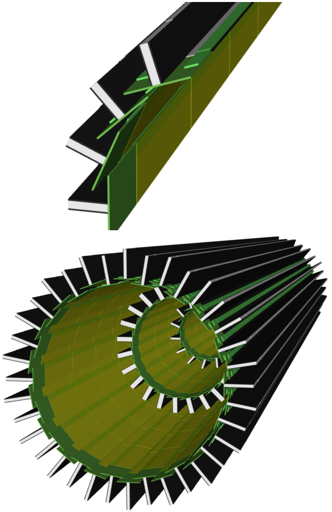
Vertex inner barrel

- $r_{\text{min}} = 13.7\,\text{mm}$, 2 mm to beam pipe (can we go closer?)
- Correct material stack, flexes, end-of-stave hybrid, insensitive sensor areas (2 mm)
- Proxy volume for stave holding structure
- Support structure CAD model can be imported (more details in backup), service cones missing
- Material budget in line with 0.3% per layer at $\cos(\theta) = 0$ (CDR assumption)





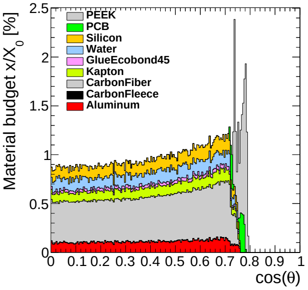
First layer

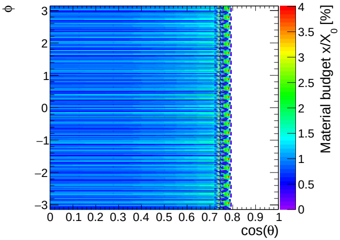


Vertex inner barrel, without support

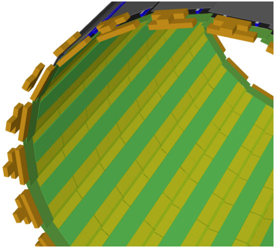
Vertex outer barrel

- Correct material stack, correct description of ATLASPix3 insensitive peripheries
- Proxy volumes for truss structure and cooling pipes
- Proxy volume for end-of-stave holder (orange, material budget contribution optimised with F. Palla)
  - → Still significant contribution

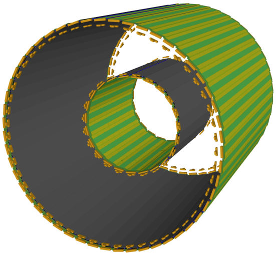




Complete outer barrel



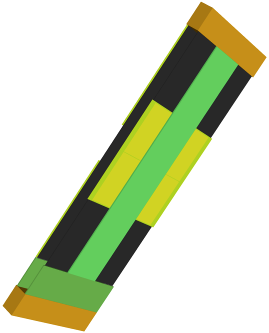
Middle tracker



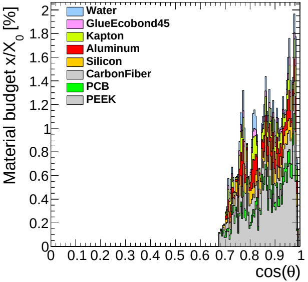
Complete vertex outer barrel system

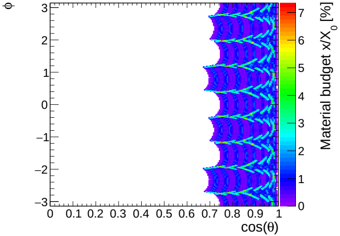
Vertex disks

- Correct placement of all modules in r and z
- Missing vertex disk global support
- Very uneven x/X_0 distribution

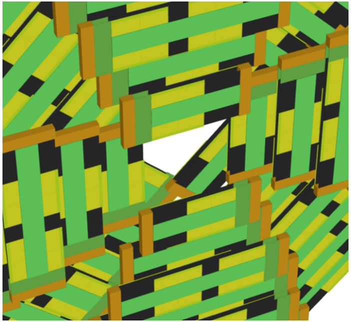


One short stave

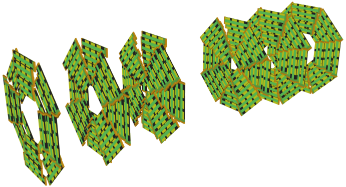




Disk 0

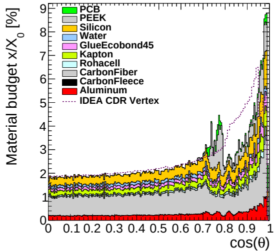


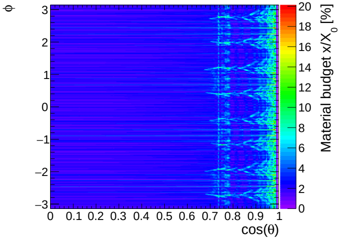
Disk 0 zoom-in



Complete vertex disks system

Complete system





Complete vertex system

- Material budget comparable with CDR estimate
- First working version on k4geo, update imminent with some fixes (getting rid of last overlaps)
- Plan to include last missing volumes using DDCAD
- Look at all material budget evaluations as a lower limit, there's always gonna be more added! (e.g off-detector cabling)
- No drift chamber tracking available yet → instead use CLD and iLCSoft reconstruction
  - Frankenstein approach: Remove CLD vertex detector (and a couple of Inner Tracker layers and disks) and instead insert IDEA vertex, run CLD full simulation
  - Results foreseen for FCC Week next month
- How can we further improve vertex detector performance?

Sensor-only vertex detector

University of Zurich[UZH]

DMAPS in 65 nm TPSCo process

- More logic per cm^2
- Lower power consumption → Air cooling
- Enables 12" wafers → Wafer-scale bent sensors!

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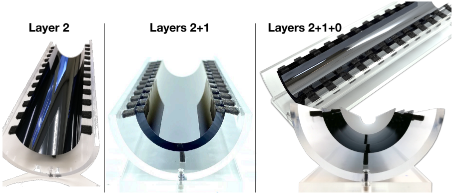
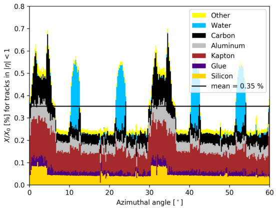
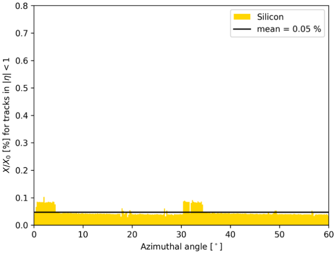
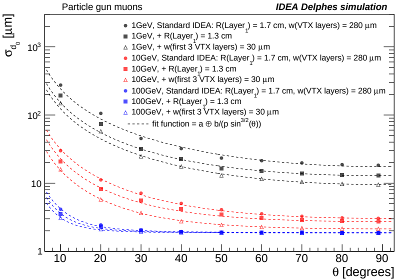


Layer assembly concept for ALICE ITS3 [6]





Material budget in ALICE ITS2 (left, [7]) and silicon only (M. Mager)



L. Freitag (BSc. thesis [8])

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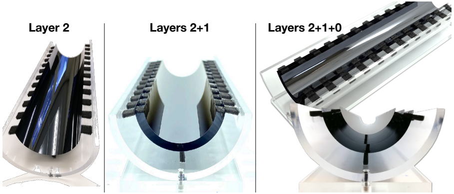

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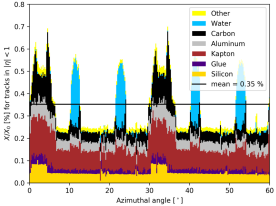

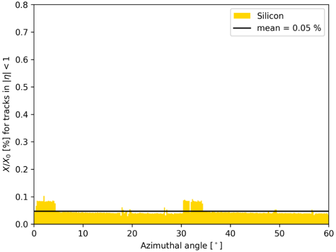

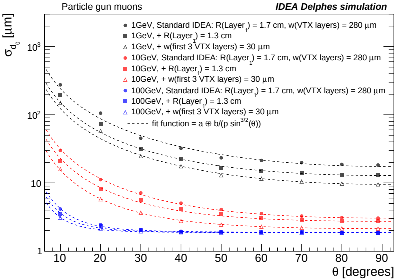

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L. Freitag (BSc. thesis [8])

How can such a vertex detector be realised at FCC-ee? → See also here

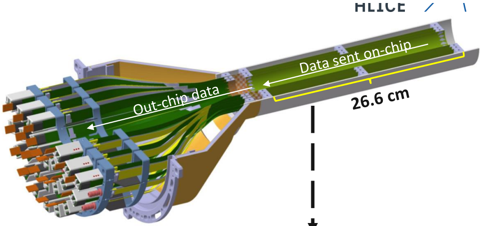
ALICE ITS3 layout

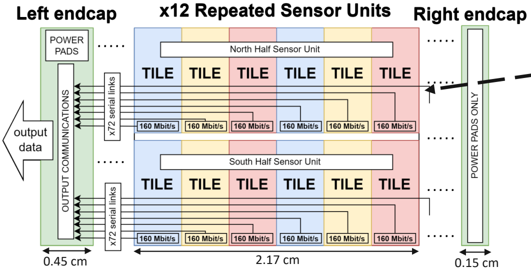
University of Zurich[UZH]

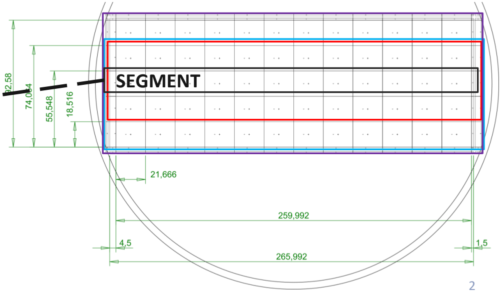
ITS3
- Wafer-scale Monolithic Active Pixel Sensors (**MAPS**)
- Cylindrical sensors of radii 18/24/30 mm

Architecture requirements (**Stitching)**
- Dies divided into 3,4 or 5 **Segments**
  - **2 endcaps** on the edges
  - **12 Repeated Sensor Units** (RSU)
    - *12 tiles per RSU*

Data transfer on-chip to the left edge (26.6 cm)





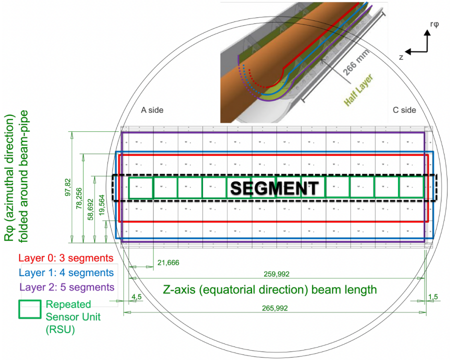


M. Rodriguez @ TWEPP 2023

Differences between ALICE ITS3 and FCC-ee

University of Zurich[UZH]

- First layer at smaller radius, from 18 to 13.7 mm
  - → Mechanically okay, electrically to be demonstrated
  - → First layer to use just two segments to reach smaller radius
- ITS3 readout only in one direction → We want to measure forward-backward asymmetries extremely precisely
  - → Read and power from both sides where possible
- ITS3 doesn't care too much about forward coverage → We do. down to $\theta = 140$ mrad
  - → Need to find solution for 3rd and 4th layer! → Multiple wafer-scale sensors in a row in z
  - → Ensure flexes, cables, etc. are not in front of lumical
- ITS3 doesn't care too much about hermeticity → We do.
  - → Cannot overlap multiple staves/ladders as in ATLAS/CMS
  - → Evaluate impact of only $\sim 95\%$ coverage per layer (chip service region and gap between sensors)
  - → Increase number of layers from 3 to 4 to ensure at least three hits



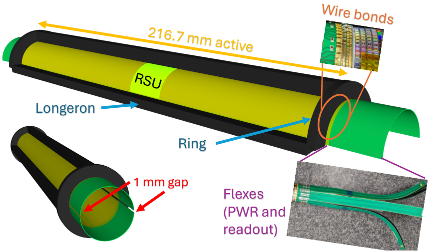
Ultra-light vertex concept principles

Layer 1 and 2

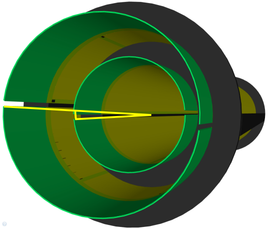
- Coverage down to 125 mrad (155 mrad) for layer 1 (layer 2)
- Gap of 1 mm between half-barrels, layer 2 rotated in ϕ by 8° to avoid overlap with layer 1
- Readout and power from both sides

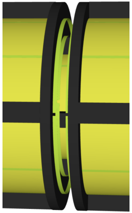
Layer 3 and 4

- Two sensors per side, readout only on sides, power on sides and center (power wire)



Layer 1 layout

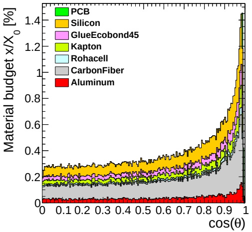

Layer 1+2


$z =$ region with layer 3 and 4

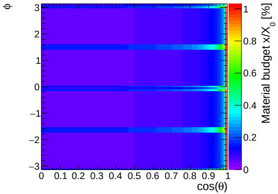
First material budget evaluation (preliminary!)

University of Zurich[UZH]

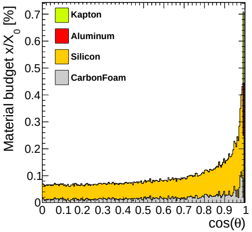
Layer 1 (classic vertex)



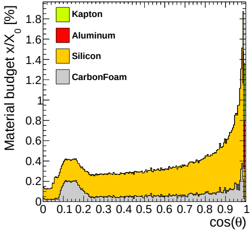
Ultra-light layer 1 ($cos(\theta)$ vs. ϕ)



Ultra-light layer 1



Ultra-light layer 1–4

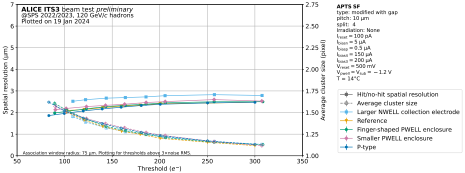


Material budget reduction of ~ 5, uniform distribution in ϕ except for longeron locations

MAPS R&D towards FCC-ee vertex detectors

- APTS Source Follower characterisation last year
  - Comparing different collection electrode designs
  - Studying in-pixel efficiency
- CE-65 characterisation since last year

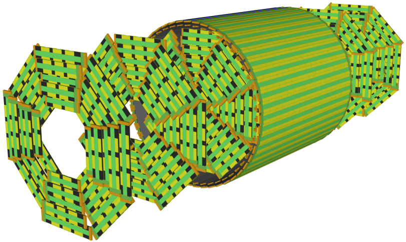
→ Continue with 65 nm development, hopefully together with many other institutes!



R. Wittwer, TREDI2024

FCC-ee detector simulation

- Implemented IDEA vertex detector (and Silicon Wrapper) in DD4hep
- Study IDEA vertex detector performance
- Investigate ultra-light vertex detector concept
- Study beam backgrounds in IDEA vertex
- Started hit digitisation inside Key4hep using Allpix^2-generated LUT à la M. Bomben



Establishing Swiss FCC initiative, with planned focus on vertex detector development

With trigger ($\sim$ 200 kHz rate) or without?

- Problem is incoherent pair background in first vertex layer
- Occ $= 70 \times 10^{-6}$, 25 μm pixels $\rightarrow$ 1 GHz hit rate $\rightarrow$ with trigger $O(150\,\text{Mb/s})$, without trigger $O(25\,\text{Gb/s})$ per $25.6 \times 6.4\,\text{mm}^2$ ARCADIA module (see F. Bedeschi)
- Impact on power consumption ($\rightarrow$ and material budget)?
- n.b: Safety factor of 5 and cluster size of 3 assumed, $\mathcal{L}$ increased since study
- Connected to choice of high vs. low charge sharing sensor

How good should the spatial resolution be? At what cost?

Are curved wafer-scale MAPS feasible for FCC-ee?

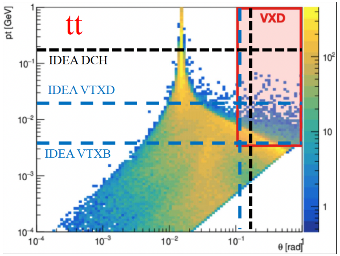
- No show-stopper so far

Technologies for ultimate vertex detector performance

- Wireless readout, on-detector intelligence
- Vertex inside beam pipe (ALICE3), but beware of wakefield induced heat!

Table 2: Number of pairs produced per bunch crossing (BX) at the four working points, and maximum occupancy measured in the barrel and endcaps of the vertex detector and tracker (respectively VXDB, VXDE, TRKB, TRKE).

		Z	WW	ZH	$t\bar{t}$
1	Pairs/BX	1300	1800	2700	3300
10^{-6}	O_{max}(VXDB)	70	280	410	1150
10^{-6}	O_{max}(VXDE)	23	95	140	220
10^{-6}	O_{max}(TRKB)	9	20	38	40
10^{-6}	O_{max}(TRKE)	110	150	230	290



A. Ciarma

Thanks!

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http://cds.cern.ch/record/2851362. BSc thesis, presented 01 Feb 2023.

University of Zurich[UZH]

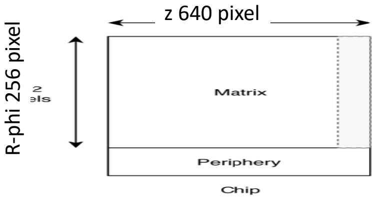
Istituto Nazionale di Fisica Nucleare

Module concept inspired by ARCADIA INFN R&D

- Depleted Monolithic Active Pixel Detectors (DMAPS) sensor and back-side processing already tested on silicon
- Pixel size 25x25 μm^2 , 50 μm thick
- Active area 640 pixel (16 mm) in z and 256 pixels (6.4 mm) in $r-\varphi$
- Chip periphery plus an inactive zone: total of 2 mm in $r-\varphi$
- Chips are side-abuttable in z

Composed of 2 pixelated parts: total of 8.4 mm $(r-\varphi)$ × 32 mm (z)

- Power budget not established yet: assume (reasonably) $50\ \mathrm{mW/cm^2}$



F. Palla , see talk at FCC US week at BNL

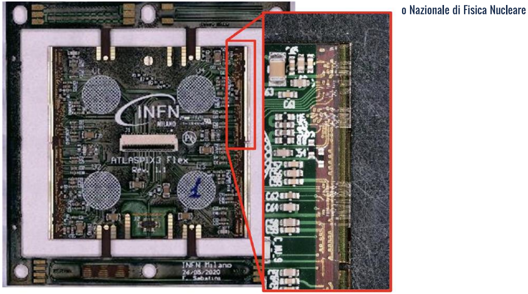
Outer tracker module

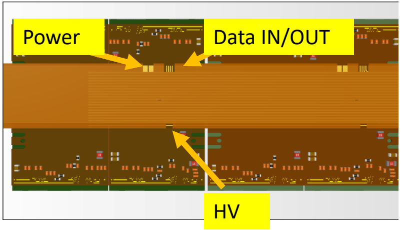
University of Zurich[UZH]

- Based on ATLASPIX3 R&D
  - DMAPS
  - 50 x 150 μm^2
  - Up to 1.28 Gb/s downlink
  - TSI 180 nm process
  - 132 columns of 372 pixels

  - Active (total) length (r-phi x z)
    - 18.6 (21) mm x 19.8 (20.2) mm
  - Module is made of 2x2 chips – total length:
    - size 42.2 mm x 40.6 mm

  - Power budget not established yet:
    assume $100\ \mathrm{mW/cm^2}$

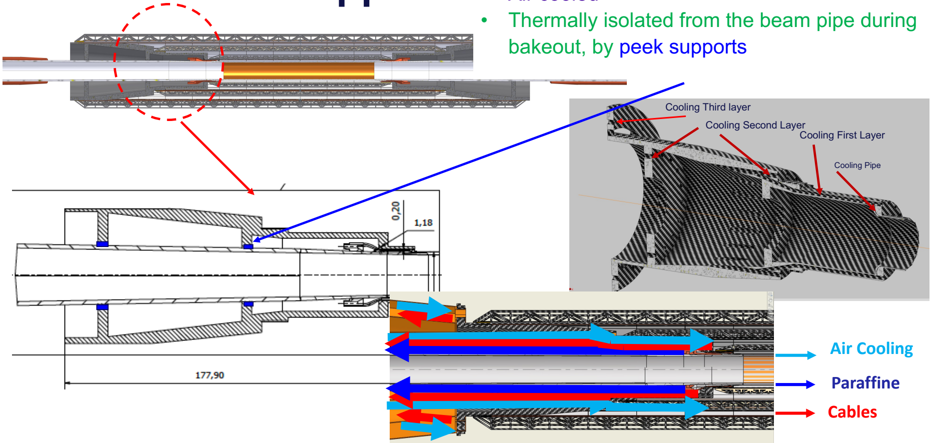




F. Palla , see talk at FCC US week at BNL

Inner Vertex support

- Anchored to the conical chamber
- Air cooled
- Thermally isolated from the beam pipe during bakeout, by peek supports



F. Palla, 2nd FCC US Workshop

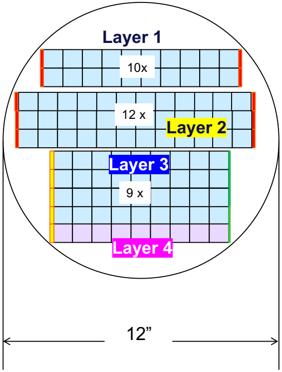
Data rates issues *(see F. Bedeschi talk at 7th FCC Workshop)*

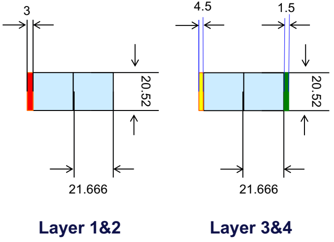
- **Largest data rates occur at the Z energy**
- **Expected data rates per BX/module [cluster size 5]**
  - From machine backgrounds (Incoherent pair creation – safety factor of 3) ~ 19 hits/BX/module
  - From collisions (200 kHz) ~ average ~<1 hit/BX/module
- **Inner layer ~400 MHz/cm^2 → ~25 Gb/s per module**
  - might be reduced if cluster size is only 2 – as measured for many MAPS
  - *ALICE3 hit rate ~100 MHz/cm^2 (pixel size 10μm x 10μm)*
  - 2nd layer ~10x less data volume
- **Triggered readout**: for 200 kHz the data bandwidth per module, rate is only 150 Mb/s
  - Impact on physics?

- **All these depend on pixel pitch, thickness, R/O architecture, bias voltage.**
  - For a review see M. Winter talk at March 11 meeting

F. Palla, 2nd FCC US Workshop

Same reticle for all layers





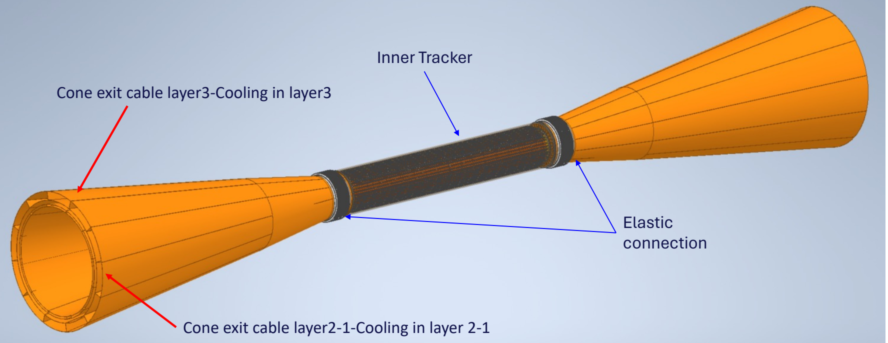
Layer	Radius (mm)
1	13.7
2	20.23
3	26.76
4	33.3

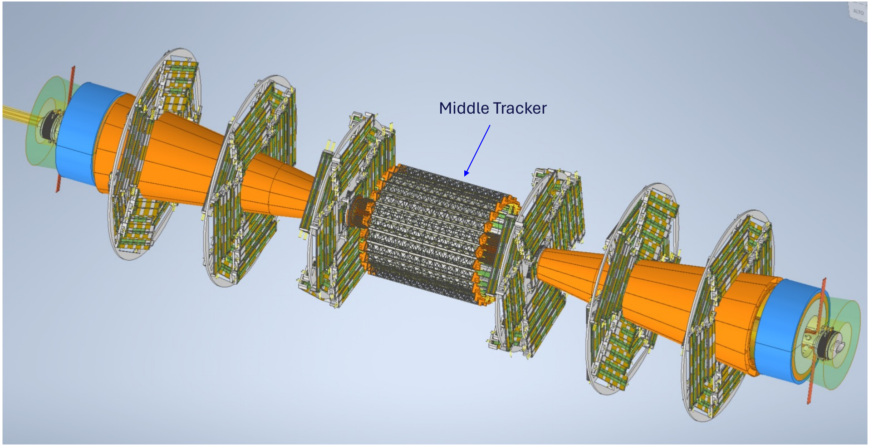
	Power density $[\mathrm{mW\,cm^{-2}}]$		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left End Cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

Power dissipation in ITS3
(not necessarily the same for FCC-ee)

- RSU~ 50 mW/cm^2 (depends on Temp.)
- LEC ~ 700 mW/cm^2

Service cones for cooling and cables




Middle Tracker

Differences between ALICE ITS3 and FCC-ee

- First layer at smaller radius, from 18 to 13.7 mm
  - → Mechanically okay, electrically to be demonstrated
  - → First layer to use just two segments to reach smaller radius
    - Assuming same RSU size (= reticle size of CMOS process of given silicon foundry) of $19.564 \times 21.666\,\text{mm}^2$ (in $r - \phi \times z$) then radius would be 12.77 mm.
    - Can consider more complex approach using *edge* reticle pieces to reach any desired radius for the first layer
  - → Assume perfect reticle size in $r - \phi$ of 21.02 mm to get to $r = 13.7$ mm for the first layer

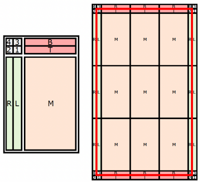
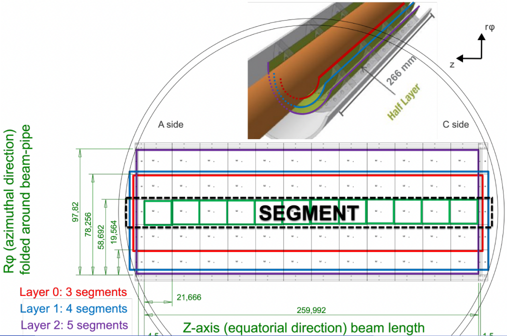
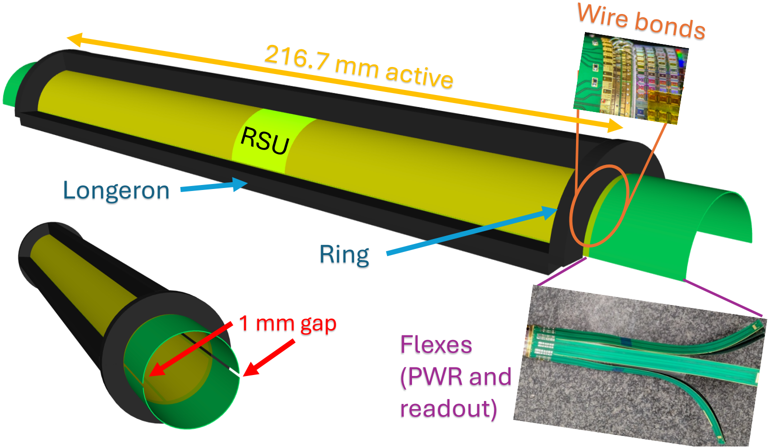


Figure 3.32: Principles of stitching. Left: design reticle with sub-frames (M, B, T, R, L, 1-4. Right: exposures on the wafer and resulting circuits (not to scale).

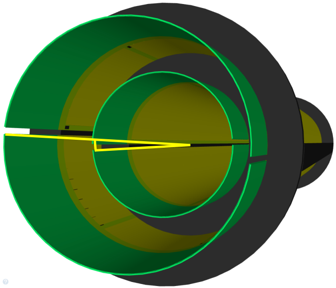


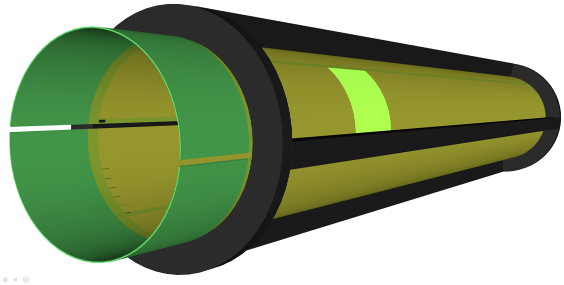
- 10 RSUs and 2 ECs long, $\theta_{min} = 125.8$ mrad, $|cos(\theta)| < 0.992$ (106.35 mrad assuming 20 mm flex)
- Two half-barrels two segments wide each, 1 mm gap, readout and power from both sides



Layer 2

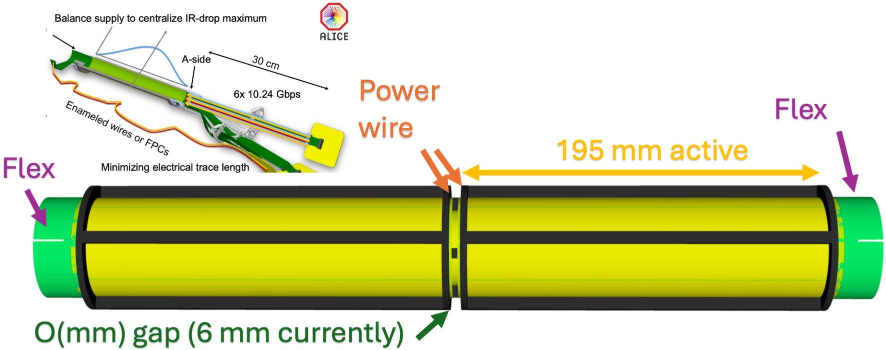
- 12 RSUs long (limit given 12 inch wafer size), at $r = 20.39\,\mathrm{mm}$
- Coverage down to $\theta_{\mathrm{min}} = 155.58\,\mathrm{mrad}$, $|cos(\theta)| < 0.991$
- Rotated in ϕ by 8° to avoid overlap with layer 1
- Could slightly twist sensor to minimise gaps in coverage e.g. at $z = 0$, in-between RSUs





Layer 3

- $r = 27.08\,\text{mm}$, two sensors per side, with 9 RSUs each
- Coverage down to $\theta_{\text{min}} = 135.93\,\text{mrad}$, $|cos(\theta)| < 0.991$
- Readout on sides, power on sides and center (power wire)



Layer 4

- Same length as layer 3, sensors are five RSUs wide, at $r = 33.77\,\text{mm}$
  - Simpler mechanical assembly given same length of layer 3 and 4 (sacrificing forward coverage)
- Coverage down to $\theta_{\text{min}} = 168.94\,\text{mrad}$, $|cos(\theta)| < 0.986$
- Gap at $z = 0$ could be mitigated by having asymmetric design with sensors with 10 and 8 RSUs on the $z > 0$ and $z < 0$ sides respectively