ER1-ASIC Results.

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DESY – FEC

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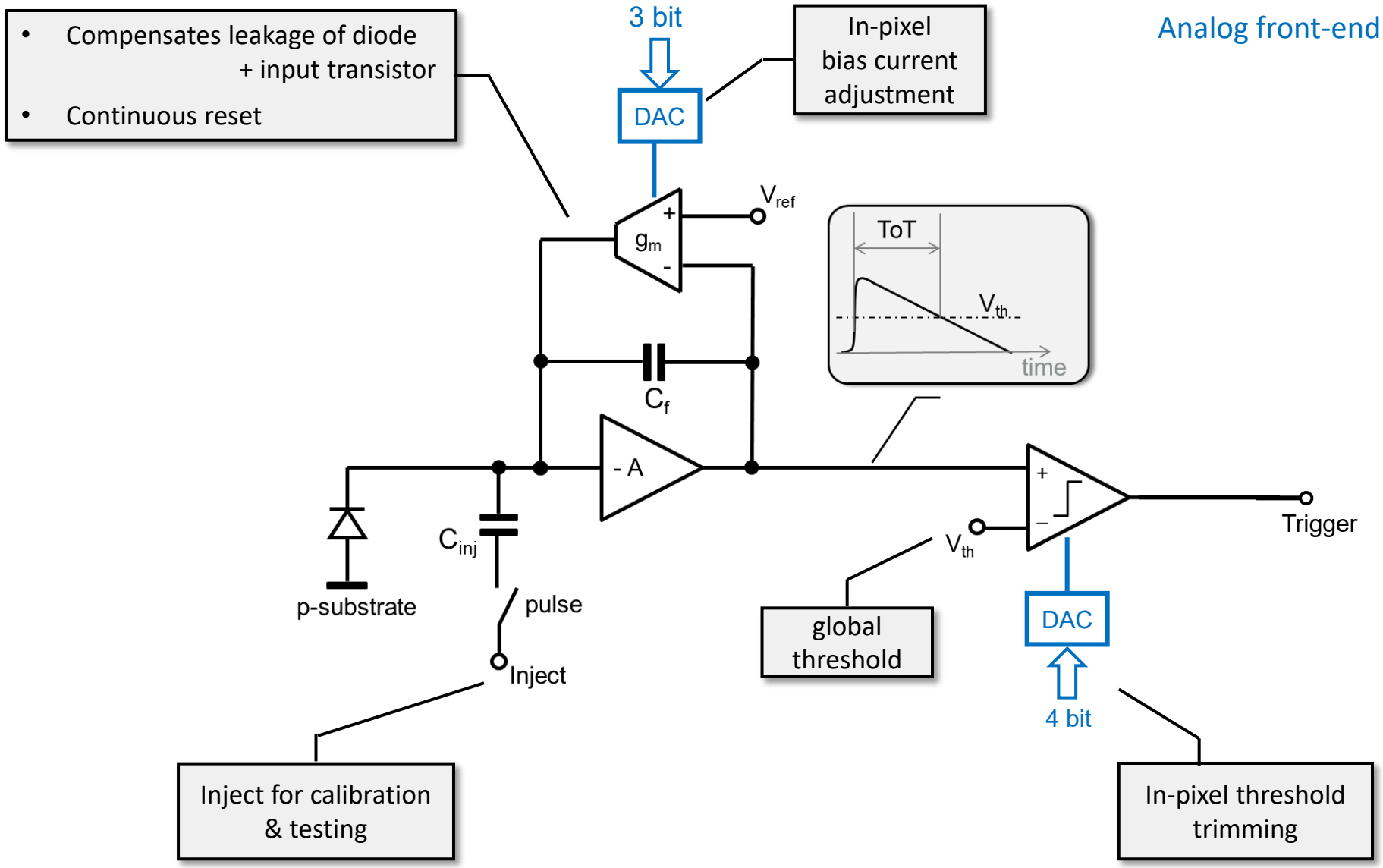
HELMHOLTZ SPITZENFORSCHUNG FÜR GROSSE HERAUSFORDERUNGEN

DESY.

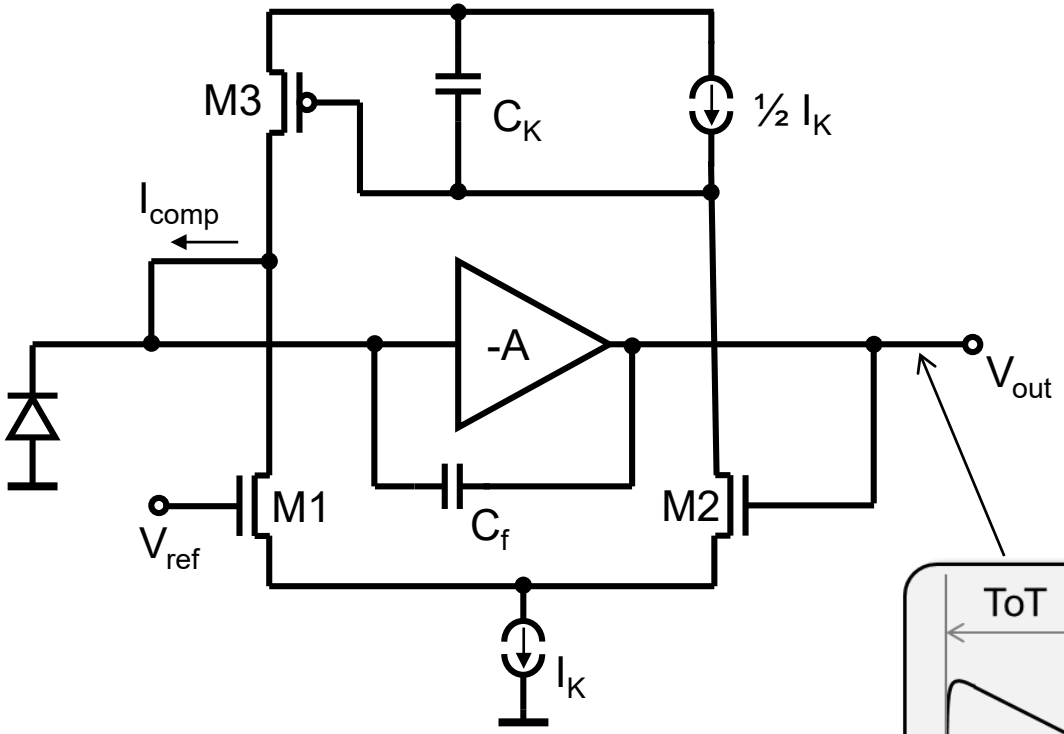
In-Pixel analog data processing

Analog front-end for H2M and testchips

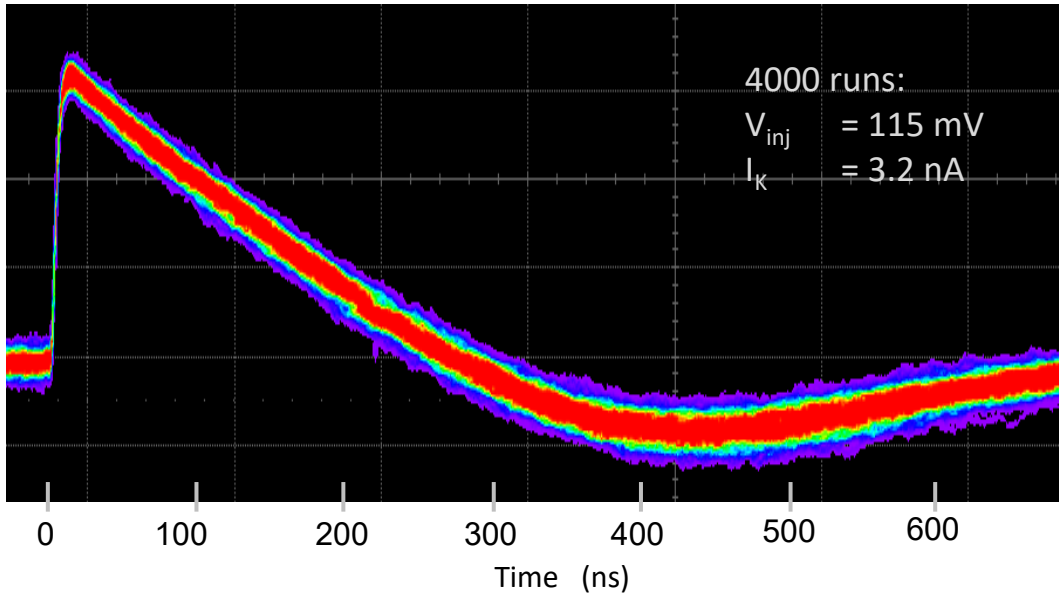


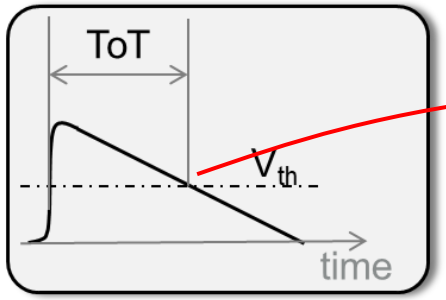
CSA with Krummenacher FB

Charge Measurement



CSA Output

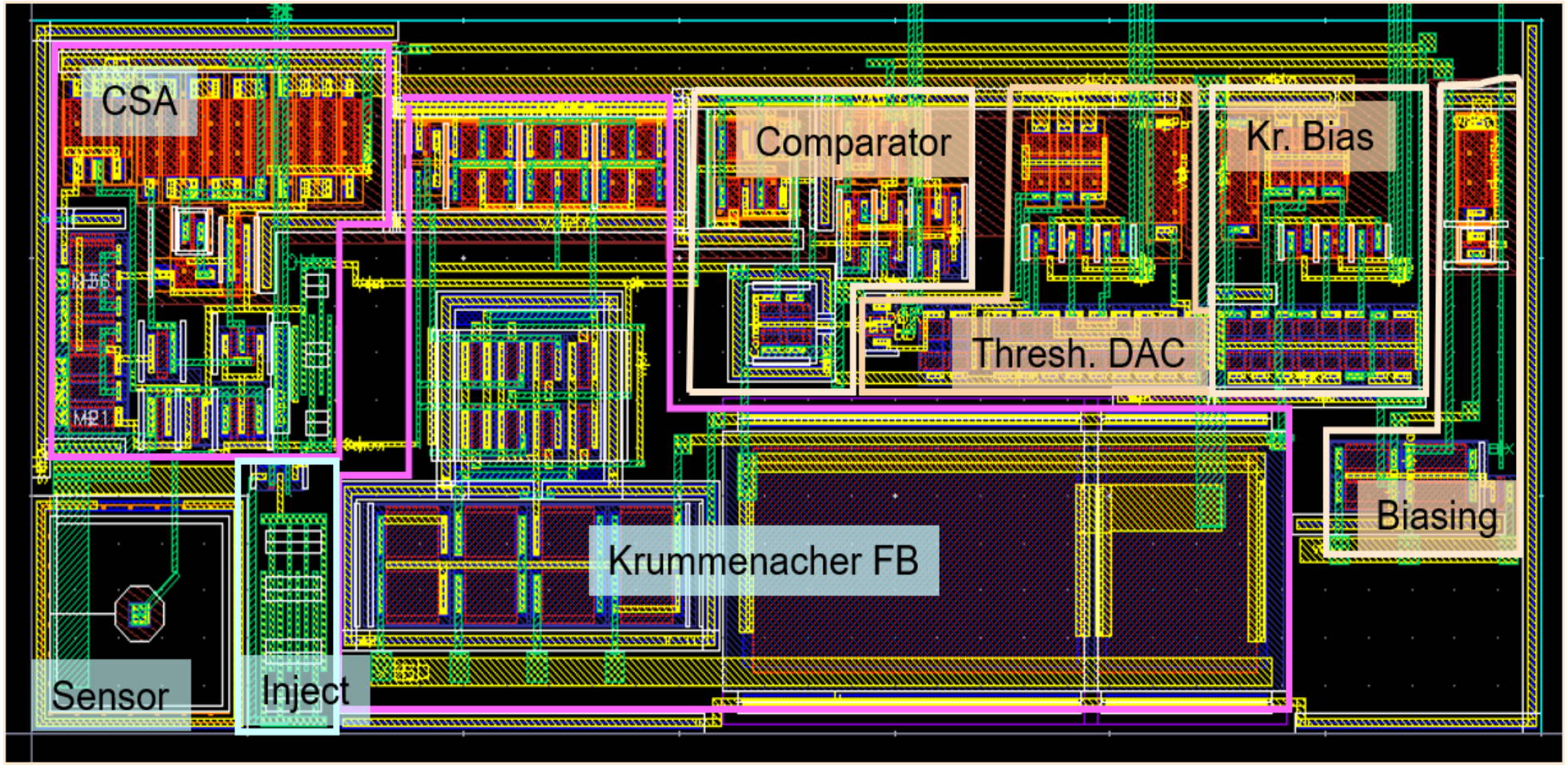




Required: slope of falling edge should be constant, independent on Q_{in} → ToT ~ Q_{in}

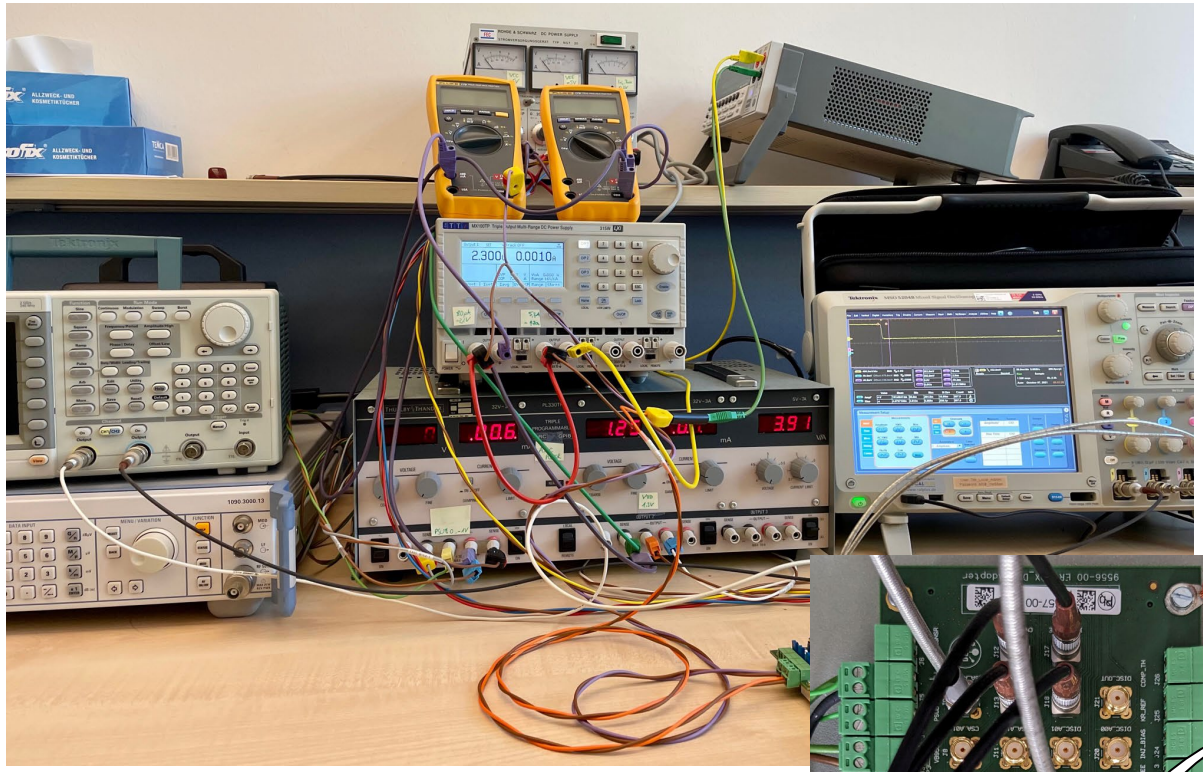
Pixel Design

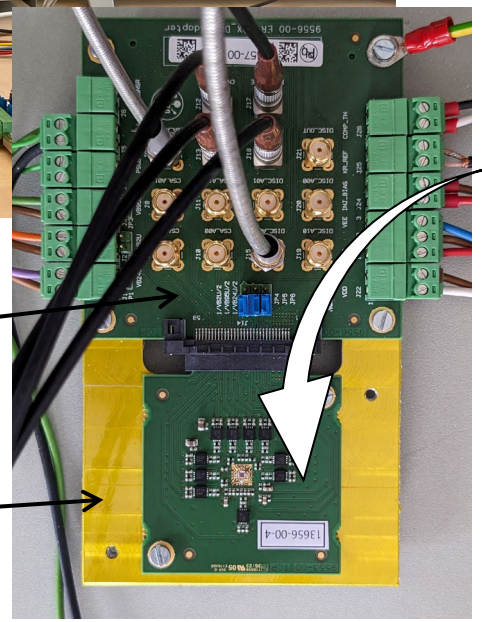
Layout

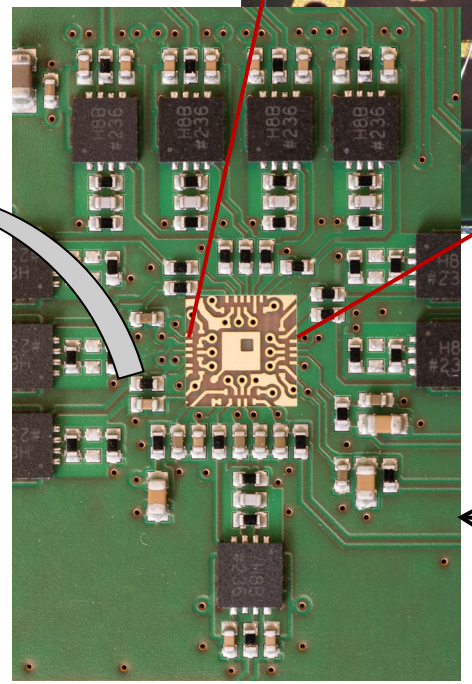


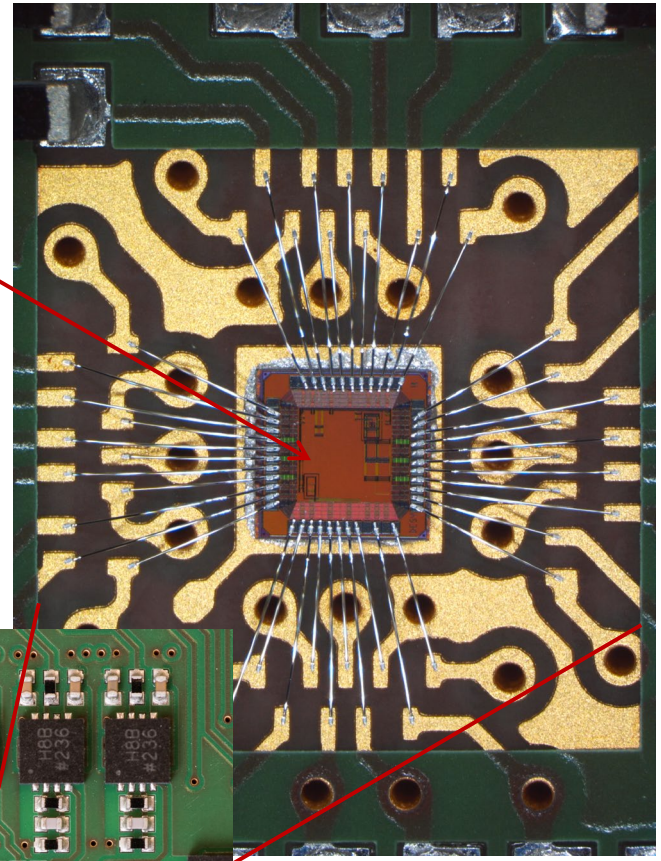
- Area: 35µm × 15µm
- M1 & M2 wiring
- Sensor: 5µm × 5µm

Test-Setup









ER1 Testchip

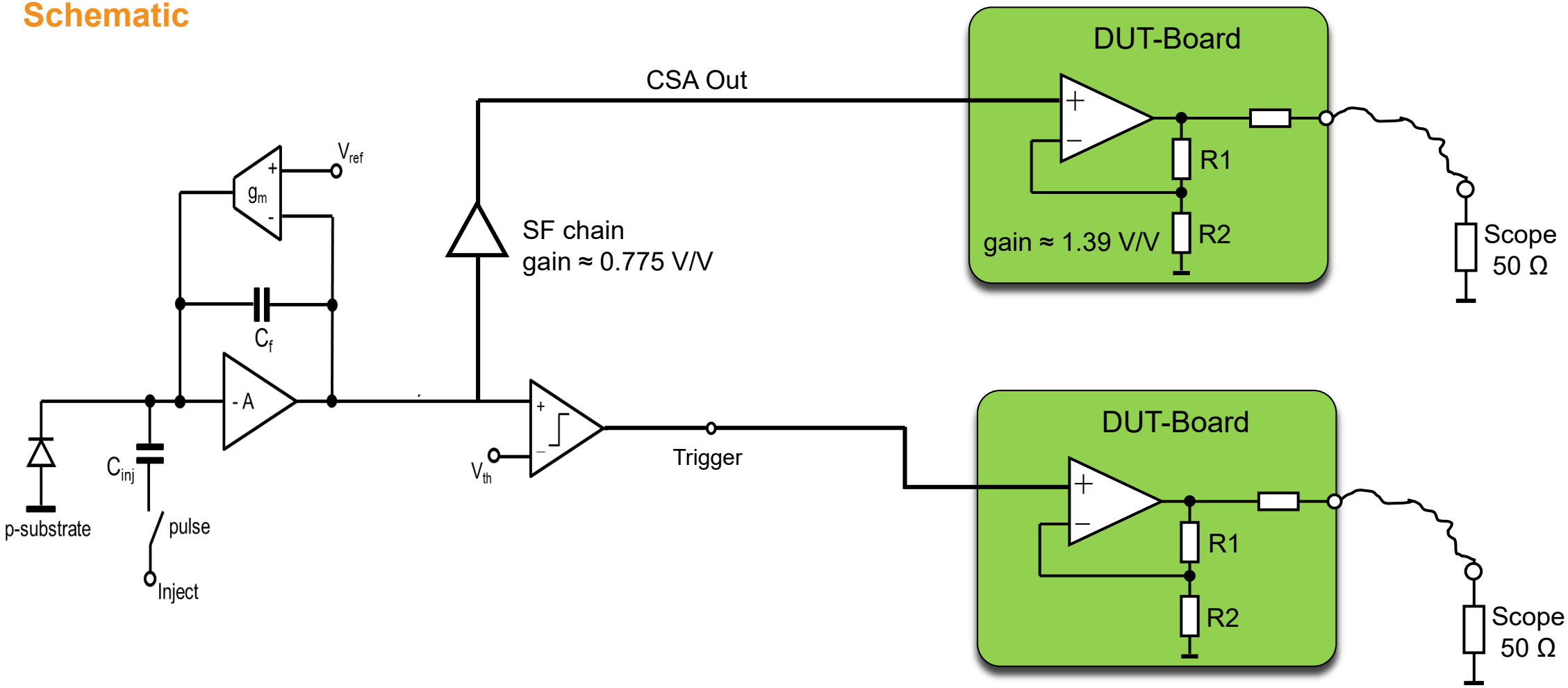
Adapter Board

DUT-Board in Al-cover

DUT-Board

Test Setup

Schematic



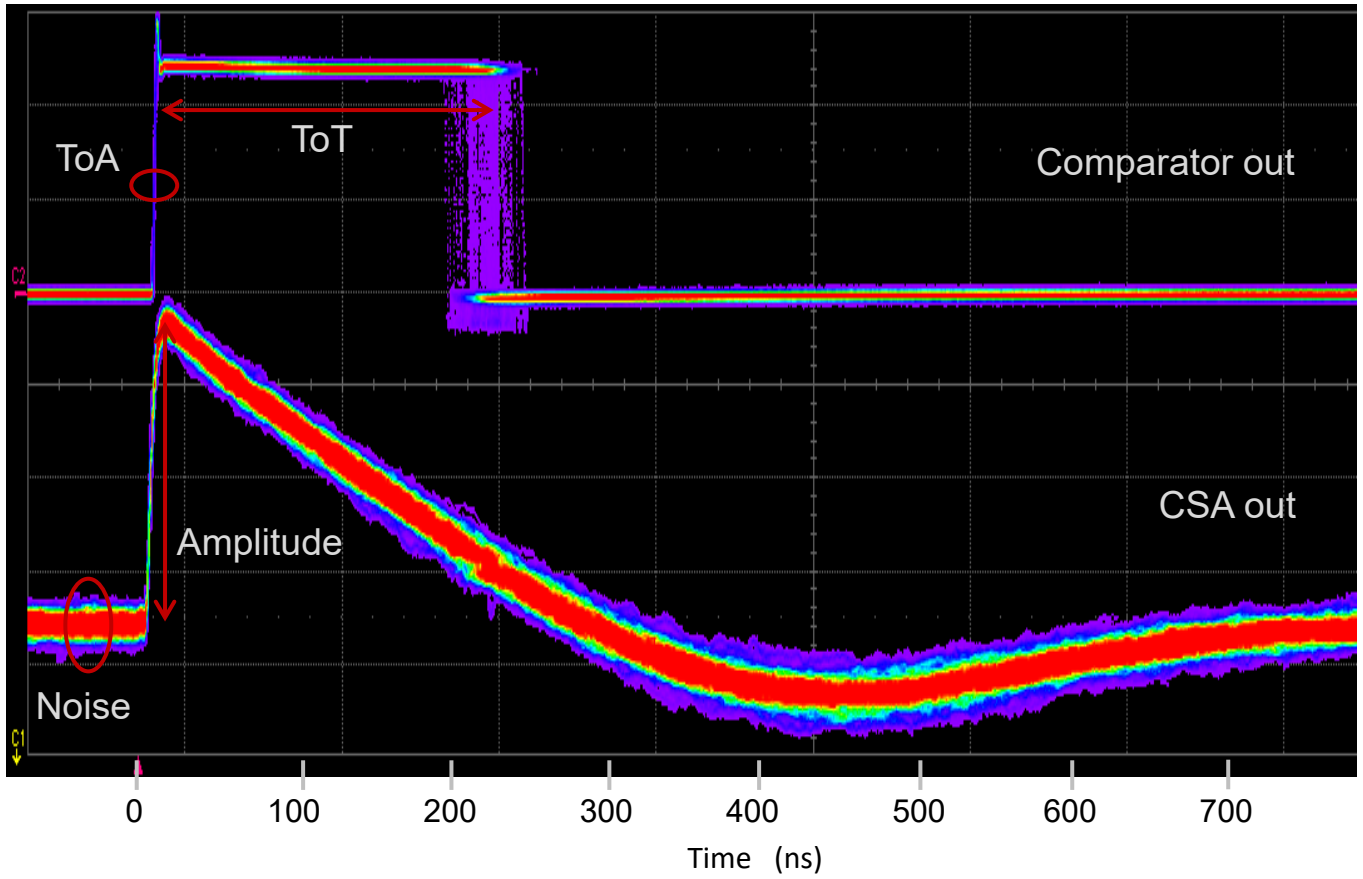
- Bandwidth limitation by buffers ~ 110 MHz

  → min. rise time ~ 4 ns

Measurements

Charge Inject – Bare Electronic Channel

Triggered on inject pulse

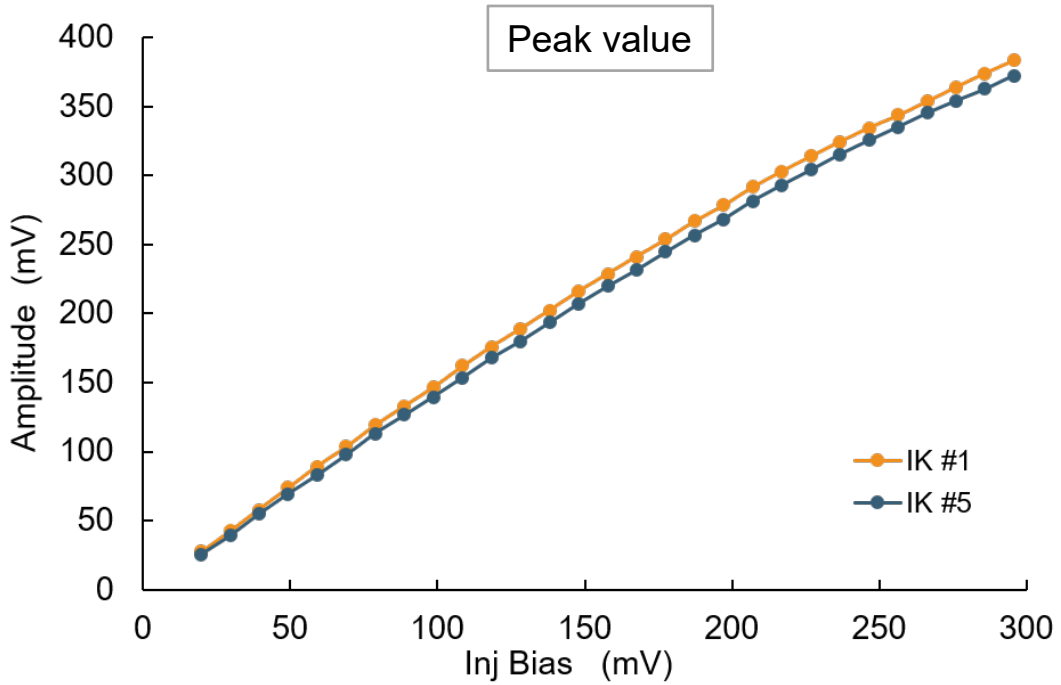


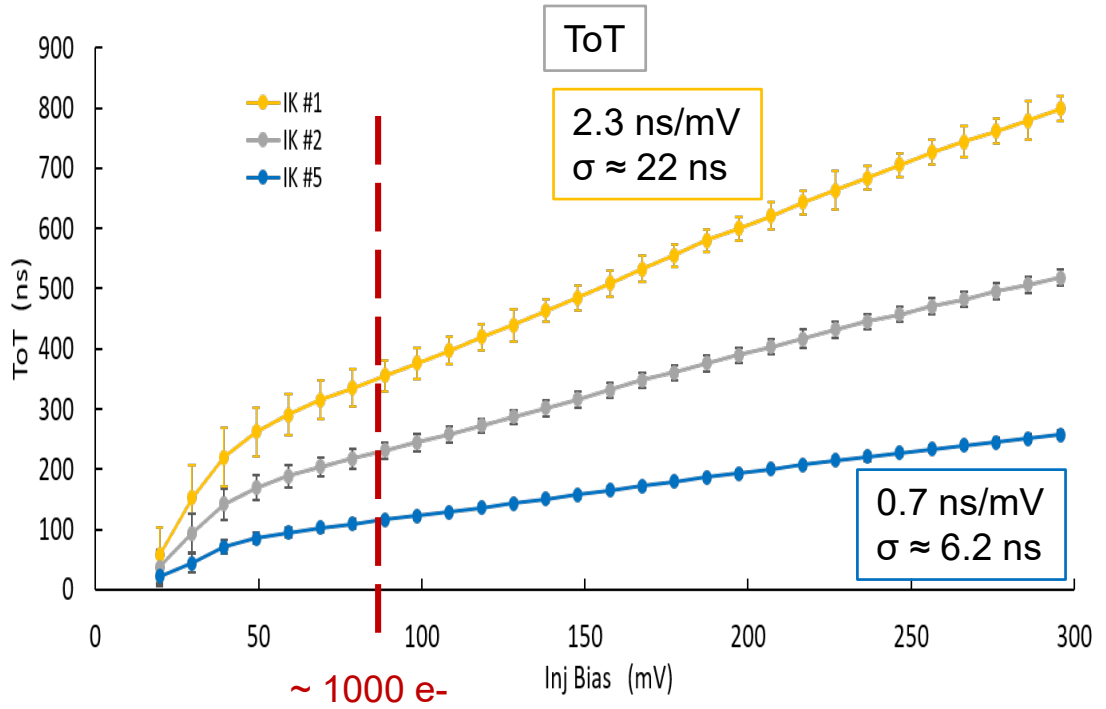
Conditions:

- Supply Voltage: 1.2 V
- PWELL: -1.2 V
- Inject Voltage sweep: 20mV … 300 mV
  230 e- … 3460 e-
  @ C_{inj} 1.85 fF

Measurements

Amplitude – Time-over-Threshold





- gain: 1.52 … 1.46 V/V
- nominal: $C_{inj} / C_f = 1.54$
- Baseline Noise: ~ 5.6 mV_{rms}

- Non-linear: for Inj Bias < 50 mV ~ 570 e-

2000 acquisitions per data point

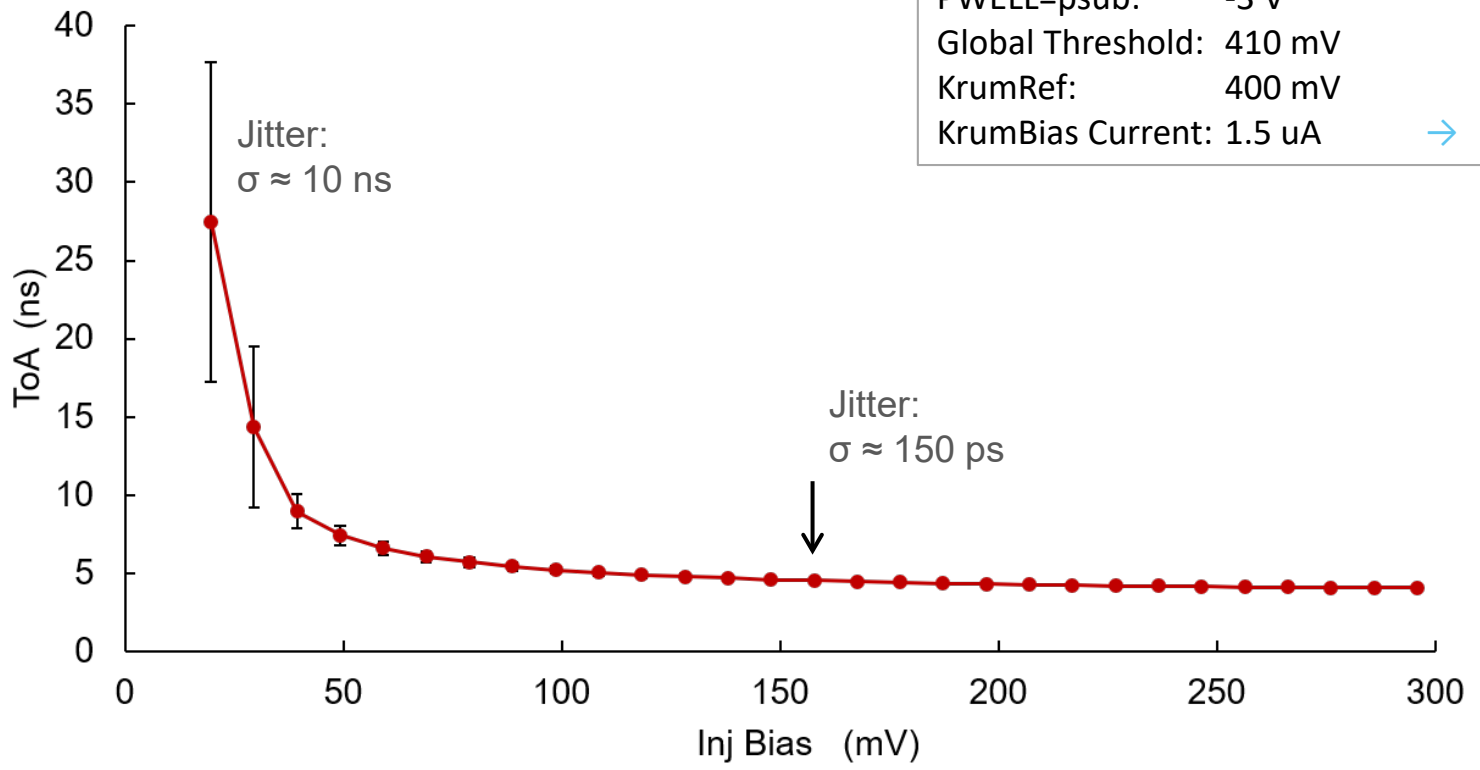
PWELL=psub:	-3 V	Pixel settings:	
Global Threshold:	410 mV	Thres Trim:	7
KrumRef:	400 mV	KrumBias:	paramter
KrumBias Current:	1.5 uA		

Measurements

Time-of-Arrival ToA

- Time walk: limited bandwidth of CSA **+** signal dependent comparator delay
- Input dependent jitter: scaled with rise time of CSA output

PWELL=psub:	-3 V		Pixel settings:
Global Threshold:	410 mV		Thres Trim: 7
KrumRef:	400 mV		KrumBias: 2
KrumBias Current:	1.5 uA	→	Ik = 1.6 nA



Measurements

Threshold Scan - Pixel Block

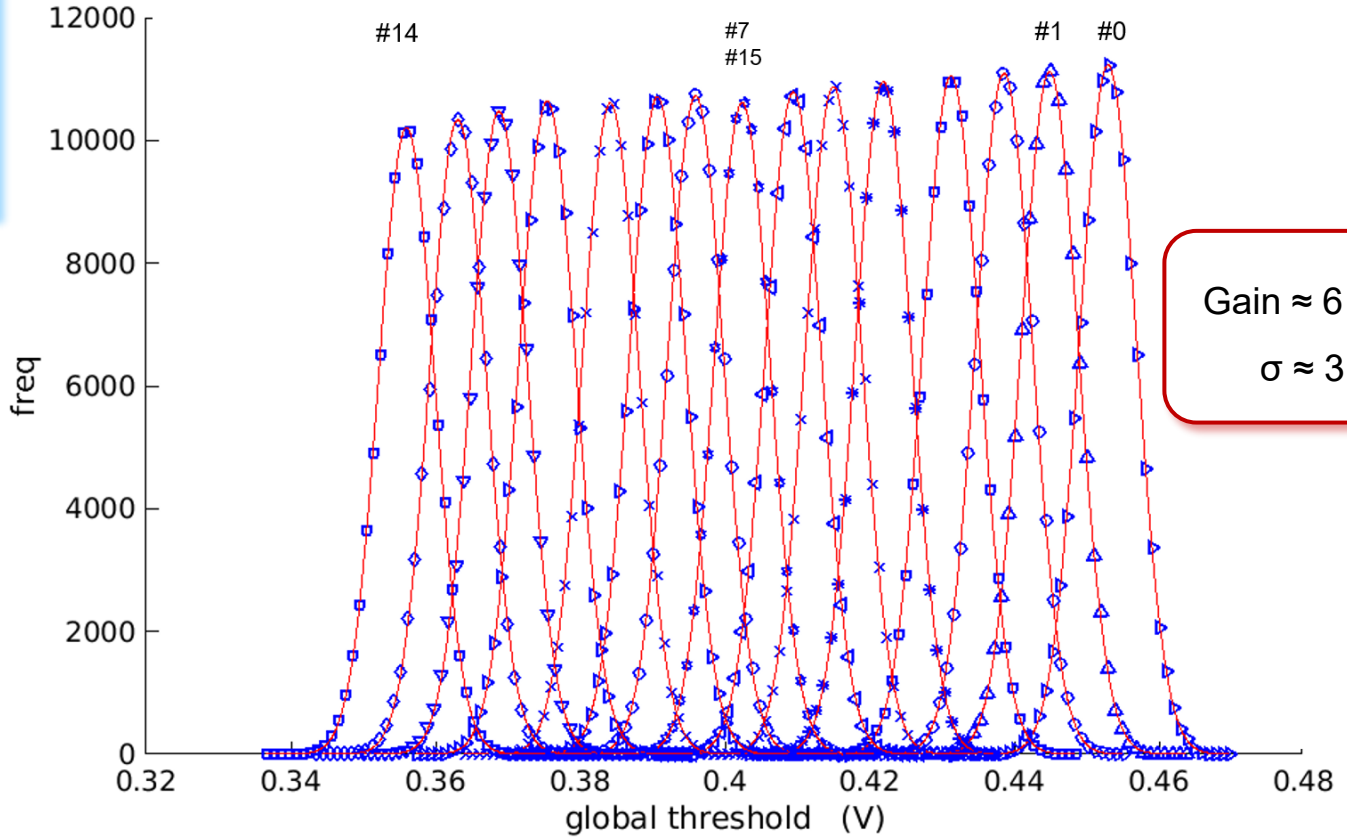
- No input
  1. For all DAC settings #0..#15
  2. Sweep Comp thres V_{th}, step size 800µV
  3. Count rising & falling edges @ Comp Out

PWELL=psub: -3 V
KrumRef: 400 mV
KrumBias Current: 1.5 uA

Pixel settings:
KrumBias: 2 → Ik = 1.6 nA

2k samples per data point

MSB changes current direction



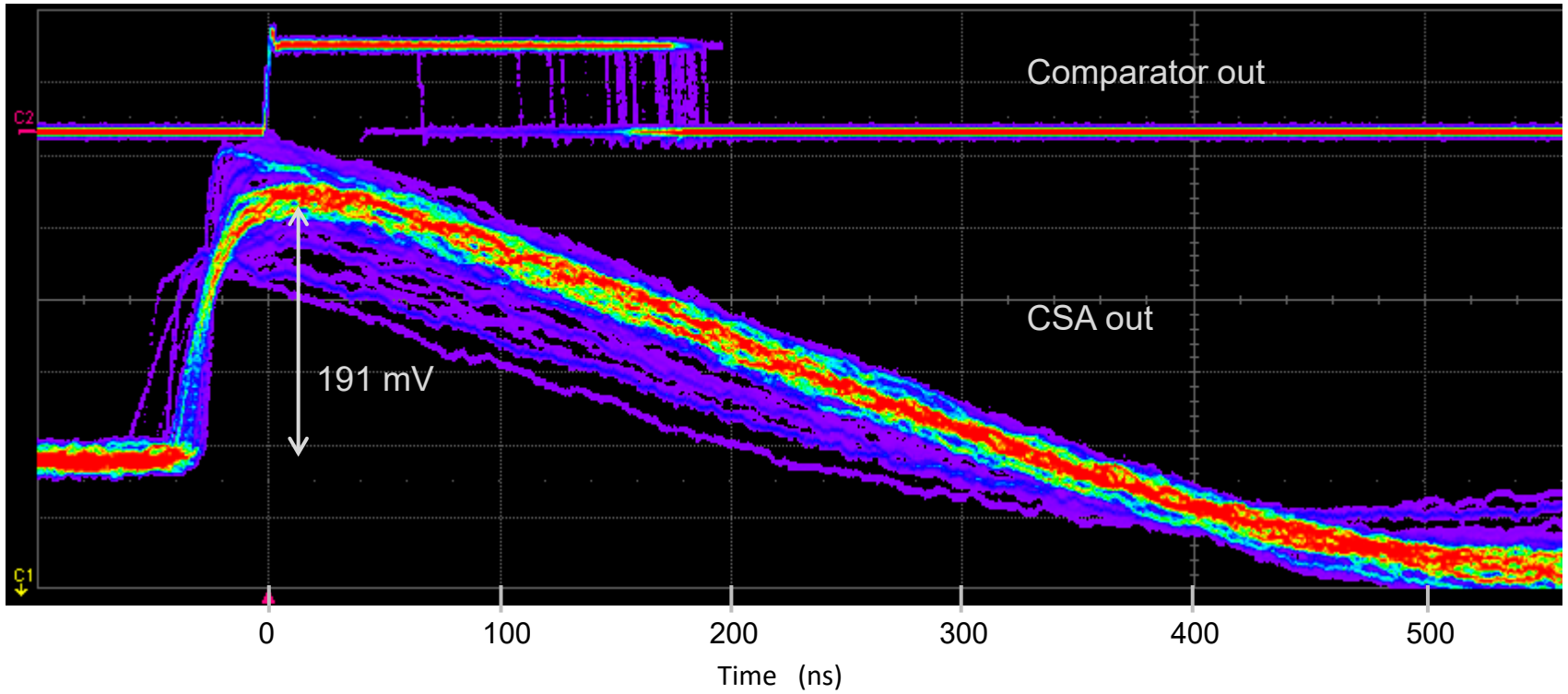
Gain ≈ 6 mV/DAC#

$\sigma \approx 3.8\ mV_{rms}$

X-Ray Irradiation

FE-55 response

2000 pulses



Si: 273 e-/keV

→ Mn-K_α ≙ 1610e-

gain: 118.6 mV/ke-

→ $C_f \approx 1.35$ fF

- Amplitude spread not only noise effect also charge collecting effect in sensor
- Sensor needs further optimization

FE-55 Irradiation

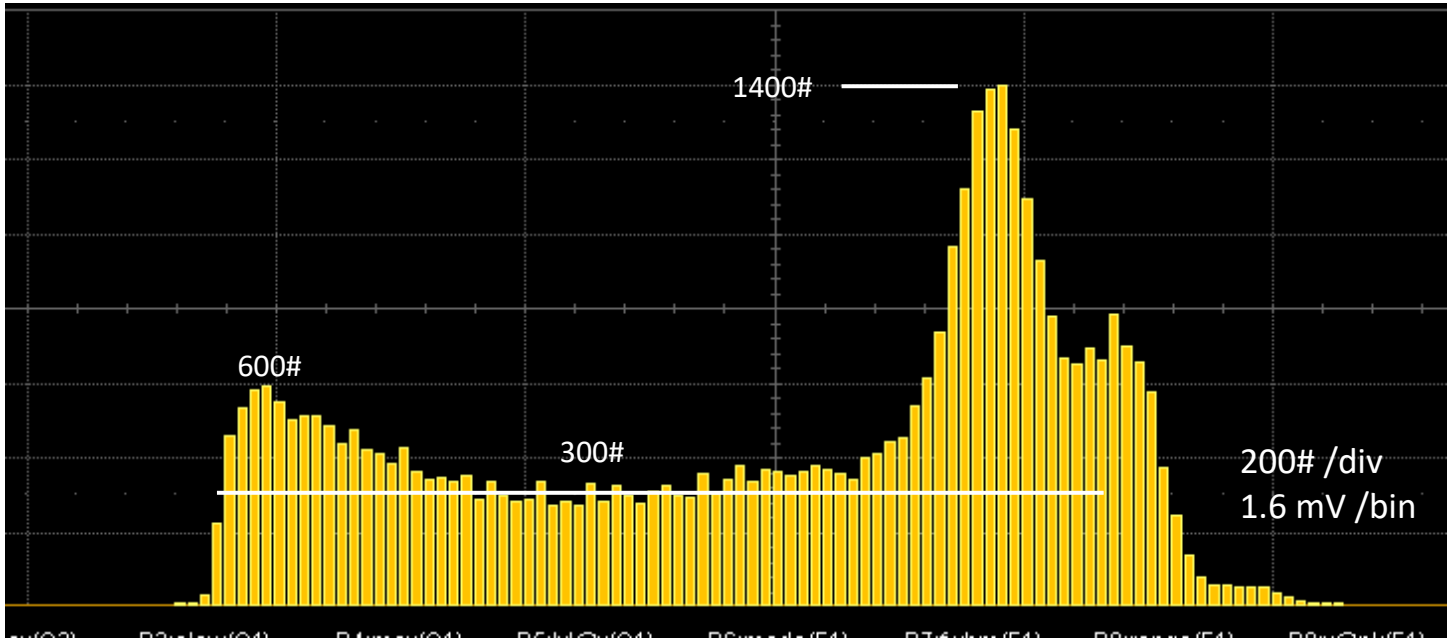
CSA Output

PWELL=psub: -4 V
Global Threshold: 300 mV
KrumRef: 290 mV
KrumBias Current: 2.156uA

Pixel settings:
KrumBias: 5
Thres Trim: 8

40k samples

Amplitude histogram:



Peak: 548.93 mV
BL: 338.861 mV
Kα 5.9 keV → 1610 e-

Amplitude: 210.07 mV / 1.08 = 194.5 mV
Gain: ~120.8 µV/e-
Noise: σ = 4.9 mV_{rms} ENC ~ 40.6 e-

Threshold: ~ 345 e-

Lessons learned

- ASICs are working, H2M and ER1 testchips as well
- Pixel size too large
- N-wells affect the charge collection in pixel
- MIP - signal (gen. charge) lower than expected ~25%
- Larger signal gain needed
- Krummenacher architecture reaches its limits, gain too low for small currents, dominates noise behavior

New Ideas on ASIC

Very rough

- Assumed occupency ~300 Mhits/cm²/s,
  with 4 pix/hit gives 1.2 Gpix/cm²/s
- Each active pixel generate 8bit+8bit=16bit Address
- Results in ~20 Gb/ cm² / s

Sub matrix of 256-by-256 pixel, pitch 20µm

Then 4 sub matrices give ~ 1 cm²

Simple Hit no-Hit decision

Fast link: combines 2 cm² → **40 Gb optical link**

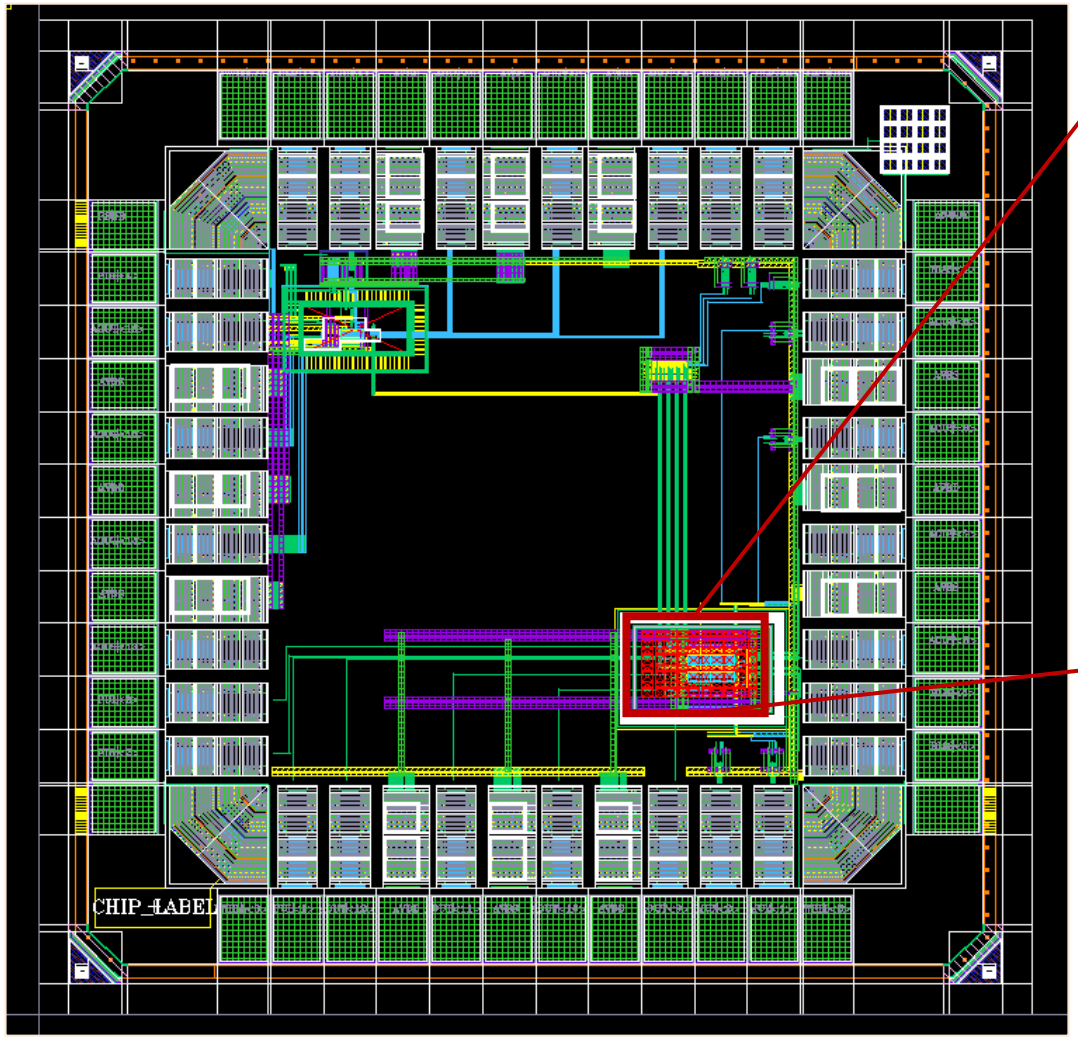
Design tasks:

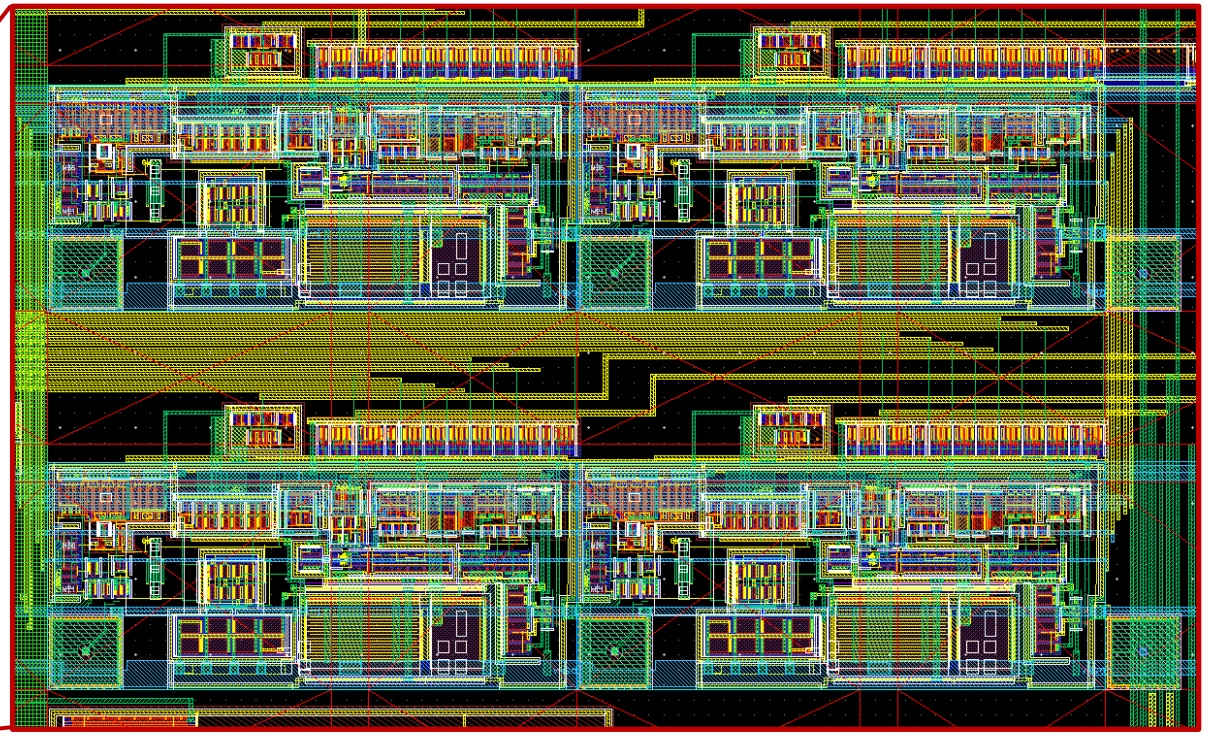
Analog Pixel design	Address-Data collection &Timing ?	Data concentration Ser & Mux

Backup.

Electronics & Mini-Matrix Testchip

ER-Submission

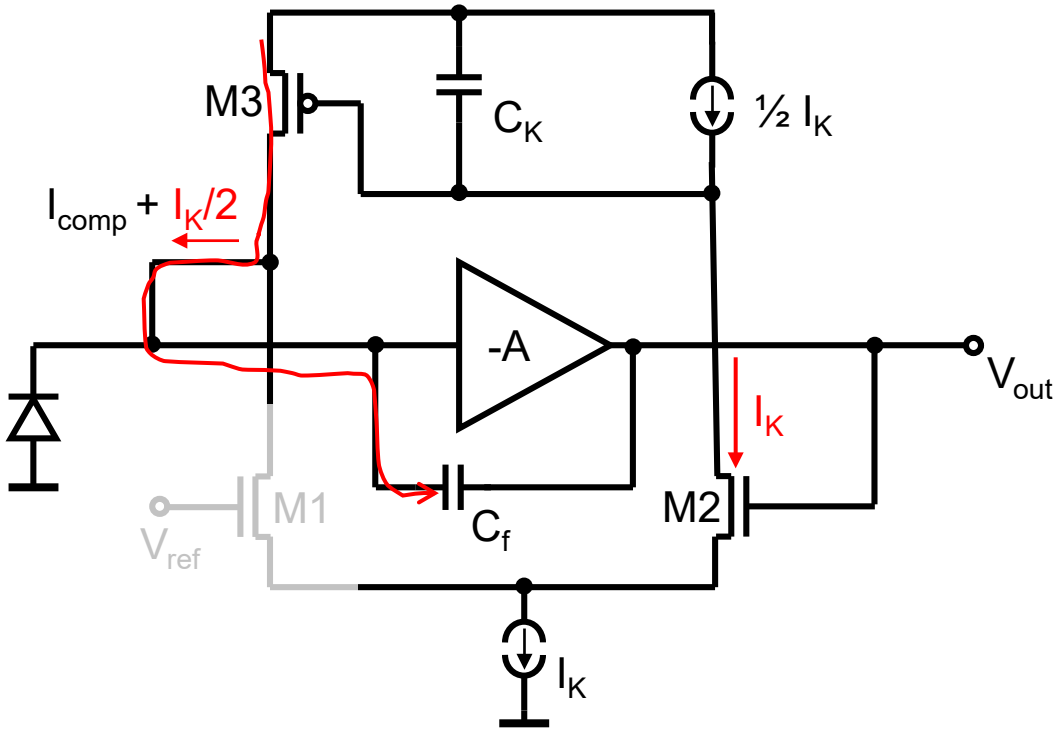


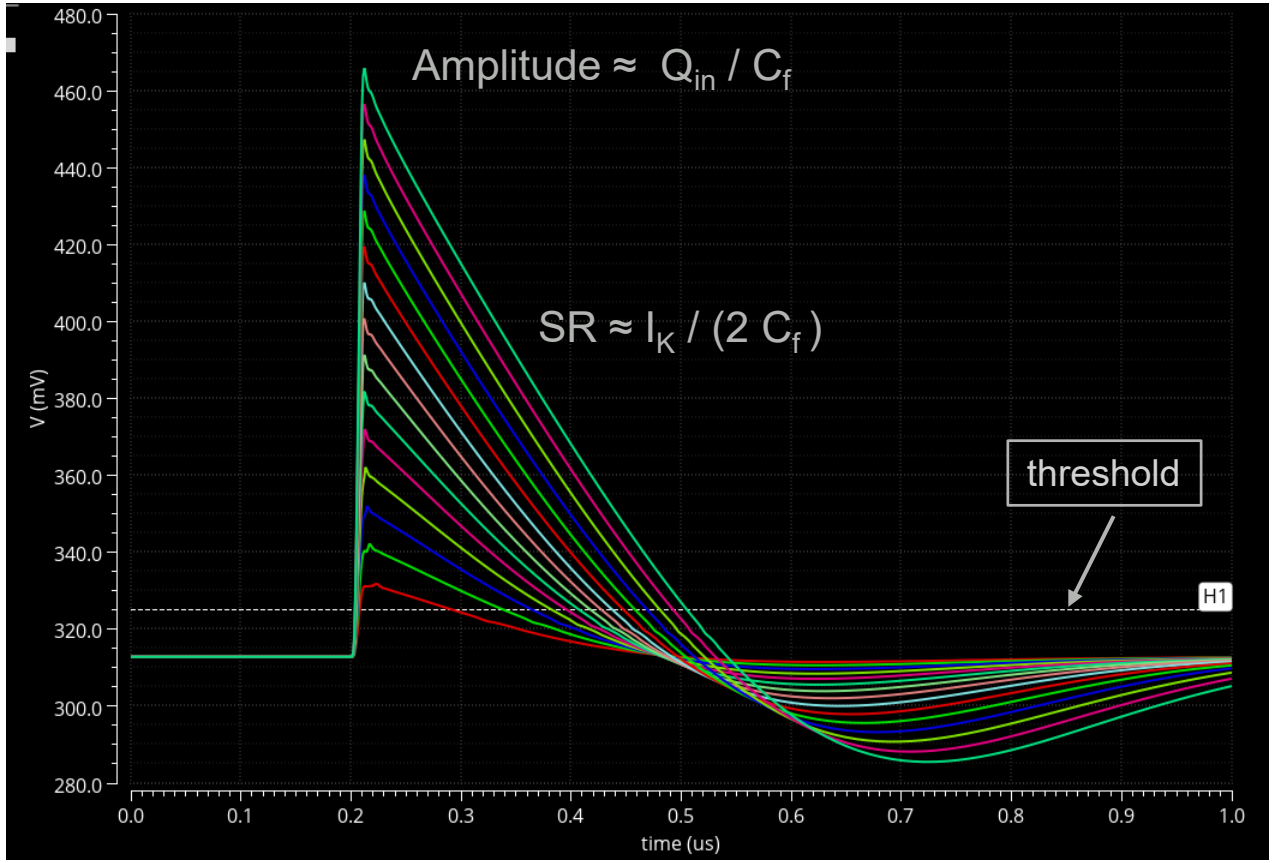


- 4x4 Pixel
- External access to CSA and discriminator output
- Slow-Cntrl to adjust comp. threshold & Krummenacher Bias
- Single Front-End w Inject

CSA with Krummenacher FB

Non - Linearity





- SR not constant wrt input charge

  → $I_K = f(Q_{in})$

- Fundamental limit of Krummenacher FB

  @ Qin ≈ 500e-

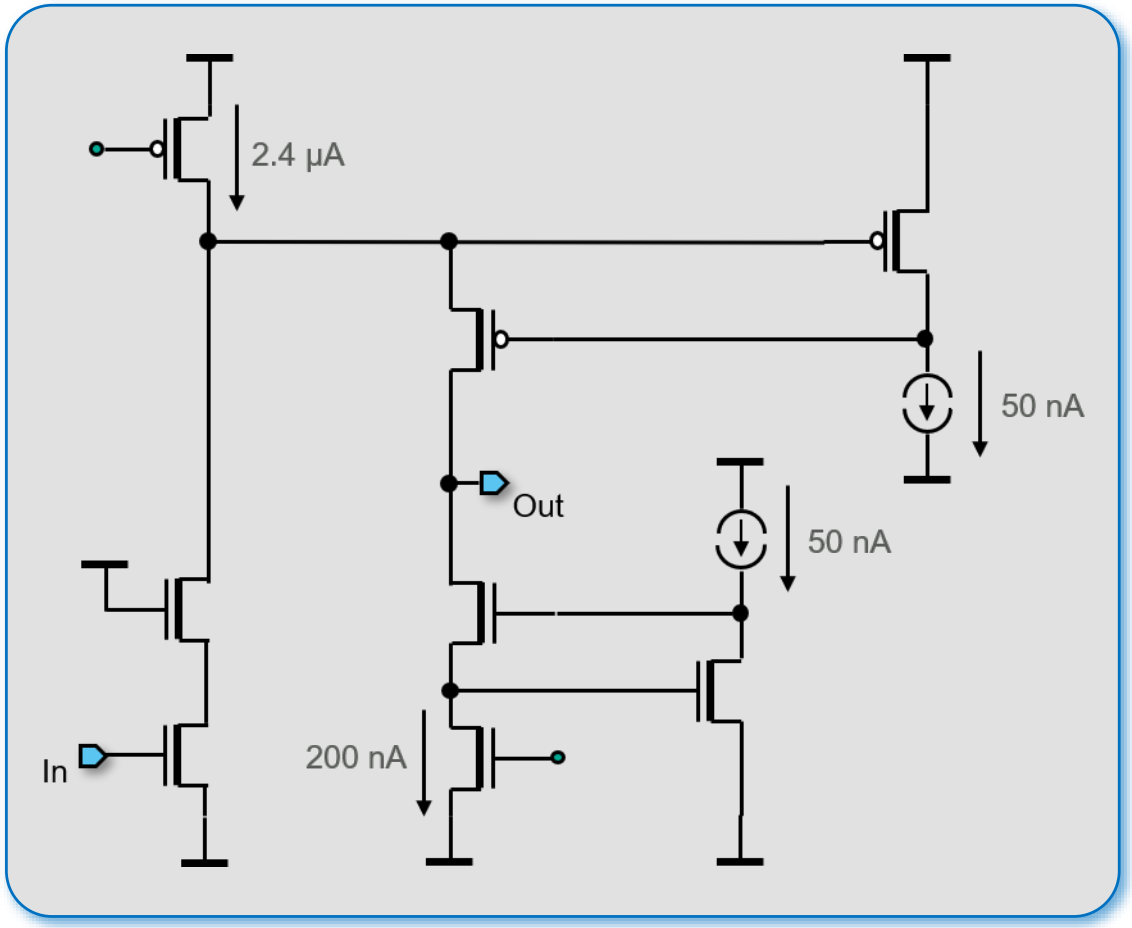
$$ToT \approx 2 / I_K \cdot Q_{in} - 2\, V_{TH} \cdot C_f / I_K$$

⇨ Gain = $2 / I_K$

Gain Stage

Circuit Aspects

- Single-ended 2-stage folded cascode amplifier
- All bias currents/voltages generated from single 2.4 µA source
- Boosted output impedance due to regulated cascodes
- High DC gain: > 90 dB
- GBW: > 400 MHz
- Low Power: 3.2 µW @ 1.2 V
- NMOS input device: g_m 60 µS, typ



Time - Continuous Comparator

Circuit Aspects

- Differential input, 2-stage comparator
- Differential pair with NMOS mirror load
- Transimpedance stage provides:
  - low input impedance
  - small time constant
  - large gain
- Compensation current for thres. trimming
- Low Power: 0.75 µW @ 1.2 V
- Delay: 4 … 11 ns
  signal dependent