https://www.desy.de/

Impressions from Vertex Detector Workshop

The ECFA Roadmap, DRD3 & Squaring The Circle of Requirements

Simon Spannagel

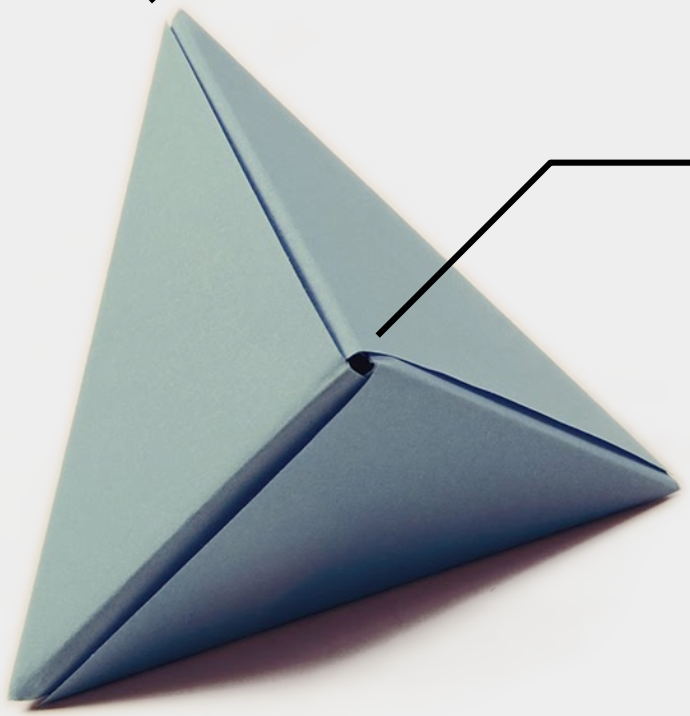
29th Future Colliders @ DESY meeting

17 May 2024

L’Apéro

Requirements for a Vertex Detector @ Lepton Colliders

Challenges for Vertex Detectors @ Lepton Colliders



Material Budget

Time Resolution

Power Consumption

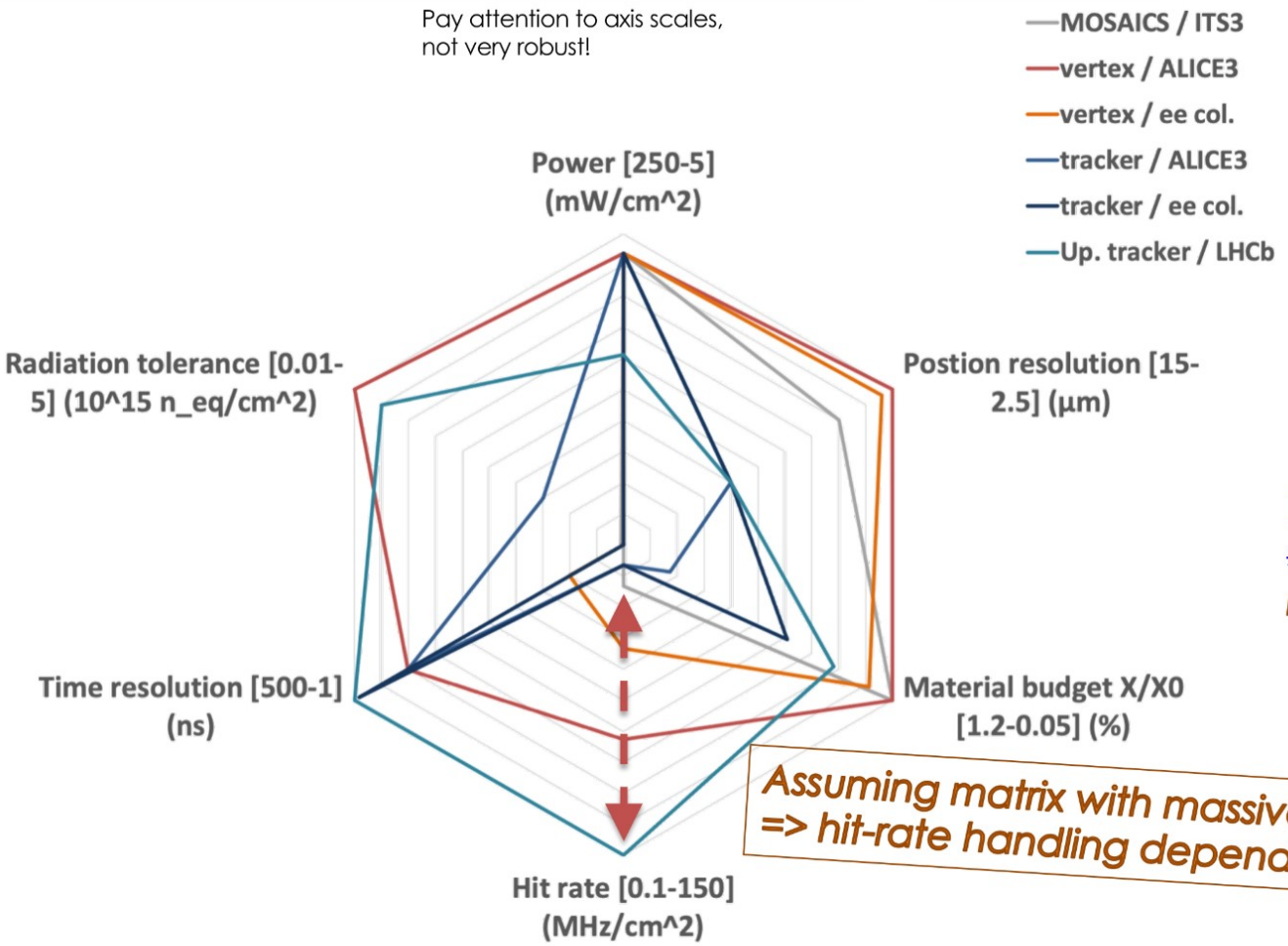
Position Resolution

Silicon Detector Requirements at Lepton Colliders

- Precision measurements especially demanding on vertex & tracking detectors
  - Momentum resolution – large lever arm, minimum scattering
  - Impact parameter resolution – high resolution, min. scattering, small radii
  - Time resolution – fast sensor response, large S/N

	Lepton Colliders		**(HL-) LHC (ATLAS/CMS)**
Material budget	< 1% X_0		10% X_0
Single-point resolution	≤ 3 µm		~ 15µm
Time resolution	~ ps – ns		25ns
Granularity	≤ 25 µm x 25 µm		50µm x 50µm
Radiation tolerance	< 10^{11} n_{eq} / cm^2		**O(10^{16} n_{eq} / cm^2)**
Duty cycle	< 0.01 ‰ @ ~ms (linear)	100 % @ ~ns (circular)	100 % @ 25ns

Specifications: the graph



<= greyish: where we stand

<= reddish: vertex requirements

<= blueish: tracker requirements

Do we need as many ~~sensors~~ as experiment?
matrices

Assuming matrix with massive parallel read-out => hit-rate handling depends on periphery

J. Baudot

L’Entreé

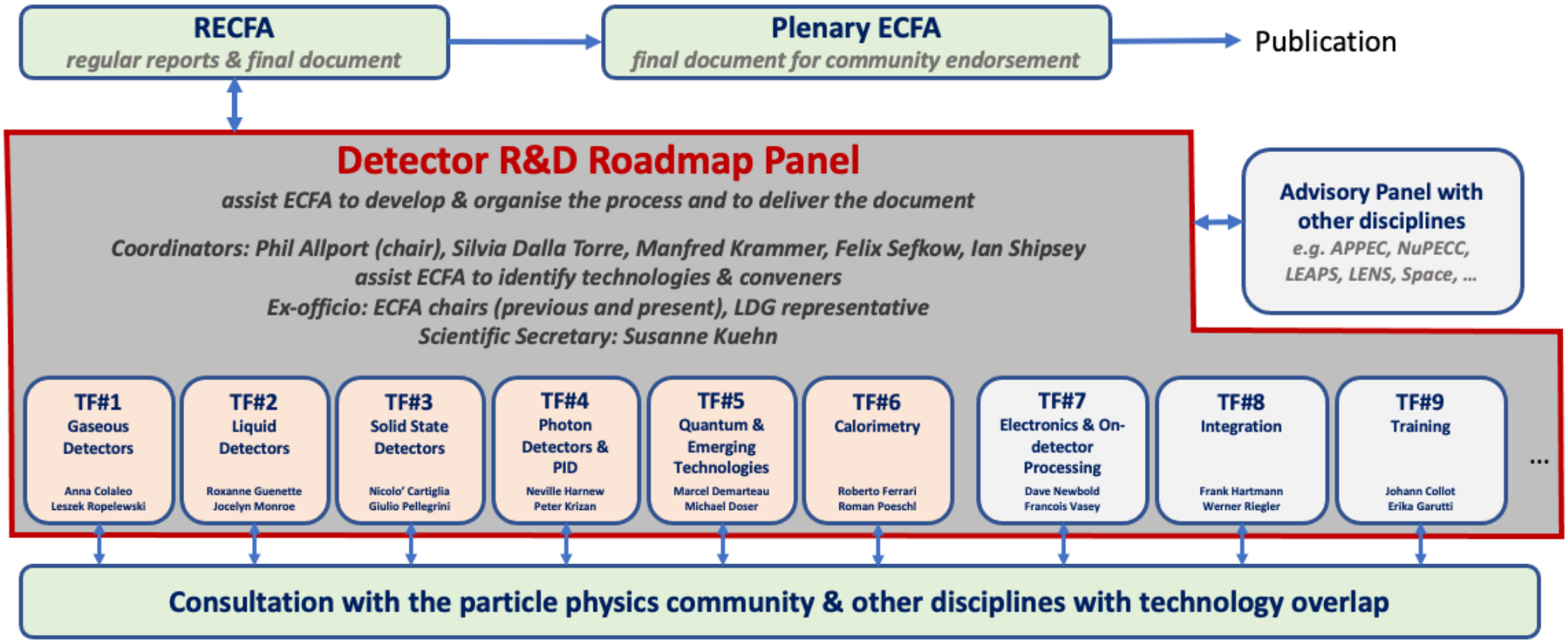
ECFA Detector R&D Roadmap & the DRD Collaborations

Goal of the ECFA Detector R&D Roadmap

“The [European Strategy for Particle Physics update] calls upon ECFA to develop a global detector R&D roadmap that should be used to support proposals at the European and national levels. That roadmap aims to define the backbone of detector R&D required to deploy the community’s vision for both the near- and longer-term.”

ECFA Roadmap Document @ CDS

Organization to structure the consultation with the community



Solid state

DRDT 3.1 Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors

DRDT 3.2 Develop solid state sensors with 4D-capabilities for tracking and calorimetry

DRDT 3.3 Extend capabilities of solid state sensors to operate at extreme fluences

DRDT 3.4 Develop full 3D-interconnection technologies for solid state devices in particle physics

Electronics

DRDT 7.1 Advance technologies to deal with greatly increased data density

DRDT 7.2 Develop technologies for increased intelligence on the detector

DRDT 7.3 Develop technologies in support of 4D- and 5D-techniques

DRDT 7.4 Develop novel technologies to cope with extreme environments and required longevity

DRDT 7.5 Evaluate and adapt to emerging electronics and data processing technologies

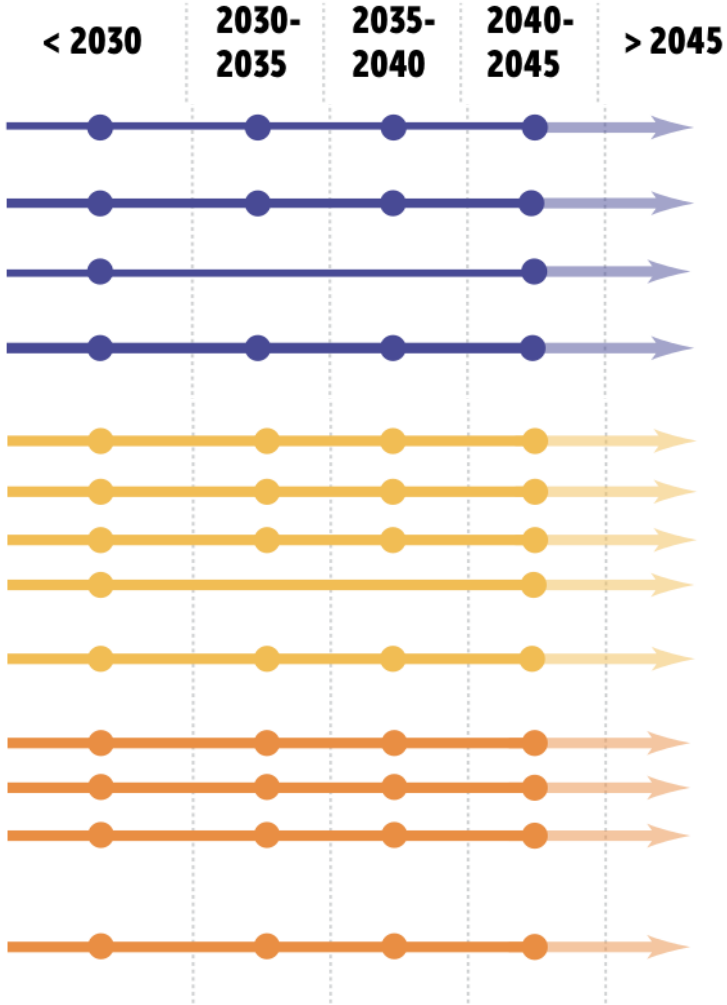
Integration

DRDT 8.1 Develop novel magnet systems

DRDT 8.2 Develop improved technologies and systems for cooling

DRDT 8.3 Adapt novel materials to achieve ultralight, stable and high precision mechanical structures. Develop Machine Detector Interfaces.

DRDT 8.4 Adapt and advance state-of-the-art systems in monitoring including environmental, radiation and beam aspects



DRD3 Common Project Proposal

Proposal text

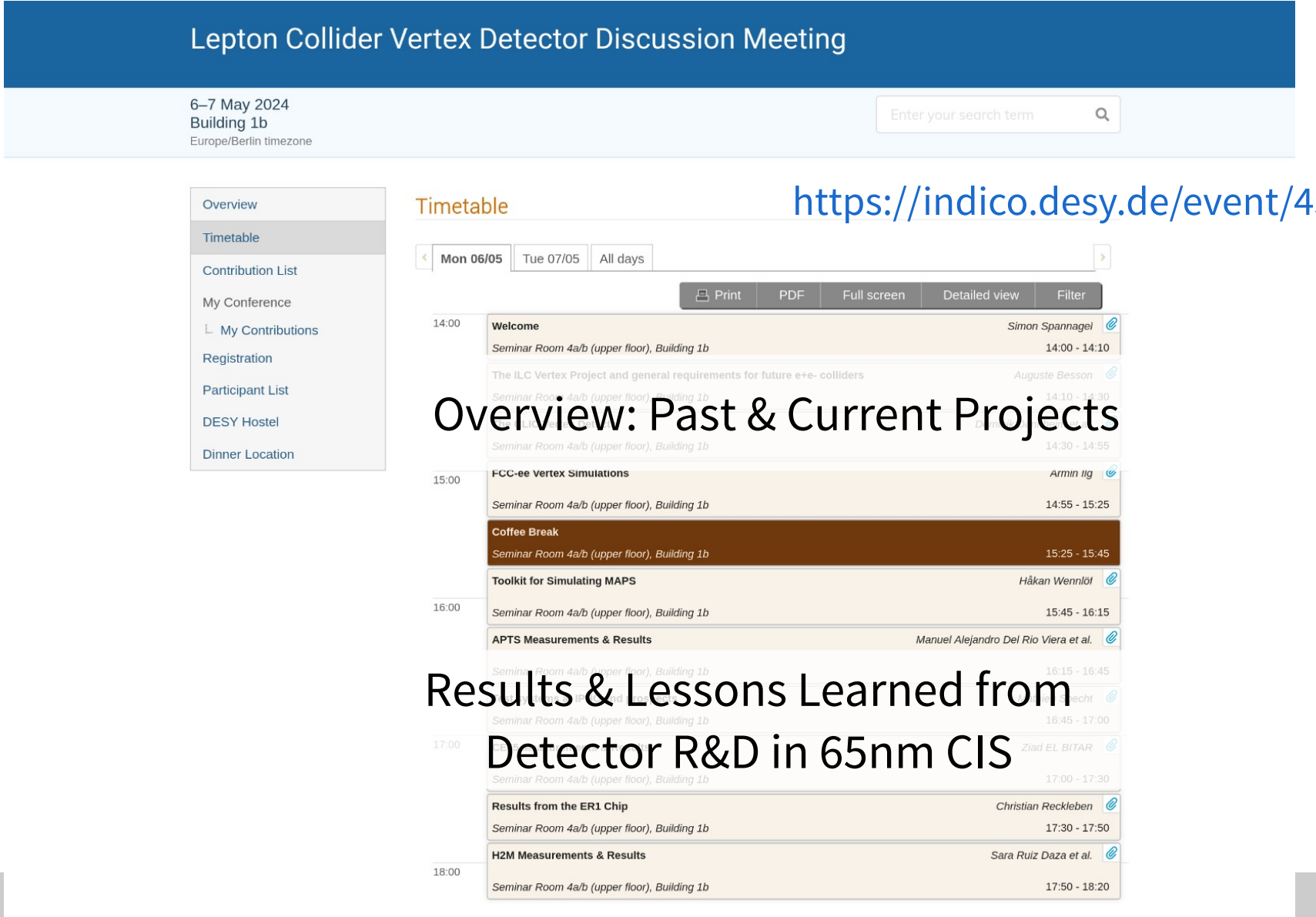
++

“Fine-pitch CMOS pixel sensors with precision timing for vertex detectors at future Lepton-Collider experiments”

- Proposal submitted last year together with APC Paris, CERN, IPHC Strasbourg, UOxford, UZurich
- Development and evaluation of monolithic fine-pitch pixel sensors implemented in advanced CMOS imaging processes, targeting the LC requirements as outlined in the ECFA detector roadmap.
- Key development targets
  - ~3 µm single-point resolution, down to ~5 ns time resolution
  - thinning to below 100 µm,
  - average power consumption below 50 mW/cm2,
  - minimal inactive periphery area, and a sensor architecture scalable to a large-area detector system.
- Develop high-resolution beam-telescope sensors as an intermediate target in a first R&D phase.

Le Plat Principal

The Lepton Collider Vertex Detector Workshop @ DESY



Overview: Past & Current Projects

Results & Lessons Learned from Detector R&D in 65nm CIS

Lepton Collider Vertex Detector Discussion Meeting

6–7 May 2024
Building 1b
Europe/Berlin timezone

Enter your search term

https://indico.desy.de/event/43834

- Overview
- Timetable
- Contribution List
- My Conference
  - My Contributions
- Registration
- Participant List
- DESY Hostel
- Dinner Location

Timetable

Mon 06/05 | **Tue 07/05** | All days

Print | PDF | Full screen | Detailed view | Filter

09:00
Requirements for a Vertex Detector at FCCee — Auguste Besson
Seminar Room 4a/b (upper floor), Building 1b — 09:15 - 09:40
Other Projects using TPSCo — Jerome Baudot
Seminar Room 4a/b (upper floor), Building 1b — 09:40 - 10:00

10:00
Coffe Break
Seminar Room 4a/b (upper floor), Building 1b — 10:00 - 10:30
Input - IPHC Brainstorming — Frederic Morel
Seminar Room 4a/b (upper floor), Building 1b — 10:30 - 10:45
Input - DESY Brainstorming — Lennart Huth
10:45 - 11:00

11:00
Discussion & Planning — Ingrid-Maria Gregor
Seminar Room 4a/b (upper floor), Building 1b — 11:00 - 12:00

12:00

Requirements, Activities & Synergies with other Projects

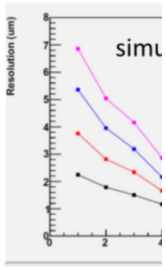
Discussion & Brainstorming (ASIC Concept, Project Structure)

Highlights

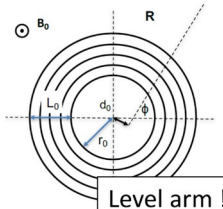
A. Besson

Spatial resolution in Higgs factories

- Typical targets:
  - ✓ σ_{sp}~3 μm for the vertex layers
  - ✓ σ_{sp}~5-10 μm for the outer tracker layers
- Resolution in each layer depends on
  - ✓ Pitch
    - In conflict with the functionnalities inside the pixel
    - Favored by small feature size technology
  - ✓ Charge deposition
    - Sensitive layer thickness
  - ✓ Charge sharing (SNR vs resolution)
    - Depletion
    - Staggered pixels
  - ✓ Charge encoding
    - Binary output / ADC / Tot / etc.

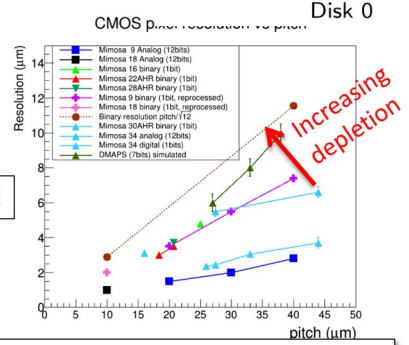


$$\sigma_{d0}{}^2 = a^2 + \left(\frac{b}{p.\sin^{3/2}\theta}\right)^2$$



$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}}\sqrt{1+\frac{8r_0}{L_0}+\frac{28r_0^2}{L_0^2}+\frac{40r_0^3}{L_0^3}+\frac{20r_0^4}{L_0^4}}$$

$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{\beta p_T} r_0 \sqrt{\frac{d}{X_0 \sin\theta}}\sqrt{1+\frac{1}{2}\left(\frac{r_0}{L_0}\right)+\frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$

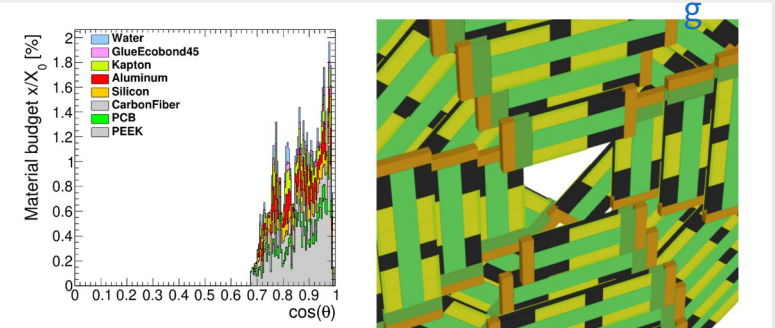


⇨ σ_{sp} ~ 3 μm ⇦⇨ pitch ~ 15-20 μm

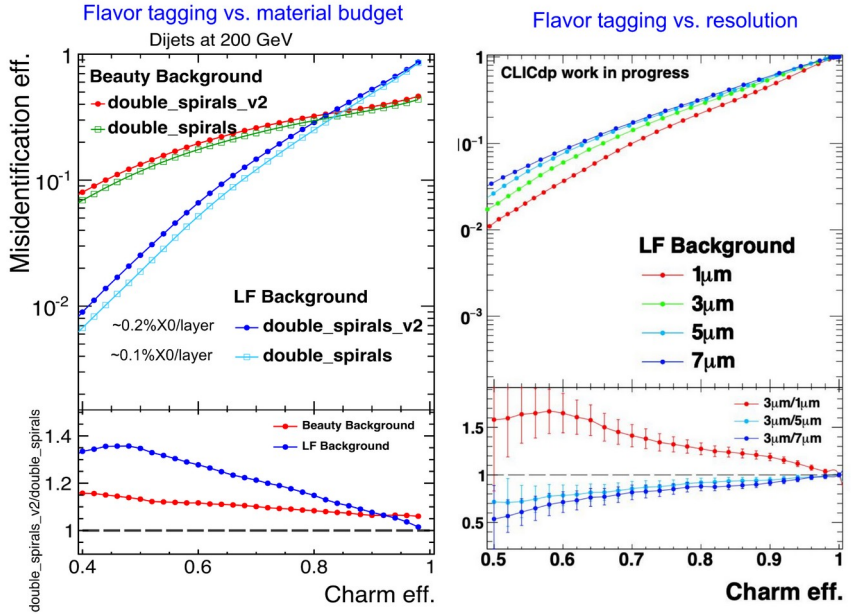
(assuming binary output, ~20 μm epi.thickness & large depletion in 180nm tech.)

May 6th-7th 2024 A.Besson, Unive 11

A. Il g



D. Dannheim



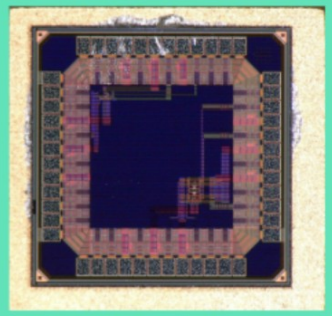
https://cds.cern.ch/record/1742993

Prototypes

International collaboration for common submissions to foundry with 65 nm CMOS imaging process, coordinated by CERN.

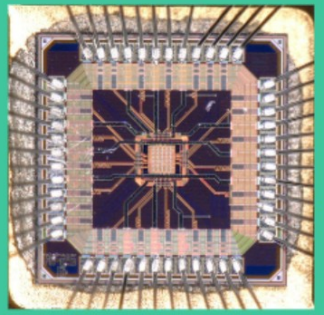
EP R&D

MLR1 (2021)



DESY Chip V1

- ★ Designed at DESY
- ★ CSA test structures
- ★ 2 × 2 pixel matrix
- ★ 16 μm pitch
- ★ Analog output



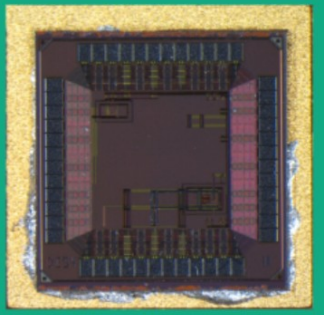
APTS

W. Deng et al.

- ★ Analog Pixel Test Structure
- ★ Designed at CERN
- ★ 4 × 4 pixel matrix
- ★ 15 - 25 μm pitch
- ★ Analog output with source follower (SF)

↳ See talk by M.A. del Río Viera

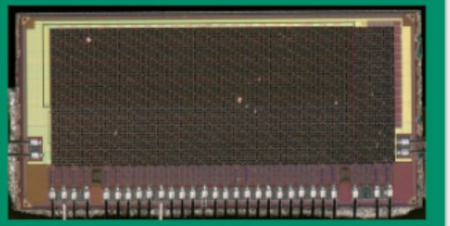
ER1 (2023)



DESY Chip V2

- ★ Designed at DESY
- ★ 2 × 2 pixel matrix
- ★ 35 × 25 μm^2 pitch
- ★ In-pixel amplifier and discriminator

↳ See talk by C. Reckleben



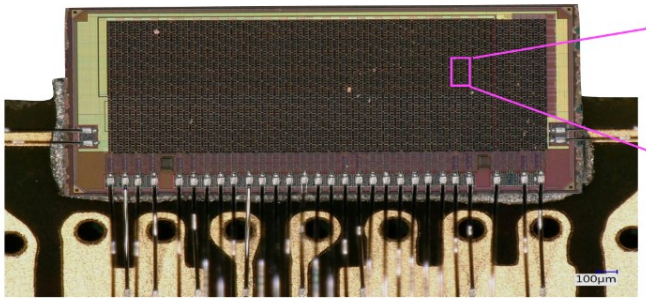
H2M

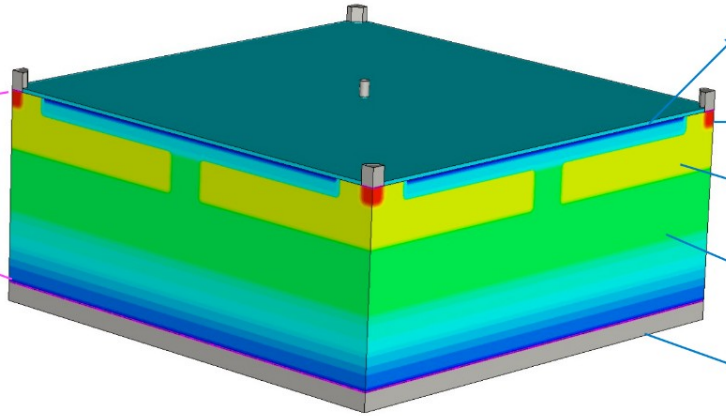
- ★ Hybrid-to-Monolithic
- ★ Designed at DESY, CERN and IFAE
- ★ 64 × 16 pixel matrix
- ★ 35 μm pitch
- ★ 4 acquisition modes

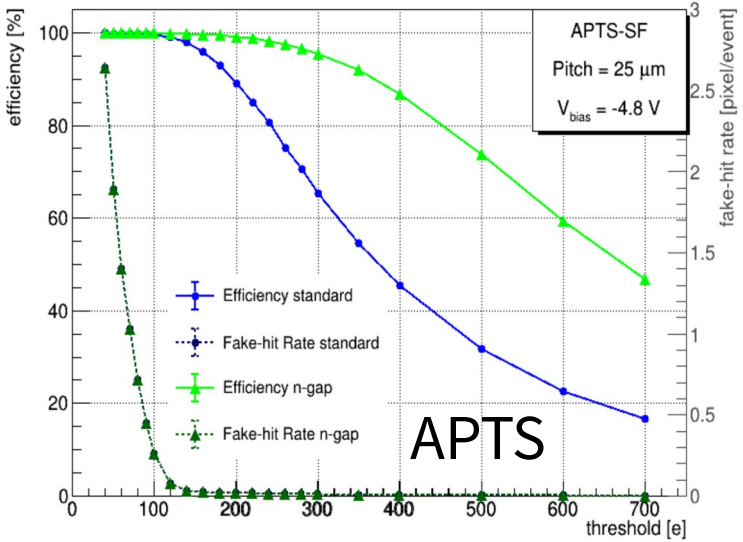
S. Ruiz Daza

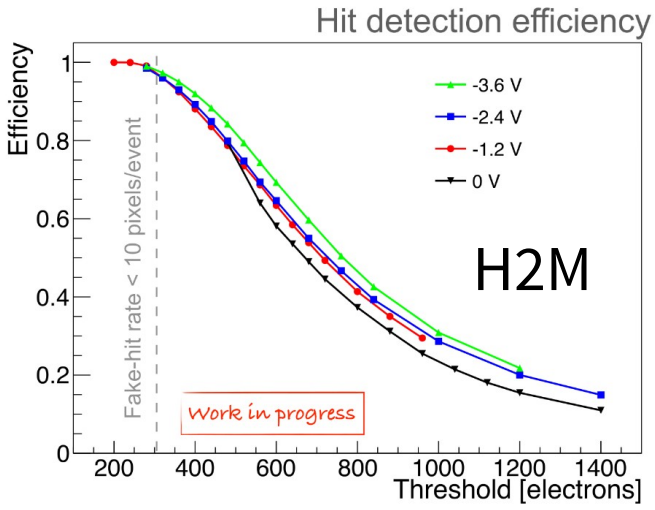
Tangerine – 65nm CIS Prototypes @ DESY

S. Ruiz Daza, M. Del Rio Viera



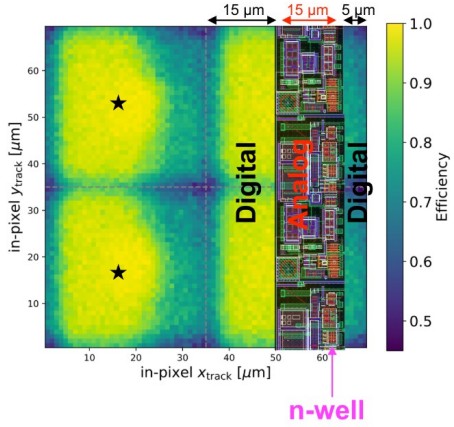






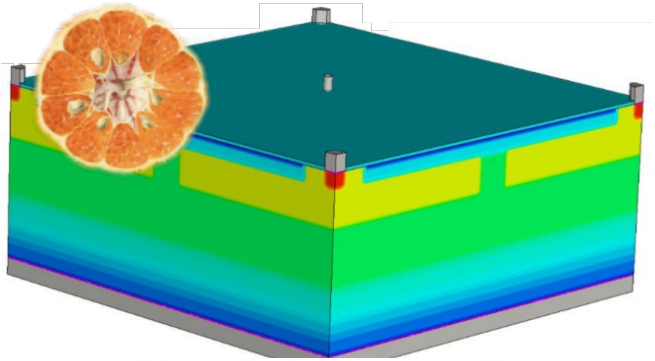
In-pixel efficiency map

V_{bias} = - 1.2 V, THL ≈ 520 e⁻



Tangerine – Simulation Toolkit for MAPS

H. Wennlöf, M. Del Rio Viera



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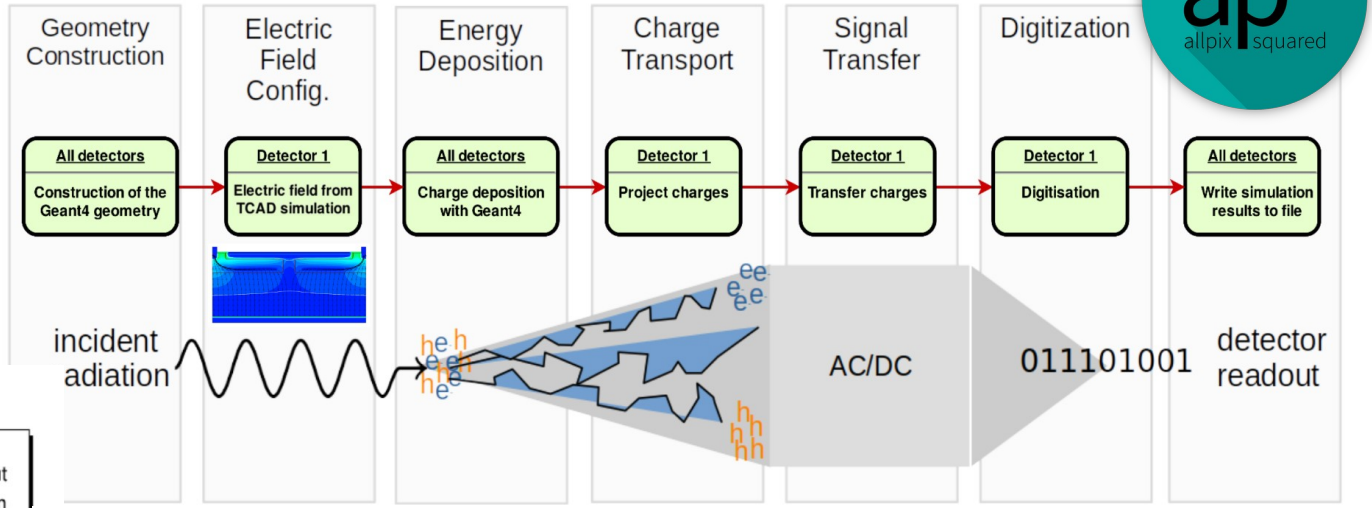
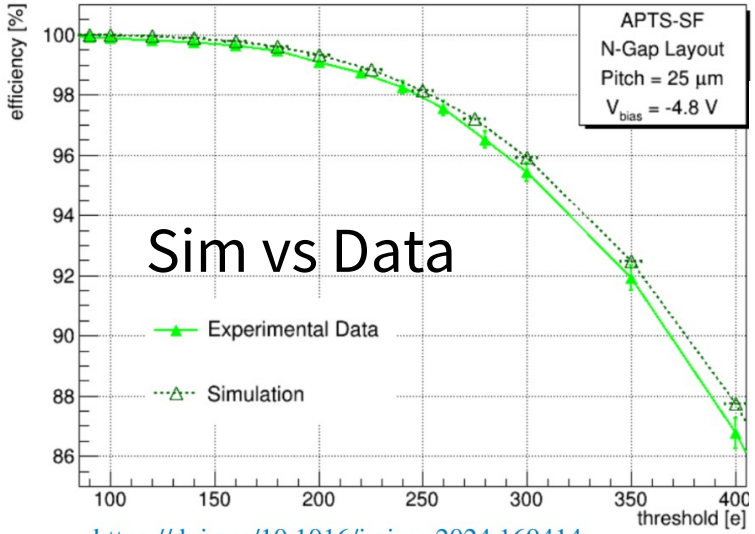
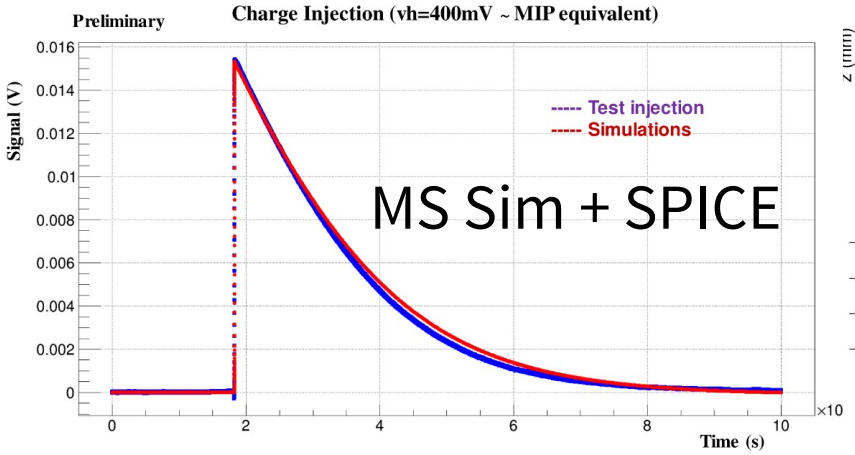
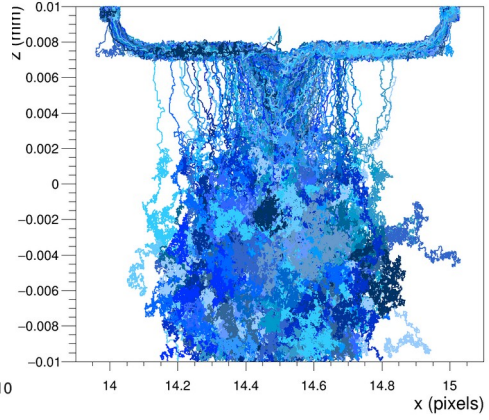


Mean efficiency vs threshold



https://doi.org/10.1016/j.nima.2024.169414

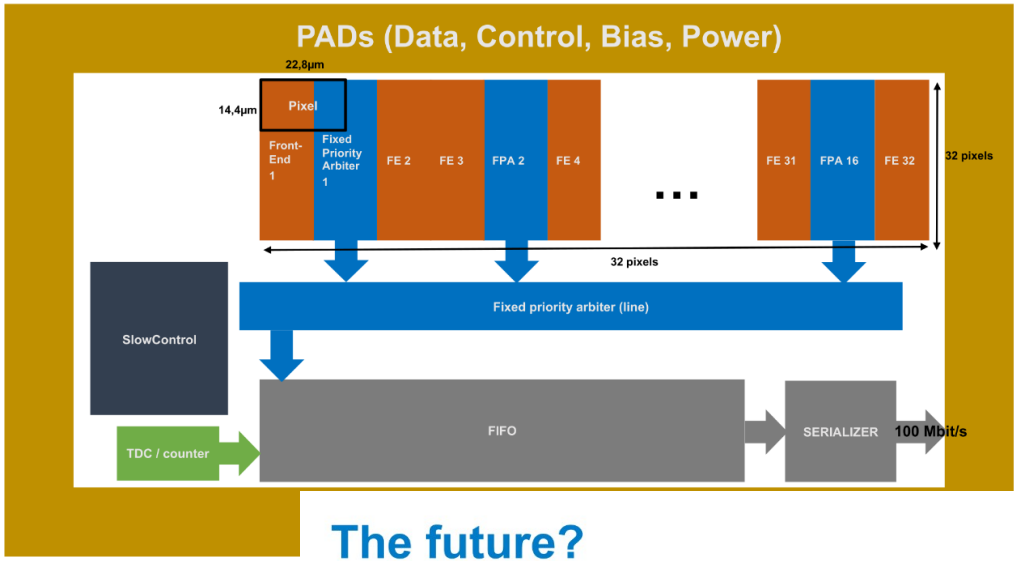




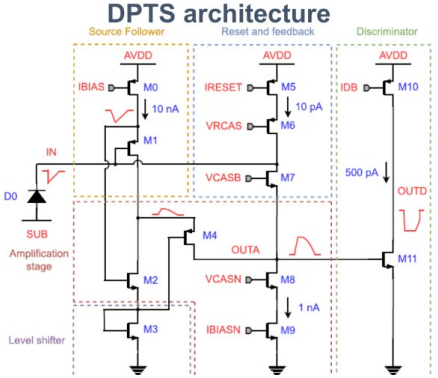
Discussion & Brainstorming

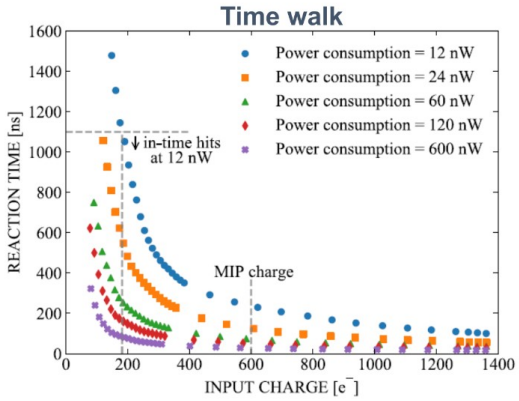
F. Morel

Front-end consideration



Another front-end can be developed





The future?

Where can we go and what could we sacrifice - not conclusive, should trigger discussions

- (Single) high power plane for timing
  - One close to vertex? ➔ bad in terms of material, good in terms of timing
  - Can we afford more?

L. Huth

- Need for stitching? Overlap of ca 25-40um thick sensor still okay? ➔ simulations
- Variable pixel pitch ➔ interconnecting pixels to reduce data output in outer layers?

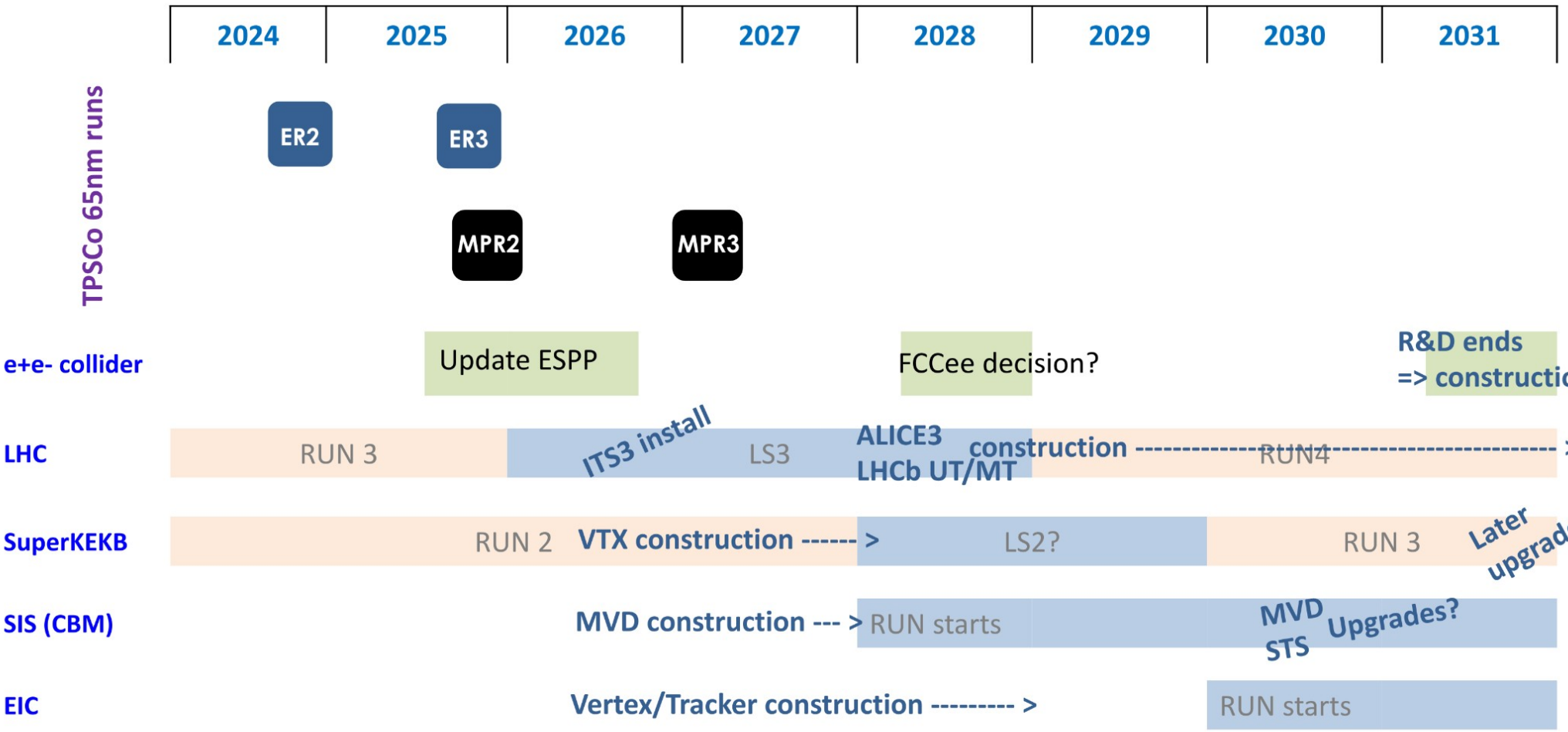
Les Entremets de Fromage

Timeline & Structure of a Vertex Project

Perspective on experiments (with MAPS)

J. Baudot

(Note: Mu3e not there)



CMOS Sensors for Vertex Detectors @ Lepton Collider Experiments

WP1: Simulations	WP2: ASIC Design	WP3: Data Acquisition	WP4: Testing & Characterization	WP5: System Demonstrator
Task 1: Sensor Optimization / TCAD	Task 1: Pixel Front-End	Task 1: Caribou 2 Development	Task 1: Summary of current 65nm Demonstrator Results	Task 1: Concept, Design of Mechanics & Cooling
Task 2: Detector Performance / Allpix Squared	Task 2: Matrix Architecture & Readout	Task 2: Demonstrator Preparation (SW, FW, PCB)	Task 2: Lab Characterization, FE Optimization, Calibration	Task 2: Prototype Construction
Task 3: Physics Performance / Geometry Optimization	Task 3: Periphery, DACs & Slow Control		Task 3: Testbeam Characterization, Performance	
	Task 4: Transceivers & Readout			

Le Dessert

Summary & Outlook

Summary

- Requirements to a lepton collider vertex detector very demanding & not yet met in any detector prototype / technology demonstrator
- Formation of large-scale R&D collaborations to structure research towards achieving requirements of Lepton Collider detectors
- DESY strongly involved in technology exploration, proponent of DRD3 (Silicon) common project for vertex detector
- Called for first (informal) meeting to collect results & ideas, gauge interest & structure the project
- Now preparing “proto-project” proposal for DRD3


DESY.