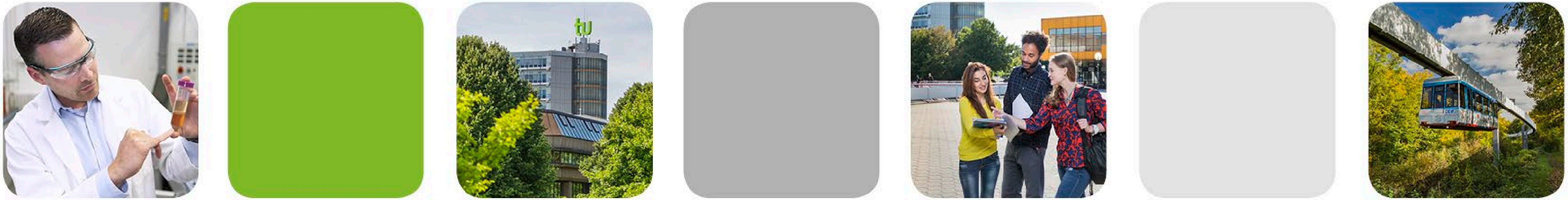
Si Detectors for Future Colliders

Dr. Jens Weingarten
AG Kröninger



Detector requirements

Physics
- flavour tagging, low pT tracking, vertex/jet charge determination
- momentum resolution, tracking efficiency, track separation, low pT fake track rejection
- (up to tertiary) vertex resolution few µm
- momentum resolution $\frac{\sigma_{pT}}{p_T^2} \approx 2 \times 10^{-5}\ \mathrm{GeV}^{-1}$

Environment
- bunch separation 20 - 3000 ns (except CLIC: 0.5 ns), power pulsing@ linear colliders, not @ circular ones
- beamstrahlung (i.e. beam induced background) high for linear, low for circular colliders

Detector Requirements

- large lever arm → R_{min}, R_{max}
- coverage |cos θ| < 0.99 (→ η > 2.7 ?)

➔ large area (Si Wrapper@IDEA: ~90 m²)

- single point spatial resolution:
  - ~3 µm for vertex detector
  - ~10 µm for tracking detector
- time resolution: ~1 ns (<100 ps for TOF layer)

- radiation hardness: O(100 kRad/yr) & O(10^{11}) n_{eq}/yr

- low mass: 0.1 - 0.2 % X_0 per layer
  (+ beam pipe ~0.14% X0@ILC or ~0.3% X0@FCC)
  → gas flow cooling
  ➔ low power: ≤50 mW/cm²
- low mass services
  ➔ power distribution, data rate (silicon photonics?)

Power challenges

adapted from A. Besson

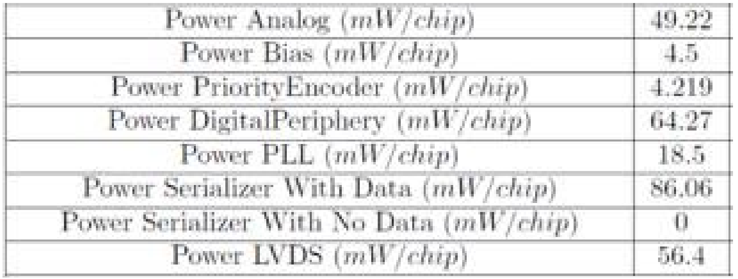
Power requirement conflicts with all other parameters

- Low material → Baseline is air flow cooling
  → max. power density not quite clear: 20 - 50 mW/cm²?
- Driving parameters
  - number of channels → pixel pitch, single-point resolution
  - charge collection speed → time resolution
  - data rate → on-chip and off-chip data transfer
  - total surface
- Power sharing
  - Analog part: 25-50% → pixel density, charge collection speed
  - Digital part: 25-50% → on-chip data transfer, clock frequency
  - Output driver: 25%

→ Architecture optimization crucial
  - priority encoding, asynchronous design, etc

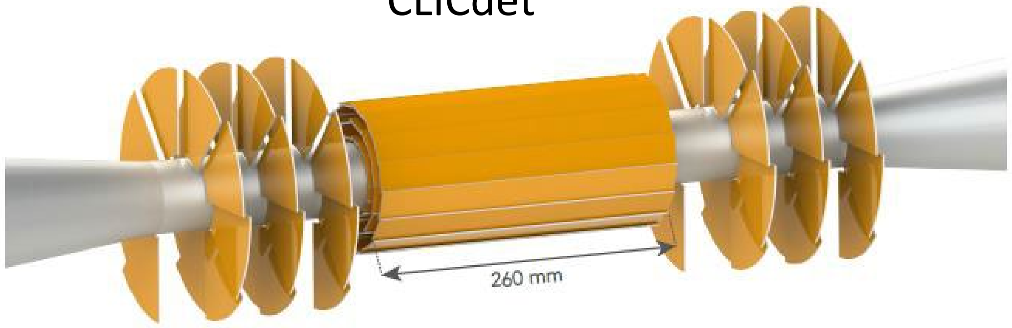
→ Technology: 180nm to 65nm ~50% power reduction

→ Disk layers might hinder air extraction



Power Analog ($mW/chip$)	49.22
Power Bias ($mW/chip$)	4.5
Power PriorityEncoder ($mW/chip$)	4.219
Power DigitalPeriphery ($mW/chip$)	64.27
Power PLL ($mW/chip$)	18.5
Power Serializer With Data ($mW/chip$)	86.06
Power Serializer With No Data ($mW/chip$)	0
Power LVDS ($mW/chip$)	56.4

CLICdet



Detector concepts

Number of common topics to be addressed, but all detector concepts include different Silicon detectors:

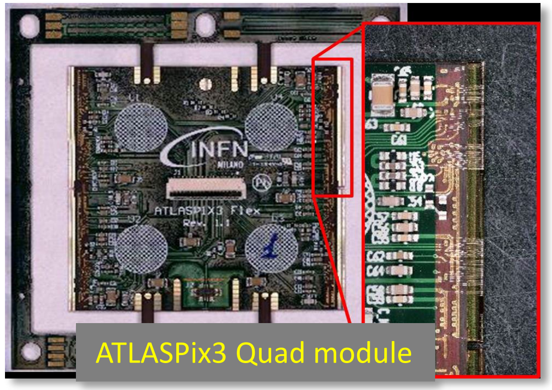
- Vertex detector
- Tracking detector
- TOF layer for particle ID

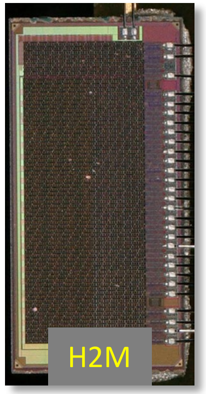
➔ Development can (should?) be split into

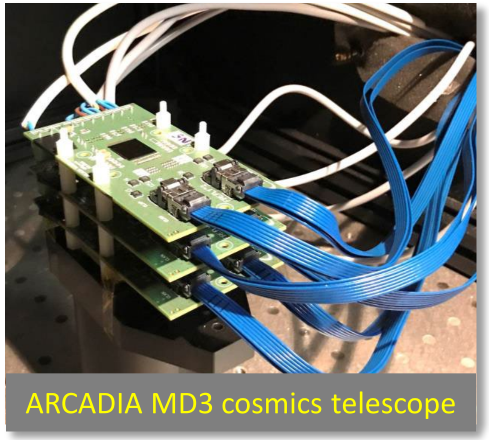
- extremely high performance: improve space and/or time resolution
  - single-point resolution ≤ 3µm non-trivial today
  - timing at small radius very challenging: O(1ps)
- high performance, large area: reduce cost per area
  - lower hit density and longer TOF at large radii

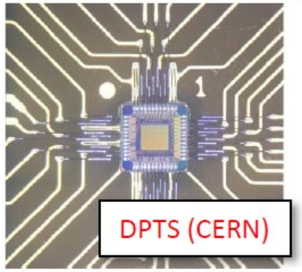
R&D Efforts

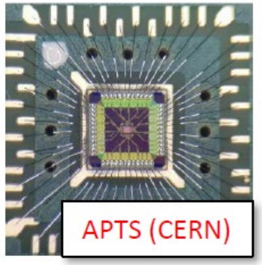
Large number of development lines - a selection


ATLASPix3 Quad module

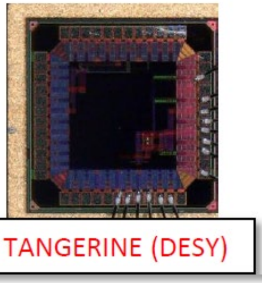

H2M

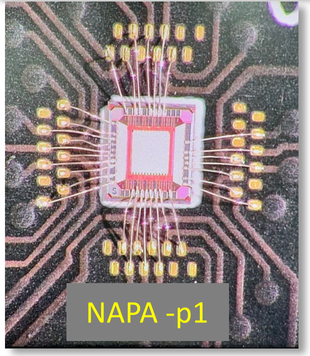

ARCADIA MD3 cosmics telescope


DPTS (CERN)

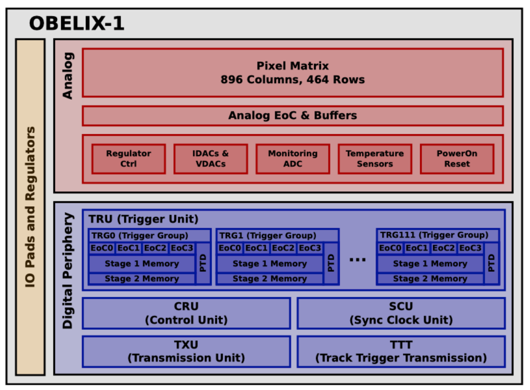

APTS (CERN)

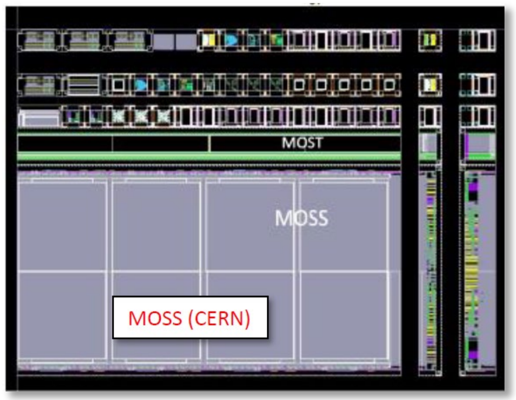
And probably many more…
Apologies to all I forgot!


TANGERINE (DESY)


NAPA -p1


CE-65 (IPHC)





MOSS (CERN)

Most focussed on monolithic detectors
But: Hybrid detectors are not dead!

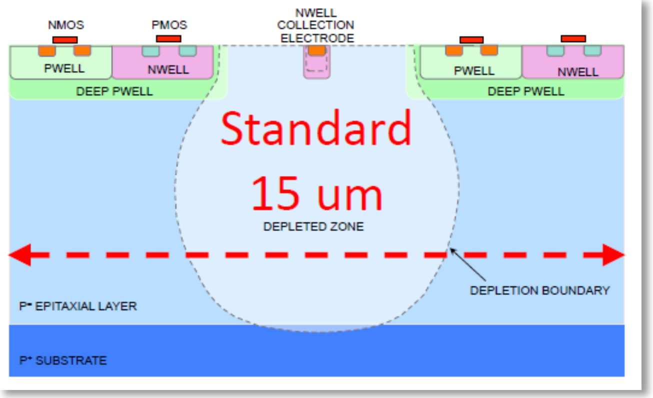
Technologies by Requirement - 1

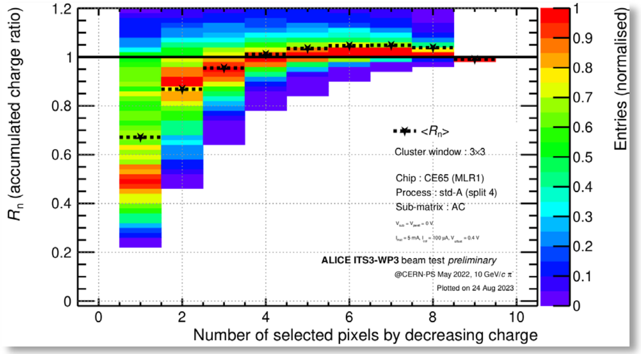
Spatial Resolution

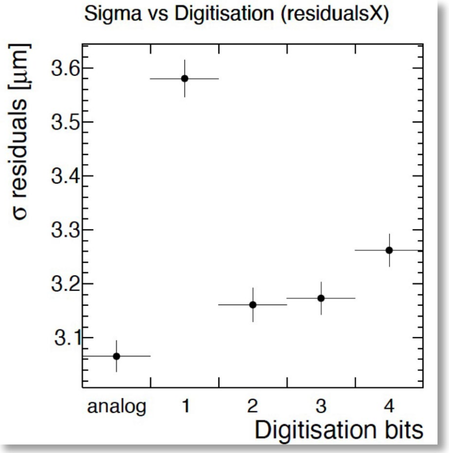
Resolution in each layer depends on

- Pixel pitch
  - most prototypes: 10 - 35 µm
  - in conflict with in-pixel functionality
- Charge deposition → sensitive layer thickness
  - epi layer thickness ~10 µm
  - DMAPS thickness 50 µm
- Charge sharing
  - charge cloud width vs pixel pitch
  - w/o noise: σ ≥ p/2
- Charge encoding
  - # ADC bits

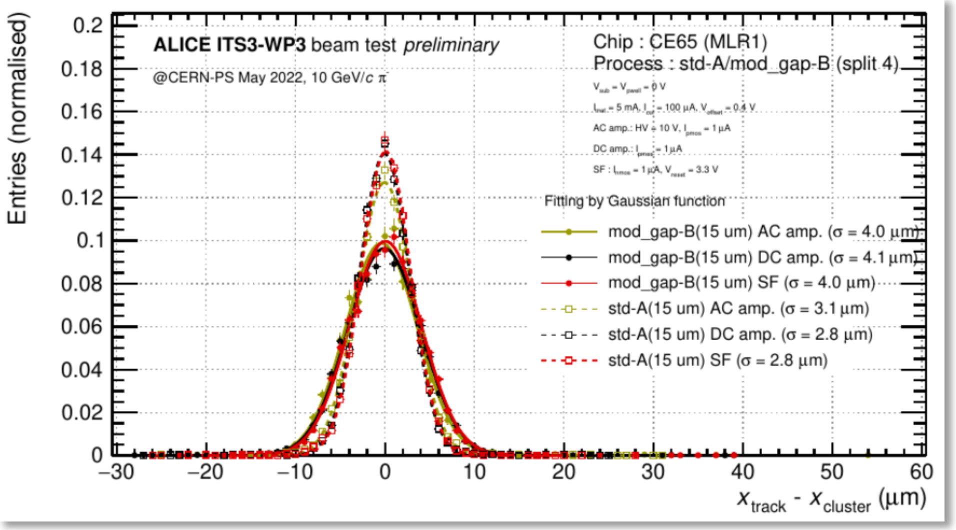
➔ σ_{sp} ~ 3 µm seems achievable







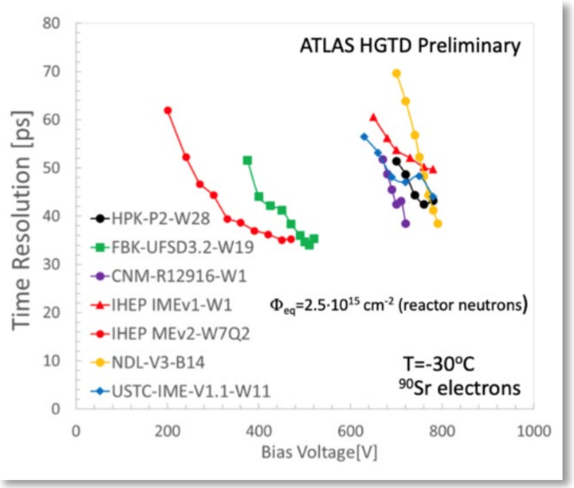
PhD G. Sadowski



Technologies by Requirement - 2

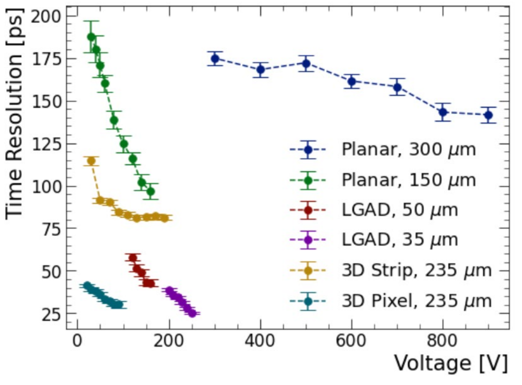
Timing Resolution

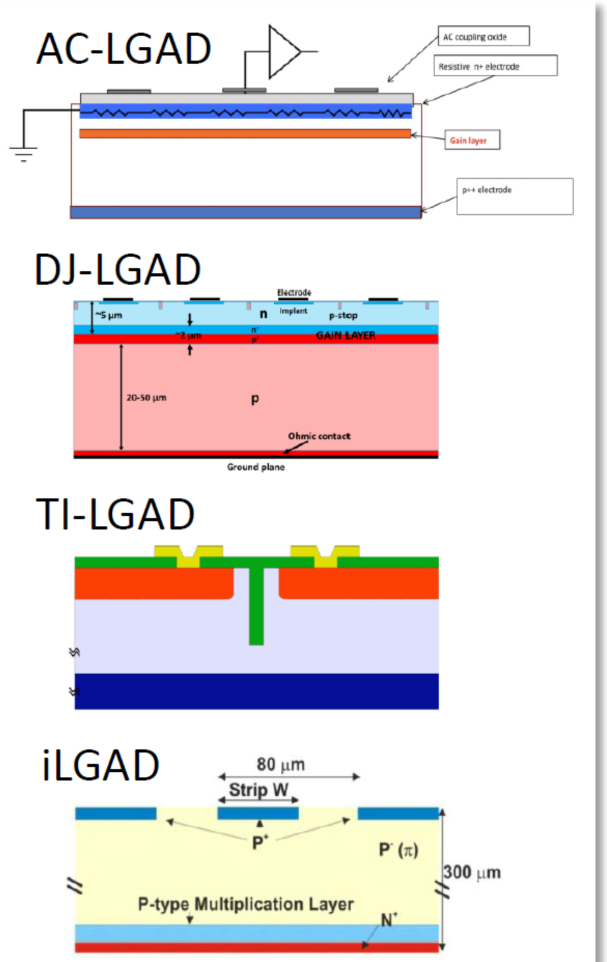
Many applications
- TOF particle ID
- pile-up suppression
- tracking pattern recognition, shower analysis
- physics of long-lived particles



σ_{total}~35 ps demonstrated by ATLAS HGTD and others

Directions in R&D
- LGADs, e.g. Resistive Silicon Detectors
  - LGADs with continuous gain layer
  - charge collection through resistive n-layer
- hybrid 3D silicon detectors
- CMOS detectors with gain layer





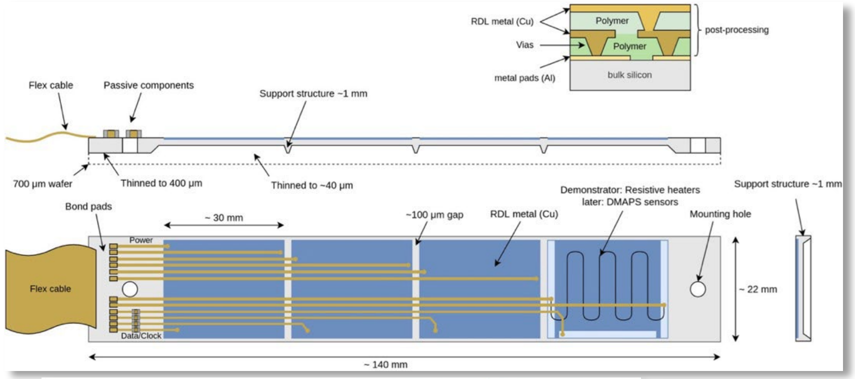
E. Currás, VERTEX 2020
N. Cartiglia, TF3

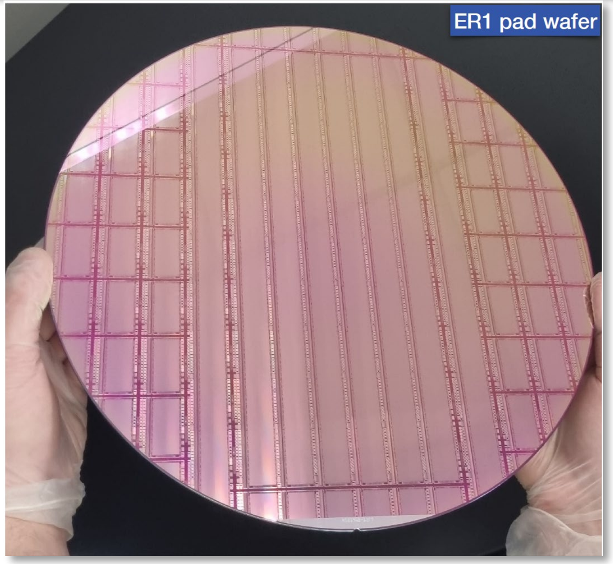
Technologies by Requirement - 3

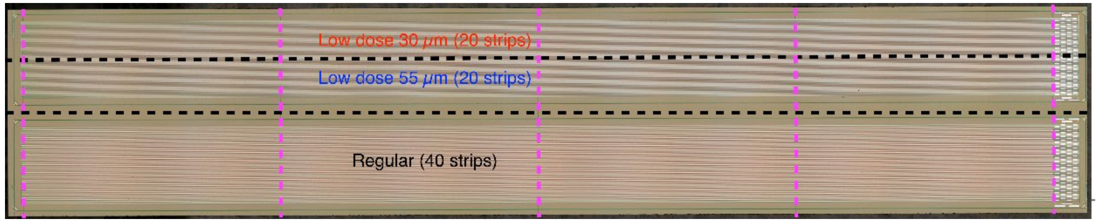
Large Area

Since there is some confusion in DRD3…
These detectors don’t need ultimate performance but high yield and production capacity (at the vendor and when building modules), affordable cost, efficient connections and services

- reduce production cost for “classic size” sensors
  - hybrid passive CMOS sensors (pixel & strip)→ production, interconnection (wafer-to-wafer bonding, etc)
  - monolithic active CMOS strip sensors
- wafer scale sensors
  - stitching (+ bent sensors) → ALICE ITS-3
  - post-process RDL (Belle II iVTX Upgrade: 4 sensors per self-supporting ladder)







Technologies by Requirement - 4

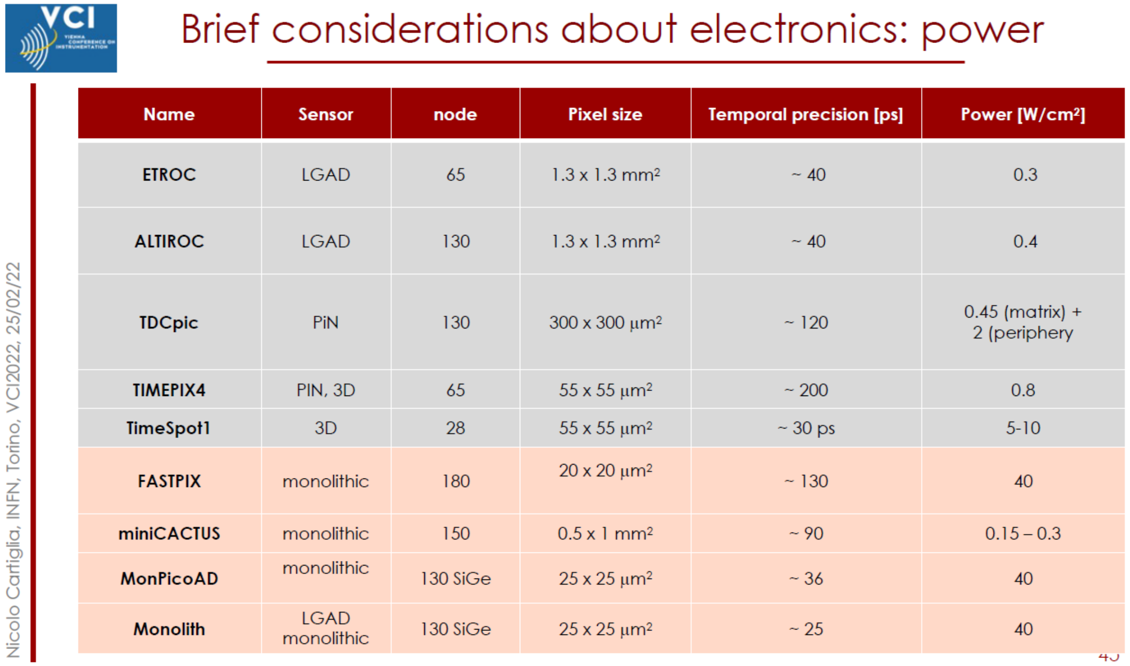
Power Consumption

- some of the prototypes reach ~100 mW/cm²
  - MIMOSIS reports 40 - 70 mW/cm², ATLASPix3.1 ~ 175 mW/cm²
  - others estimate 10 - 50 mW/cm²
- max allowable power density not very clear
  - Mu3e (He cooling) reports ΔT ≤ 50 K detector temp wrt gas inlet temp for a heat dissipation of 350 mW/cm²
- subject of DRD7.1

➔ limit not clear, but: the lower, the better

➔ need engineering support

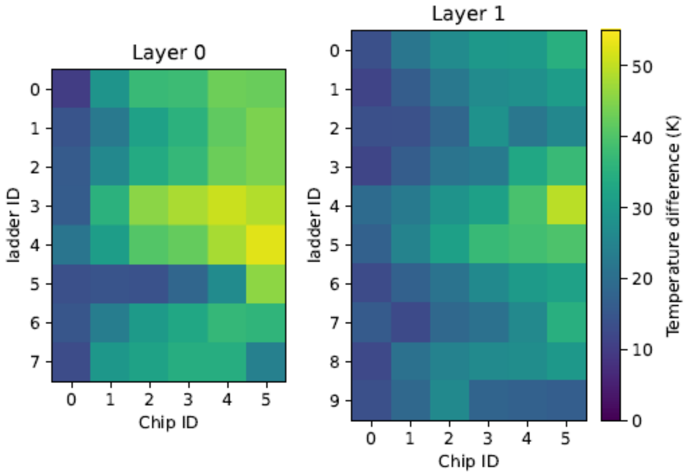
→ thermal simulation crucial

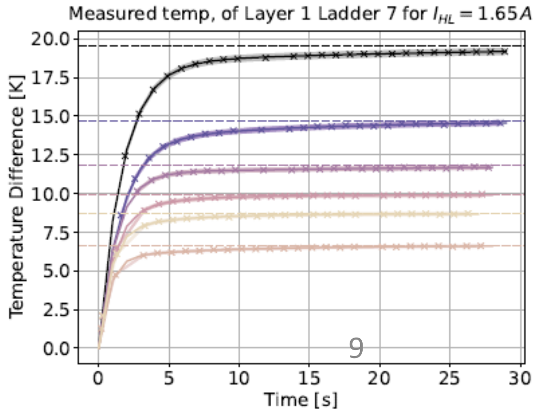


Brief considerations about electronics: power

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm²]
ETROC	LGAD	65	1.3 x 1.3 mm²	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm²	~ 40	0.4
TDCpic	PiN	130	300 x 300 μm²	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 μm²	~ 200	0.8
TimeSpot1	3D	28	55 x 55 μm²	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 μm²	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm²	~ 90	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 μm²	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm²	~ 25	40

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22

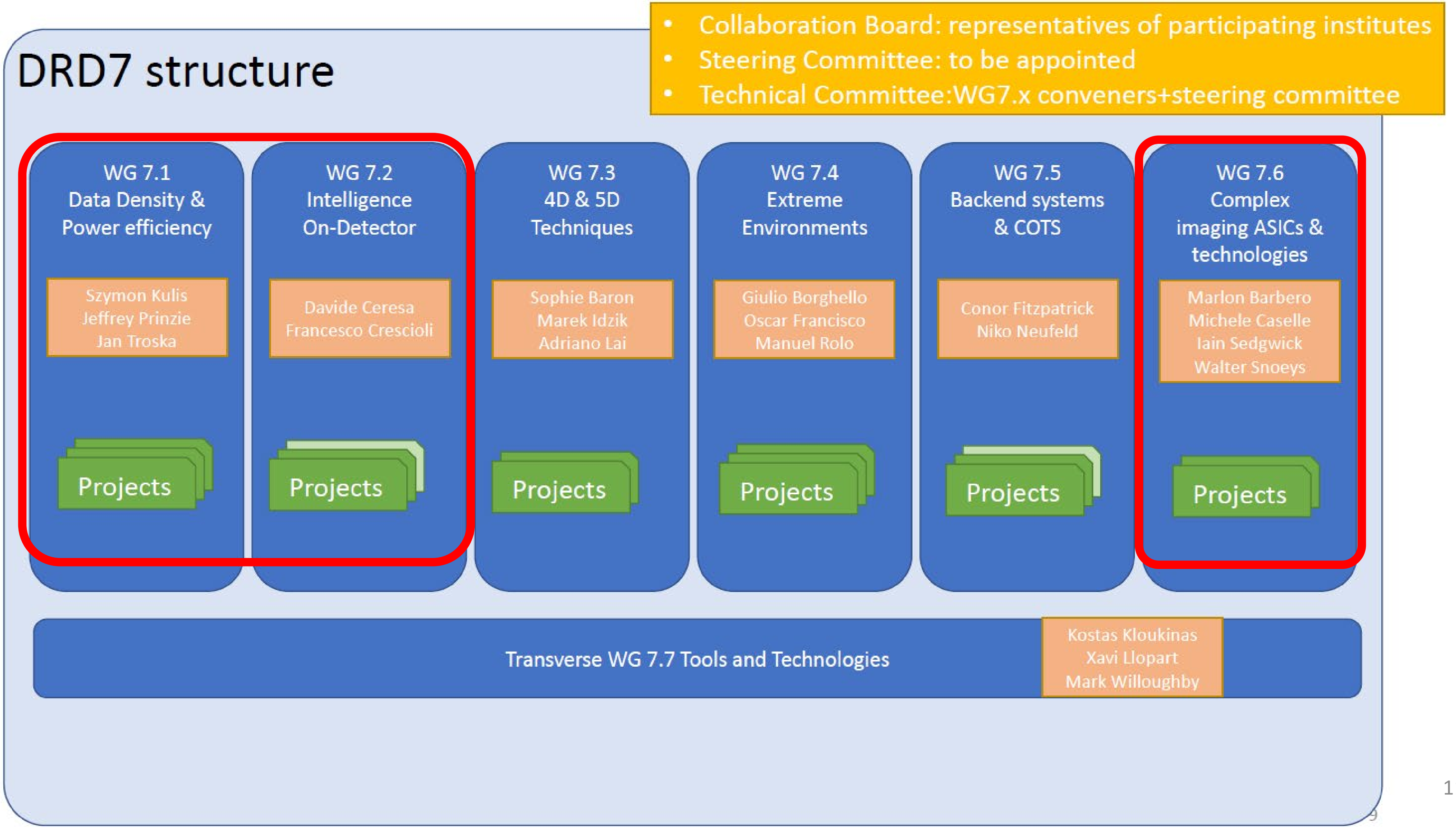




Mapping R&D to DRD3

			Working Groups							
			WG1 - Monolithic silicon technologies	WG2 - hybrid silicon technologies	WG3 - Radiation hardening	WG4 - Simulation	WG5 - Characterization techniques, facilities	WG6 - Wide bandgap and innovative sensor materials	WG7 - Interconnection technologies	WG8 - Outreach and dissemination
Working Packages	WP1 - CMOS sensors	1.1 Spatial resolution	✗			✗	✗			
		1.2 Timing resolution	✗			✗	✗			
		1.3 Read-out architectures	✗			✗	✗			
		1.4 Radiation tolerance					✗			
		1.5 Low-cost large-area CMOS sensors	✗	✗		✗	✗		✗	
	WP2 - Sensors for 4D tracking	2.1 3D sensors	✗	✗		✗	✗		✗	
		2.2 LGAD		✗		✗	✗		✗	
	WP3 - Sensors for extreme fluences	3.1 wide band-gap materials								
		3.2 diamond-based detectors								
		3.3 extreme fluence: silicon detectors								
	WP4 - 3D-integration and interconnection	4.1 integration: fast and maskless interconnect		✗					✗	
		4.2 3D in-house post-processing for hybridization		✗					✗	
		4.3 Advanced interconnection techniques		✗					✗	
		4.4 mechanics and colling	✗	✗					✗	

Mapping R&D to DRD7



DRD7 structure

- Collaboration Board: representatives of participating institutes
- Steering Committee: to be appointed
- Technical Committee:WG7.x conveners+steering committee

WG 7.1
Data Density &
Power efficiency
Szymon Kulis
Jeffrey Prinzie
Jan Troska
Projects

WG 7.2
Intelligence
On-Detector
Davide Ceresa
Francesco Crescioli
Projects

WG 7.3
4D & 5D
Techniques
Sophie Baron
Marek Idzik
Adriano Lai
Projects

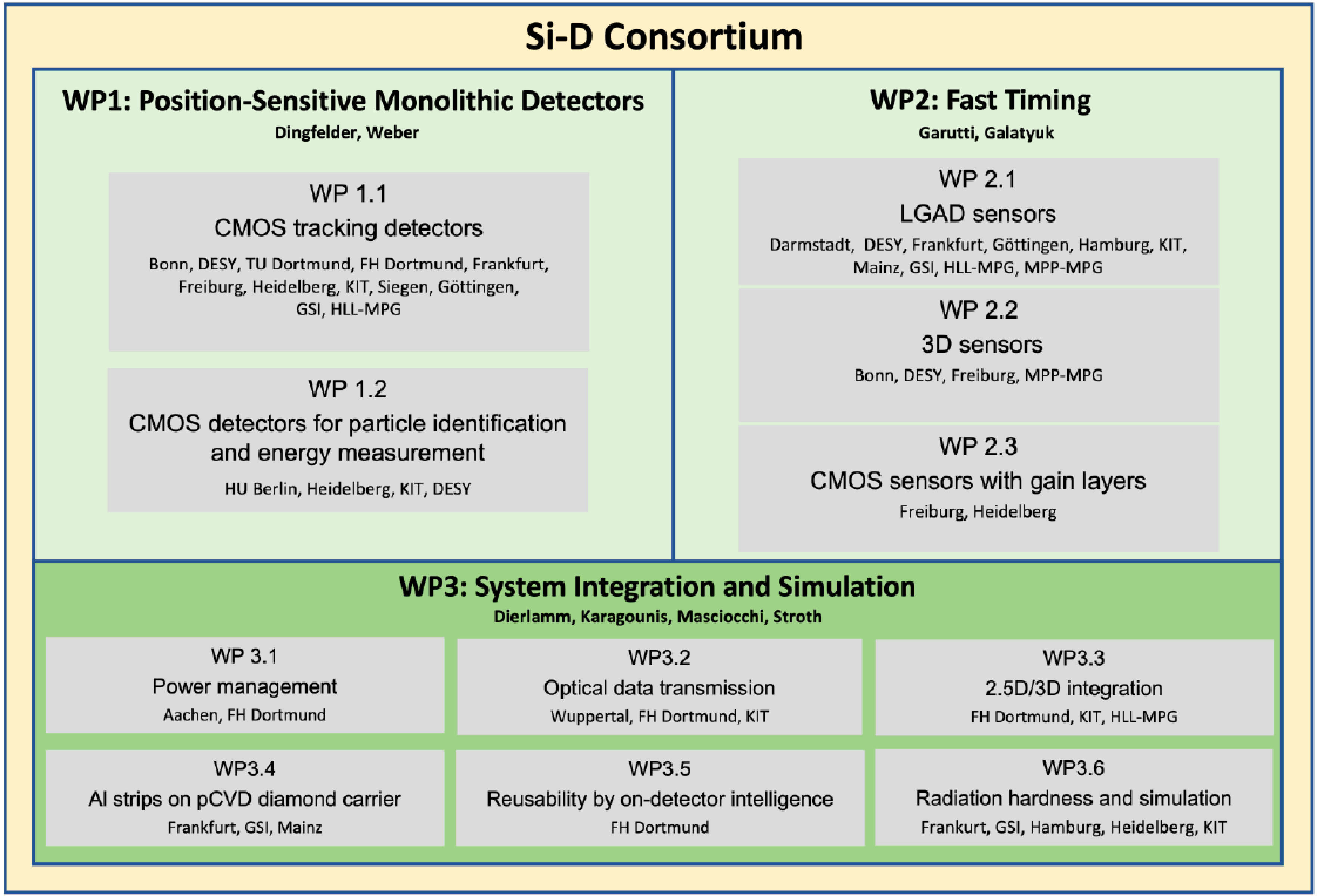
WG 7.4
Extreme
Environments
Giulio Borghello
Oscar Francisco
Manuel Rolo
Projects

WG 7.5
Backend systems
& COTS
Conor Fitzpatrick
Niko Neufeld
Projects

WG 7.6
Complex
imaging ASICs &
technologies
Marlon Barbero
Michele Caselle
Iain Sedgwick
Walter Snoeys
Projects

Transverse WG 7.7 Tools and Technologies
Kostas Kloukinas
Xavi Llopart
Mark Willoughby

Mapping R&D to Si-D



Si-D Consortium

WP1: Position-Sensitive Monolithic Detectors
Dingfelder, Weber

WP 1.1
CMOS tracking detectors
Bonn, DESY, TU Dortmund, FH Dortmund, Frankfurt, Freiburg, Heidelberg, KIT, Siegen, Göttingen, GSI, HLL-MPG

WP 1.2
CMOS detectors for particle identification and energy measurement
HU Berlin, Heidelberg, KIT, DESY

WP2: Fast Timing
Garutti, Galatyuk

WP 2.1
LGAD sensors
Darmstadt, DESY, Frankfurt, Göttingen, Hamburg, KIT, Mainz, GSI, HLL-MPG, MPP-MPG

WP 2.2
3D sensors
Bonn, DESY, Freiburg, MPP-MPG

WP 2.3
CMOS sensors with gain layers
Freiburg, Heidelberg

WP3: System Integration and Simulation
Dierlamm, Karagounis, Masciocchi, Stroth

WP 3.1
Power management
Aachen, FH Dortmund

WP3.2
Optical data transmission
Wuppertal, FH Dortmund, KIT

WP3.3
2.5D/3D integration
FH Dortmund, KIT, HLL-MPG

WP3.4
Al strips on pCVD diamond carrier
Frankfurt, GSI, Mainz

WP3.5
Reusability by on-detector intelligence
FH Dortmund

WP3.6
Radiation hardness and simulation
Frankurt, GSI, Hamburg, Heidelberg, KIT

Starting points for discussion

Si-D consortium covers all requirements

→ Use it to consolidate collaboration: Production cost, person power
but also: specialization of groups

→ Transport collaboration into DRDs ➔ Start writing proposals

Rich R&D landscape

→ Do we want to concentrate efforts now?

→ If not, how do we decide, when to converge?

→ Which technologies are worth concentrating on?
Process lifetime, industry interests, availability/accessibility of foundries, affordability now and in 20 years

With all the uncertainties, how do we keep experts interested enough until 20XY? Sustainability

→ Huge (or no) competition with industry

→ Low threshold contributions: MSc theses

Thank you for your attention

Backup

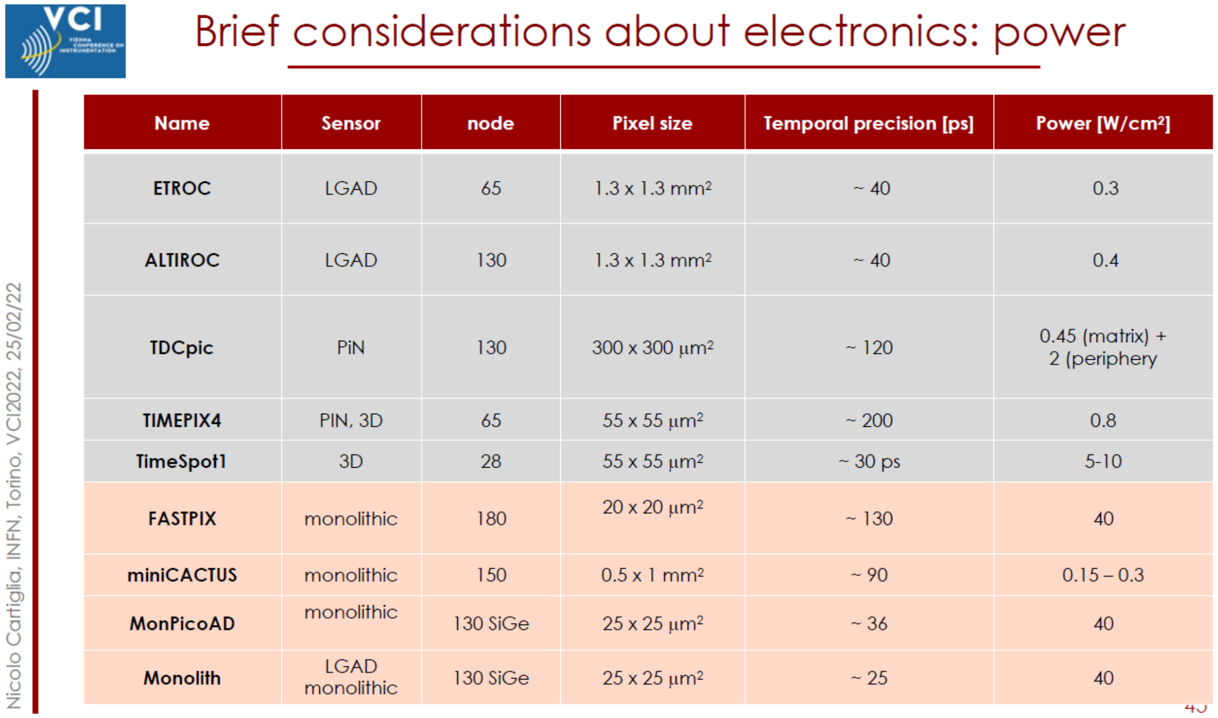
Collider	ILC		CLIC	FCCee			CEPC		Detector requirements
Bunch separation (ns)	330/550		0.5	20/99/3000			25/680		moderate time resolution (except CLIC)
Power Pulsing	yes		yes	no			no		very low power
beamstrahlung	high		high	low			low		moderate radiation hardness
Detector concept	SiD	ILD	CLICdet	CLD	IDEA	LAr	Baseline	IDEA	
B Field (T)	5	3.5	4	2	2	2	3	2	
Vertex det.	Si Pixel	Si Pixel	Si Pixel	Si Pixel	Si Pixel	Si Pixel	Si Pixel	Si Pixel	
Vertex Rmin (mm)	16	16	31	~12	~12	~12	16	16	
Tracking det.	Si Strip	TPC	Si Pixel	Si Pixel (+RICH?)	DC/Si Strip	DC/Si Strip	TPC or Si Strip	DC/Si Strip	
Tracker Rmax (m)	1.25	1.8	1.5	2.2	2.0	2.0	1.8	2.1	
Disks	4 + 4	2 + 5	6 + 7	3 + 7	3		2 + 6		

Contributions to timing resolution:

$$\sigma^2_{\text{total}} = \sigma^2_{\text{det}} + \sigma^2_{\text{elec}} + \sigma^2_{\text{clock}}$$

- σ_{det} from Landau fluctuations, σ_{clock} from clock jitter

$$\sigma^2_{\text{elec}} = \underbrace{\left(\frac{t_{rise}}{S/N}\right)^2}_{\text{jitter}} + \underbrace{\left(\left[\frac{V_{thr}}{S/t_{rise}}\right]_{RMS}\right)^2}_{\text{timewalk}} + \underbrace{\left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2}_{\text{TDC binning}}$$



Brief considerations about electronics: power

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm²]
ETROC	LGAD	65	1.3 x 1.3 mm²	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm²	~ 40	0.4
TDCpic	PiN	130	300 x 300 μm²	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 μm²	~ 200	0.8
TimeSpot1	3D	28	55 x 55 μm²	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 μm²	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm²	~ 90	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 μm²	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm²	~ 25	40

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22