DC-DC and serial powering tests in ATLAS

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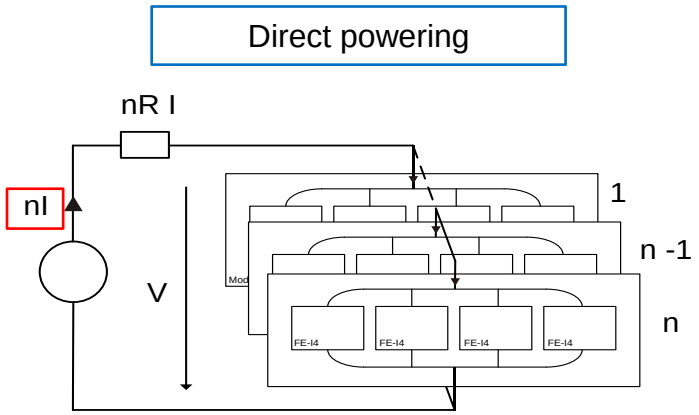
on behalf of the ATLAS power working group

Outlook

- Introduction
- SP and DC-DC conversion powering schemes for the pixels
  - Serial powering: Shunt-LDO and SP stave prototype
  - DC-DC: x2 charge pump DC-DC converter
- Summary of strips R&D activities on powering
- Conclusion

Introduction

- Powering scheme of the ATLAS tracker (strips + pixels): direct powering
  - Low efficiency (20 - 50%), very massive
- Not feasible for high luminosity upgrades: higher detector granularity & smaller feature size FE technology → higher current → higher power losses on cables + prohibitive amount of cables



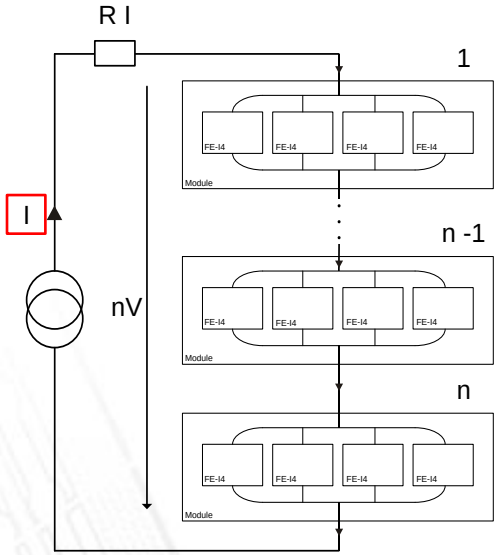
- For the upgrades of the ATLAS tracker for HL-LHC, two powering scheme are investigated
  - Serial powering (SP)
  - DC-DC conversion

- Aim: reduce the amount of transmitted current wrt direct powering
  - The voltage drop on cables (RI) decreases → higher power efficiency
  - The cable cross section decreases → lower material budget

SP vs. DC-DC

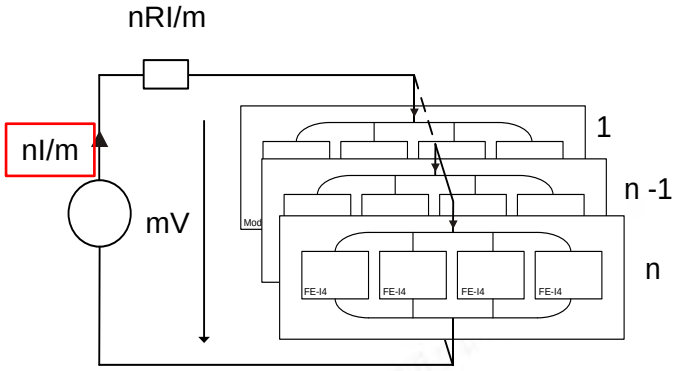
Serial powering

- Number of modules = n
- wrt direct powering the current scales of a factor n: nI → I



DC-DC conversion

- Conversion factor = m
- wrt direct powering the current scales of a factor m: nI → nI/m

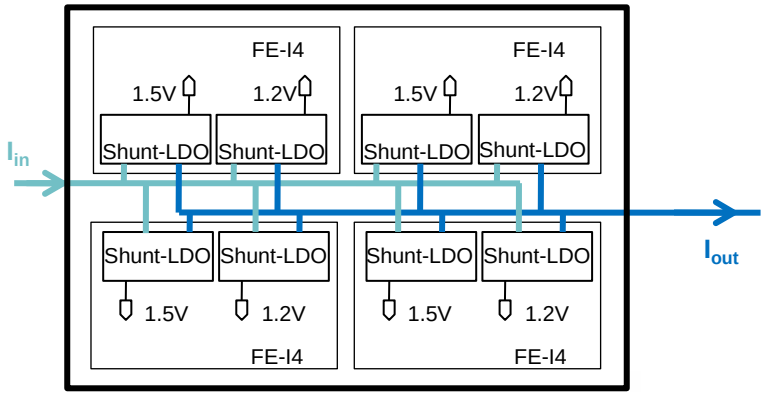


SP = DC-DC in terms of power efficiency and material reduction if n = m

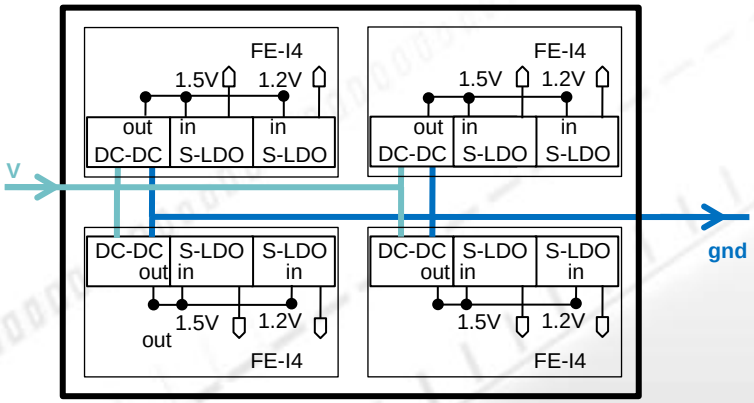
Powering schemes for pixels

Discrete regulators/converter are not an option for pixels cause they would introduce too much material → all regulators/converters on-chip

Current distribution on module



Voltage distribution on module



Serial power

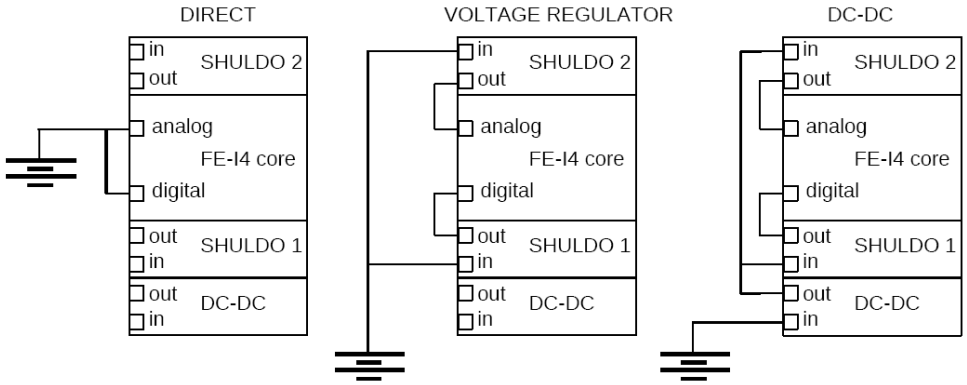
- Chain of 8-10 modules powered in series, i.e. current flows from module to module
- On module the current splits in parallel between the FE chips
- On-chip voltage generation
  - 2 shunt-LDO regulators/FE
- Note: 8 Shunt-LDO regulators on module are operated in parallel

DC-DC conversion

- Direct power with on-chip DC-DC converter
- Switched capacitor DC-DC converter

FE-I4A powering

- FE-I4A is the prototype of the next generation pixel FE chip for upgrades
- FE-I4A can be powered using different options, none of which is hard wired inside the chip
  - Direct
  - Shunt-LDO regulators, in shunt or linear mode
  - X2 charge pump DC-DC converter



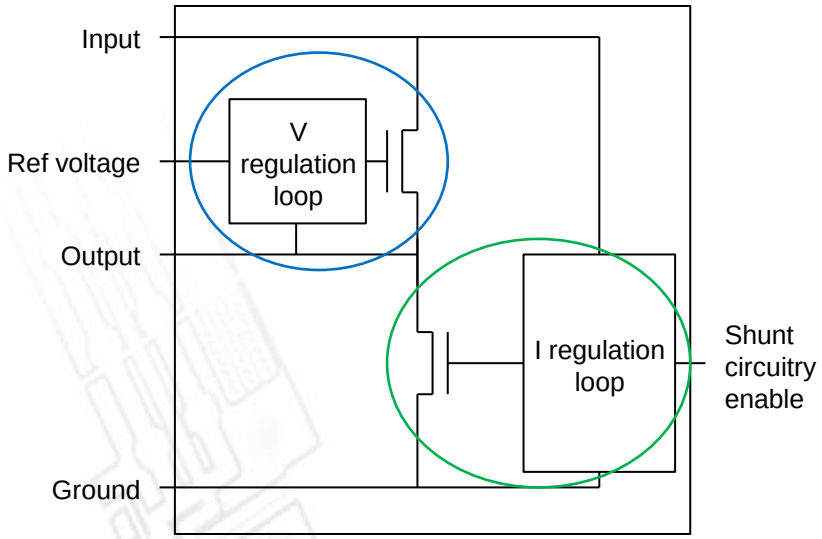
- FE-I4A power consumption
  - VDDA = 1.5V, Ia = 0.300 – 0.380A
  - VDDD = 1.2V, Id = 0.100 – 0.180A

History of SP for pixels in Bonn

- R&D on serial powering in Bonn started almost 10 years ago
- Early activities resulted in the "Serial powering Proof of Principle"
  - Half a stave of the current ATLAS pixel detector was powered in series
  - No performance degradation wrt direct powering
  - No noise pick up through the power lines
- Following these results decision was taken to propose serial powering for the upgrades of ATLAS pixel detector
- Work started on a new regulator concept: the Shunt-LDO
  - Two prototypes demonstrated the working principle and showed good results
  - Integrated 2 shunt-LDO regulators in FE-I4A
    - Characterization of the regulator in FE-I4A → done
    - Characterization of modules powered with the Shunt-LDO → ongoing
    - Serial powering stave prototype with FE-I4A → starting, next

Shunt-LDO regulator simplified

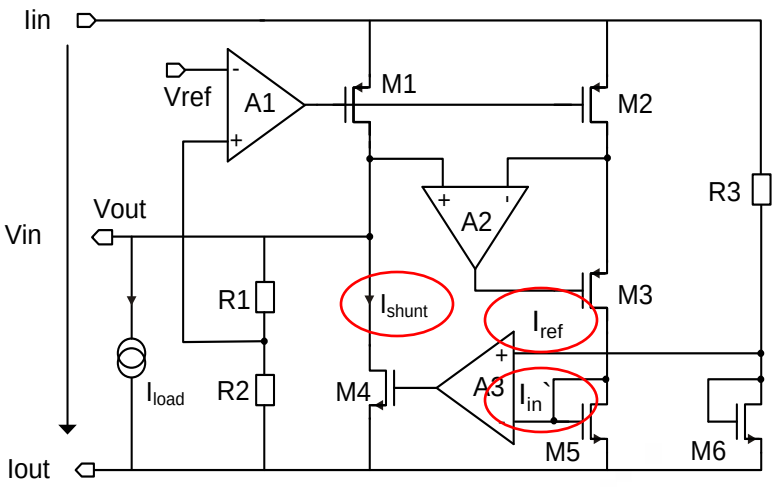
- 2 regulation loops
  - V regulation loop (LDO): provide a constant V_{out}
  - I regulation loop (shunt): when enabled can
    - Set a minimum current limit under which the current through the regulator cannot go (1)
    - Keep the current though the regulator constant independently of the load (2)
- Multiple configurable working modes for use in
  - LDO mode & partial shunt mode → powering schemes requiring linear regulation
  - Shunt mode → serially powered systems requiring shunt regulation



		Partial shunt	LDO	Shunt
V regulation loop		✓	✓	✓
I regulation loop	ON	✓ (1)		✓ (2)
	OFF		✓	
Input	V	✓	✓	
	I			✓

Shunt mode

- Dedicated serial powering working mode of the regulator
- In this mode the current through the regulator is kept constant independently of variation of the load current
  - Fraction of M1 current is mirrored (M2, A2, M3) and drained in M5 → I_{in}`
  - Reference current defined by resistor R3 & drained into M6 → I_{ref}
  - I_{in}` and I_{ref} compared in A3 → M4 shunts the current (I_{shunt}) not drawn by the load

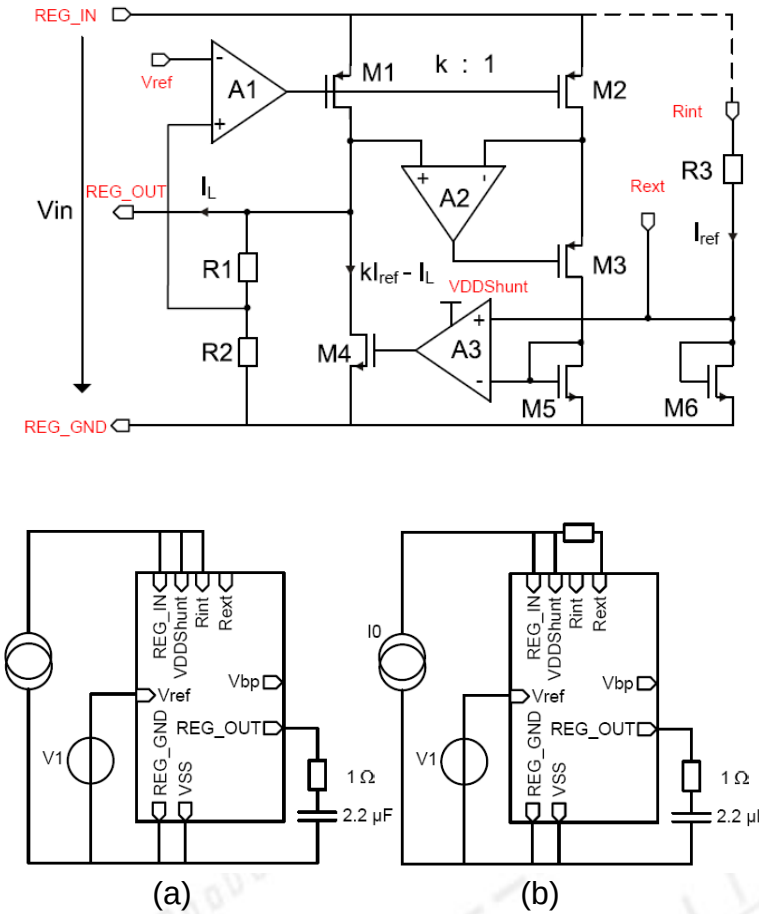


Benefits wrt standard shunt regulators:

- Shunt-LDO regulators generating different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution
- Capability of shunting extra current if one of the parallely placed regulators fails (I_{shunt} increases)

Shunt-LDO regulator in FE-I4A

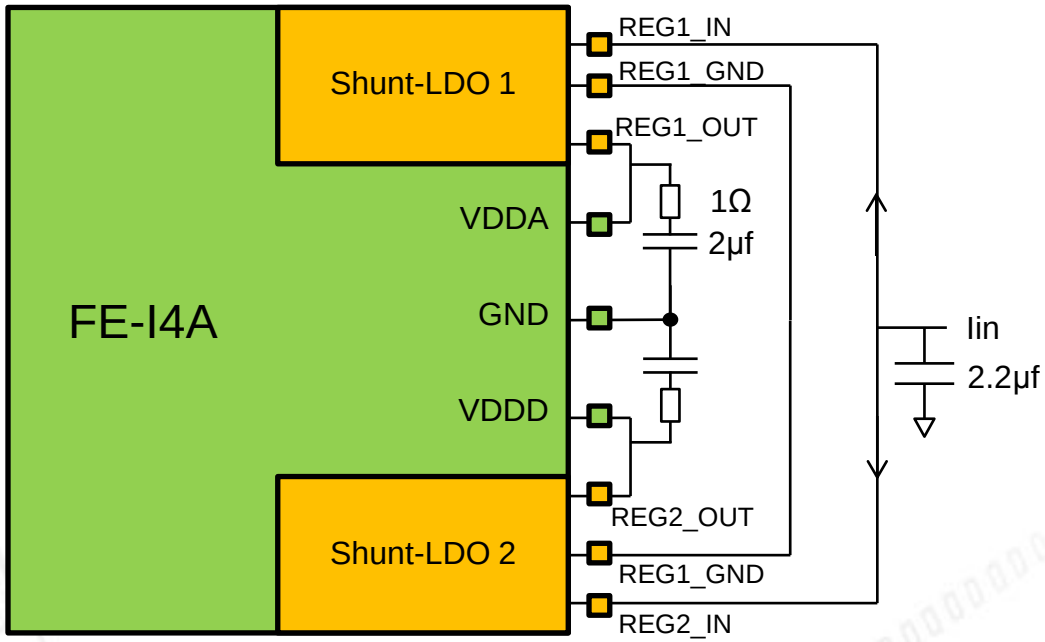
- REG_IN = 0.5 – 0.6A / 1.4 – 2.5V
- REG_OUT = 2 · Vref = 1.2 – 1.5V
  - V_{ref} has to be provided externally
- Shunt circuitry
  - Enable: Bias V = VDDShunt = REG_IN
  - Reference resistor to set I_{shunt}
    - Internal resistor = Rint = 2KΩ
    - External resistor = Rext
- Working mode selectable via wire bonds
  - Shown here: shunt mode



Shunt mode configuration via wire bonds, using Rint (a), or Rext (b)

Shunt-LDO configuration to power FE-I4A

- To power the FE-I4, the two shunt-LDO regulators on chip are connected in parallel, i.e. same input and ground connection
- The output of the regulators are connected to VDDA and VDDD

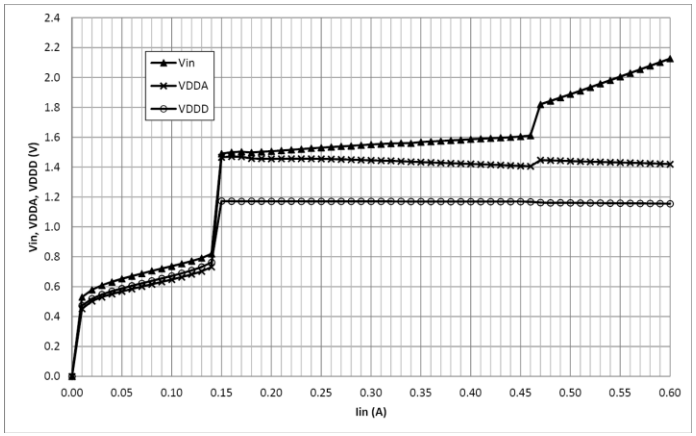


Shunt-LDO regulators configuration on board
(only input, output and ground connection shown here)

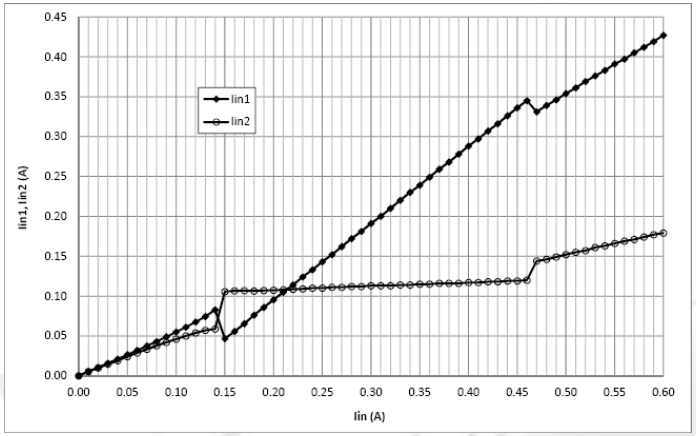
Shunt-LDO characterization

- Voltage generation
  - For I_{in} > 0.470A the outputs are regulated
  - The decrease of VDDA/D with I_{in} is due to the decrease of the effective V_{ref} seen by the chip
  - 0.150 – 0.470A: non stable operation, the regulator oscillates
- Current distribution
  - Improved shunt operation: 2 Shunt-LDO regulators can be operated in parallel with different shunt current
- Load regulation = $\Delta V_{out}/\Delta I_{load}$ = 150mΩ
  - Simulations: <30mΩ
- For regulation
  - Min I_{shunt} = 5mA
  - Min V_{drop} = 100mV

Voltage generation

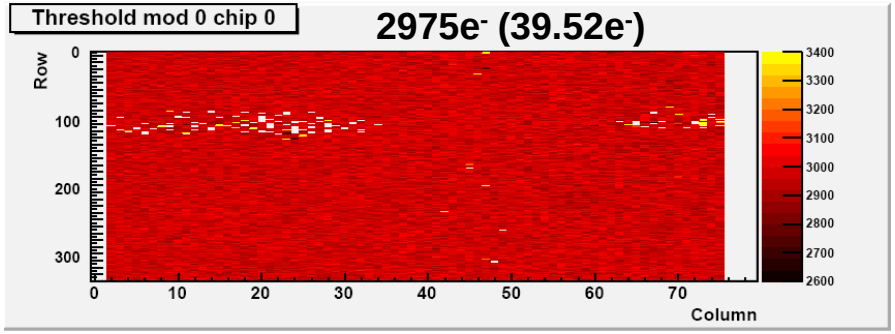


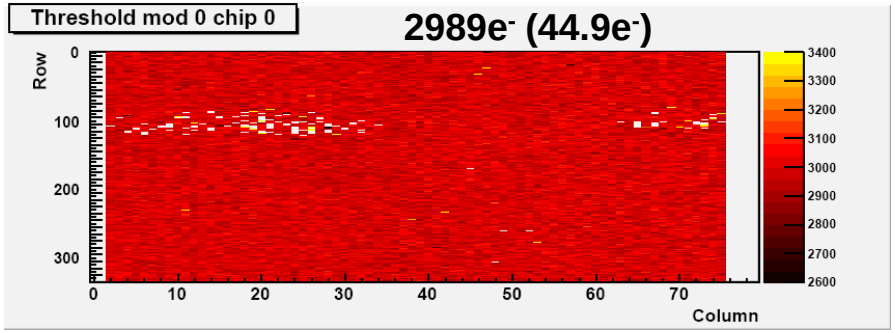
Current distribution



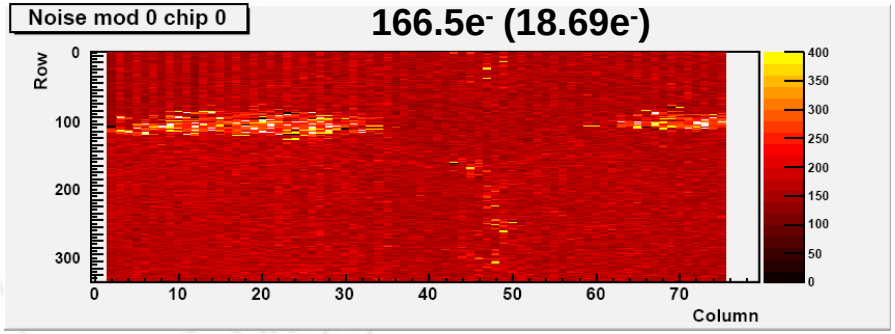
FE-I4: threshold and noise

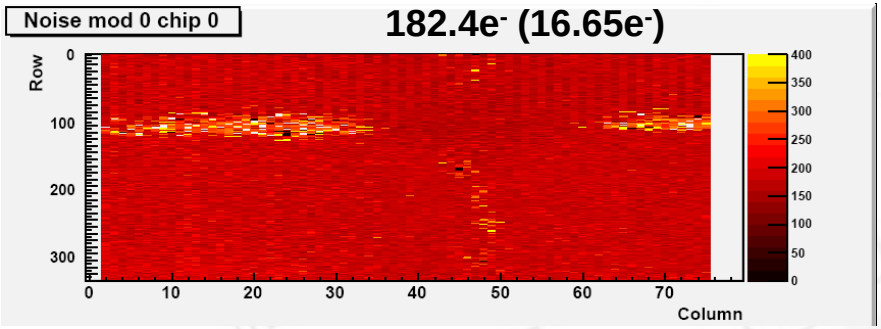
- Threshold map
  - Target threshold: 3000e-





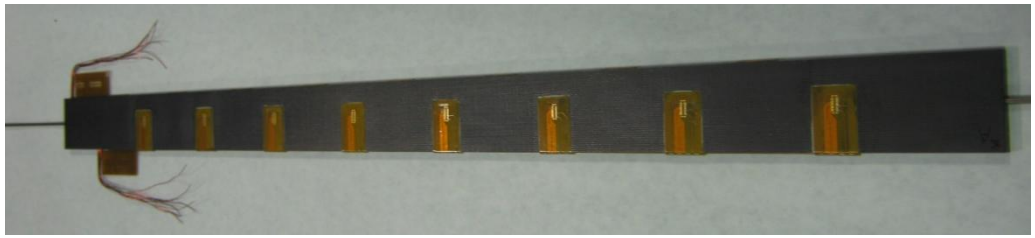
- Noise
  - Noise increases but values are still within the noise dispersion

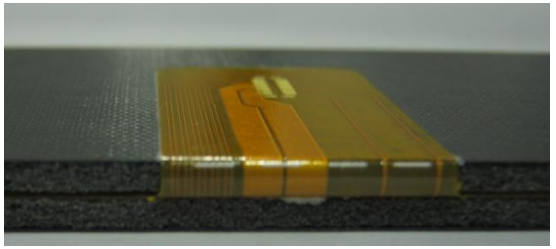




SP for pixels: next steps

Outer layer stave prototype with embedded cable

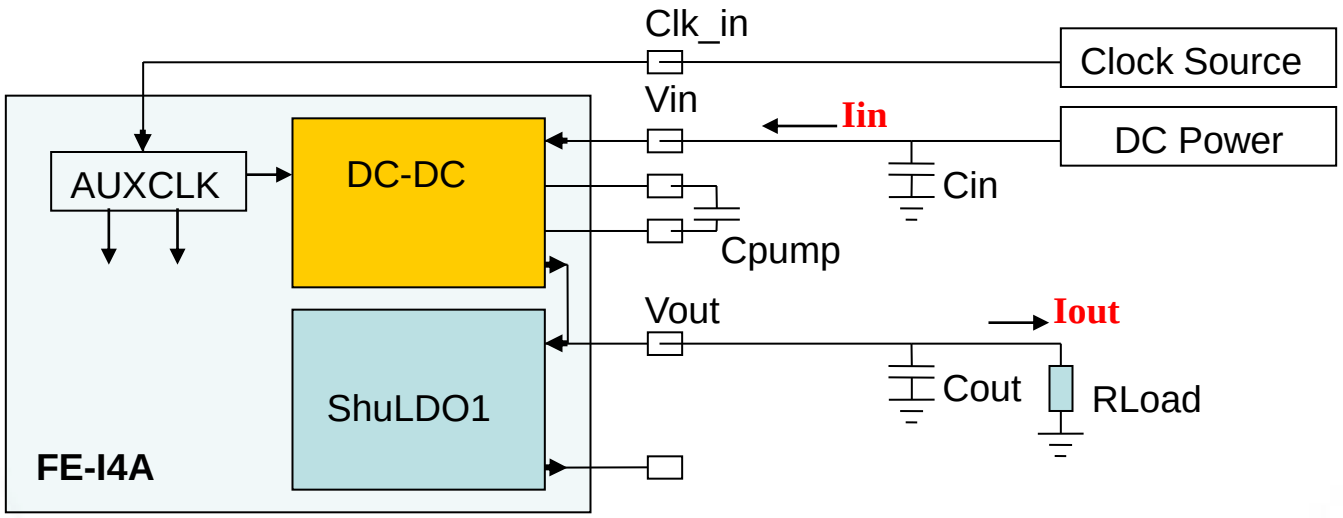




- Starting to prototype a pixel outer layer stave with serial powering
- Available mechanical structure with integrated SP cable
  - Multilayer Cu cable for signals and HV compatible with all powering scheme (LBNL)
  - Al layer for LV designed for SP (Bonn)
- SP chain = 8 modules
  - Defined by cable and stave layout of this prototype version
- 2-chip FE-I4A modules
- Possibly include current source and protection chip from the strips
- Readout: USBPix test setup for 2-chip modules

DC-DC configuration in FE-I4

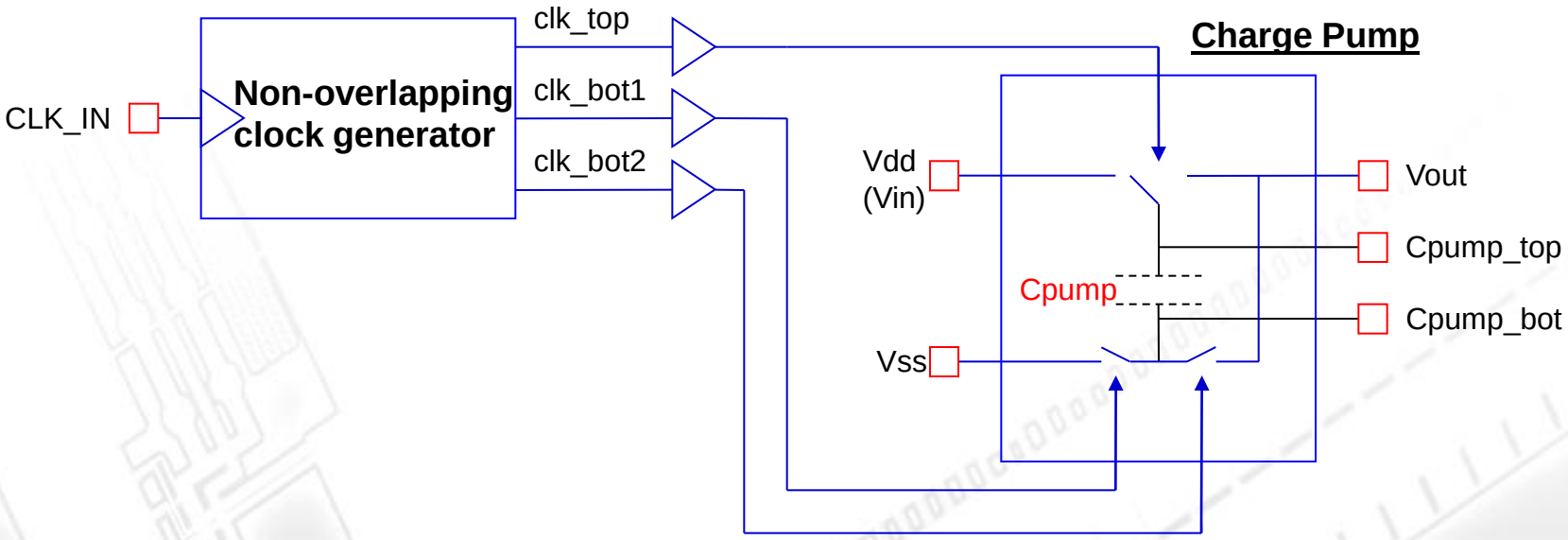
R&D on on-chip DC-DC converters is done at LBNL.



- CLOLK is provided from outside the chip. This clock also serves as auxiliary clock for the chip
- Ceramic capacitors used for the test. Cpump is mounted on the board as close to the chip as possible
- DCDC_OUT and ShuLDO1_IN are connected in the chip and share the same pad
- As a "devide-by-two" converter, ideally: Iout=2Iin & Vout=Vin/2

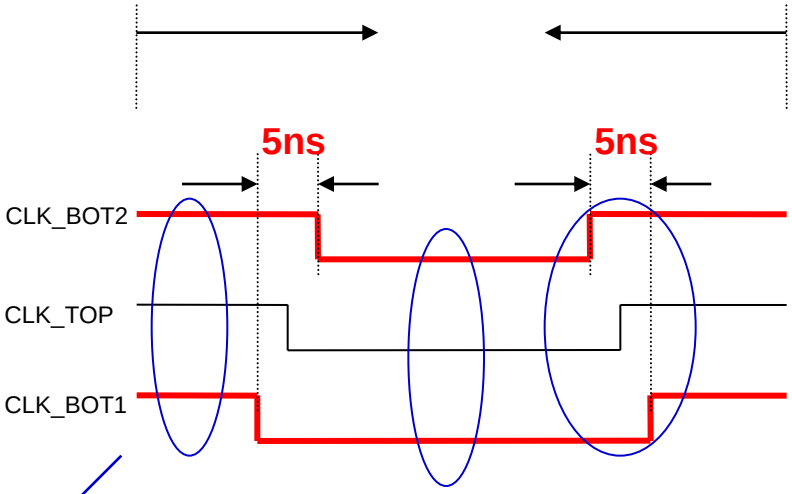
DC-DC circuit in FE-I4A

- Non-overpapping Clock generator:
  - generates 3 internal clock signals from CLK_IN
  - the same frequency but different phase
- Charge pump:
  - consists of 4 transistors working as switches
  - manipulates the pump capacitor under control of clock signals

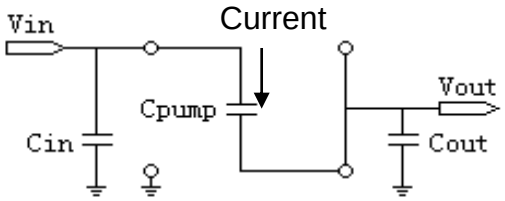


Non-overlapping clocks

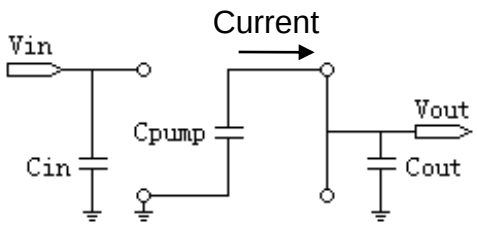
- 5ns gap between CLK_BOT1 and CLK_BOT2 to eliminate adverse discharging.



During transition, need these gaps to guarantee correct sequence of switching.

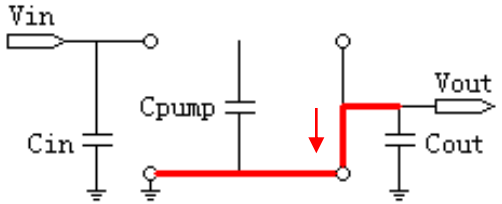


Charge Phase



Discharge Phase

No Good!
Avoid it!



Adverse discharging

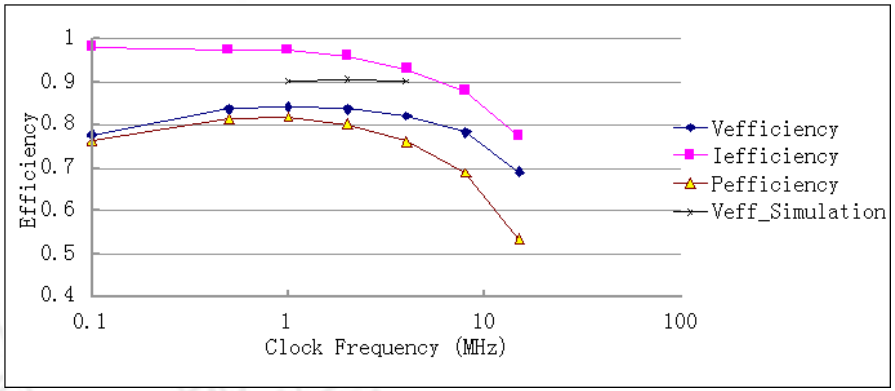
Test results

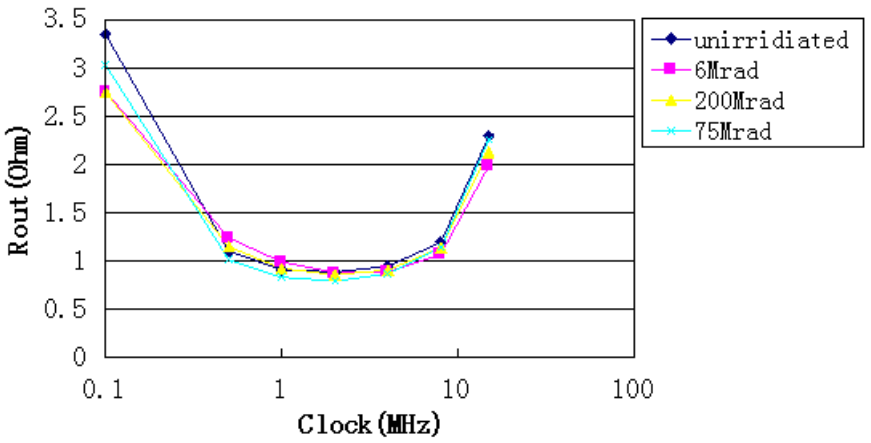
Efficiency vs Clock frequency

- Simulation result shows Vefficiency around 90%, while the test result shows Vefficiency of about 84% (Schematic simulation).
  - Post-layout simulation probably will give us different numbers.
- 1MHz is the optimal frequency for this tested chip.

Rout on irradiated chips

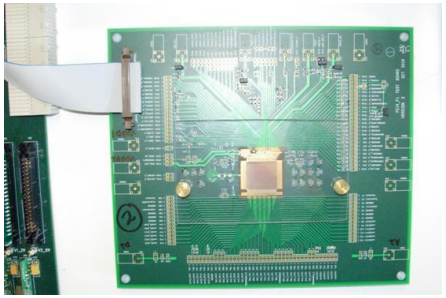
- 3 chips irridiated in Los Alamos last Dec. with different dose.
- The DC-DC seem immune to irradiation.
- 3.3V thick oxide transistors were used in the DC-DC design, while in commercial chips this kind of transistors are normally used in I/O circuit. This is the first measurement showing their radiation-hardness property.

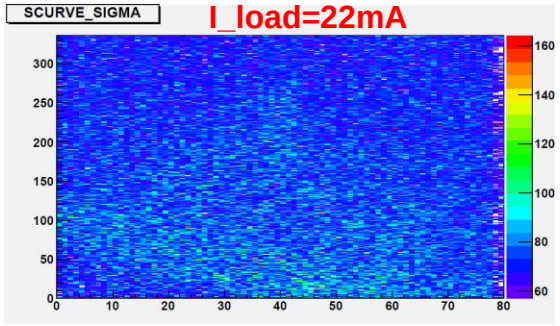


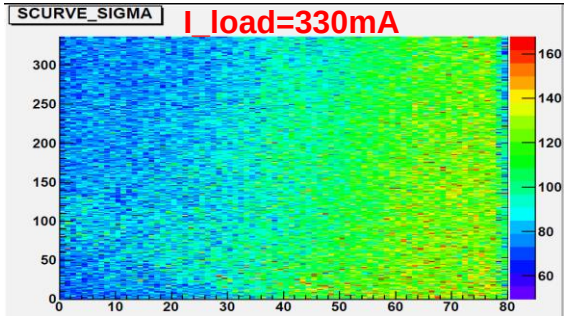


DC-DC induced noise

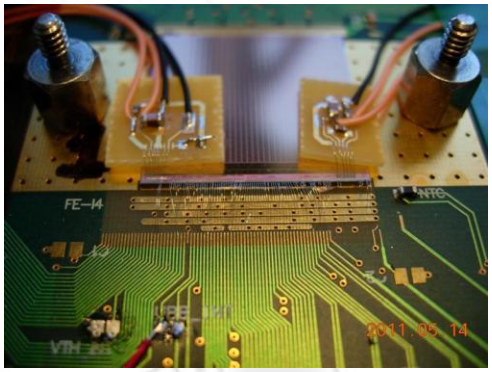
- Noise increased as long as DC-DC running even without using it to power the chip
  - Noise depends on DC-DC current

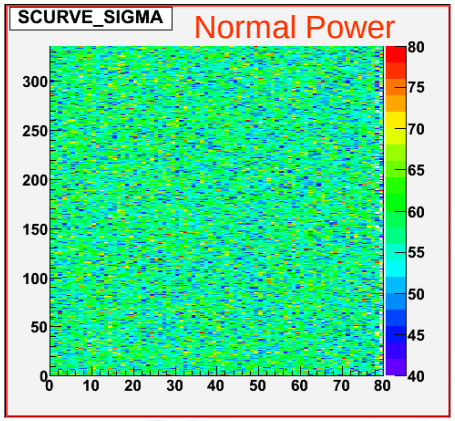


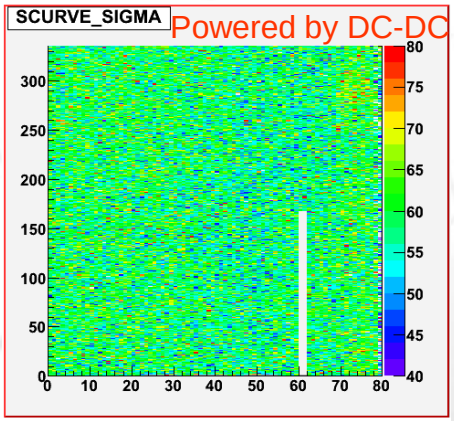




- Problem investigated changing the DC-DC external configuration
- The noise increased only slightly
- Noise does not seem to be intrinsic in the design → more investigations needed

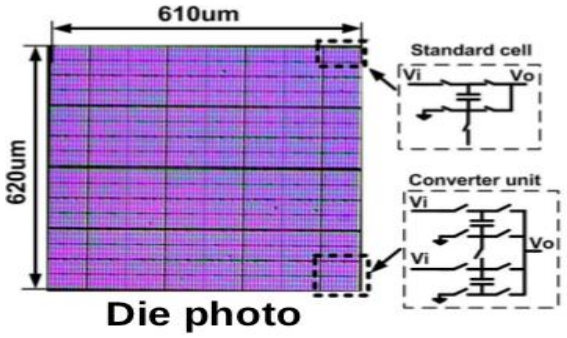






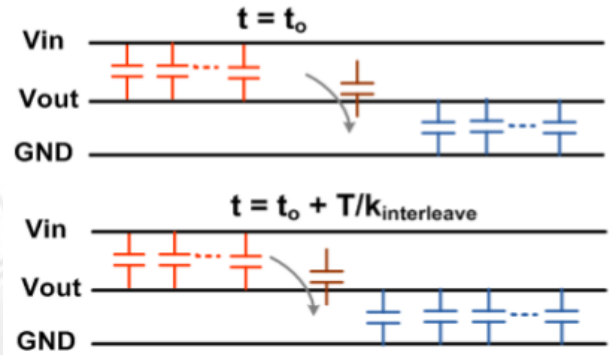
DC-DC conversion for pixels: next steps

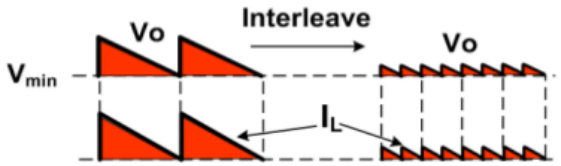
- The simple converter in FE-I4A is a good proof of principle
- For a real application follow R&D being done for industry using interleaved phase designs with on-chip capacitors (no external components). This will likely be investigated in 65nm pixel chip prototypes, and possibly also in the 130nm ABC strip readout chip



- **Flying cap: MOS, 32-way interleaved**
- **Supports 0.6V ~ 1.2V from 2V input**

Multi-Phase Interleaving





See: H.-P. Le, et al. "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," IEEE Journal of Solid-State Circuits, Sept. 2011.

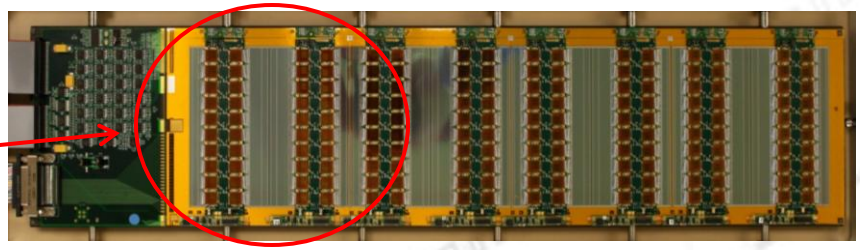
Strips R&D on powering (1)

All material shown on strips is taken from "ATLAS Strip Tracker Stavelets", P. Phillips, TWEPP, Vienna, September 26-30 2011

- Stavelets are being prototyped and tested with both serial powering and DC-DC conversion with up to 4 modules
- Module
  - One Sensor
  - Two Kapton Hybrids
  - Each Hybrid has 20 ABCN-25 ASICs
    - 250nm prototype of strips FE chip, ABCN-130 (130nm)

- Main difference wrt pixels is that regulators/converters can be external

module



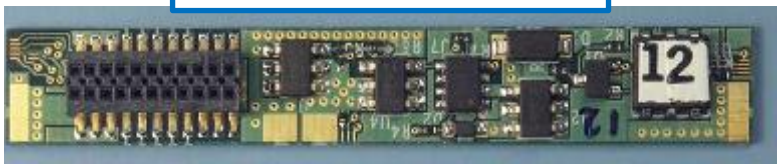
Strips R&D on powering (2)

- Serial powering
  - Integrated and external shunt circuitry
  - Custom Current Source
  - Power protection board
- DC-DC conversion
  - Buck converter developed by the microelectronics CERN group
  - Peak power requirement of one 20 chip ABCN-25 hybrid exceeds capability of AMIS series rated for 130nm designs
  - Dedicated DC-DC module provided by the CERN group based on commercial chip

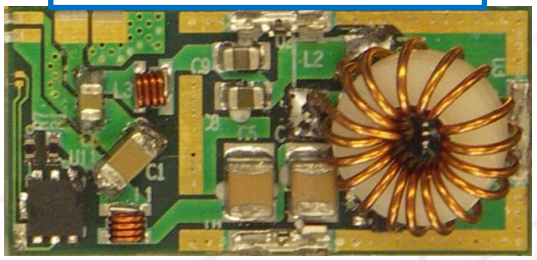
M-shunt plugin

Custom Current Source

Power Protection Board

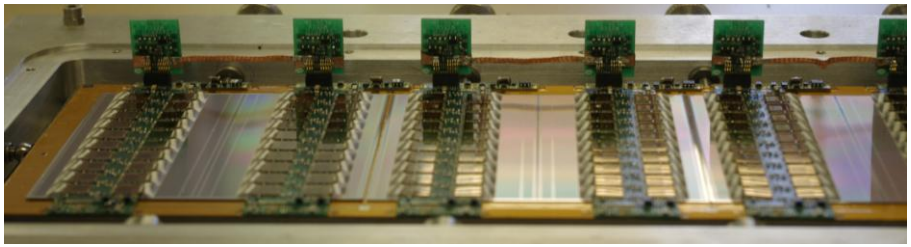


DC-DC converter board



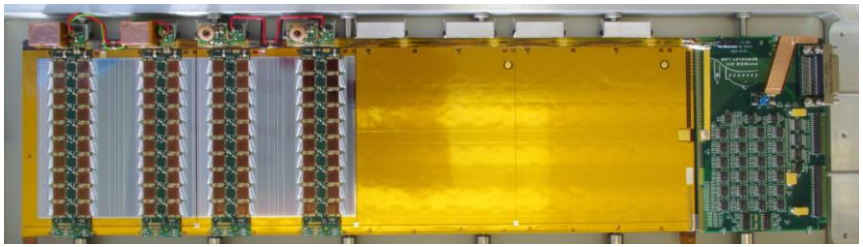
Strips R&D on powering (3)

- SP stavelet fitted with 4 single sided short strip silicon detector modules



- System functionality successfully demonstrated: bypass system, custom current source
- Initial ENC results close to expectation
- Detailed investigation of susceptibility to noise signals correlated with readout activity (DTN)
- Next: Submission of a Serial Power & Protection (SPP) Chip, work continues to determine the best balance of performance

- DC-DC stavelet fitted with 2 single sided short strip silicon detector modules



- Different hookup configurations tried to achieve reasonable performance
- Different shielding thicknesses investigated
- Next: add more modules

- Similar ENC values for both schemes
- Slightly better DTN performance for DC-DC, but both acceptable

To date, either technology would be a viable powering solution for the ATLAS short strip tracker

Conclusion

- R&D activities on powering schemes including serial power and DC-DC conversion are well advanced for both pixels and strips in view of upgrades for high luminosity in ATLAS
- Serial powering
  - Regulators prototyped
  - Concept extensively proved at system level from both pixels and strips
- DC-DC conversion
  - Converter working principle demonstrated for both external buck converter (CERN group) and integrated switch capacitor DC-DC converter (LBNL)
  - System test started with external DC-DC buck converter (strips)

- <u>Pixels future plans:</u>
  - Serial power is the only realistic option with FE-I4 → likely to be chosen option for a staged installation in 2018
  - On chip DC-DC conversion expected to be a strong competitor in next generation of FE chip (65nm) → later upgrades (>2020)
  - Plan: prototype with SP with FE-I4 based modules and if next generation FE with DC-DC converter is developed in time for 2018 decide at that point