HHA 2011

The future of pixel detectors

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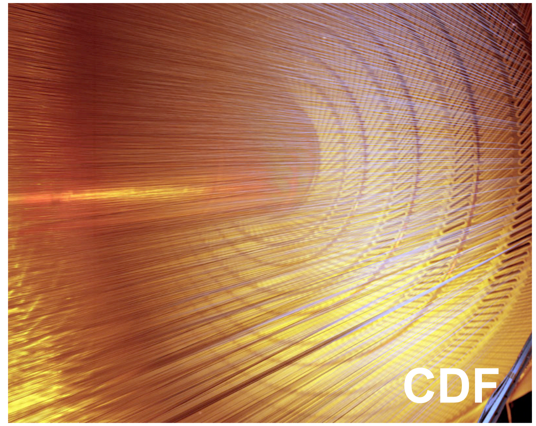
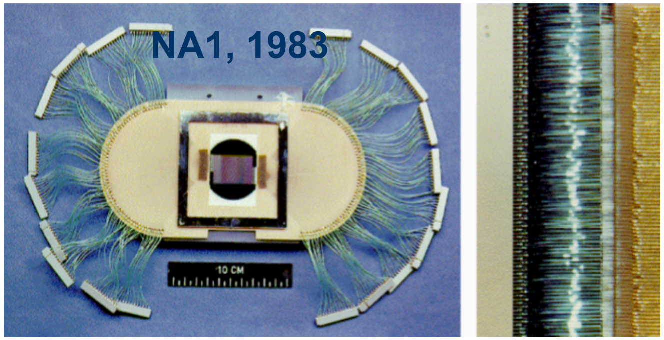
One slide on "the past"

wire chambers

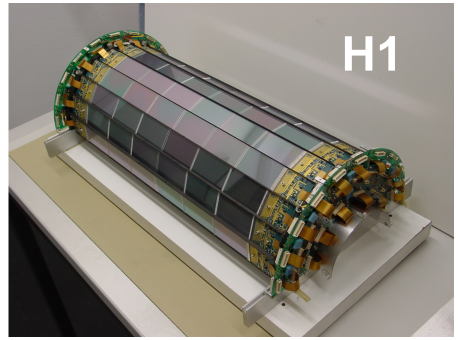
→ electronic recording of particle tracks

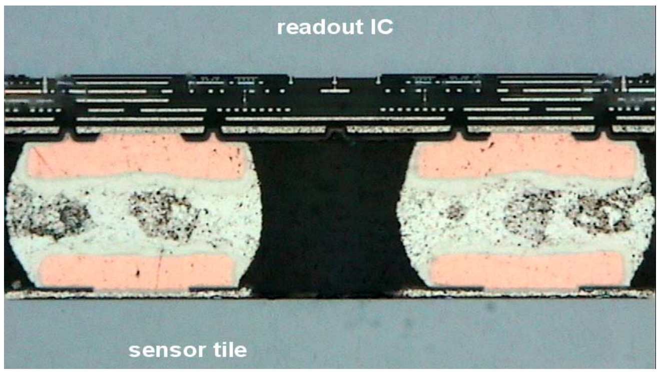




silicon strip detectors

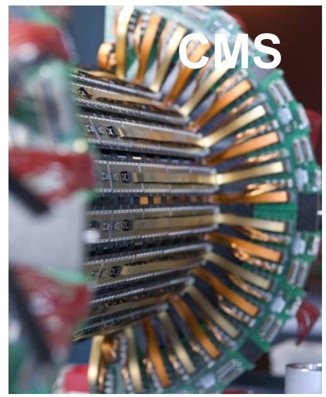
→ measurement of ps – lifetimes and decay vertices

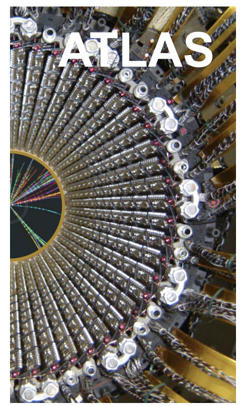




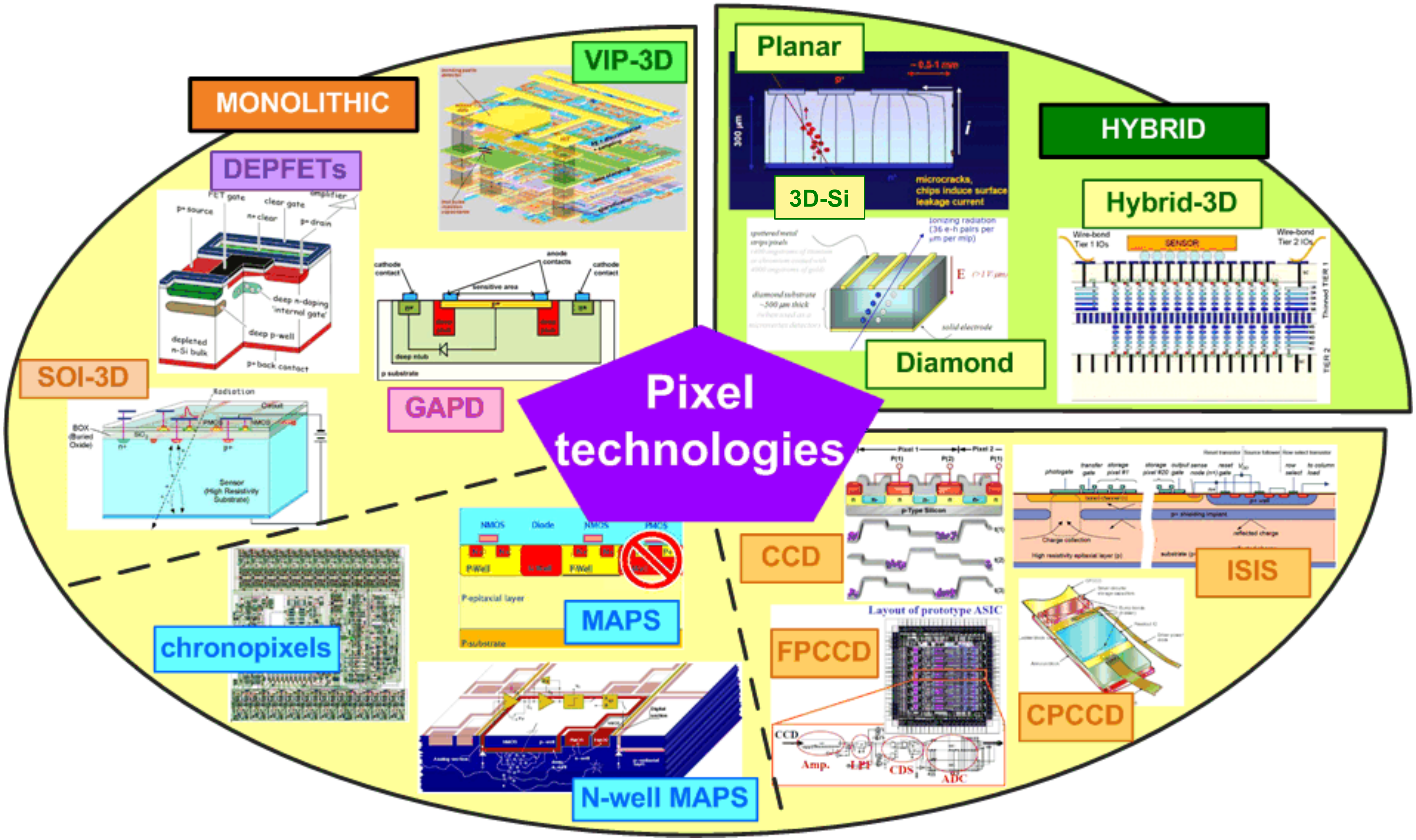
pixel detectors

→ point measurement (3D) in high rate environments like LHC



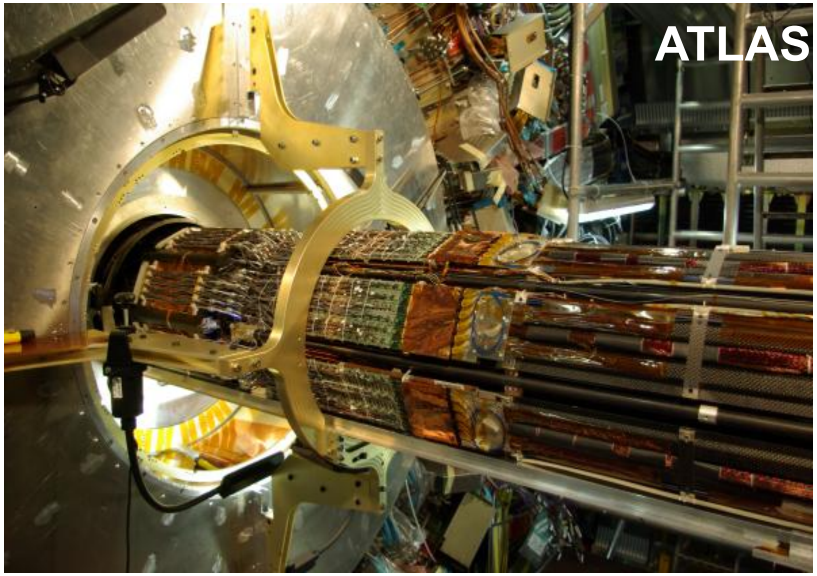


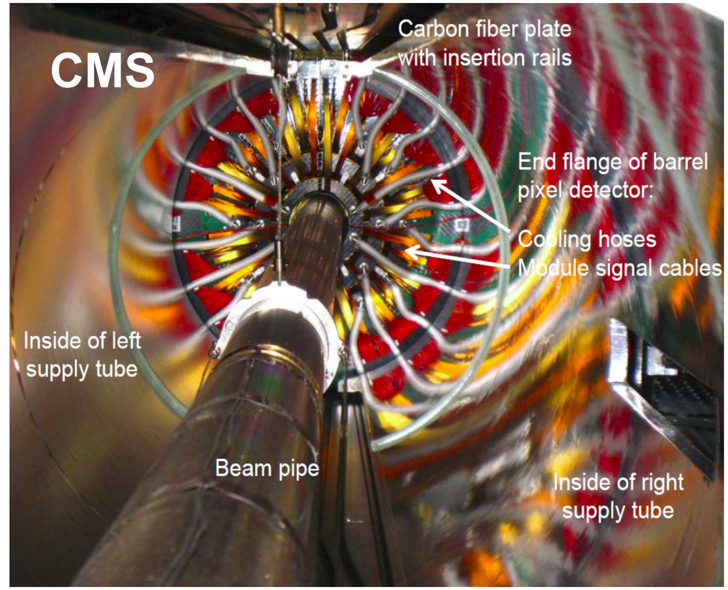
The variety of pixel technologies



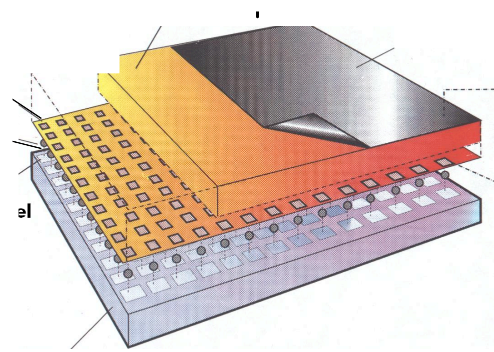
The combination of high resolution, low mass and low power is a substantial challenge

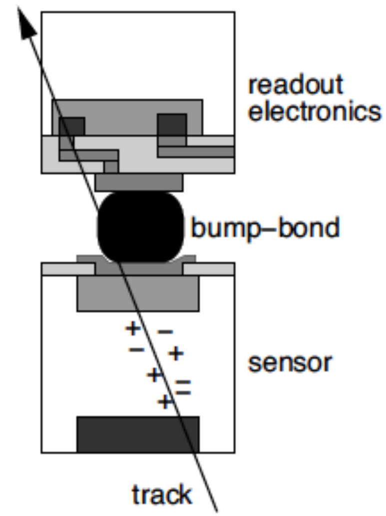
Today's "state of the art" of running detectors





all based on
"Hybrid Pixel Detectors"





Rate and radiation challenges at the innermost pixel layer

Hybrid Pixels

	BX time	Particle Rate	Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	kGy per lifetime*
LHC (10^{34} $cm^{-2}s^{-1}$)	25	1000	1.0×10^{15}	790
sLHC (10^{35} $cm^{-2}s^{-1}$)	25	10000	10^{16}	5000
SuperBFs (10^{35} $cm^{-2}s^{-1}$)	2	400	$\sim 3 \times 10^{12}$	100
ILC (10^{34} $cm^{-2}s^{-1}$)	350	250	10^{12}	4
RHIC (8×10^{27} $cm^{-2}s^{-1}$)	110	3,8	1.5×10^{13}	8

Monolithic Pixels

- **lower rates**
- **lower radiation**
- **smaller pixels**
- **less material**

assumed lifetimes:
LHC, sLHC: 7 years
ILC: 10 years
others: 5 years

An experimentalist's dream

- good S/N
- µm space resolution
- ~ns time resolution
- > 10 MHz / mm^2 rate capability
- radiation hard to 5 MGy
- radiation length per layer < 0.2% x/X_0
- all in one monolithic pixel "chip"

Reality

hybrid pixels

- good S/N — ✓ (fully) depleted
- µm space resolution — ➢ ~10 µm
- ~ns time resolution — ✓ obtained at LHC
- > 10 MHz / mm^2 rate capability — ✓ tbd for sLHC
- radiation hard to 5 MGy — ✓ tbd for sLHC
- radiation length per layer < 0.2% x/X_0 — ➢ 3.5%
- all in one monolithic pixel "chip" — ➢ no, hybrid

Reality

MAPS/DEPFET

• good S/N	➢ NO / YES
• µm space resolution	✓ 1 µm tough
• ~ns time resolution	➢ slow rolling shutter
• > 10 MHz / mm^2 rate capability	➢ < 0.4 MHz/mm^2
• radiation hard to 5 MGy	➢ < 100 kGy
• radiation length per layer < 0.2% x/X_0	✓ but tough
• all in one monolithic pixel “chip”	○ not quite

Direction for the “future” = a late outline of the talk

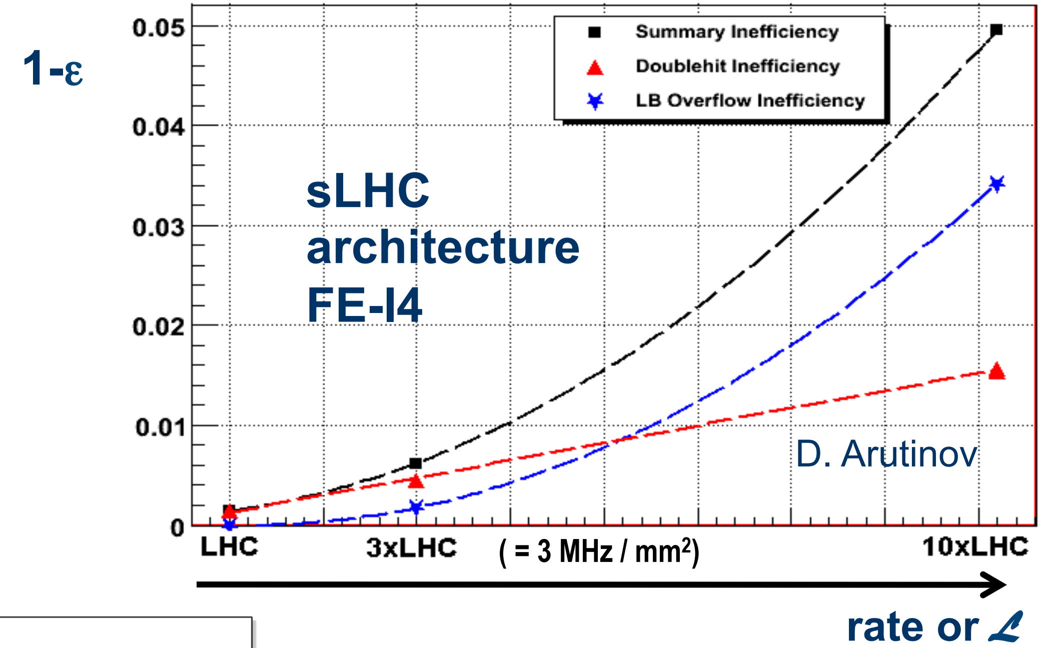
- Hybrid pixels for sLHC
  - better ICs -> pixel size and bandwidth
  - radiation hard sensors
- DEPFET/MAPS
  - thin
  - towards truly monolithic CMOS
- 3D Integration
  - vias first
  - vias last

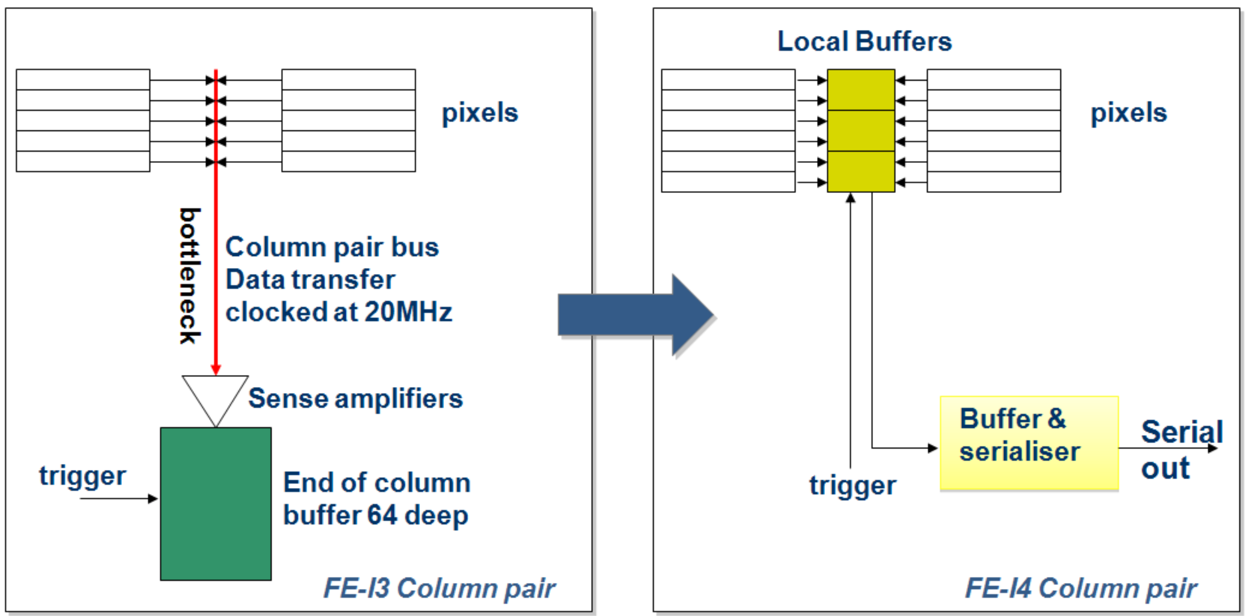
sLHC data rates

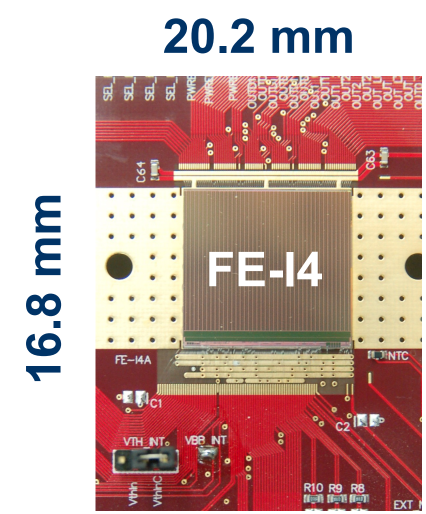
Hit inefficiency rises steeply with the hit rate

Bottleneck: congestion in double column readout

⇒more local in-pixel storage (130 nm !)
>99% of hits are not triggered
⇒ don't move them -> not blocking





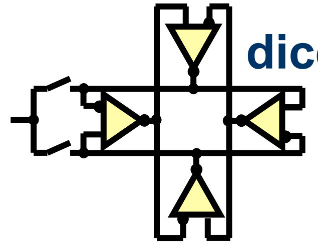


Bonn
CPPM
Genova
LBNL
NIKHEF

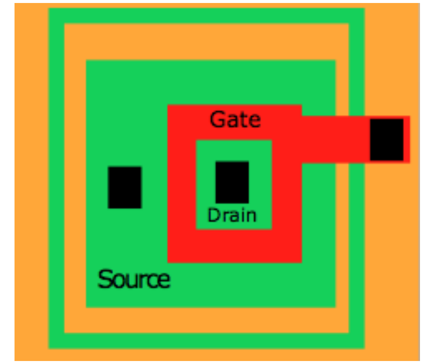
Radiation hardness to sLHC fluences $\gg 10^{15}$ cm^{-2}

❑ Chips are radhard … provided that …

- ❑ deep submicron technology used (130 nm -> 65 nm)
- ❑ “round” transistors at critical nodes
- ❑ SEU tolant digital logic is used



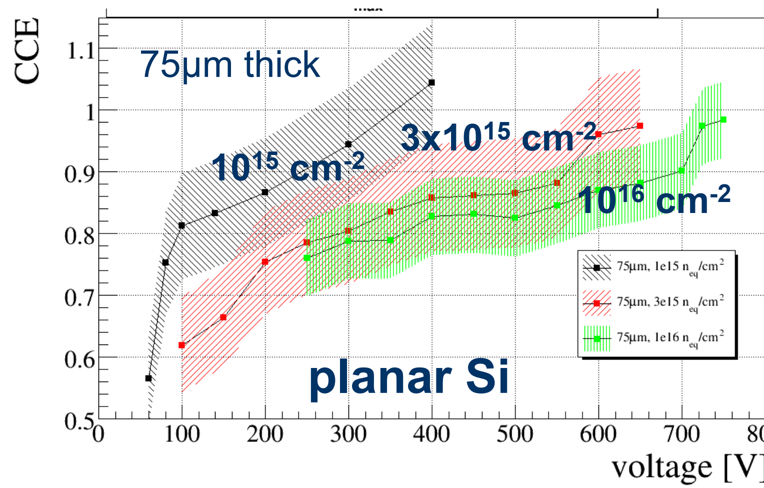
dice cell



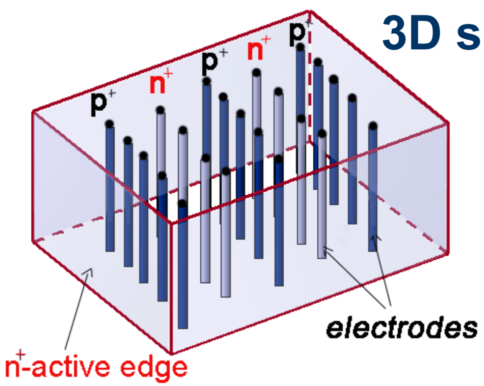
round FET

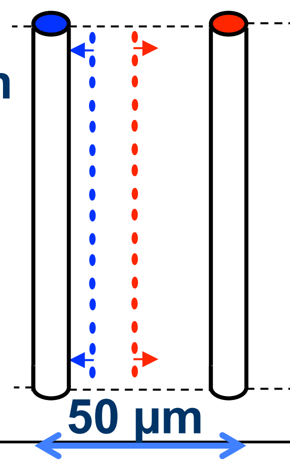
❑ Sensors are not radhard, unless …

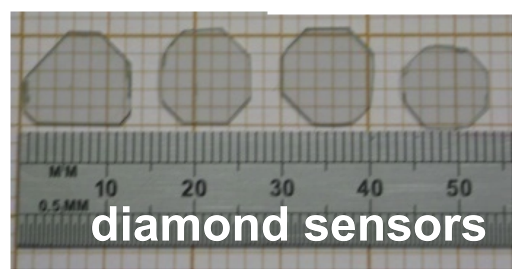
- ❑ high voltages are applied (planar Si)
- ❑ special geometries are used (3D-Si)
- ❑ intr. radhard materials are used (diamond)



3D silicon





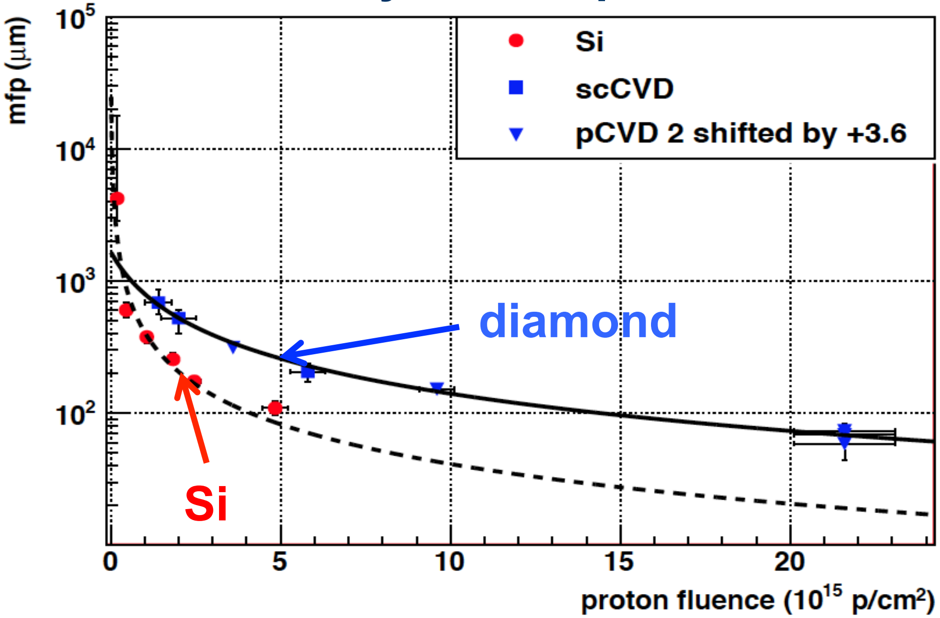


3D-Si and diamond are used as pixel modules in ATLAS IBL/DBM projects

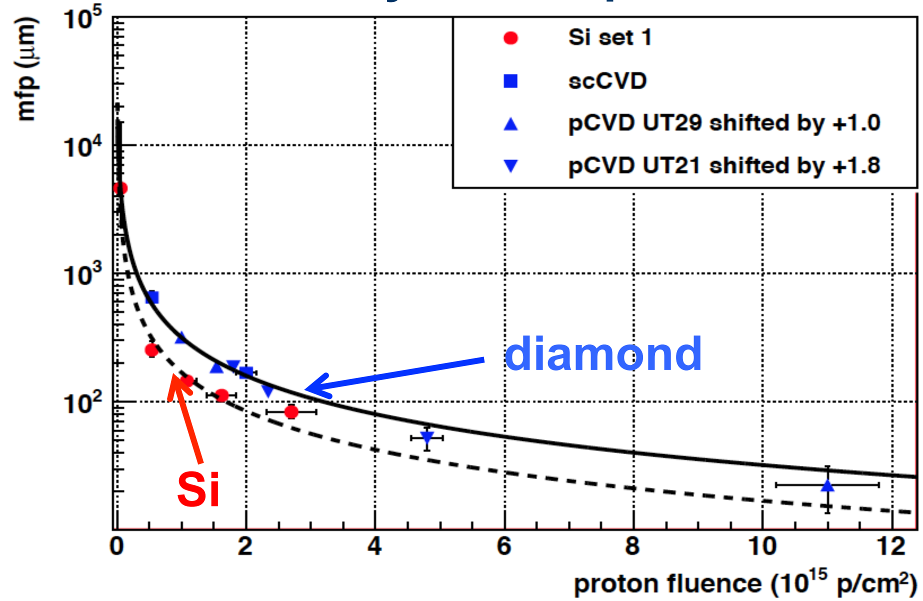
Radiation Damage: diamond versus silicon

carrier mean free path length … after irradiation: $$\frac{1}{\lambda} = \frac{1}{\lambda_0} + k\Phi$$

irrad. by 24 GeV protons



irrad. by 25 MeV protons



Reference: Silicon: A. Alfolder, IEEE Transactions on Nuclear Science, Vol. 56, No. 3, June 2009.

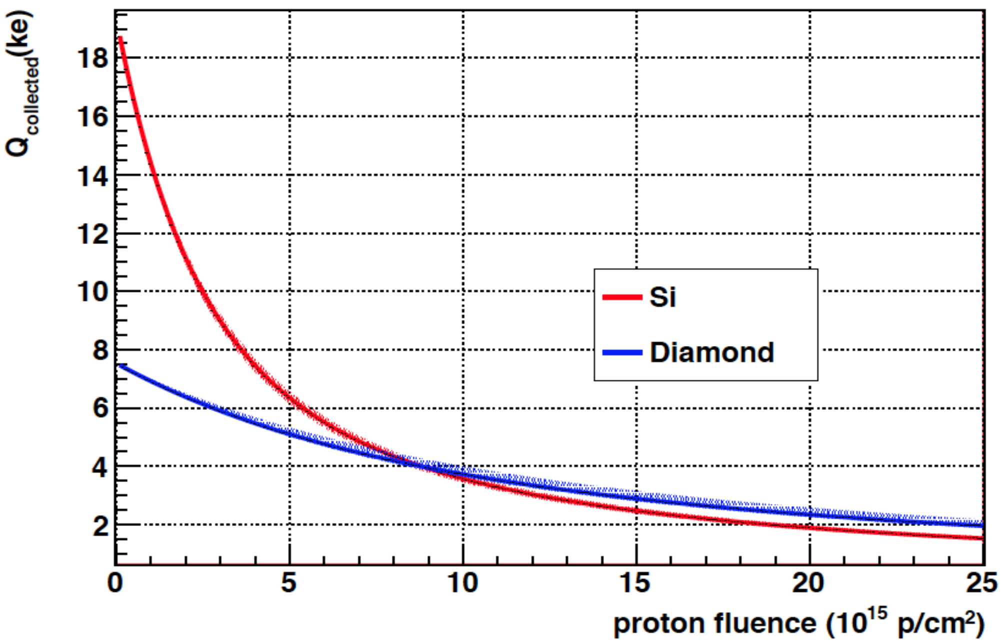
Reference: Silicon: (1)A. Alfolder, Nuclear Instruments and Methods in Physics Research A 612 (2010) 470–473. (2)G. Casse. Nuclear Instruments and Methods in Physics Research A 624 (2010) 401–404.

above fluences of ~10^{15} p/cm^{-2}
⇨ diamond is 2-3 x more radiation hard than silicon

Si, Diamond … signal after fluences > 10^{15} cm^{-2}

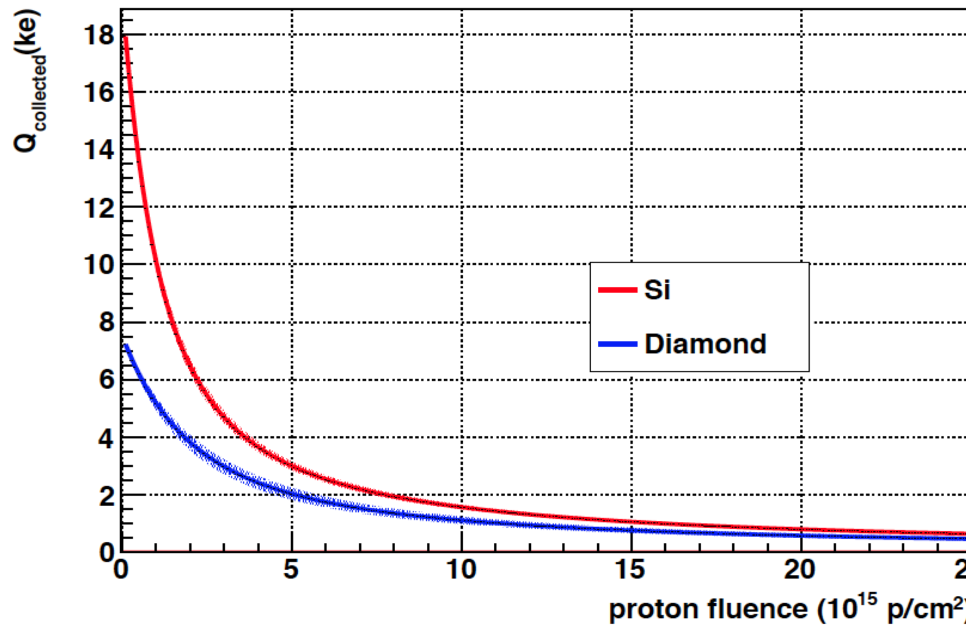
high energy

irradiation by 24 GeV protons



low energy

irradiation by 25 MeV protons

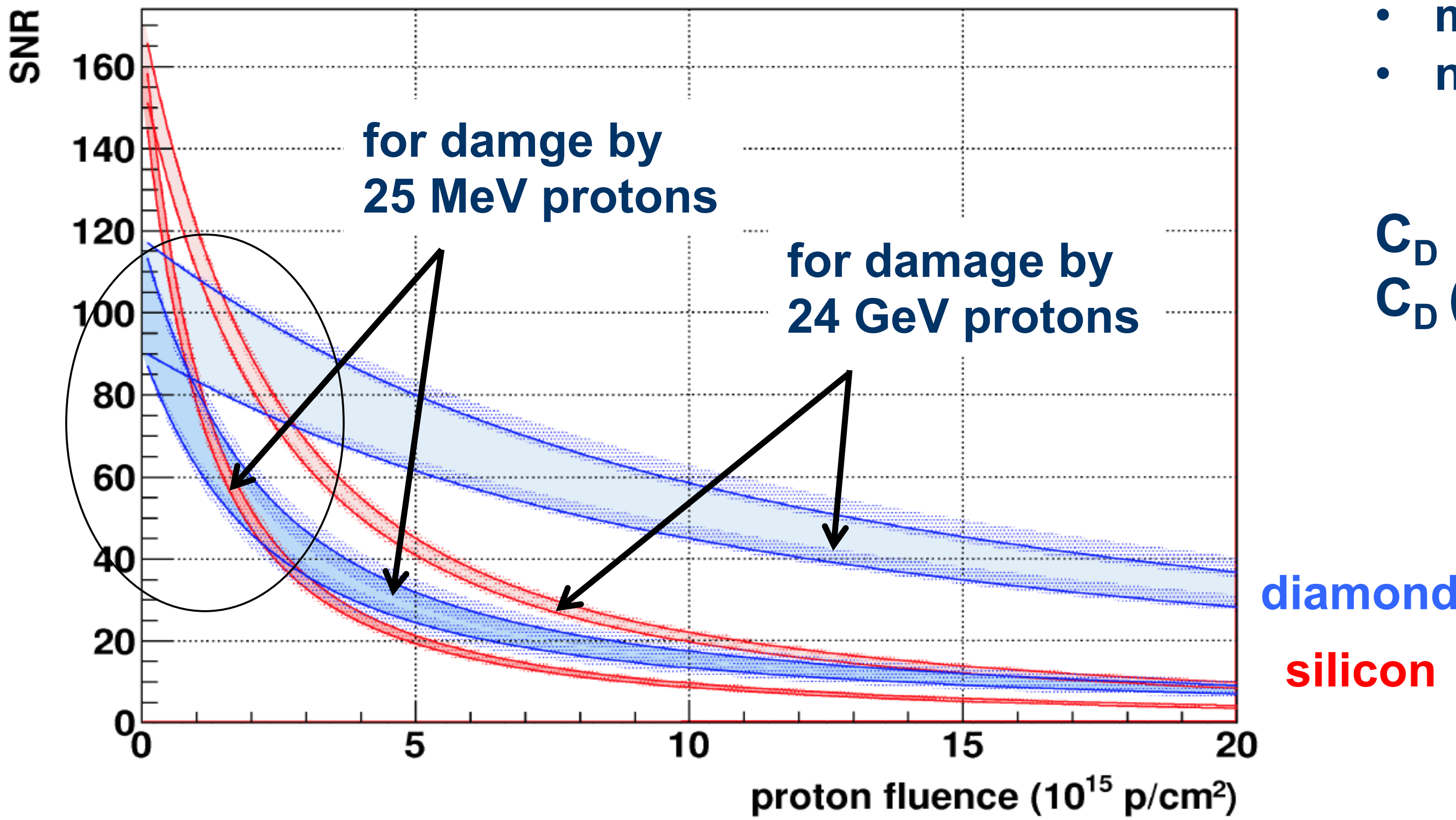


thickness = 200 µm

low energy damage is more severe than damage by high energy particles
but the damage constant ratio for Si/diamond is larger at high energies

Si, Diamond: Signal to Noise Ratio

thickness of sensors: 200 µm



advantage diamond
- **much smaller C_{in}**
- **no leak. current**

C_D (Si) = 140 fF
C_D (diam.) = 35 fF

measured (!)

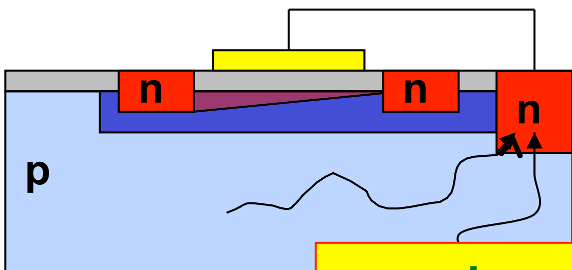
cross over around (1 – 2) x 10^{15} protons / cm²

(Semi)- Monolithic Detectors

+ **really low mass**
+ **(almost) no interconnection (but need few ASICS with large pitch > 150µm)**
– **slow (frame readout, rolling shutter)**

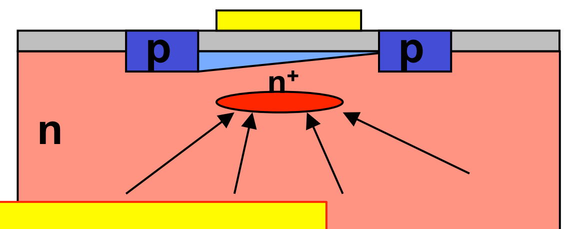
CMOS Sensors (MAPS) -> STAR
DSM CMOS with epi-layer as sensor

+ ‘standard CMOS’ process
+ CMOS circuitry, but limited to NMOS
– small signal, slow collection
– area limited by chip size



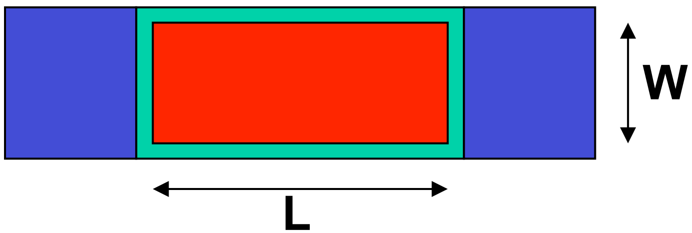
DEPFET -> Belle II
FET on fully depleted bulk

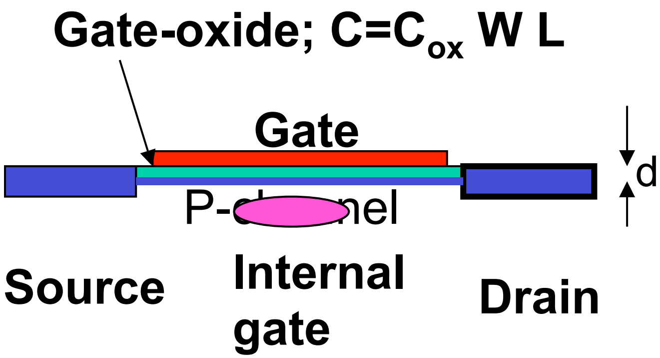
– non standard double-sided process
– simple, one stage amplifier
+ large signal, fast collection
+ wafer size sensors possible



+ **no bump bonding**
+ **very thin (50 µm resp. 75 µm) → ~0.2% x/X_0**
+ **small pixels (20x20 resp. 50x75 µm^2)**
+ **low power → less cooling**
– **radiation hardness**
– **R/O speed**

How does a DEPFET work?





A charge q in the internal gate induces a **mirror charge** αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha q / C = \alpha q / (C_{ox} W L)$ which in turn **changes the transistor current I_d** .

FET in saturation:

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right)^2$$

I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

Conversion factor:

$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3WC_{ox}}}$$

q

$$g_m : \boxed{g_q = \alpha\frac{g_m}{WLC_{ox}} = \alpha\frac{g_m}{C}}$$

DEPFET

Each pixel is a p-channel FET on a fully depleted bulk

A deep n-implant creates a potential minimum for electrons under the gate ("internal gate")

Signal electrons accumulate in the internal gate and modulate the transistor current (g_q ~ 400 pA/e$^-$)

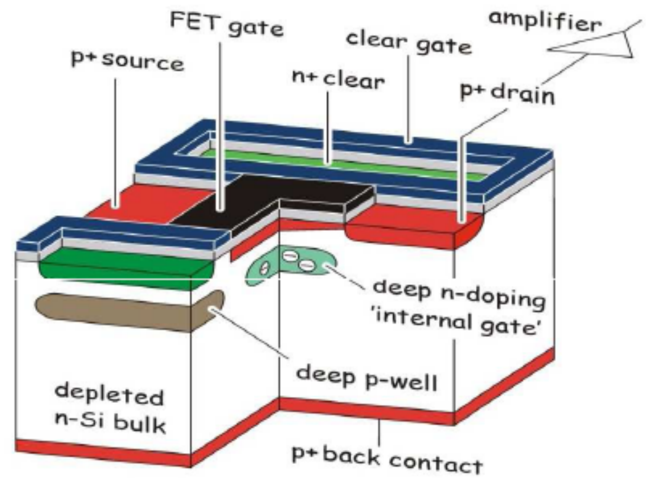
Accumulated charge can be removed by a clear contact

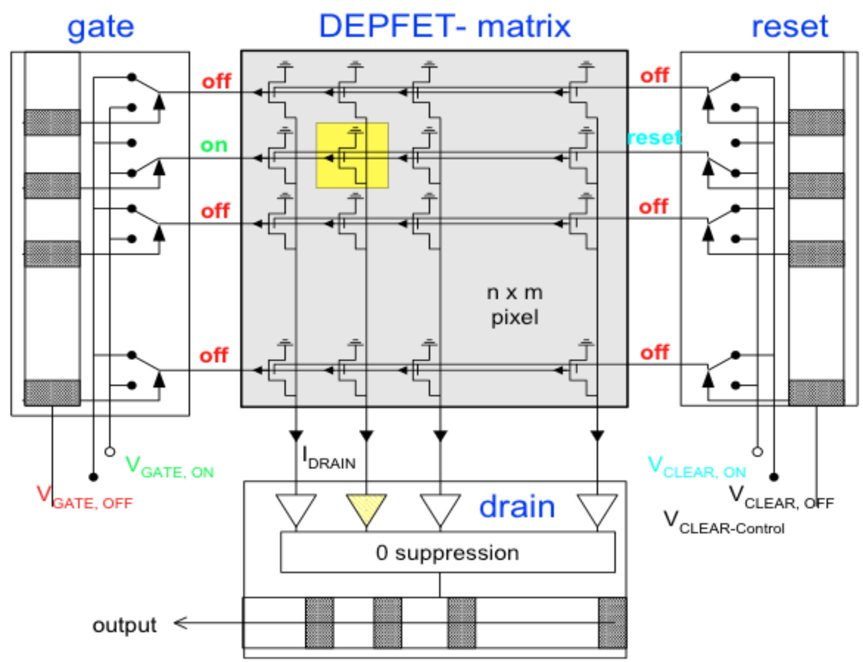
Fully depleted ⇒ large signal, fast signal collection

Low capacitance, internal amplification: => low noise

High S/N even for thin sensors (75 μm)

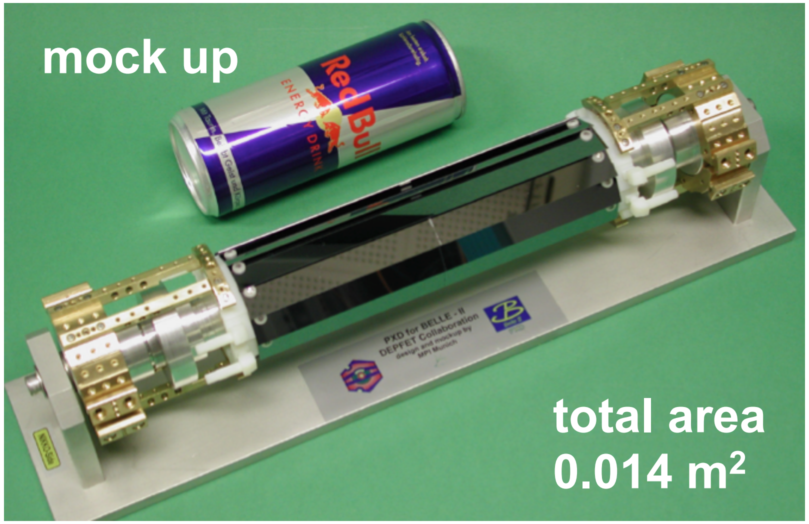
Rolling shutter mode (col. parallel) for matrix operation
⇒ 20 μs frame readout time
⇒ Low power (only few lines powered)



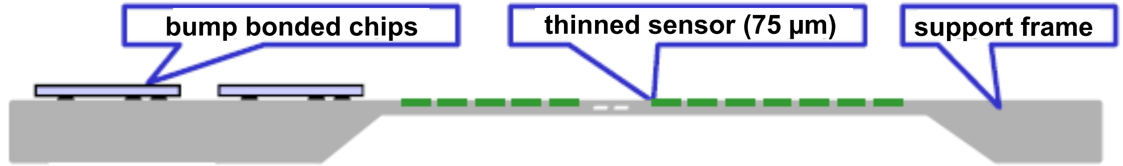


DEPFET PXD @ Belle II @ SuperKEKB

2-layer pixel vertex detector (PXD)

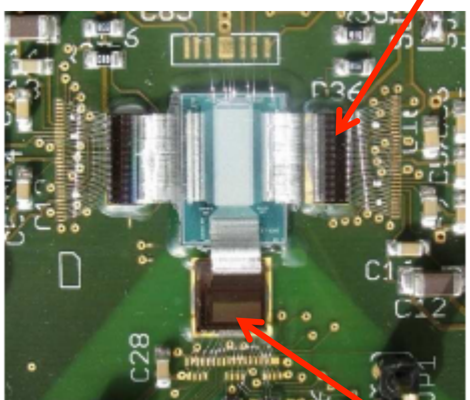


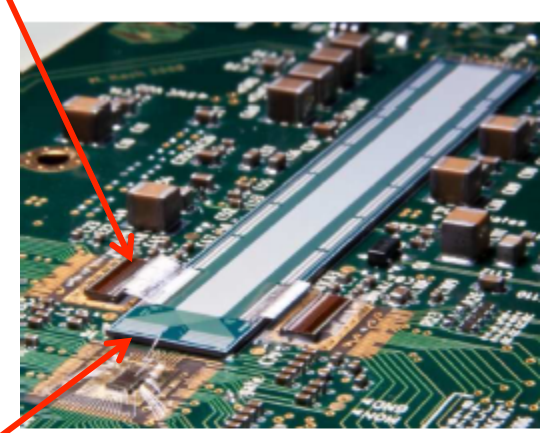
thinned by backside etching, leaving a frame

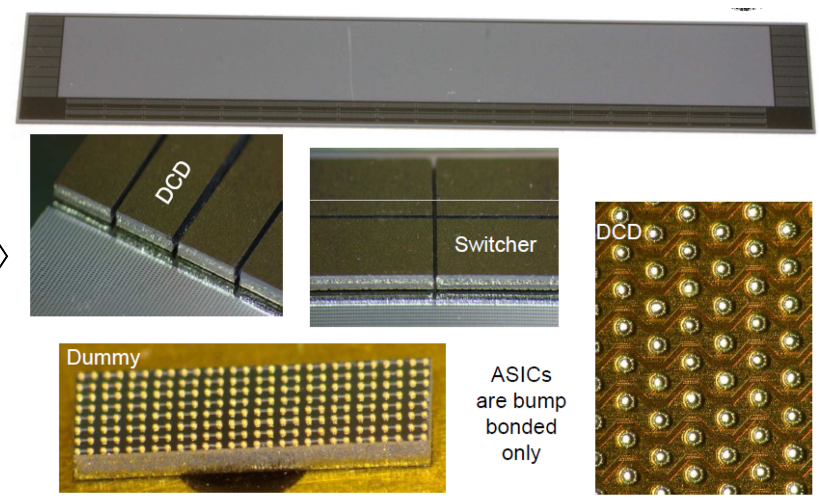


…. on their way to the final module
sensor + switcher + DCD + DHP

ladder control ICs







R/O ICs

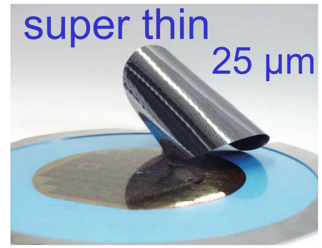
Monolithic Pixel Sensors … an attempt of a sorting (1)

❑ MAPS = Monolithic Active Pixel Sensor

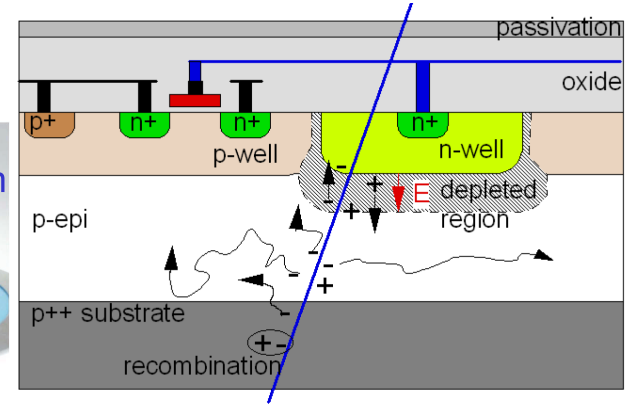
use thick epi-Si layer in some CMOS processes for sensing

- (1) Q - collection by diffusion (small, slow)
  (2) only nMOST in active area, no pMOST
  (3) not radhard

can be made super thin

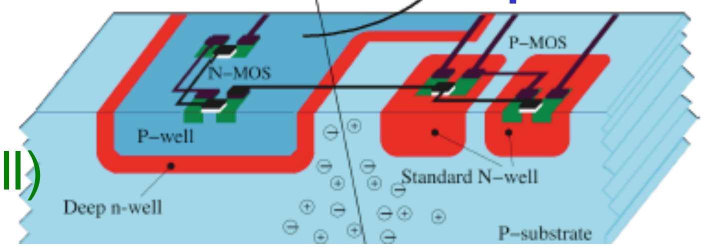


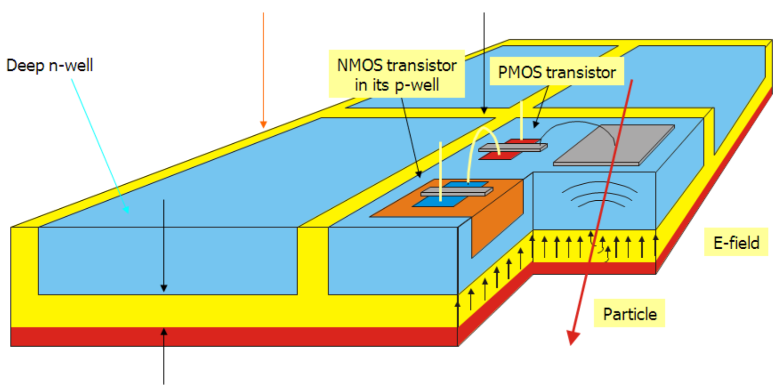
→ STAR @ RHIC



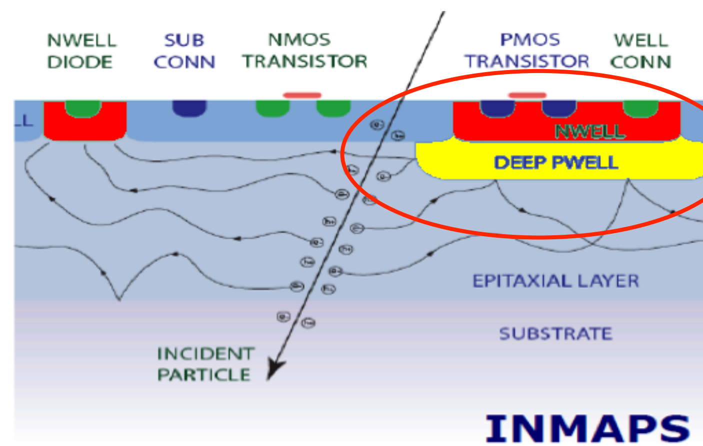
- several developments to improve (1),(2)
  - ➢ large deep n-well, pMOST on the side (65nm)
  - ➢ shield PMOS-nwell by a pwell (quadrupel well)
  - ➢ higher bulk resistance (-> depletion -> better Q-coll)
- developments to improve (1),(2),(3)
  - ➢ HV CMOS (AMS 350 nm -> 180 nm)

→ SuperB





I. Peric

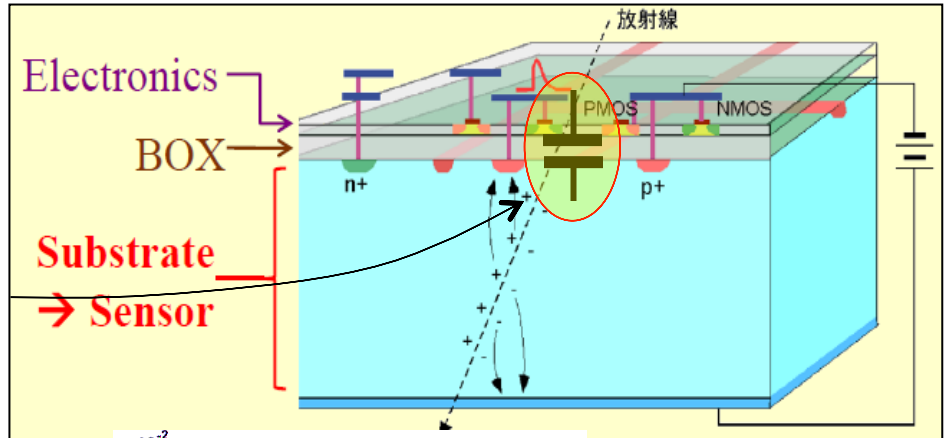


Monolithic Pixel Sensors … an attempt of a sorting (2)

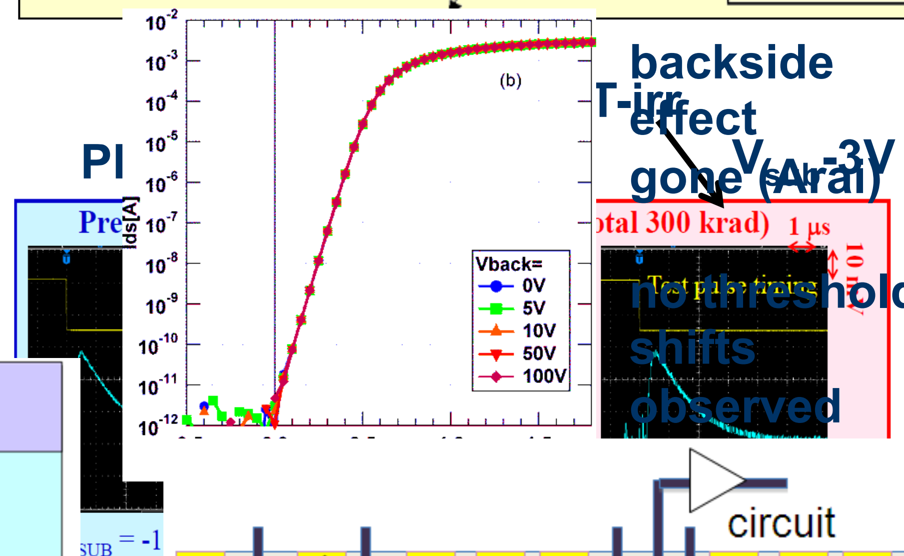
❑ SOI pixels (Silicon On Insulator)

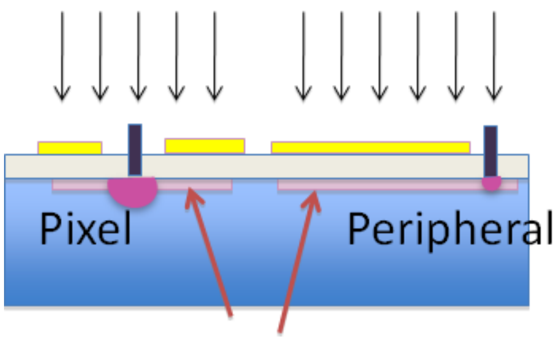
use depleted bulk for Q-collection coupled into CMOS layes separated from bulk by a thick buried oxide (BOX) layer (OKI, Japan)

- backgate effect “BOX is a capacitance”
- on irradiation holes are trapped in BOX

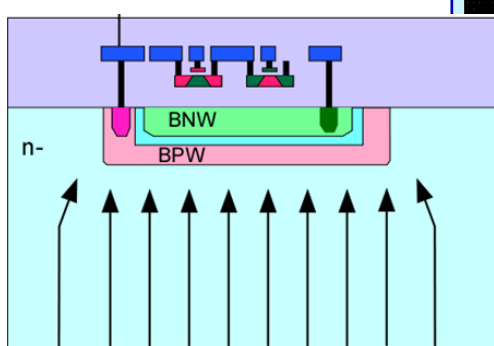


- several attempts to improve this
  - buried p-wells
  - nested wells
  - “double SOI” structures

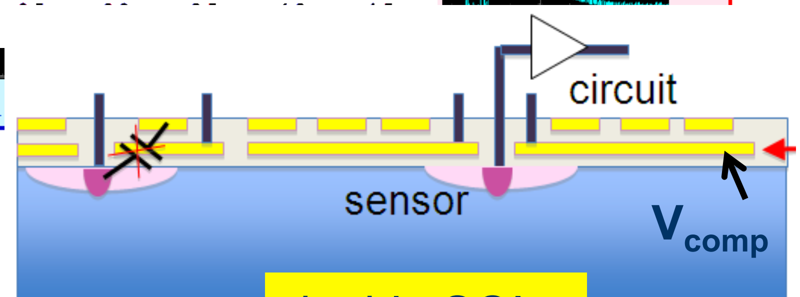




buried p-wells

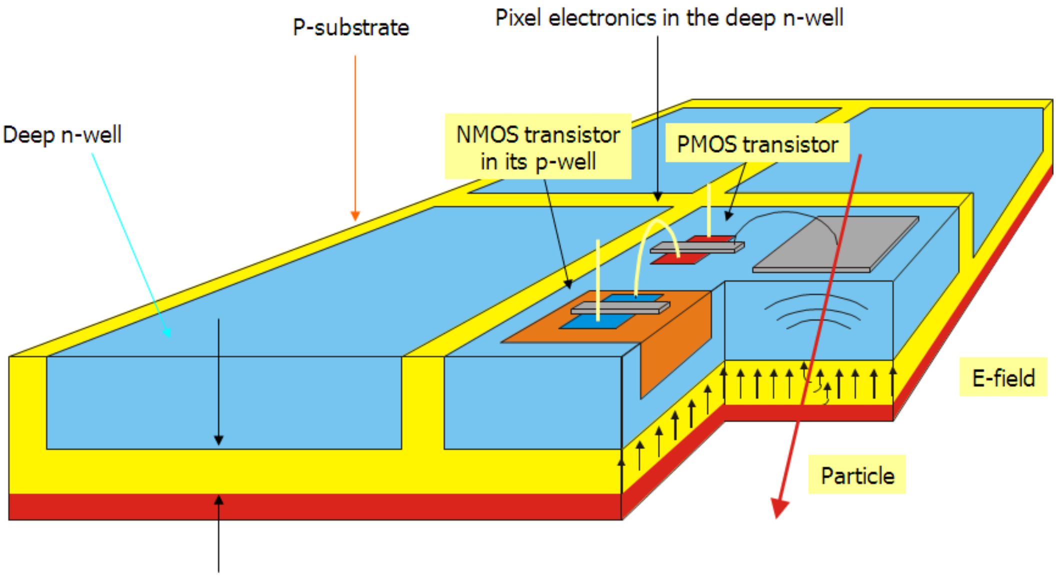


nested wells



double SOI

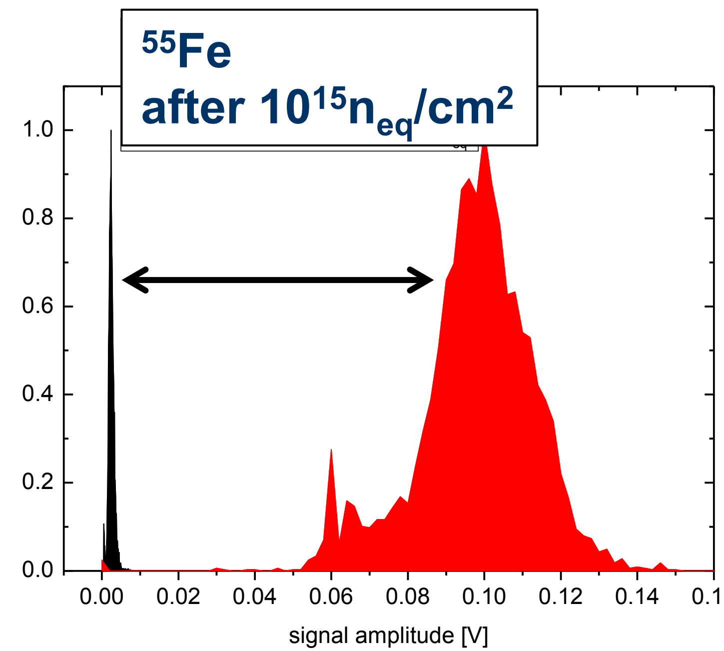
MAPS in HV technology



Ivan Peric, HD

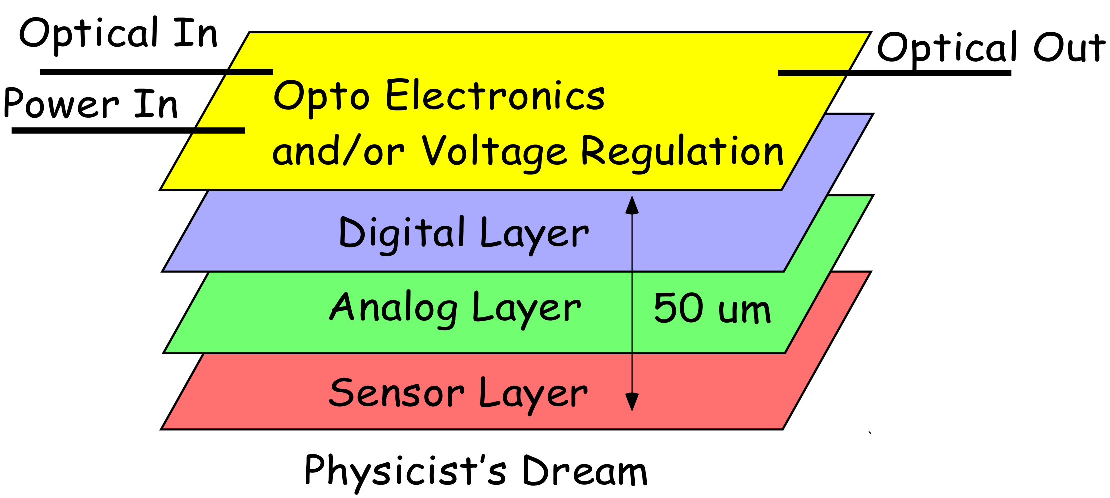
- all electronics in same deep n-well (triple well), which also collects Q
- Q-coll. in depl. volume by drift in E
- 350 nm AMS -> 180 nm IBM/AMS

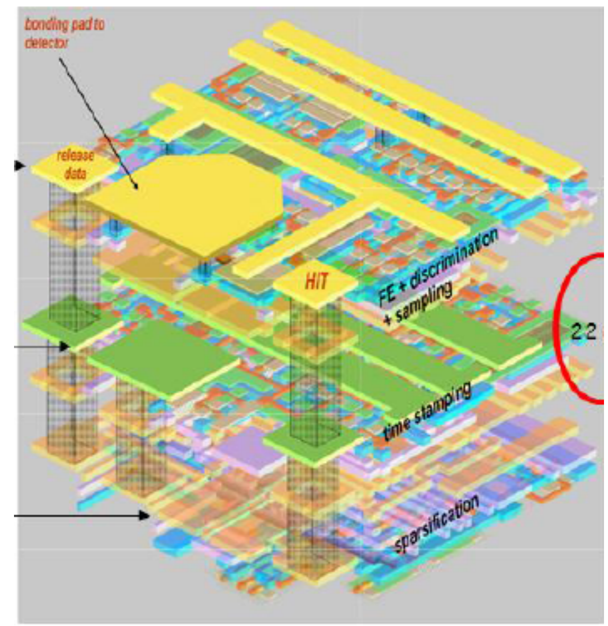
- CMOS in active pixel (but not high density)
- ~full charge collection efficiency
- high S/N (~100)
- small pixels (21x21 μm^2)
- fast
- radiation hard to 10^{15} n_{eq} / cm^2 or 300 Mrad
- ~10 μW / pixel
- rel. large collecting electrode (→ Q dep. bulk effect)
- cap. feedback -> CMOS logic gates -> x-talk



3D integration … a hot topic

“vias first” … various CMOS layers





3D integration promises

- higher granularity
- lower power
- large active over total area ratio
- low mass
- dedicated technology for each functional layer

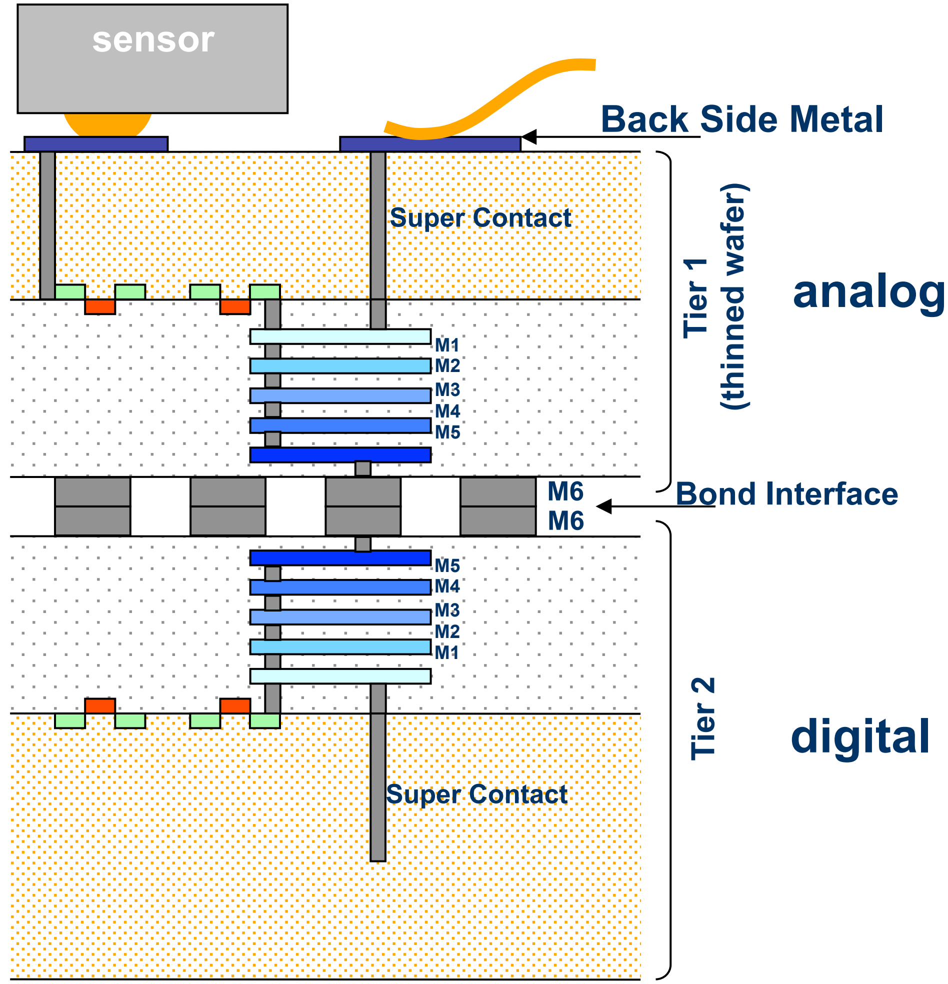
prototypes with

- **OKI**
- **MIT LL**
- **Tezzaron/ Chartered**

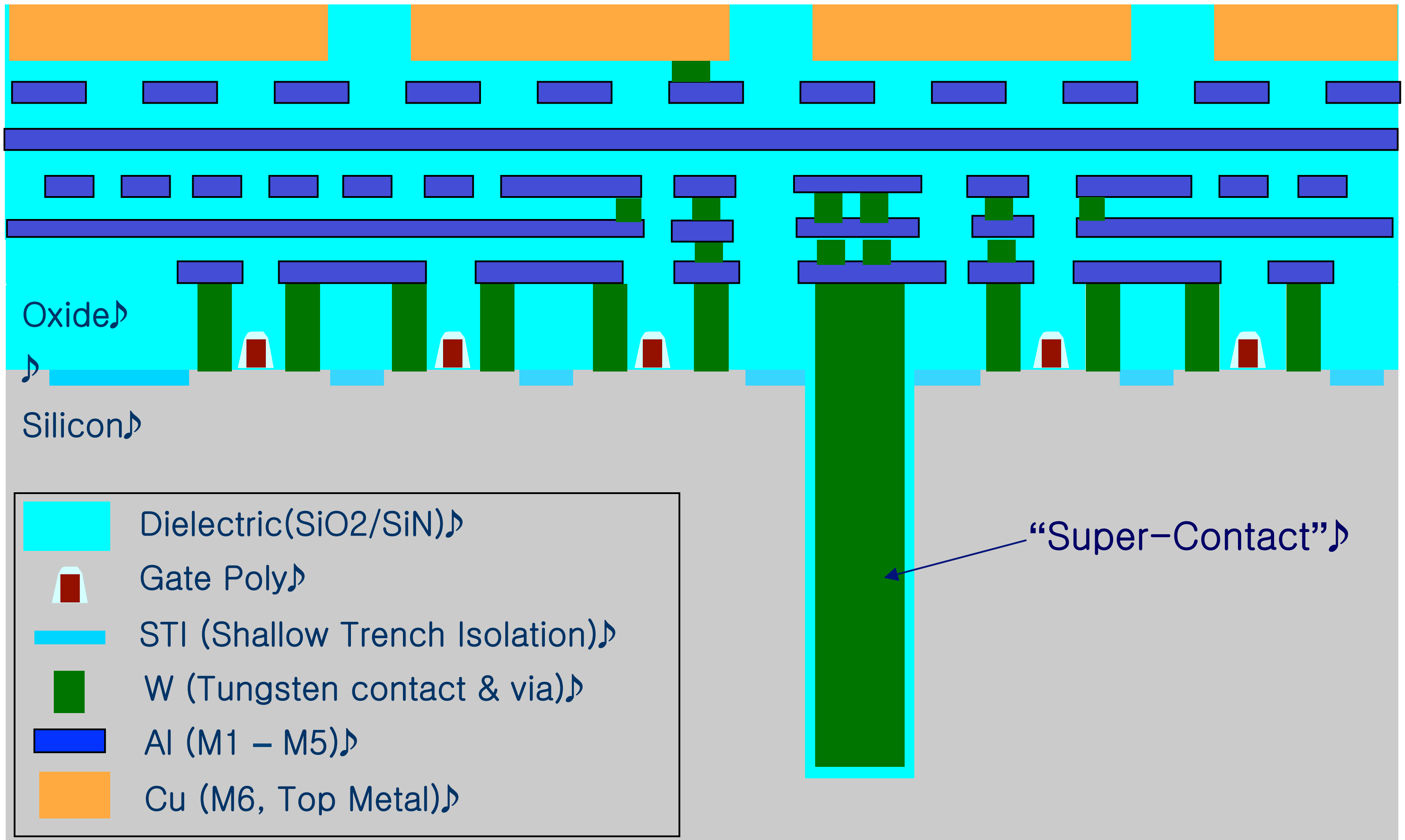
CMOS vias first …

Tezzaron/Chartered 0.13 um Process

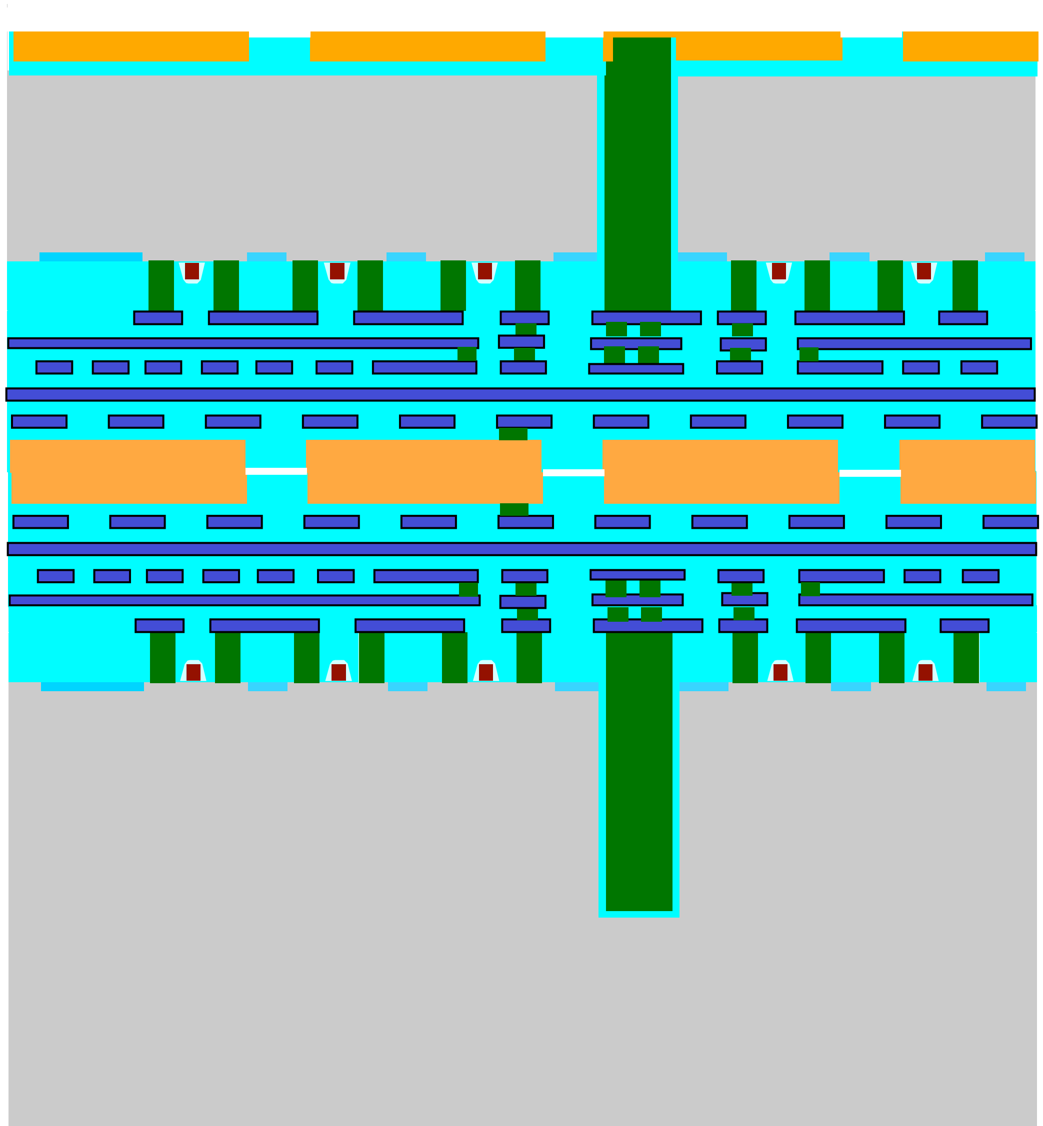
Large reticule (25.76 mm x 30.26 mm)
12 inch wafers
vias: 1.6 x 1.6 x 10 µm, 3.2 µm pitch
missing bonds: < 0.1 ppm



Wafer-Level Stacking

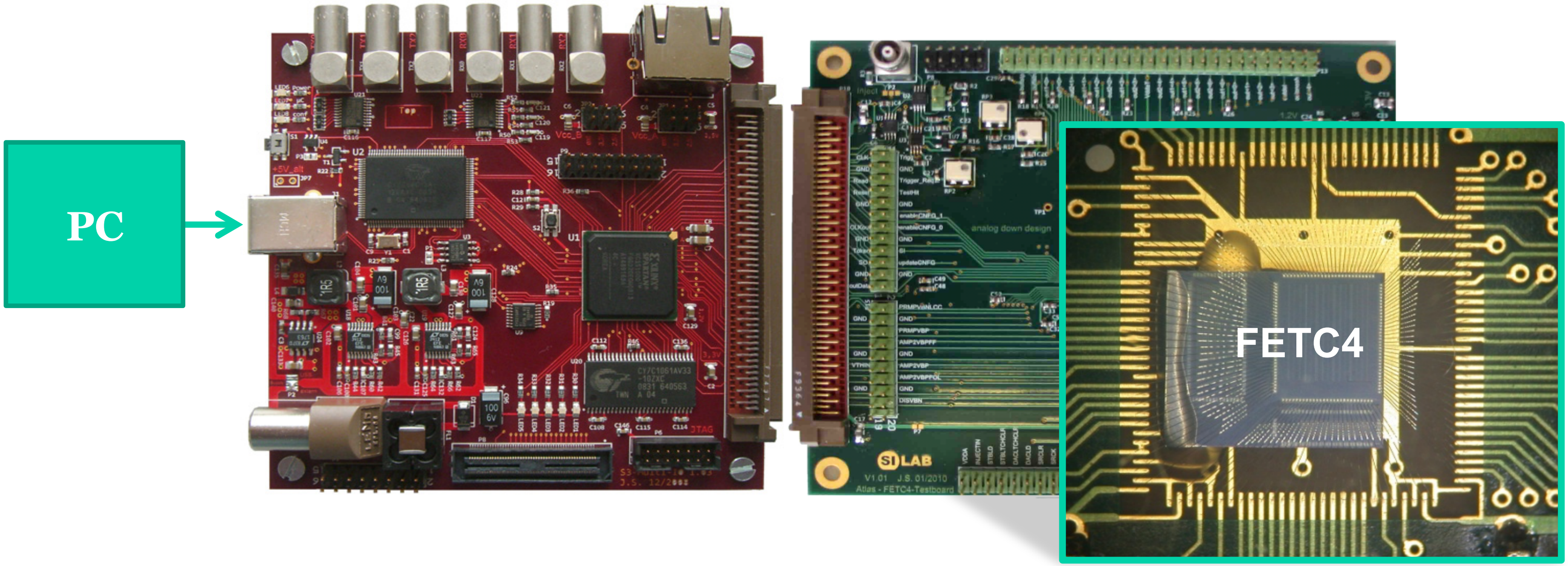


Next, Stack a Second Wafer (thin)



First ATLAS structures …

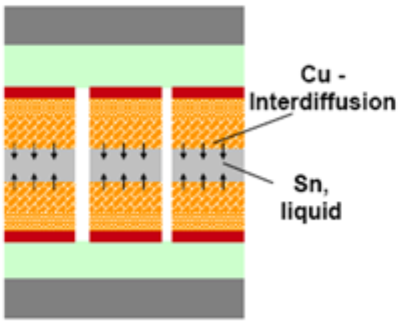
3D CMOS chip FETC4 bonded and tested.



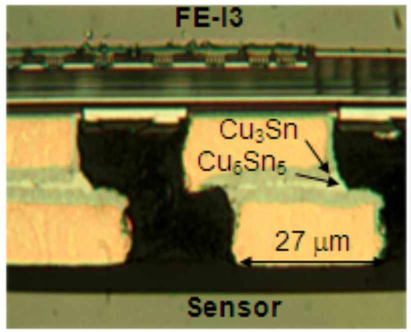
- **still some severe problems**
  - mostly alignment issues
- **analog tier thinned down to 12µm and operated stand alone**
  shows same noise behavior as un-thinned 2D

vias last … post processing

exploit: 3D integration for hybrid pixels, through silicon vias, wafer to wafer connection



Contact under Pressure
and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)



Formation of
Eutectic Alloy;
T_{melt} > 600 °C

Solid Liquid InterDiffusion (SLID)

(FhG EMFT Munich/MPI M)
alternative to bump bonding
but allows stacking of several layers

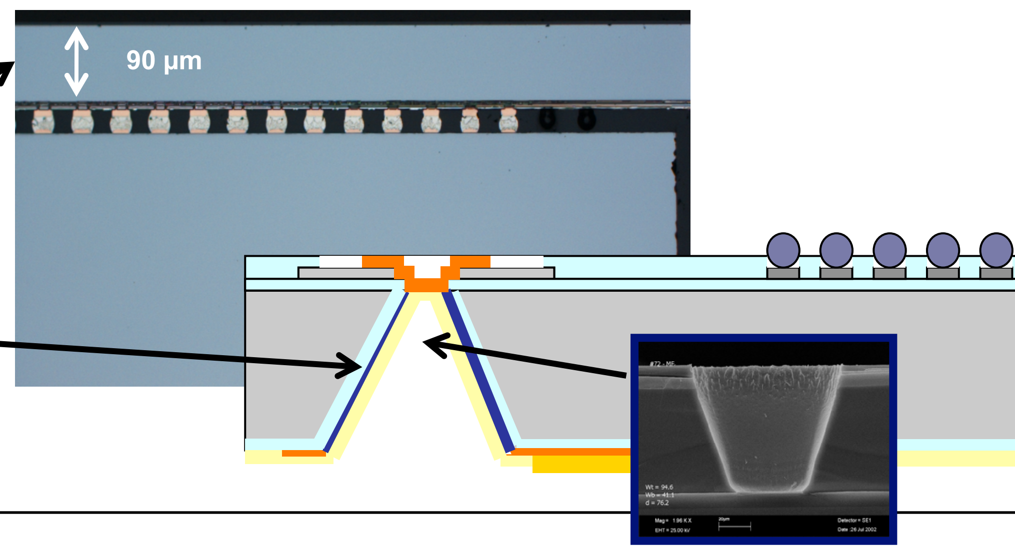
Through Silicon Vias (TSVs)

(FhG IZM Berlin / UBonn)

gain ~ 1% x/X_0 in ATLAS with

- **90 µm bumped FE-I4 chip**
- **thin Al flex**
- **serial powering**
- **TSV and backside metal routing**

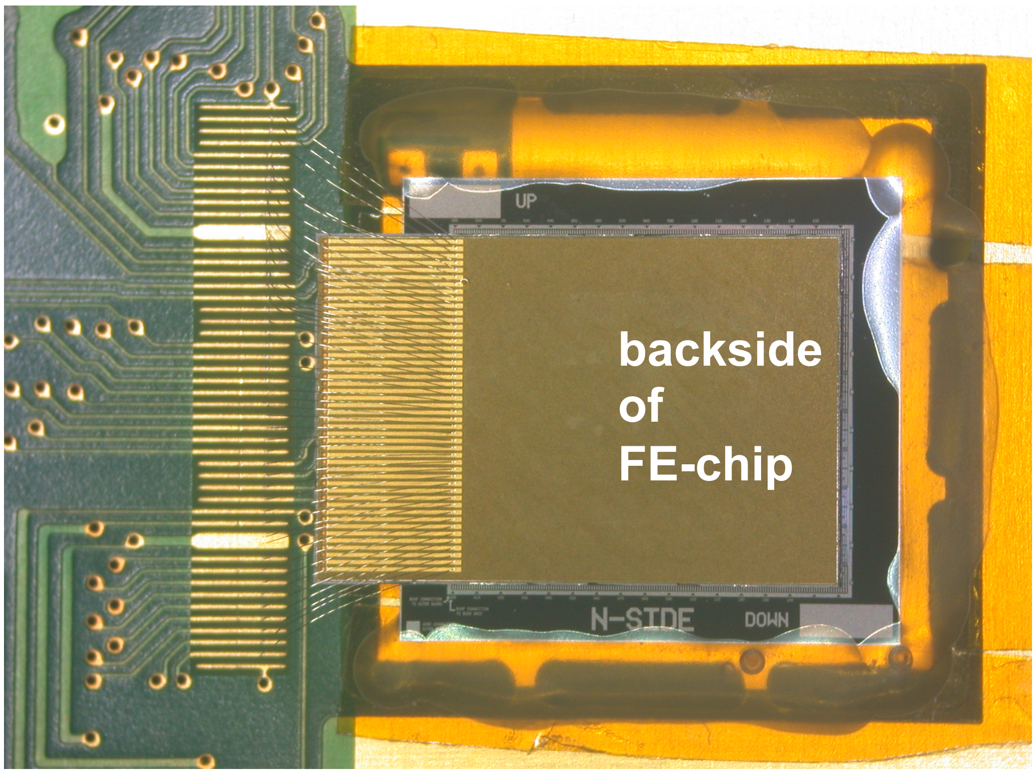
aggressive reduction in material

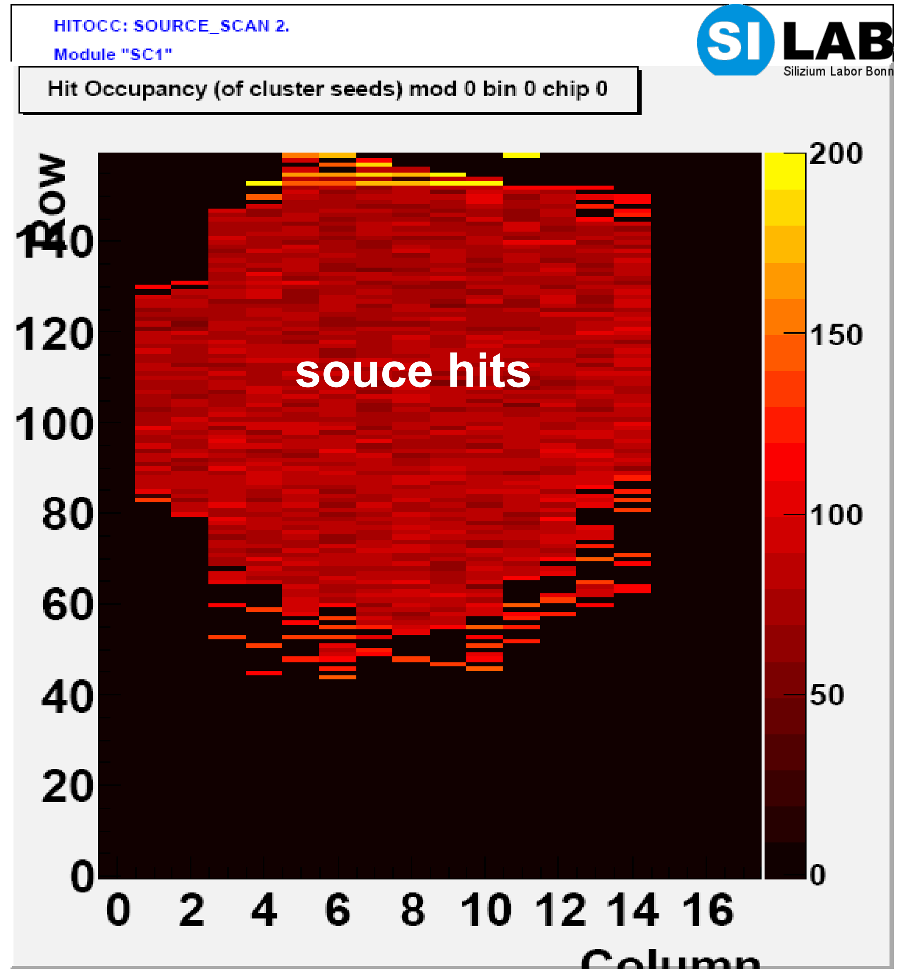


Proof of principle demonstration

ATLAS FE-I3 chip-sensor module operated through TSV and backside re-routing

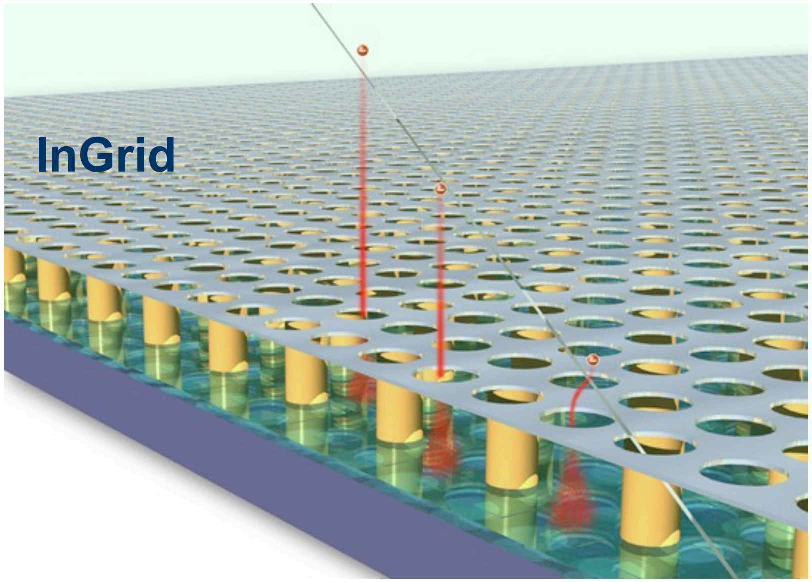
Source scan with Am-241 source

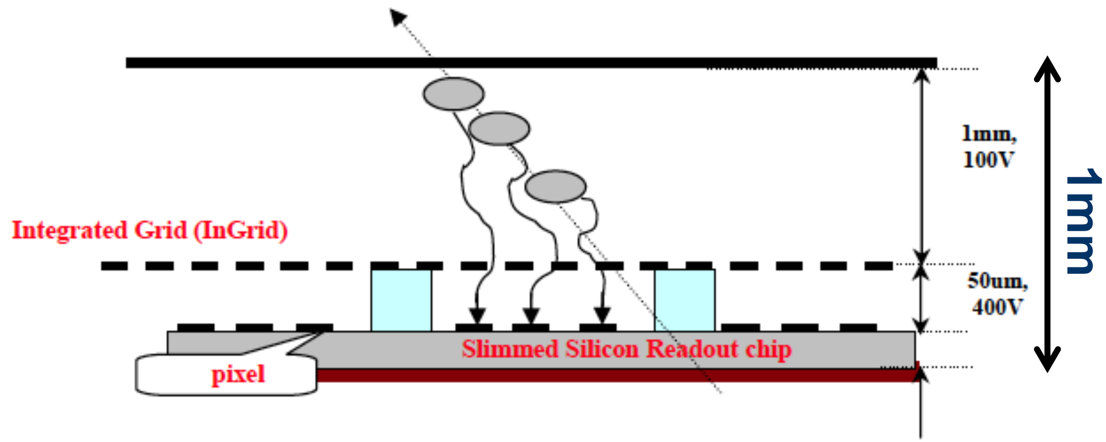




perhaps another option for the future … gaseous pixels

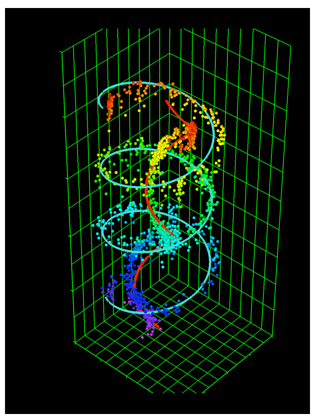
GOSSIP Harry van de Graaf et al., NIKHEF





inherently radhard and low mass

2 e- from
^{90}Sr source →



- **1 mm gas as detection medium**
- **gas gain x 1000**
- **16 ns drift time**
- **sensitive to single electrons**

- **need to prove large scale operation in LHC environment**

Conclusions

Predictions are always a gamble, but … I am quite sure that …

- for sLHC
  - only hybrid pixels, possibly with heavy 3D integration (CMOS and post-processing) will manage the environment (irradiation and rates)
  - material will not easily get below 1% x/X_0 per layer
  - … perhaps consider some gaseous advancements

- for (almost all) other applications in HEP
  - thin materials
  - high monolithic integration

  will dominate the issue.

  Here CMOS integration and integration of sensor and electronics will be the interesting challenges for the coming years.

SI LAB Silizium Labor Bonn