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PHYSICS AT THE TERA SCALE
Helmholtz Alliance

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3D Integration

5th Annual Helmholtz Alliance Workshop on "Physics at the Terascale"

Detector Project Session

08-12-2011

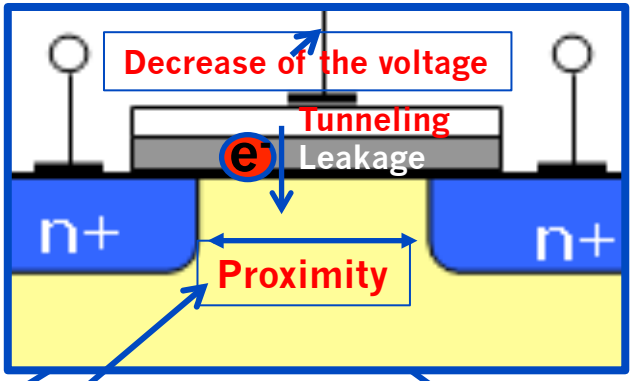
SiLAB Silizium Labor Bonn

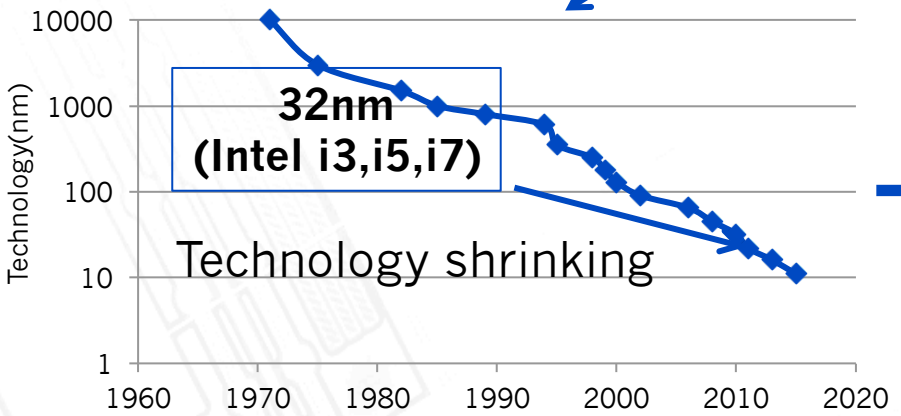
Content

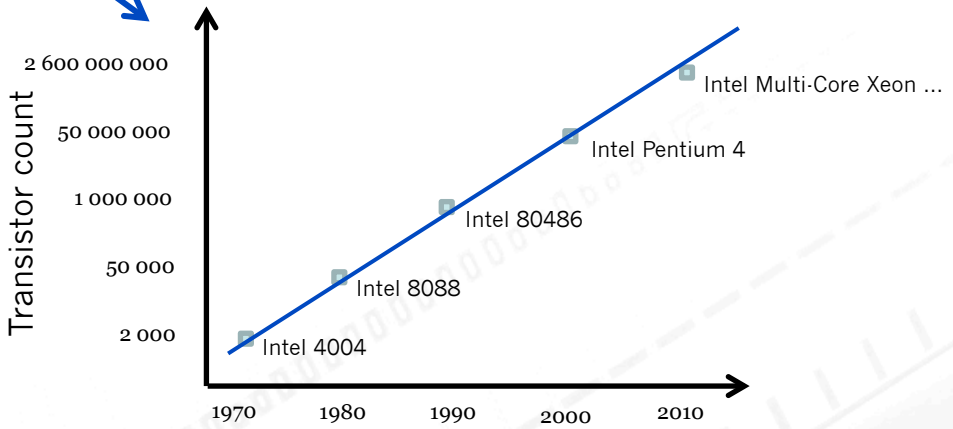
- 3D Integration
  - What is it?
  - How can it helps us for future detectors?
- A few examples:
  - Chartered/Tezzaron 3D integrated electronic for ATLAS pixel (Bonn/CPPM/LBNL)
  - TSV (Via last) development based on FE-I2/3 readout electronics (Bonn/IZM):
  - SLID and TSV (Via last) for ATLAS pixel (EMFT and MPI/HLL Munich).

Chips and Transistors

- Transistors are building blocks of digital and analog circuits.
- Nowadays chips contain millions of transistors.







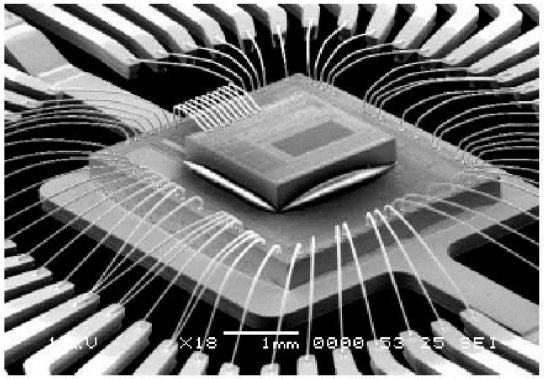
- Smaller transistors → More transistors per unit area → More functionality
- But smaller transistor size → new issues (smaller distance between “source” and “drain”, thin gates, Smaller gate voltage, tunneling effect and leakages, higher doping profile)

Limitations and Solutions

- Problems with feature size decreasing
  - New issues @ transistor level (previous slide)
  - Small feature size → increase of interconnection density making copper connections thinner, longer and closer to each other:
    - ✓ parasitic RC delays
    - ✓ parasitic inductances
    - ✓ increases heat dissipation
    - ✓ power consumption
    - ✓ noise coupling.

    ← **Wiring crisis**
  - Even if the above limitations will be circumvented mixed signal designs could suffer from the small feature size: when for the digital part this would be a natural choice, "designers' conventional wisdom" → analog performance could degrade due to small transistor size.
- 3D packaging/integration could help
  - Possible solution could be to break the IC circuit into several layers, and stack them on top of each other:
    - ✓ More transistors per unit area without decreasing feature size.
    - ✓ Interconnect vertically. Shorter distance.
    - ✓ Different technologies for different layers?
    - ✓ Compact modules integration the sensor as well

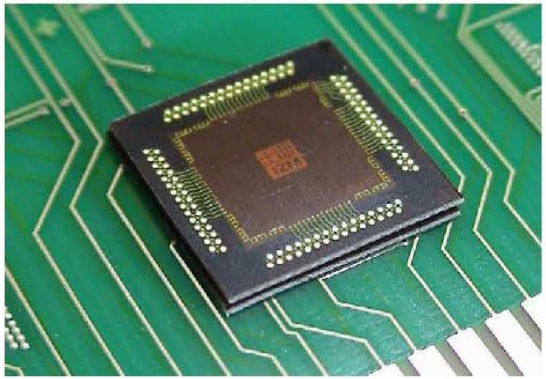
Exploiting 3rd Dimension



Source : Fraunhofer IZM

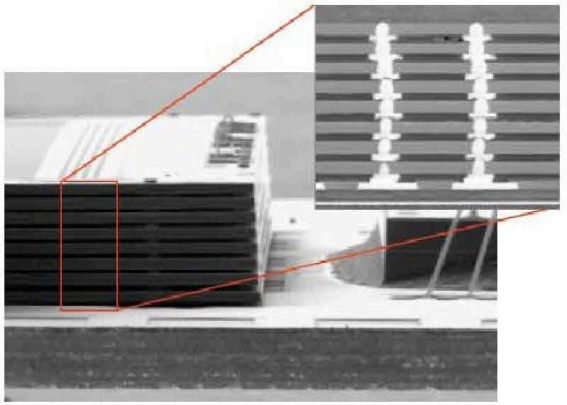
Wire-bonding

Bump-bonding



Source : Fraunhofer IZM

8-layer stack, 2Gb flash memory… ×8!!!
On 0.56mm!



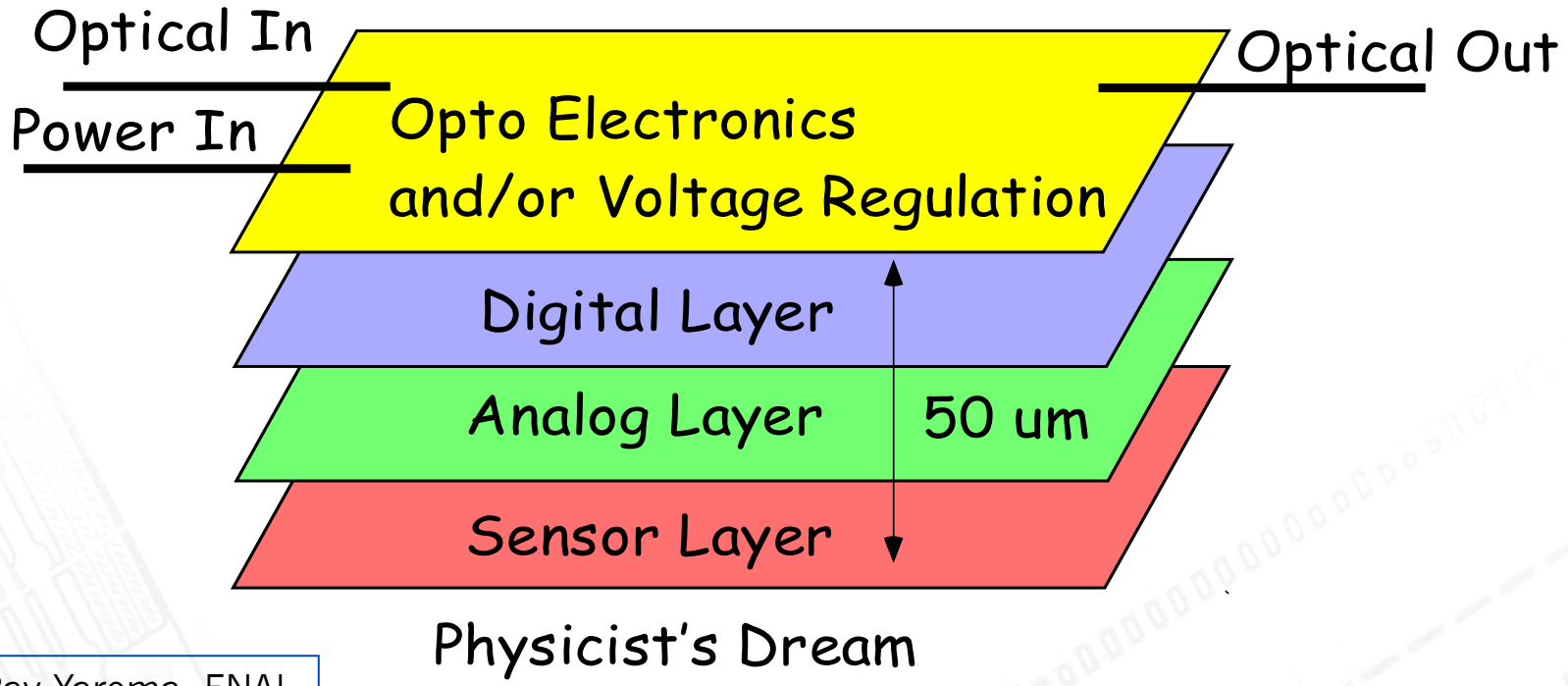
Source : Samsung Electronics

Shorter, Denser, Smaller, Faster, Less Power

Cheaper? (ultimately)

Application in HEP

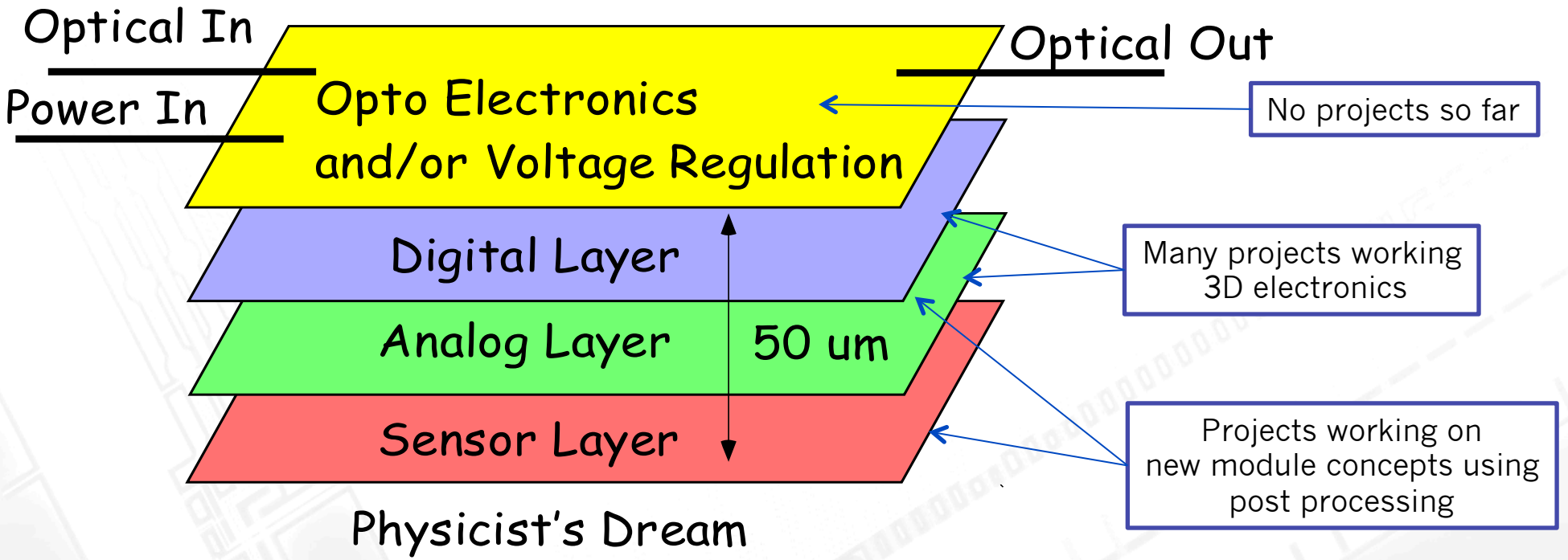
With 3D integration, one can reach higher granularity, lower power, large active over total area ratio, low mass and dedicated technology for each functional layer



Ray Yarema, FNAL

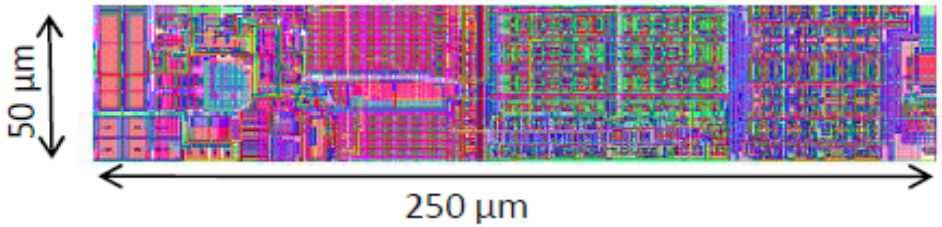
HEP 3D Projects

- In the last years many 3D projects have been launched:
  - All addressing a part a job.
  - Post-Processing (Vias last) enables compact module concepts by integration electronics with sensors → Chartered/Tezzaron.
  - 3D integrated processes (Vias first/middle) enable 3D electronics → TSV IZM and SLID/TSV EMFT.

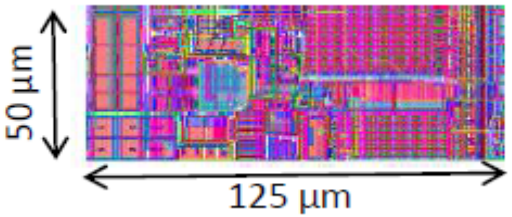


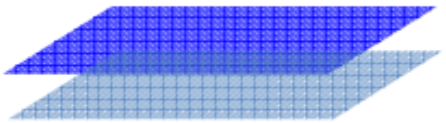
From 2D to 3D electronics

- FEI4 Pixel (IBM 130nm technology)



- 3D electronics with TSV - FETC4 (Tezzaron-Global Foundry 130 nm)
  - IC could be split in separate analog and digital parts (tiers). Technology mixing. Pixel size reduction.

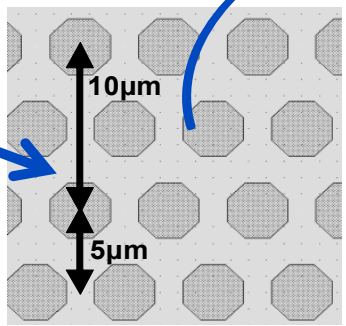


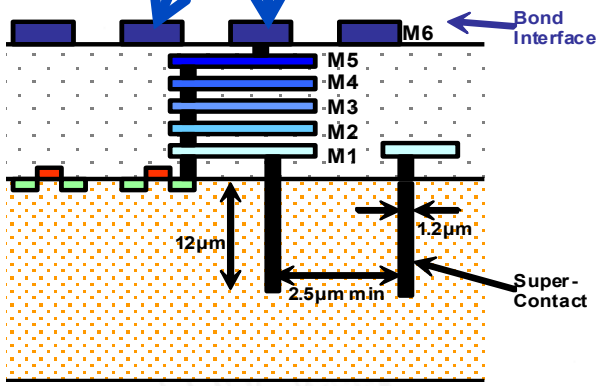


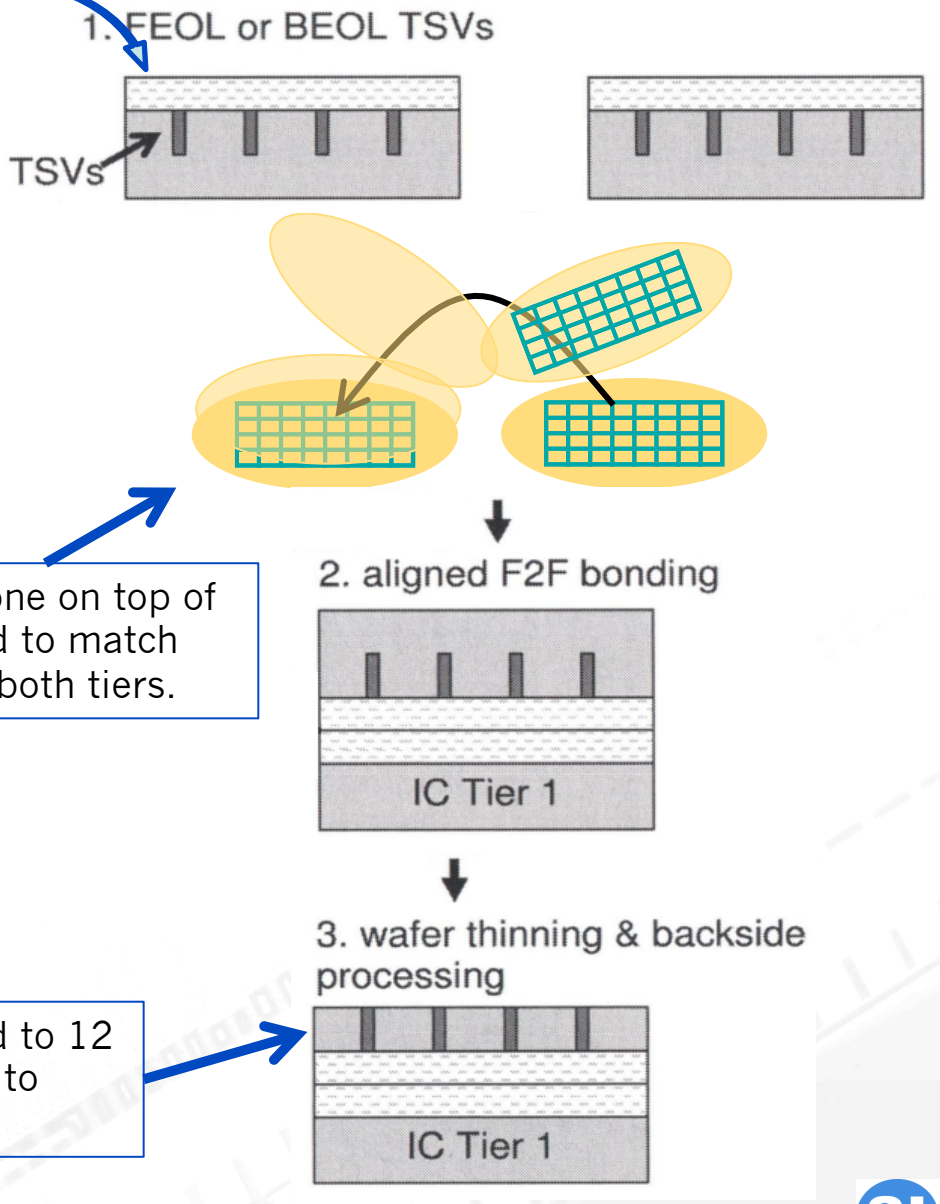
The idea was to use the same analog and digital (simplified) schematics as used in the IBM prototype to save time, and test the 3D technology and the new provider Global Foundry (also as pure 2D).

3D Tezzaron foundry process

Each wafer has special interface – “bond interface” - for electrical and mechanical inter-tier connection.



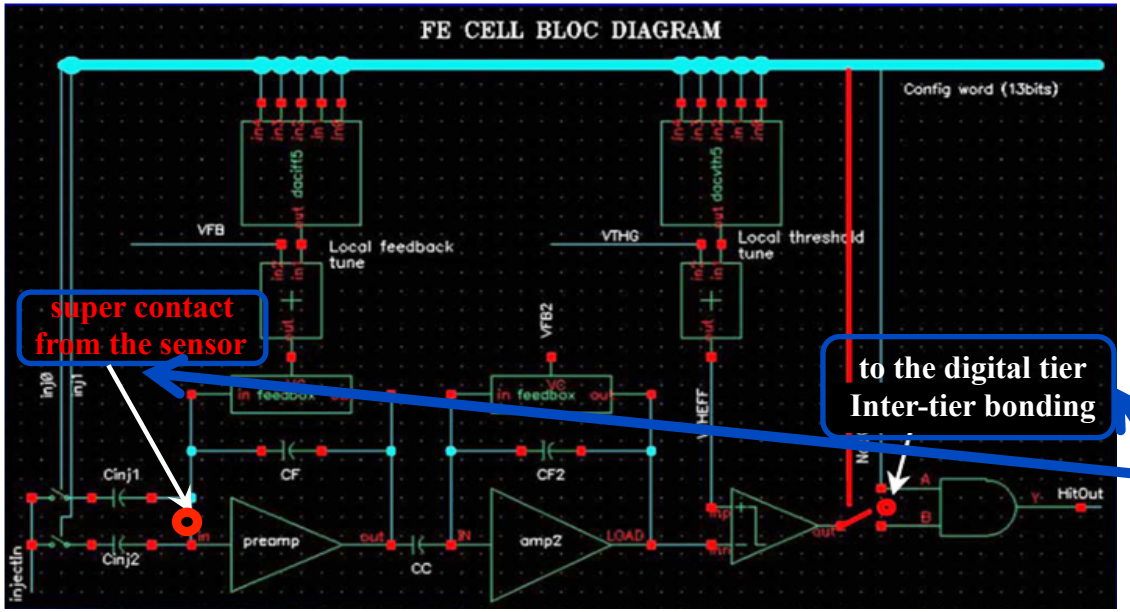


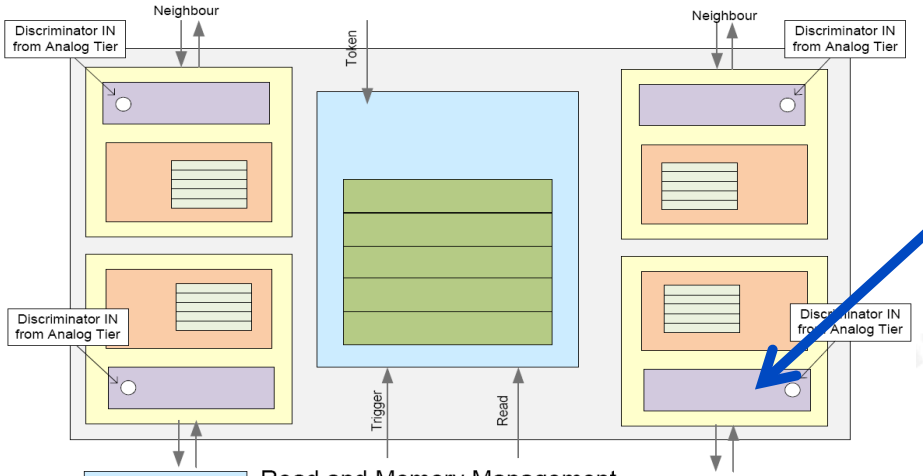


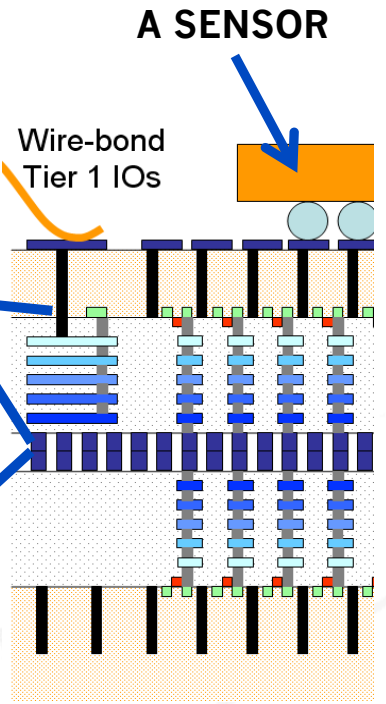
Wafers are placed one on top of another and aligned to match Bond interfaces of both tiers.

After bonding top wafer is thinned to 12 µm and diced. Thinning is needed to access TSVs

Analog and Digital Tier



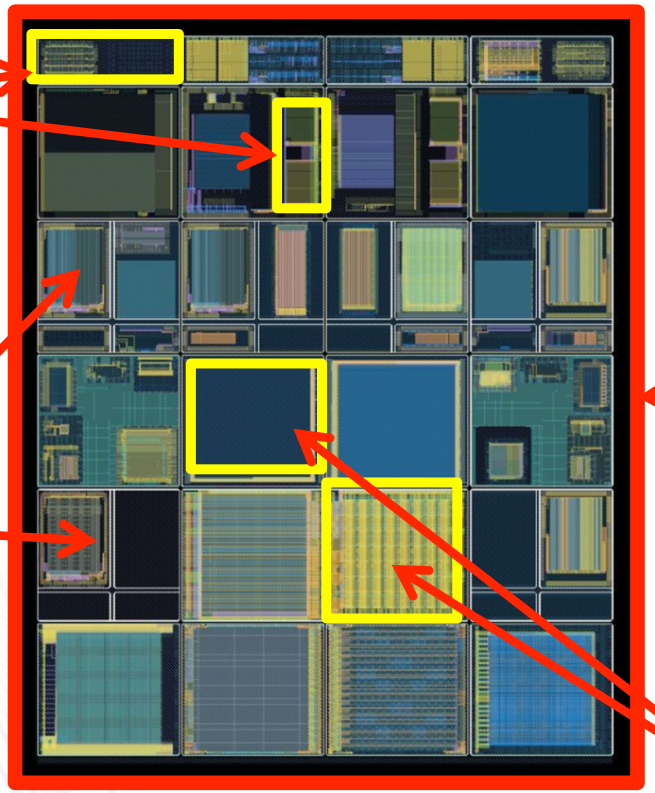




Analog pixel chain and 4-pixel Region derived from FE-I4

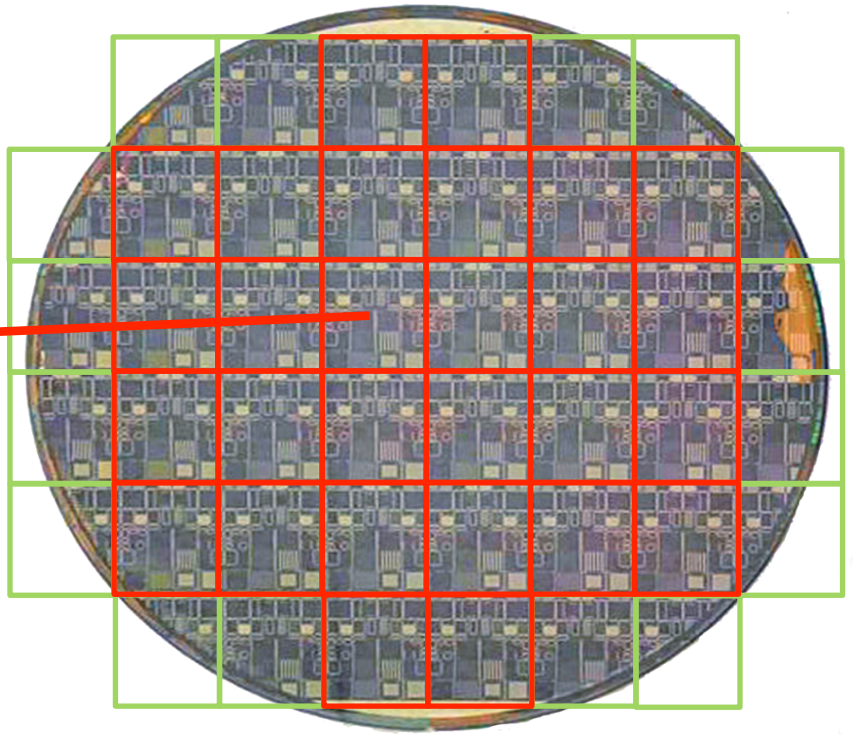
1st HEP MPW Wafer

FETC4 is a part of Multi Project Wafer where 17 groups from 6 countries (Canada, France, Germany , Italy , Poland , USA) are taking part.



Chips from other projects

FETC4 chips



Chips from other projects

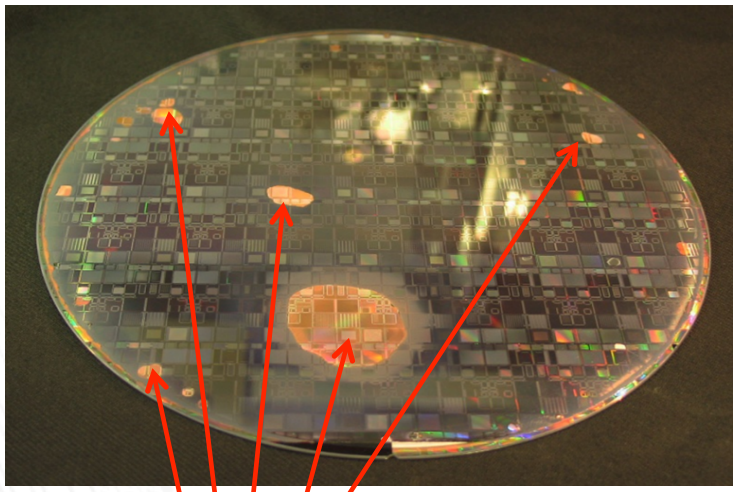
bad reticule

good reticule

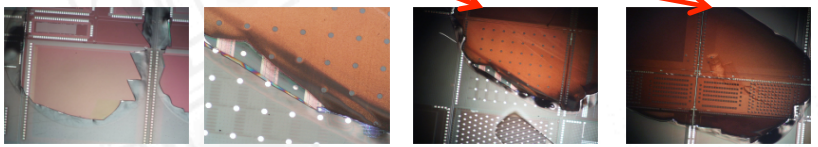
Wafer is subdivided in 24 reticules. All reticules are identical and contain more than 25 two tier designs and additional test circuits.

Received 3D Chips

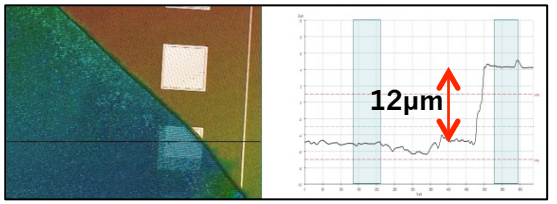
Although more than 30 single wafers were produced for bonding, due to fabrication issues only 3 bonded wafer pairs were accepted for at least some kind of testing and only one of these wafers was diced and distributed. The rest two show extensive damages on the surface.



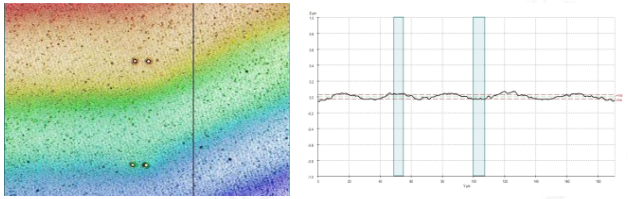
Damages on the wafer &
Close up photographs



Acoustic microscope photographs of the wafer surface



near damage. Level shift ~12µm =
= thinned layer thickness

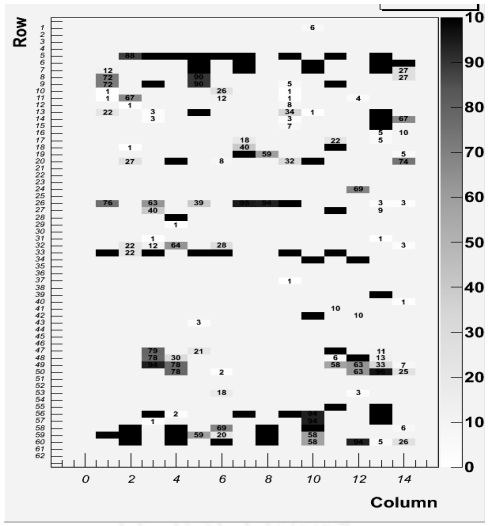


@ no damage. Level variation ~30nm

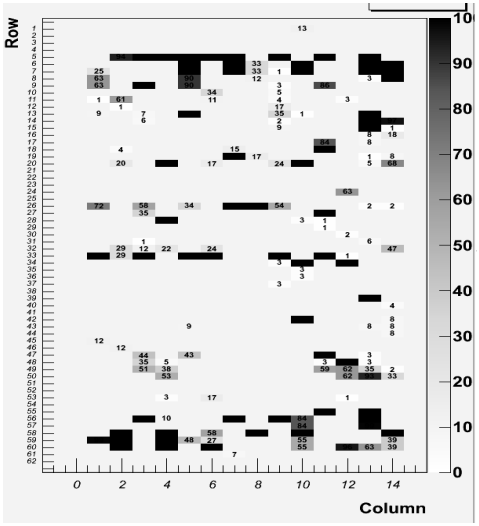
Inter-tier connection quality

Most important test was to see a communication between tiers.
Signal injected from the input of the analog tier must be detected by the digital tier.

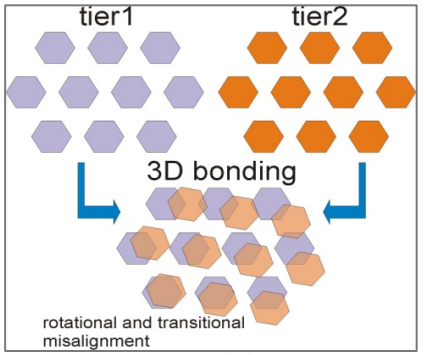
FETC4 hit map:
No injections

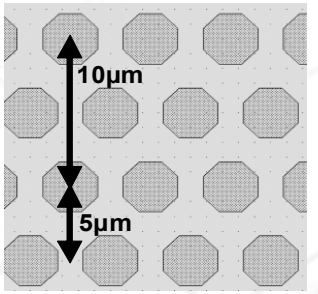


FETC4 hit map:
100 injection to each pixel

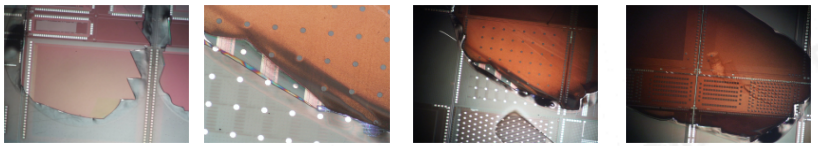


Bad electrical & mechanical connection due to misalignment of the tiers.





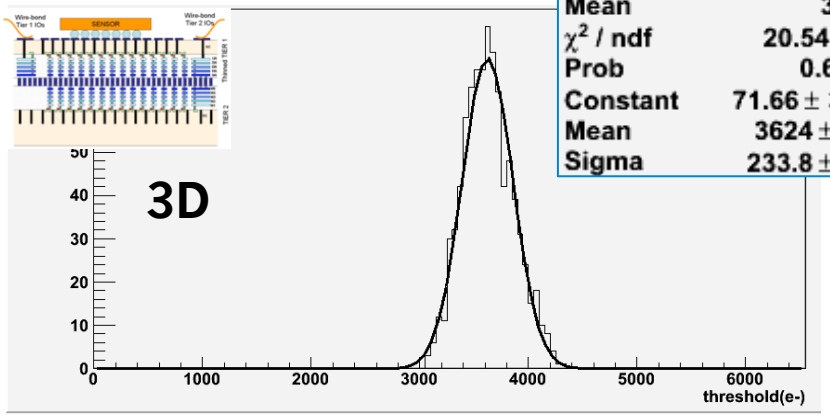
Bond interface

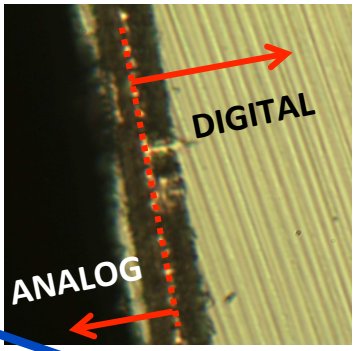


Bad mechanical connection between tiers → top tier removal during thinning process

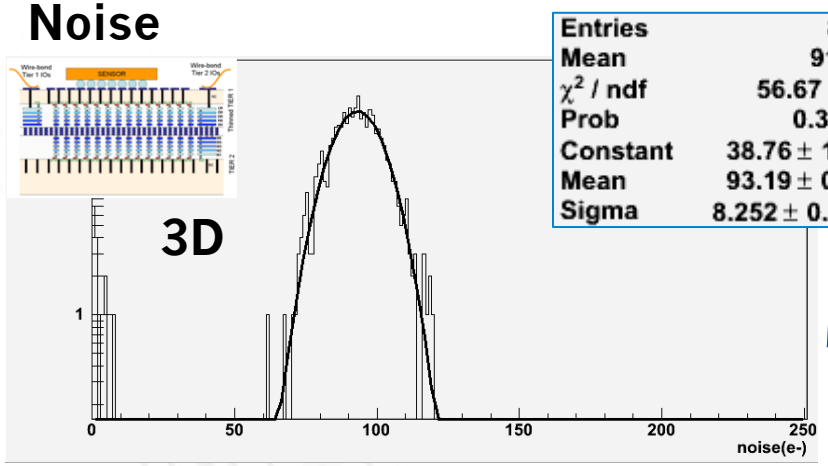
12µm analog tier performance

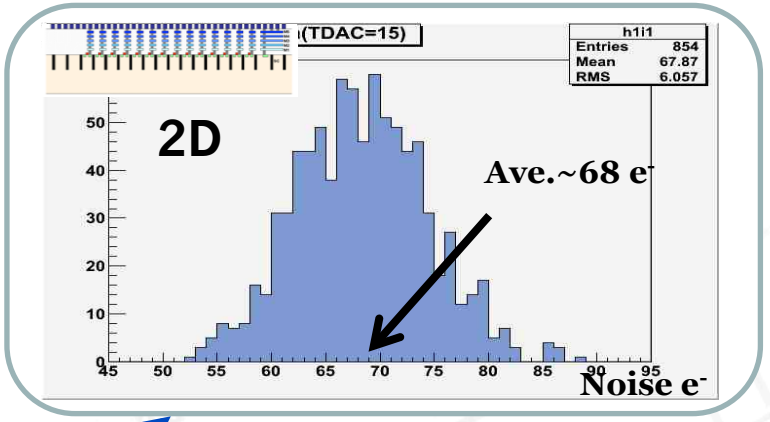
Threshold





Noise



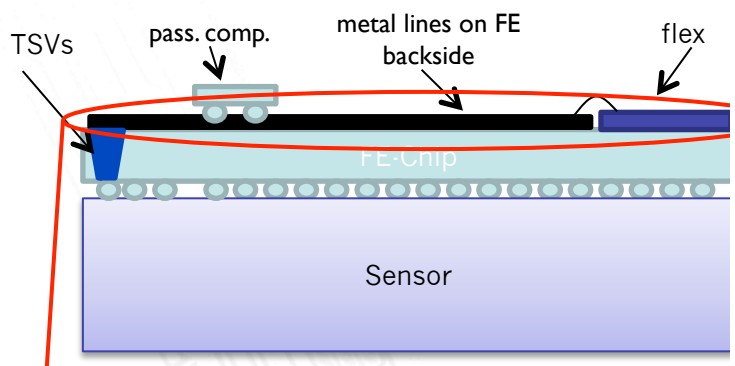


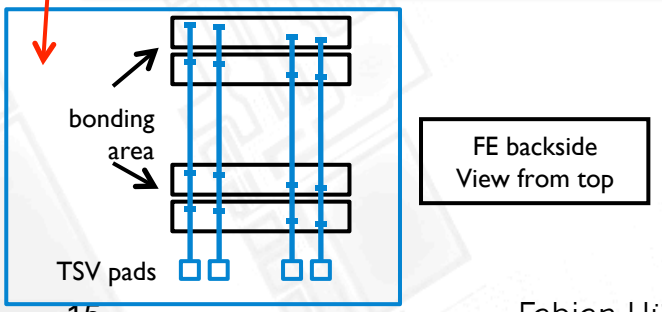
Slightly higher noise of the 3D chip wrt. 2D

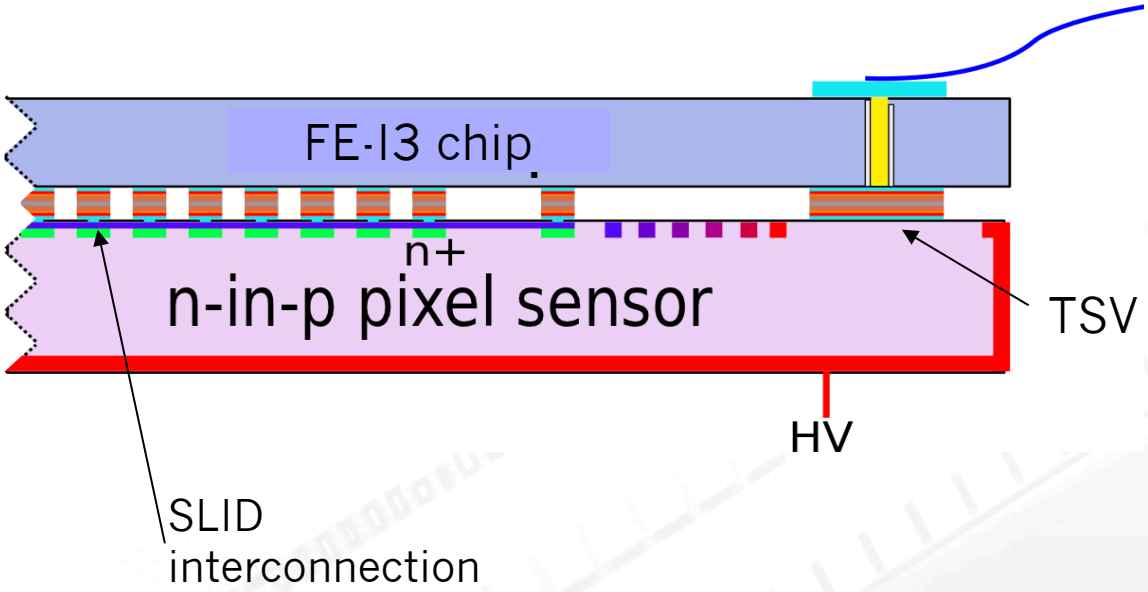
All tested prototypes are at least somehow working → thinned down analog tier (to 12 µm !!!) works, marginal noise increase.

Module concepts with TSV

- TSVs allow use of FE backside for routing → direct connection of service lines or flex on FE backside (e.g. via wire bonding)
  - Less material (no need for wings, module flex, connectors), easier interconnection
- TSVs enable 4-side buttable module concepts
  - FE-chip periphery needs to be shrunk or integrated into pixel matrix
  - Important for large scale detectors like HL-LHC trackers
- 2 approaches will be presented:
  - Fraunhofer IZM with Uni Bonn: tapered TSV on FE-I2/3 with standard bump bonding
  - Fraunhofer EMFT with MPI/HLL Munich: TSV with thin n-in-p sensors using SLID for BB



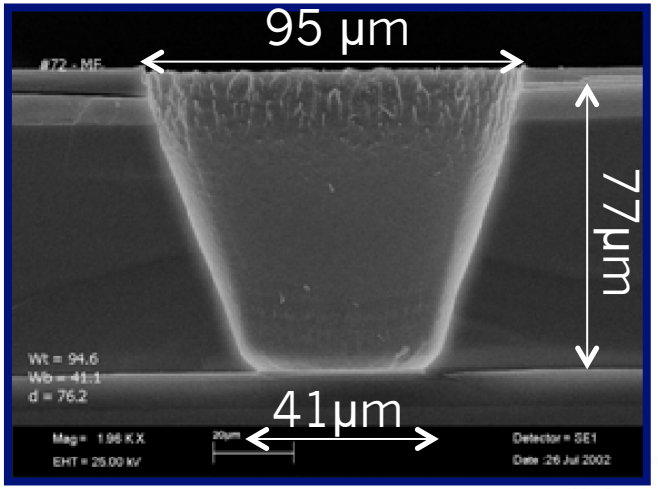


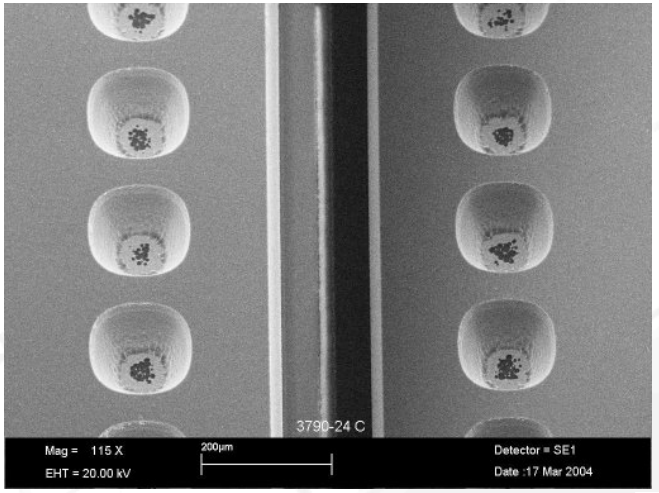


TSV etching with Tapered Side Walls

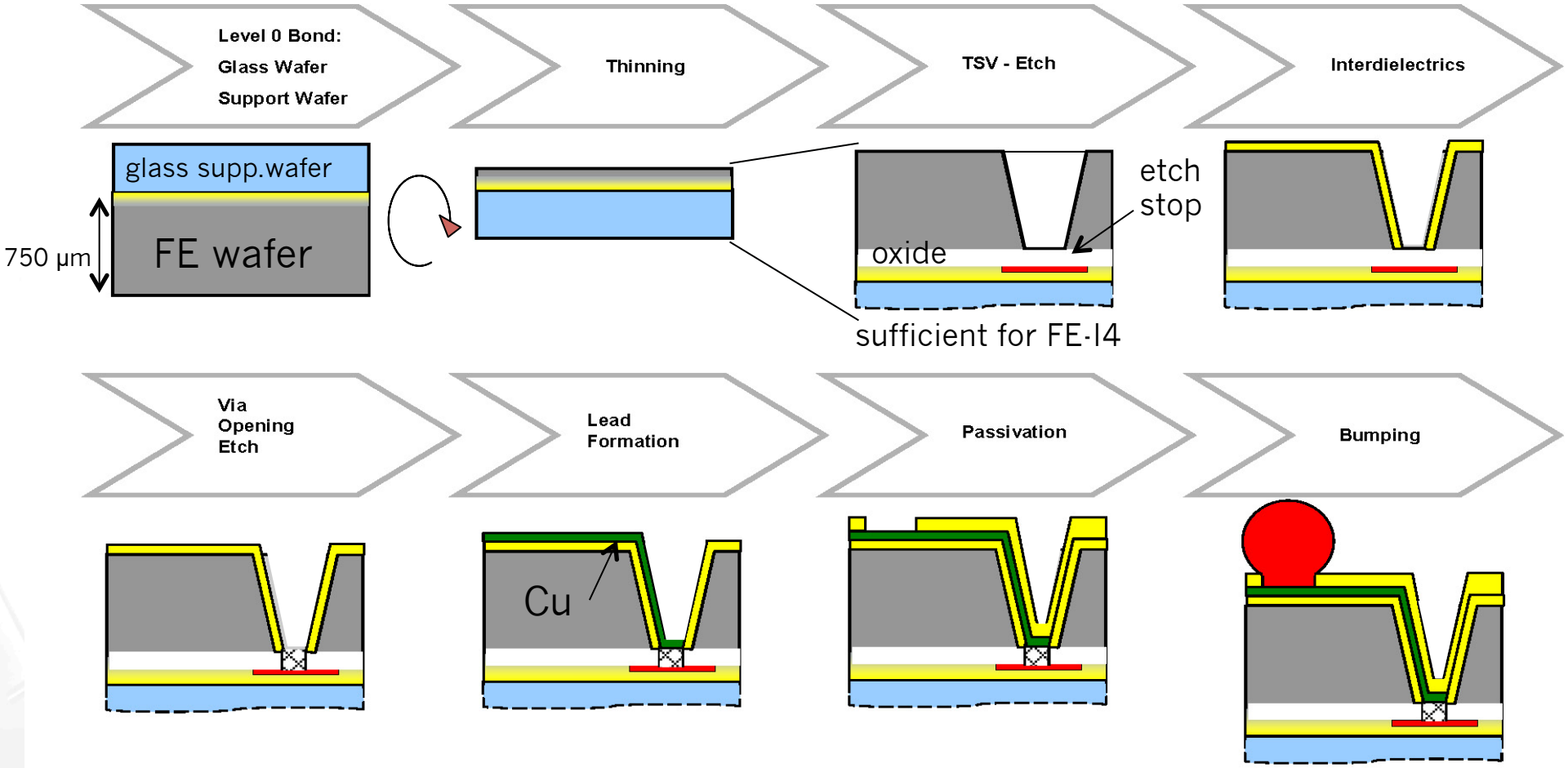
- **Tapered Side Wall TSV**
  - Vias are etched in one step and oxide is deposited after etching
  - Simpler deposition process of isolation layer using thin film polymers
- Tapered walls
  - Side angle 72°
  - In this example
    - Via diameter on the bottom: 41µm
    - Via diameter on the top: 95µm
    - Si thickness: 77µm
  - With a pad size of 150µm
    - Max Si thickness: 100µm
- Note: Straight Walls
  - Aspect ratio 2 – 5:1
  - Max Si thickness: 100 – 150µm

Tapered Side Wall TSVs on monitor wafer





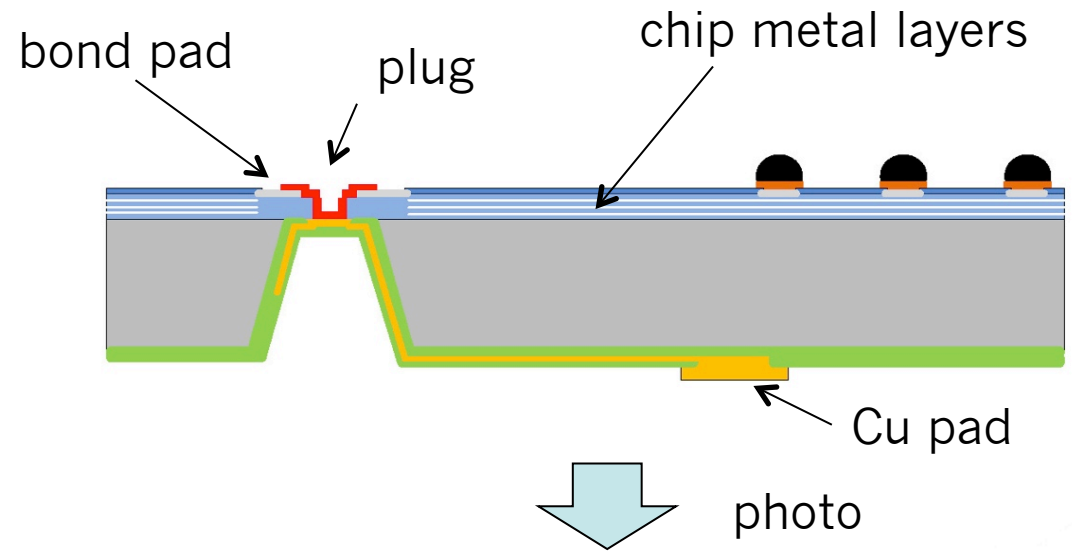
TSV: Main proces flow

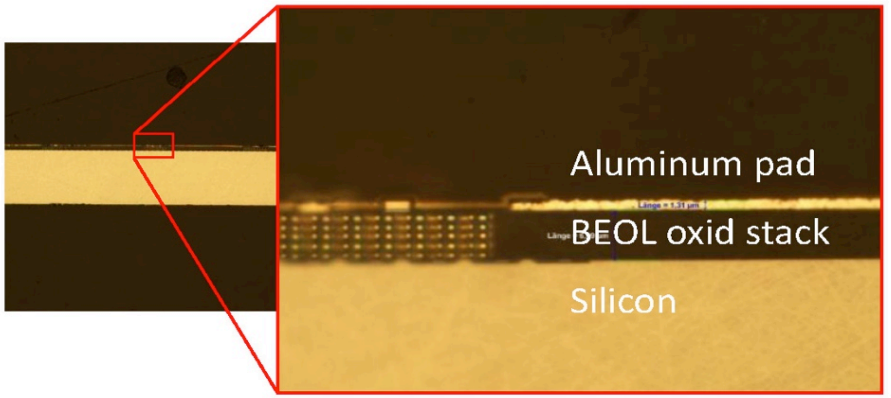


Tapered TSV for ATLAS Pixel FE-I2/3

- **Backside processing**
  - Thinning to 90µm
  - Silicon Via etching
  - Passivation
  - Cu depostion
  - Re-Distribution Layer (RDL)

- **Frontside processing**
  - Cu pad to bond pad interconnect (plug)
  - Bump deposition
  - Dicing





Tapered TSV for ATLAS Pixel FE-I2/3

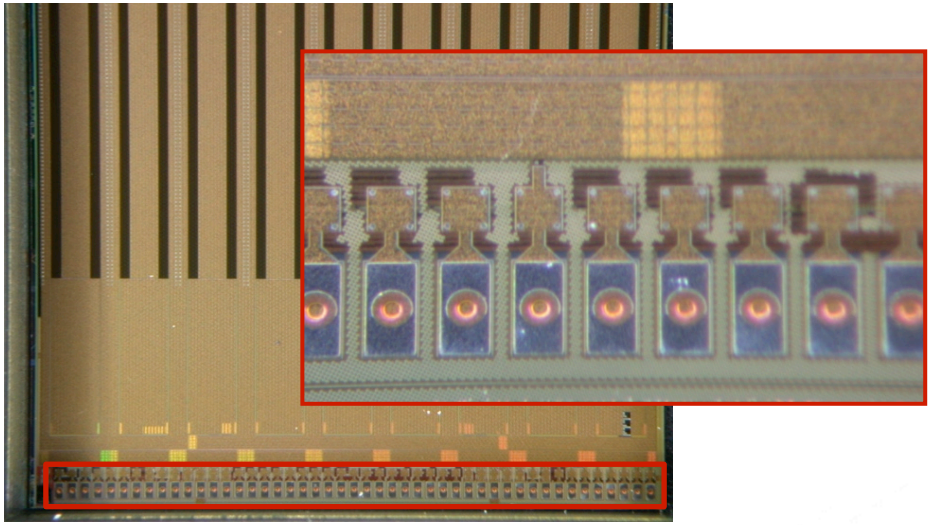
Fraunhofer IZM

- TSV interconnection from the backside to peripheral readout chip IOs:
  - Re-distribution of the pads on chip backside (RDL)

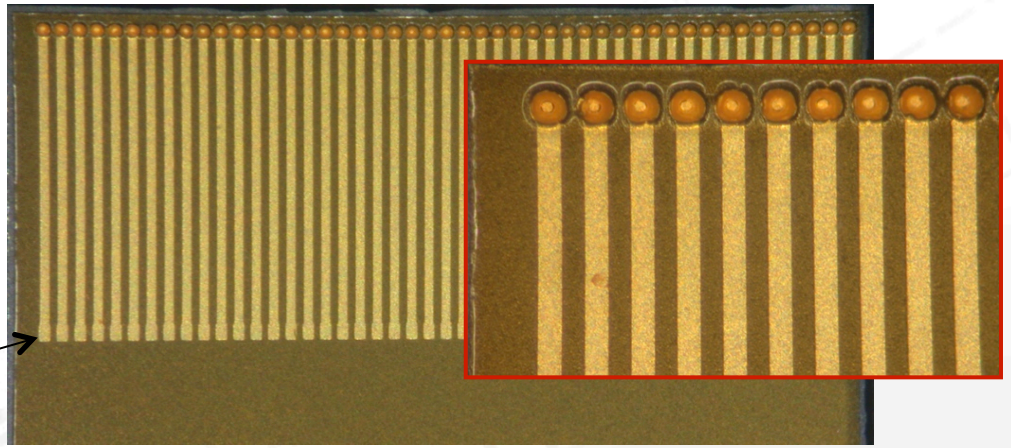
- **Status**

  Batch of 2 FE-I2 ATLAS wafer (+ monitor wafers) have been processed
  - 1 wafer without bump bonding to test the TSV alone → finished, bare chips available
  - 1 wafer with bump bonding to ATLAS pixel sensors → finished, single chip modules a[illegible]

Wire bond pads connected via TSV



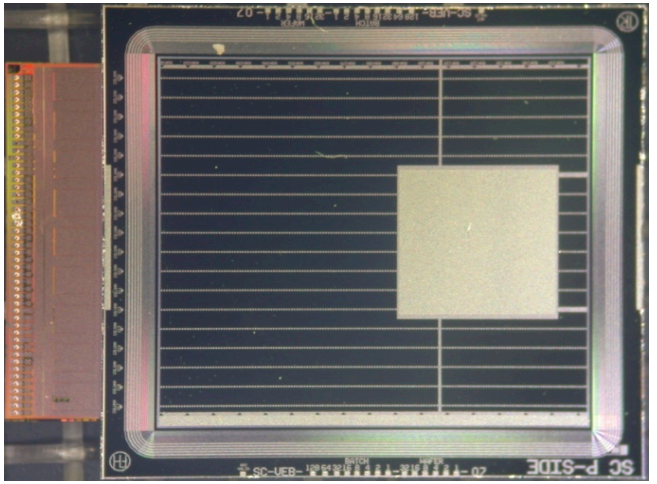
RDL



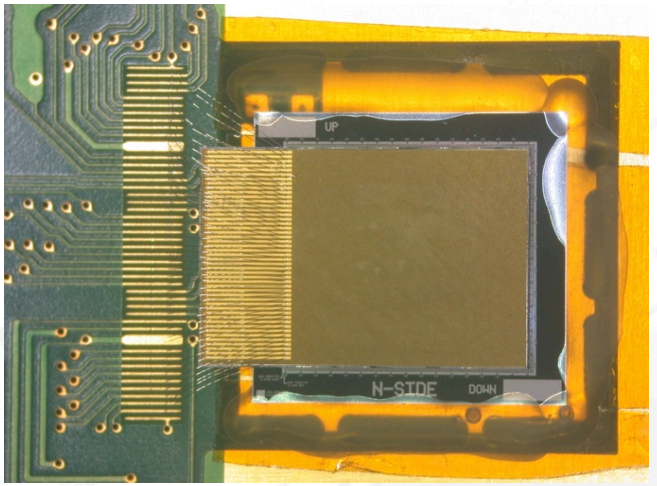
TSV modules

- Received 16 modules with
  - FE-I2 chips (wafer map available), 90µm thick, with tapered TSV and RDL
  - Planar n-in-n sensor
- 2 modules mounted on boards for electrical tests
  - Both modules work fine
- Poor quality of the flip chip process, i.e. many pixels disconnected
  - Note: it has nothing to do with the TSV process!!!
  - Standard flip chip process used instead of the dedicated flip chip process for thin chips developed by IZM to build IBL modules with thin (100 - 150µm) FE-I4 chips

Module front side

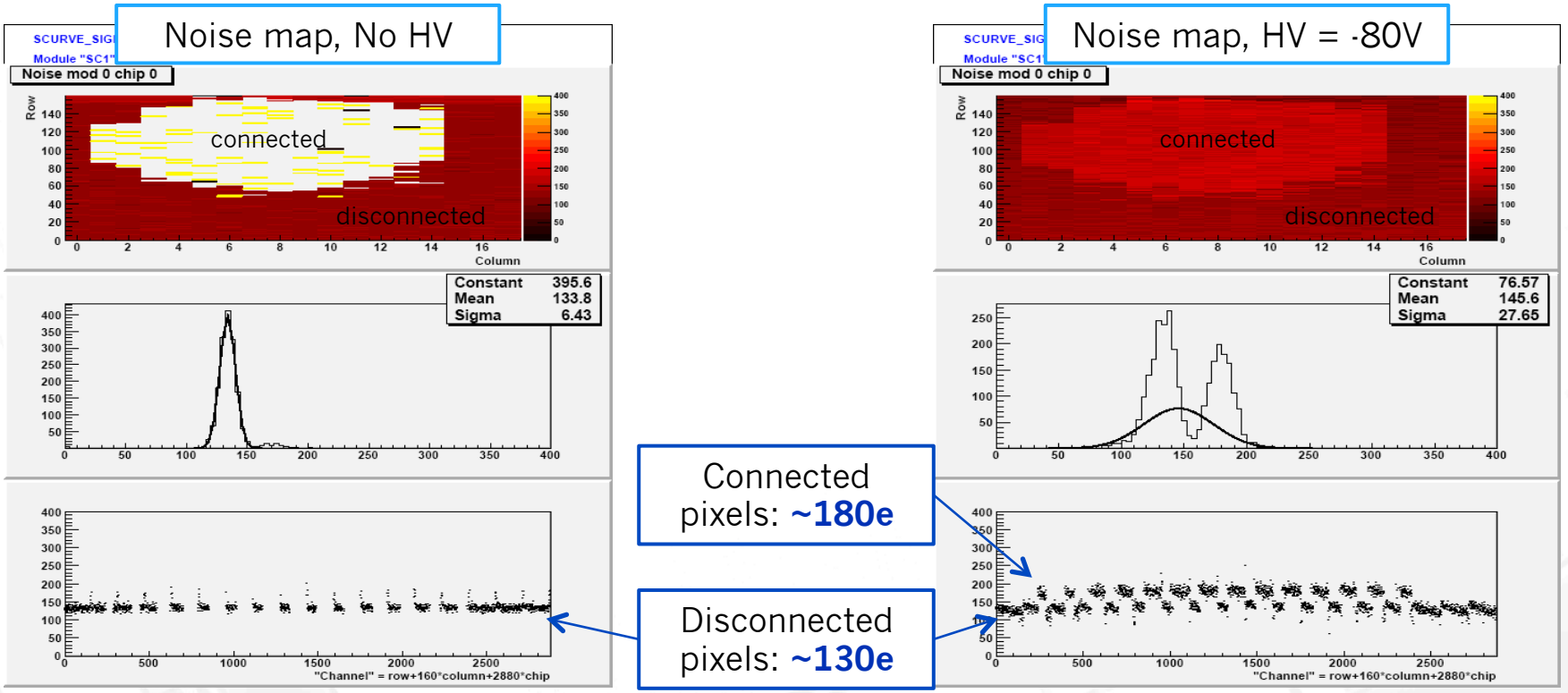


Module on board



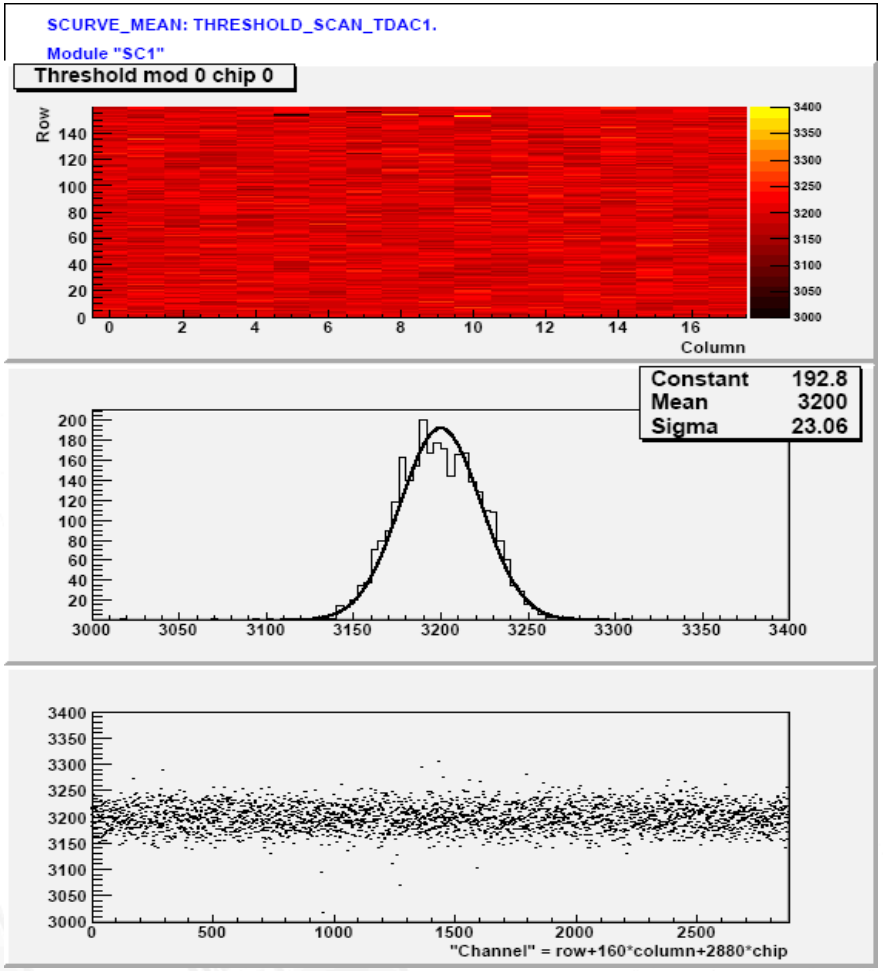
TSV module: wire bonds on backside (i.e. TSVs used for operation)

- Modules connected via TSV and RDL
- VDA = 1.5V, Ia = 77mA; VDD = 1.8V, Id = 33mA
- Noise measurement with and without HV shows disconnected pixels
  - For disconnected pixels the noise stays the same indep. of HV
- Module works fine → no indication of extra noise

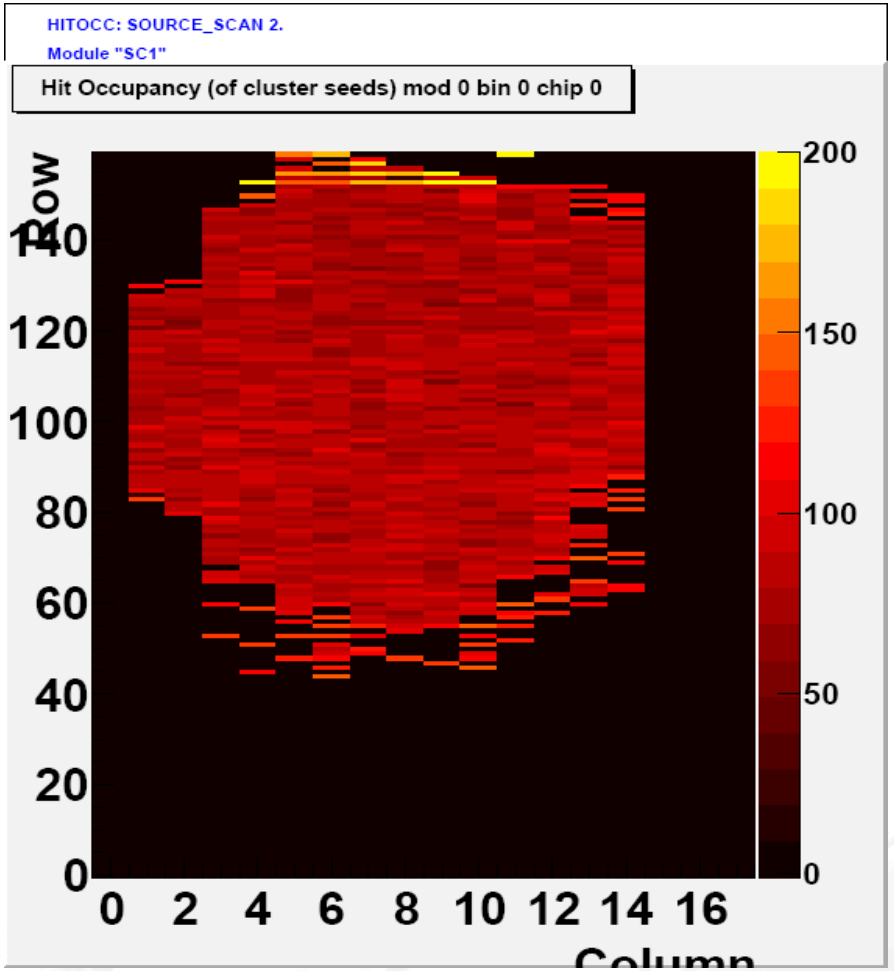


TSV module: wire bonds on backside (i.e. TSVs used for operation)

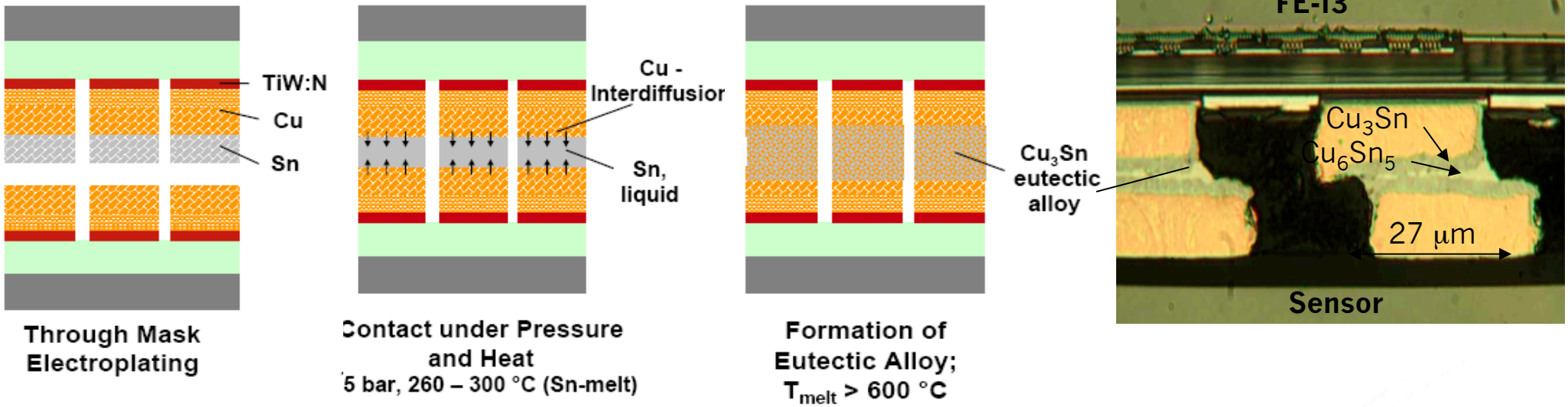
- Threshold tuning to 3200e



- Source scan with an Am-241 source



EMFT SLID Process



- Alternative to bump bonding (less process steps “lower cost” (EMFT)).
- Small pitch possible (~ 20 µm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

- However: no rework possible.

In collaboration with

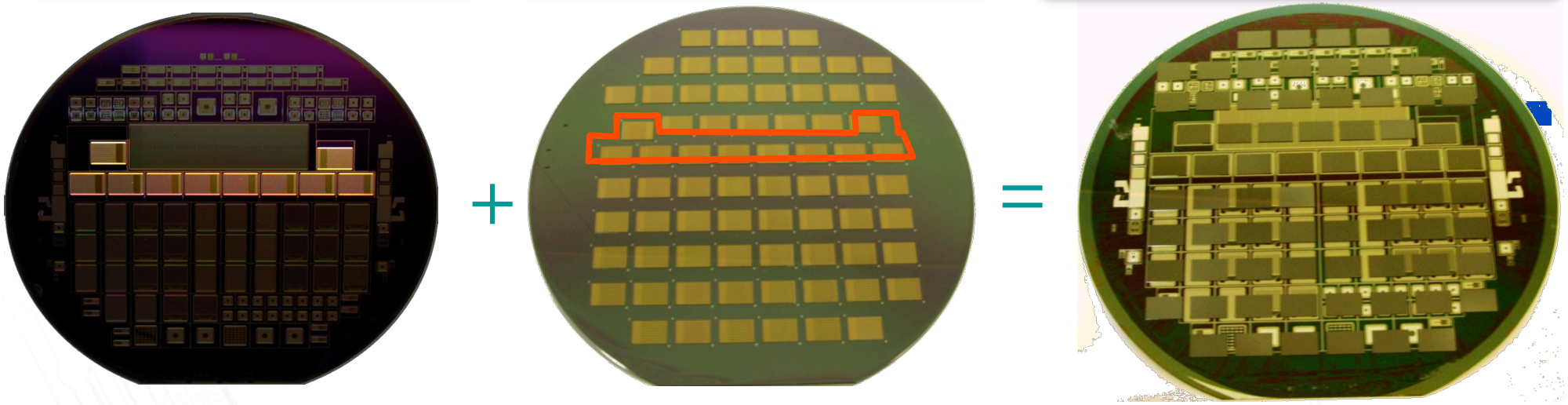
Fraunhofer EMFT

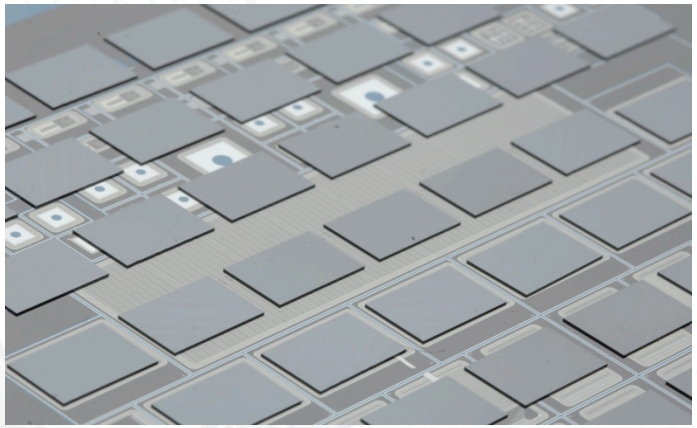
Chip to wafer SLID interconnection (with handle wafer)

Sensor wafer
75 μm active thickness

FE-I3 chips reconfigured on a 6" handle wafer

After SLID interconnection and handle wafer removal

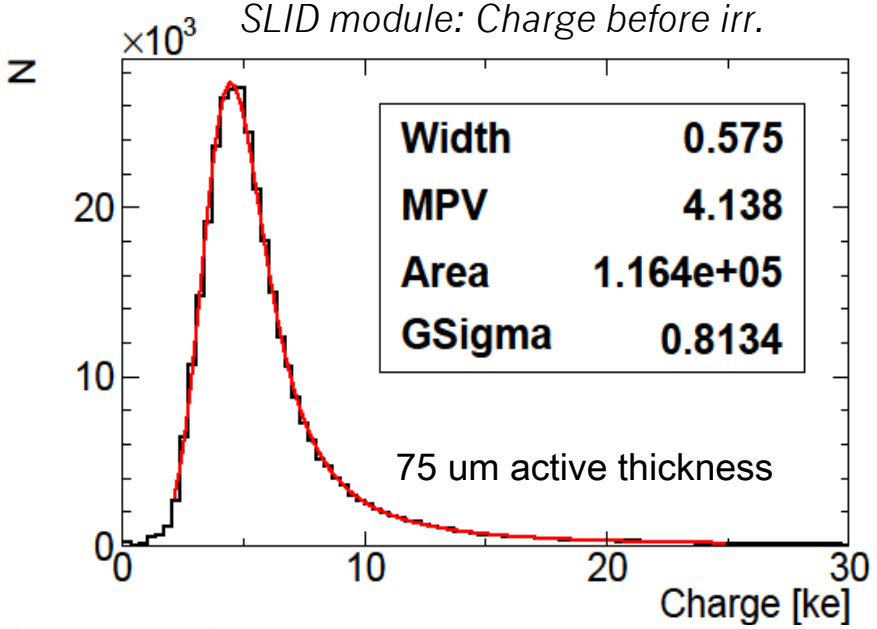


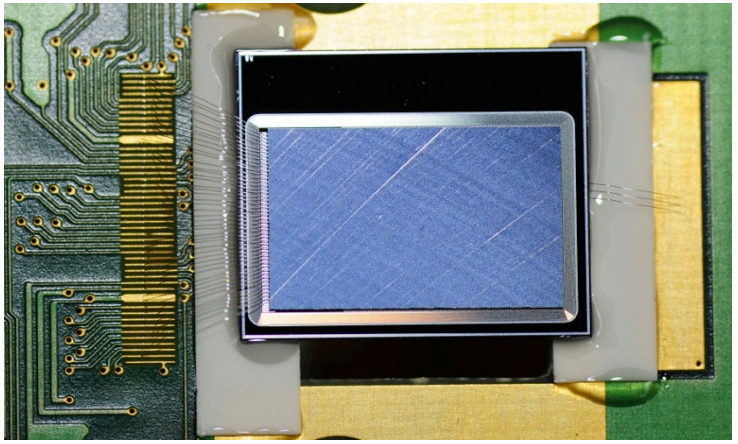


FE-I3 chips (mostly not electrically functioning) used to improve the pressure homogeneity on the wafer during the SLID interconnection

SLID modules characterization

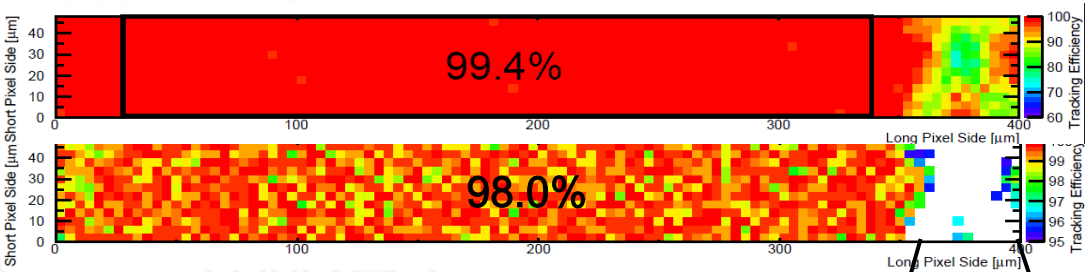
SLID module: Charge before irr.

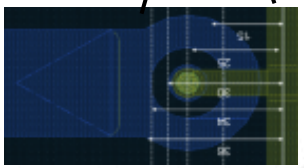




- Good Charge Collection efficiency after irradiation up to $2x10^{15}$ n_{eq}/cm^2

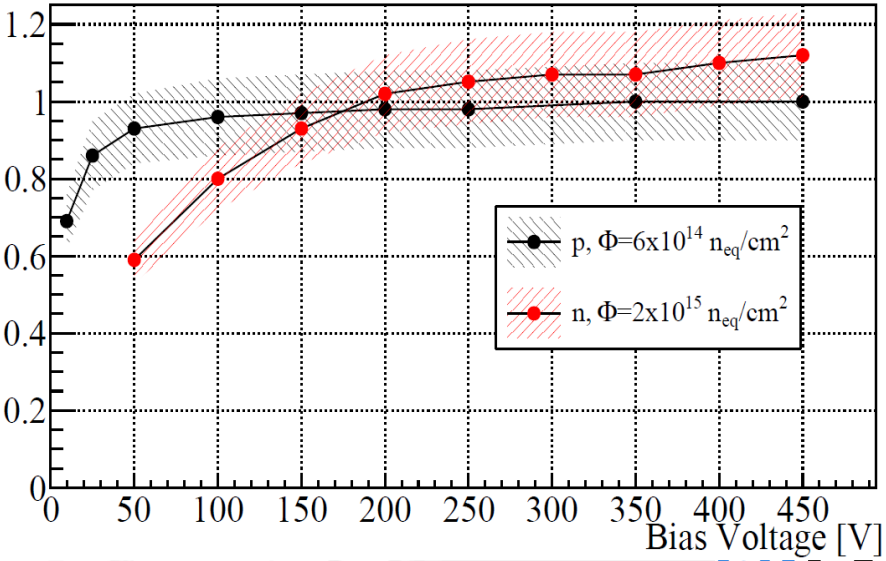
Beam-test: tracking efficiency before irr.



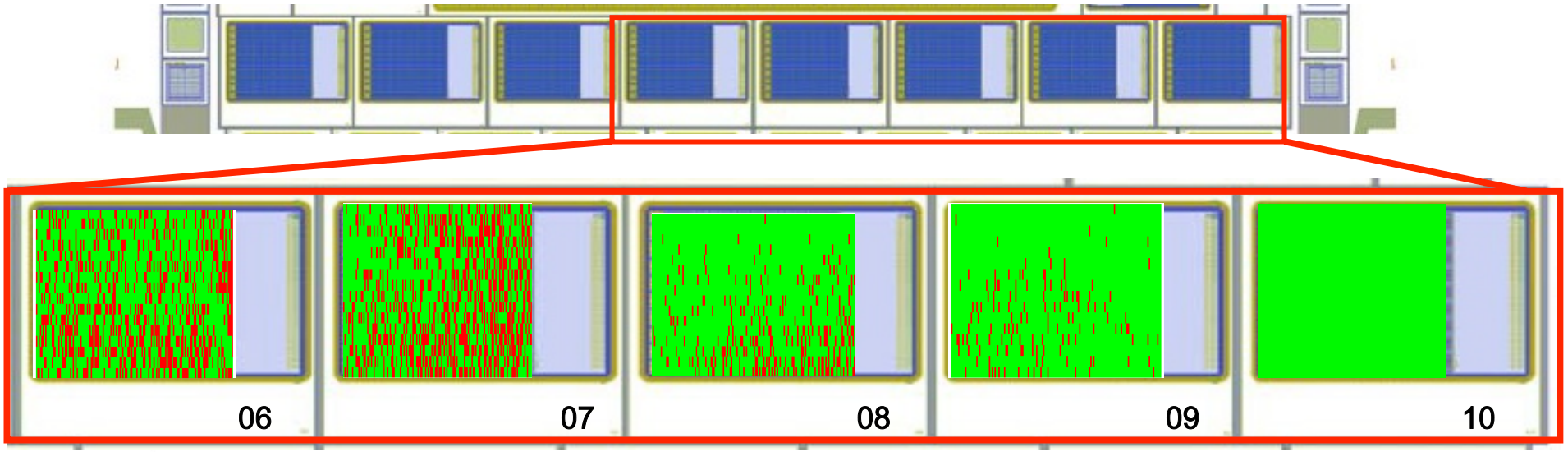


Threshold=2600 e

Need a chip capable of working at lower threshold to achieve ~100% efficiency with very thin sensors → FE-I4



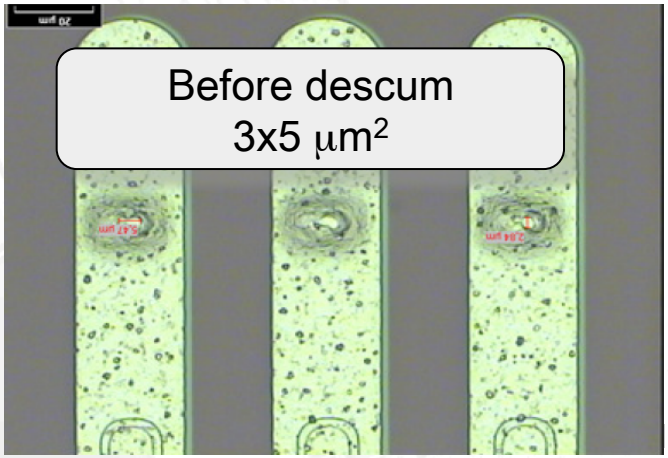
Problem of interconnection efficiency



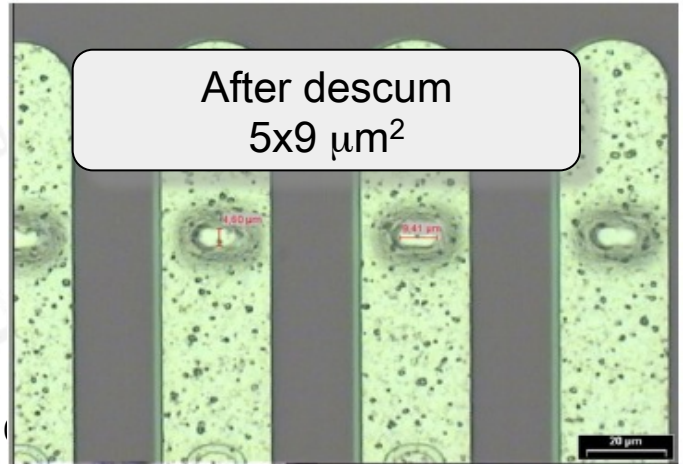
Connected channel

Unconnected channel

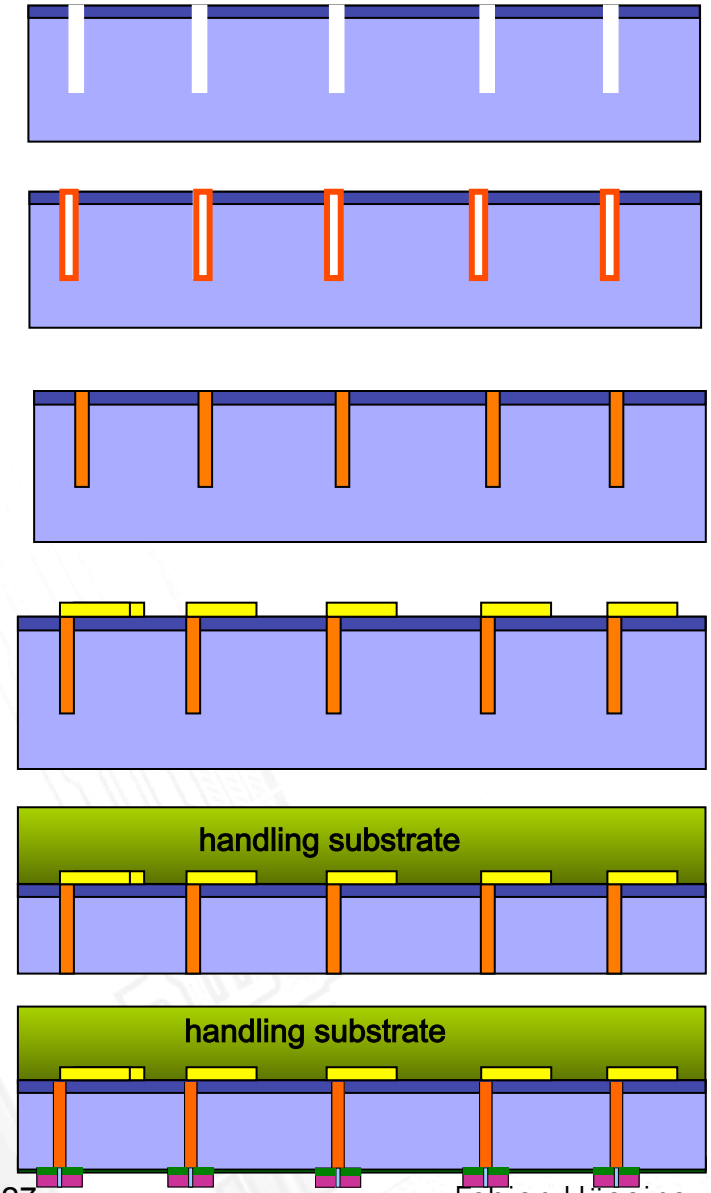
- Low interconnection efficiency towards the center of the wafer
- Not related to SLID interconnection but to bad openings in the BCB passivation in a fraction of the modules



- The problem has been solved with a further etching of the BCB layer for the 2 wafers to be interconnected to the chips with TSV



Through Silicon Vias processing

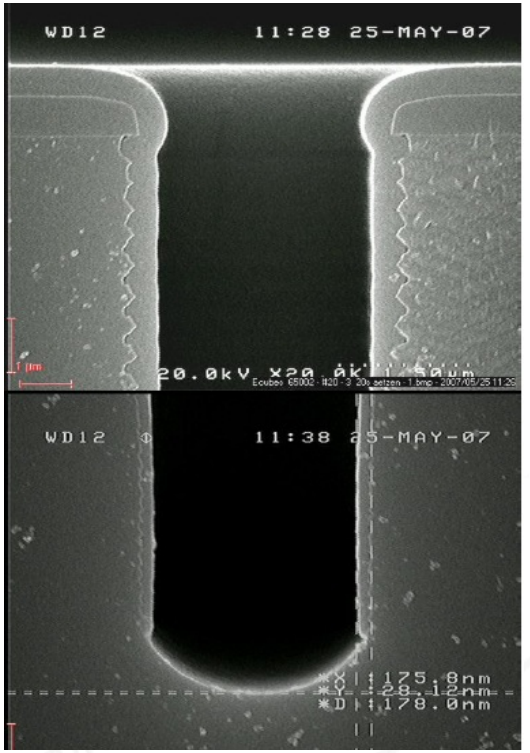


SACVD Pad Planarization, TSV Litho, Etching with Bosch process, cross section ~4x10 mm^2, depth=60 mm

TSV Isolation with SACVD SiO_2 ~ 300 nm

TSV Filling with TiN seed + CVD W

Electroplating of Cu on the front side

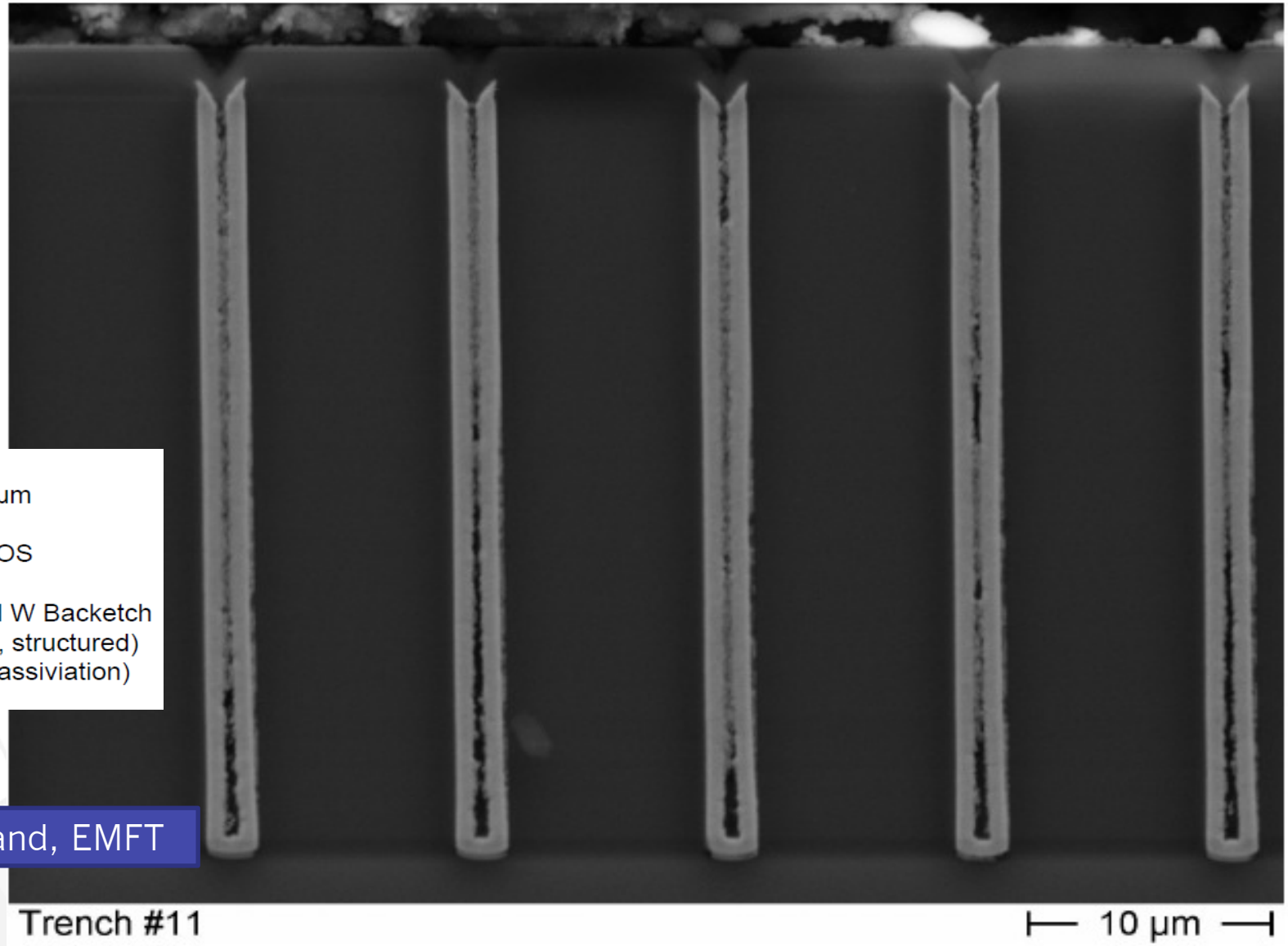


Bonding to handling substrate, thinning to 50 mm

Exposure of W in TSV and Alu spattering for creation of pads on the back-side

Through Silicon Vias processing

Fraunhofer EMFT



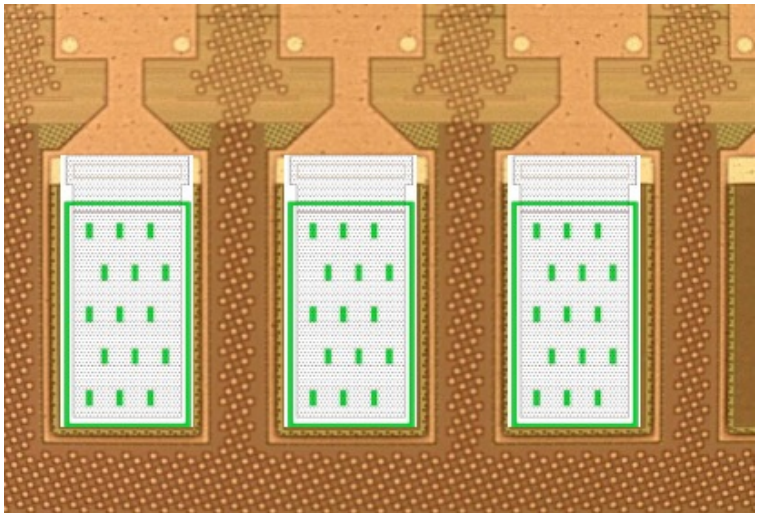
ICV-Dimensions:
3 µm x 10 µm x 50 µm

300 nm SACVD TEOS
20 nm TiN CVD
900 nm W CVD und W Backetch
800 nm M1 (AlSiCu, structured)
850 nm PN/POX (Passiviation)

Courtesy of R. Wieland, EMFT

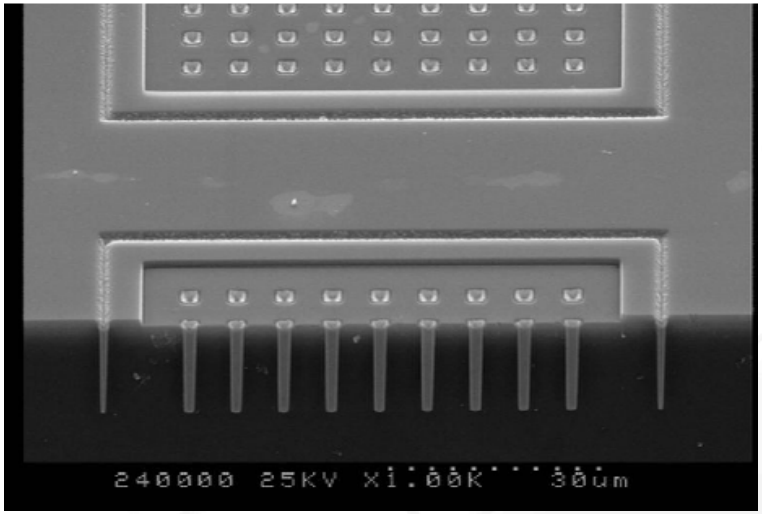
TSV in the FE-I3 chips

Fraunhofer EMFT



➢ First etching trials on dummy wafer ✓

- Performed in the un-thinned FE-I3 chips of one designated test-wafer
- Etched to a depth of ~ 60 mm
- Optimize the trench width to obtain the same depth as in the TSV



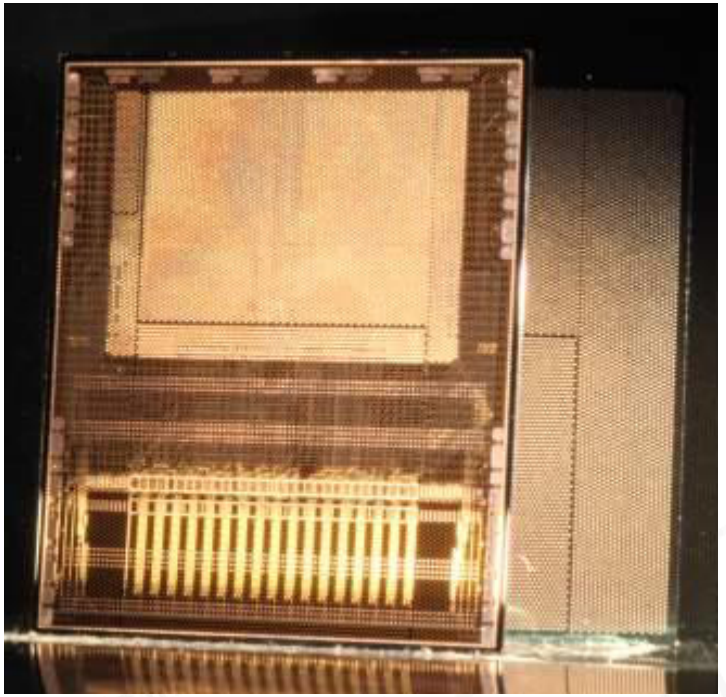
➢ Process plan of the hot FE-I3 wafer

- Local planarisation of the fan-out pads by depositing and etching of SACVD-Oxide ✓
- Perform via etching and filling in the hot FE-I3 wafer
- Connect the readout chip with SLID to the hot sensor wafers

Summary

- HEP community did the 1st successful steps to 3D:
  - Chartered/Tezzaron:
    - demonstrated operation 12µm thin analog tier.
    - 8 more wafer awaits bonding for improved inter-tier connectivity
  - TSV with IZM:
    - demonstrated TSV with backside connection on full FE-I2 modules including BB.
    - FE-I4 TSV modules BB to different sensor types in the next year.
  - SLID/TSV with EMFT:
    - successfully built SLID modules.
    - TSV for backside connection is ahead.

➔ exciting results in 3D integration still to come in the near future!



Source: Fraunhofer IZM