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ECAL-p readout status

ECAL-p LUXE workshop, 24-27 September 2024, Krakow

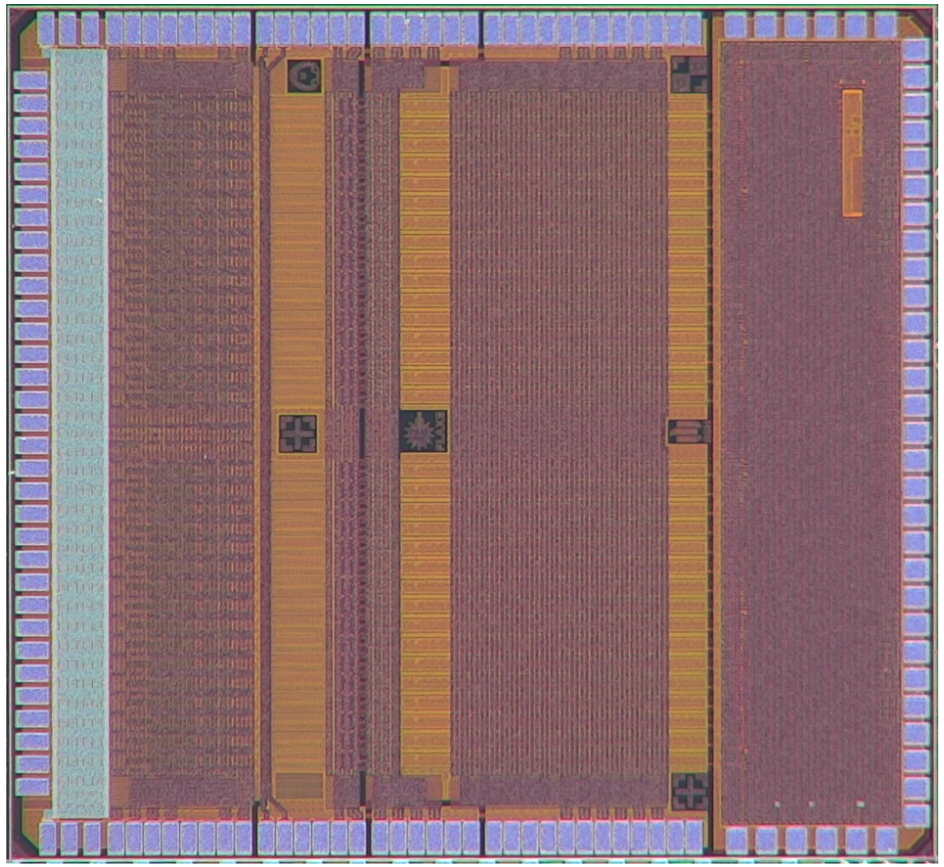
Agenda

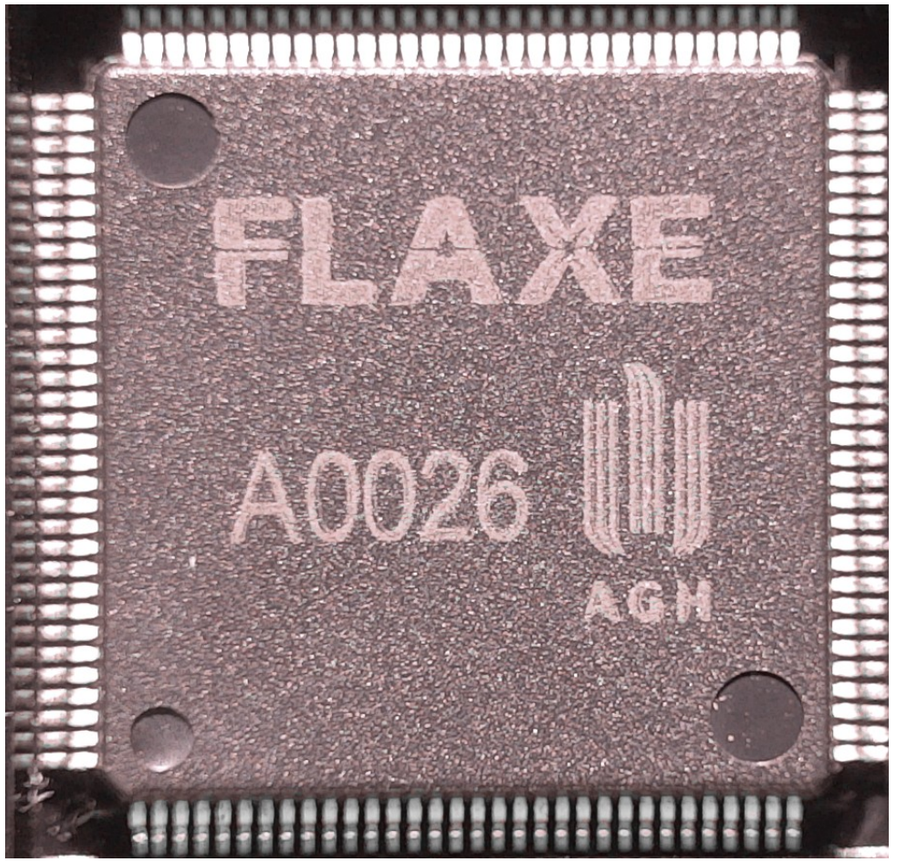
- FLAXE readout ASIC
  - Fabrication and status
  - Results
- Readout status
  - PCBs
  - DAQ – firmware and software

FLAXE ASIC status

- ~1’000 ASICs fabricated in April 2024
  - 100 bare dies (left picture) received for tests mid-June
  - First batch of 142 packaged ASICs (right picture) received mid-July

- Production failed due to (most likely) manufacturing problems – see next slides
- Packaging of the remaining ASICs canceled





FLAXE ASIC status

- Dedicated test setup for FLAXE qualification tests prepared (see next slides)
  - Two bare dies tested initially
  - All 142 packaged ASICs fully tested

- **Only 7 working ASICs found, with 20–30 functional channels each**

  - 35% of the ASICs have shorts in at least one of the power supply domains
  - 54% have extremely large power consumption (>10 times the expected)
    These ASICs shows a lot of errors / non-functional blocks

  - Only 5% of the ASICs works, none without some problems:
    - One have over-current problem
    - All of them have only 20 – 30 working / readable analogue channels
    - All of them have RAM errors (see next slides)

  - Remaining 6% failed at least one of the tests.
    Some of them needs debug, but no miracles expected...

Qualification test results are available online: http://asic.fis.agh.edu.pl/luxe

Be sure to have http, not https in address!

FLAXE ASIC status

ECAL-p readout mass tests Status and yield ASICs Tests description

ASICs data: 0081-0120

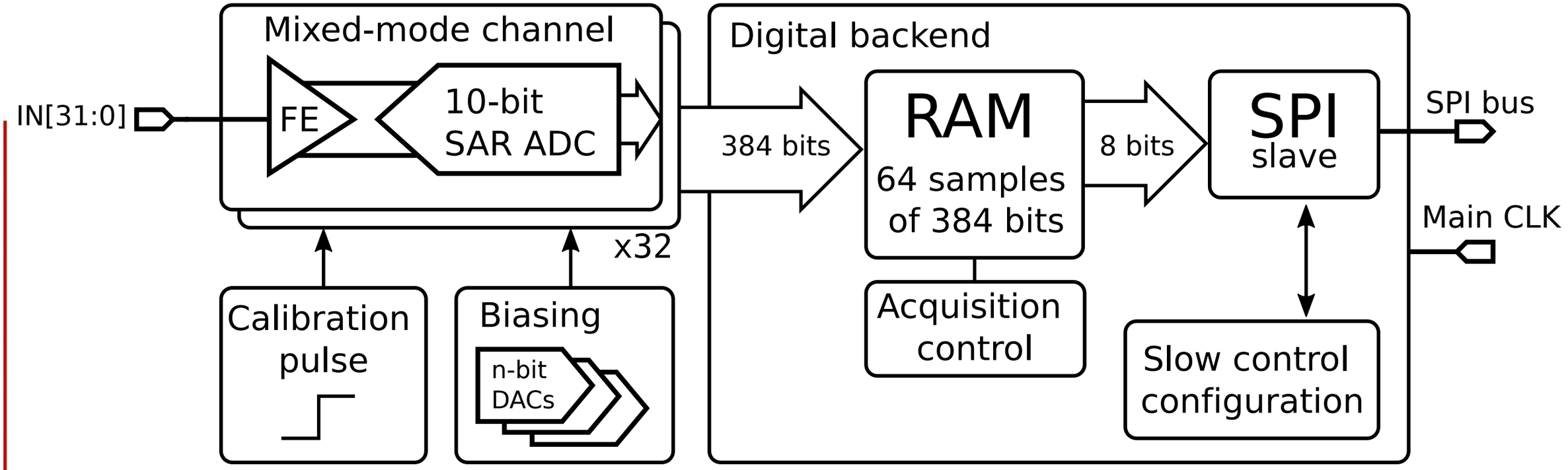
« 1-40 41-80 81-120 121-160 »

http://asic.fis.agh.edu.pl/luxe

Be sure to have http, not https!

	Power supply				SPI		Data		RAM		DACs					Channels						
ID	Shorts	Front-end Sleep / On	ADC Sleep / On	Digital Sleep / On	Read	Write	Pattern	Address	Error map	Counter	Preamp	Shaper	Krum	Calibration	Coarse pedestal	Readable channels	Common range	Pedestal & noise	TrimDAC	Pulse shape	Gain	
0080 FAIL	PASS	4.80	185.22	283.34	57	60																Details
0081 FAIL	PASS	-0.10	0.03	0.02	14	60																Details
0082 FAIL	FAIL																					Details
0083 FAIL	FAIL																					Details
0084 ACC.	PASS	2.00 32.95	6.35 16.00	36.05 36.92	1	2	0	0	154	0	PASS	PASS	PASS	PASS	PASS	31	13	29	28	16	27	Details
0085 FAIL	PASS	3.42	339.09	304.56	57	60																Details
0086 FAIL	PASS	0.02	0.03	159.56	62	60																Details
0087 FAIL	PASS	0.00 30.82	0.00 8.18	60.84 62.17	0	6	0	0	2048	0	PASS	PASS	PASS	PASS	PASS	0	64					Details

FLAXE ASIC

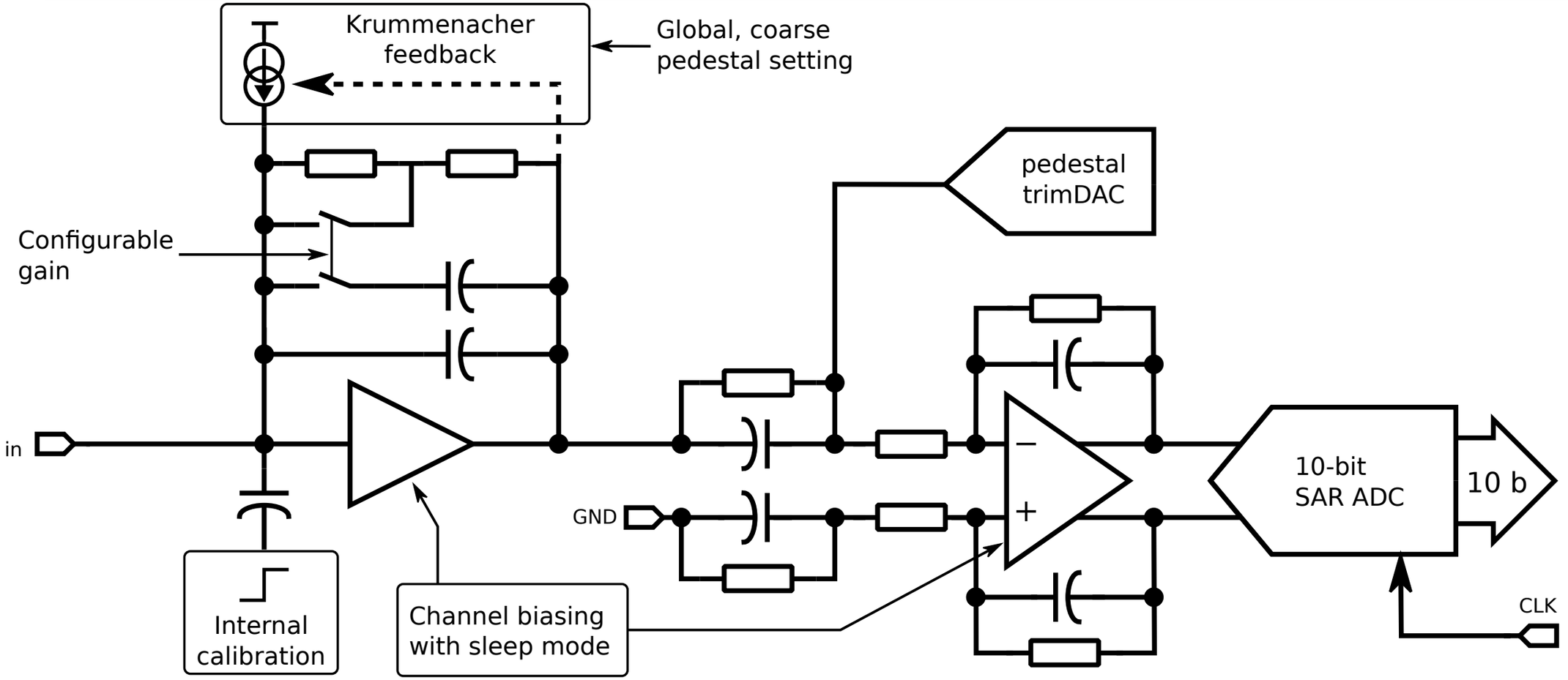


Complete SoC, 130 nm CMOS technology

- 32 channels with preamplifier, differential CR-RC shaper and 10b SAR ADC each
- Internal biasing and calibration
- Internal DAQ with RAM for 64 consecutive ADC samples from all channels
- SPI bus for data readout and slow control ASIC configuration

All the blocks have to operate correctly to enable the data acquisition

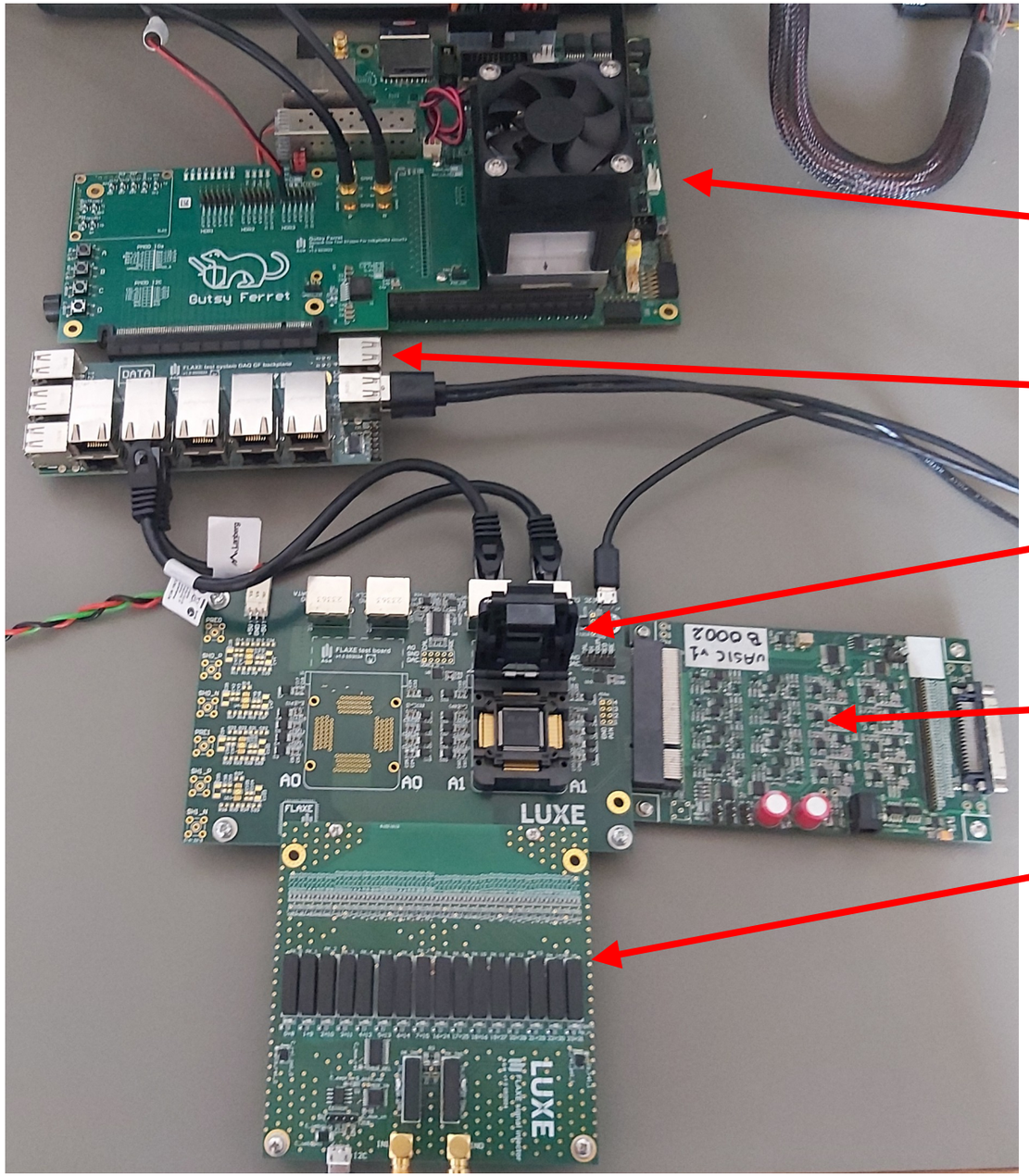
FLAXE channel



FLAME front-end channel with two improvements

- Preamplifier with two configurable gains
- Fully differential CR-RC shaper with 50 ns peaking time
- 10-bit SAR ADC working nominally at 20 MSps
- Sleep mode for power saving between bunch crossings
- Channel trimDAC range increased to cover pedestal spread

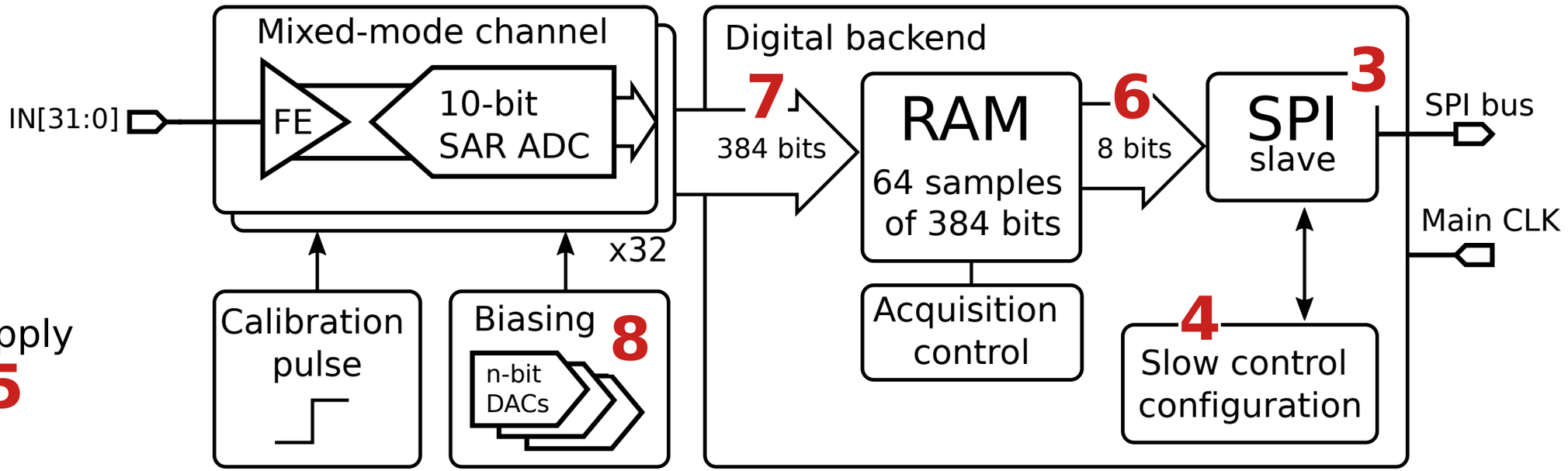
FLAXE qualification tests – setup



Custom setup build for mass tests and qualification of FLAXE ASICs

- DAQ on Zynq TEBF0808 development board (the one for FLAME TB)
- Custom interconnection board for RJ45 cables foreseen for final setup
- Custom test PCB with ZIF (zero insert force) socket for LQFP128 package
- Programmable multi-channel power supply board with monitoring
- Multichannel signal injector emulating the sensor signal
- Agilent 81150A signal generator (not shown) for clock and signal generation

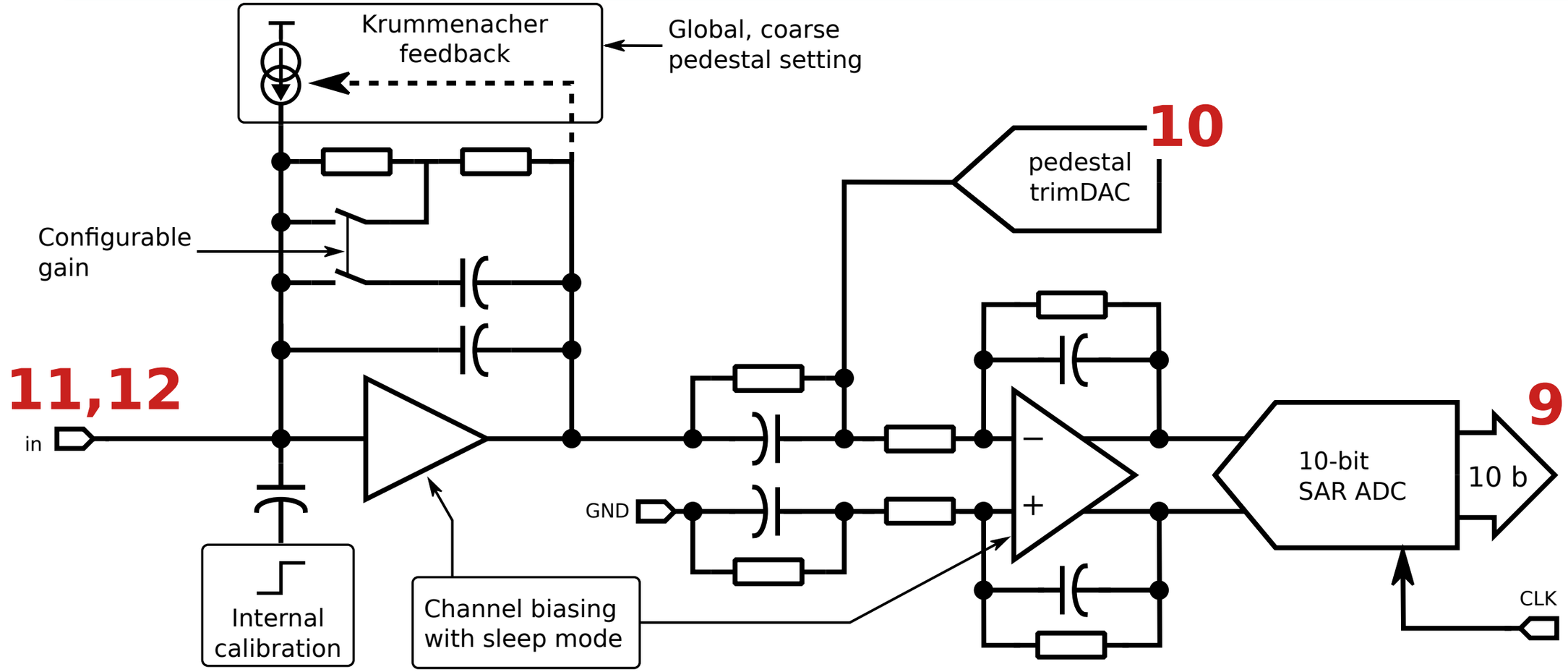
FLAXE qualification test



Power supply
1,2,5

1) Test for shorts on power supply domains: power up for 1s and measure current
2) Measure power consumption in sleep mode
3) Test SPI communication by reading default values from registers
4) Test slow control configuration by writing all possible values
5) Turn of sleep mode via SPI and measure power consumption
6) Test SPI data packager replacing data from RAM with known constant
7) Test RAM by writing known values to it and read through data package
8) Test biasing circuitry through external monitoring outputs
9-12) Test channels (next slide)

FLAXE channel

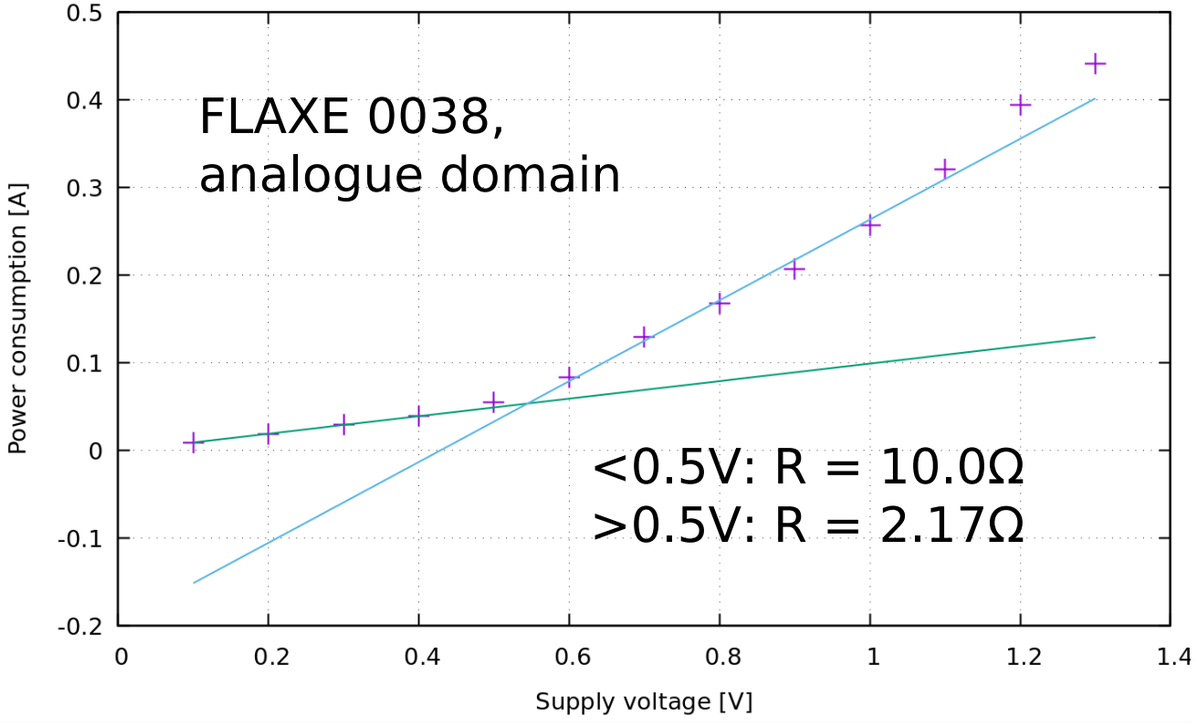


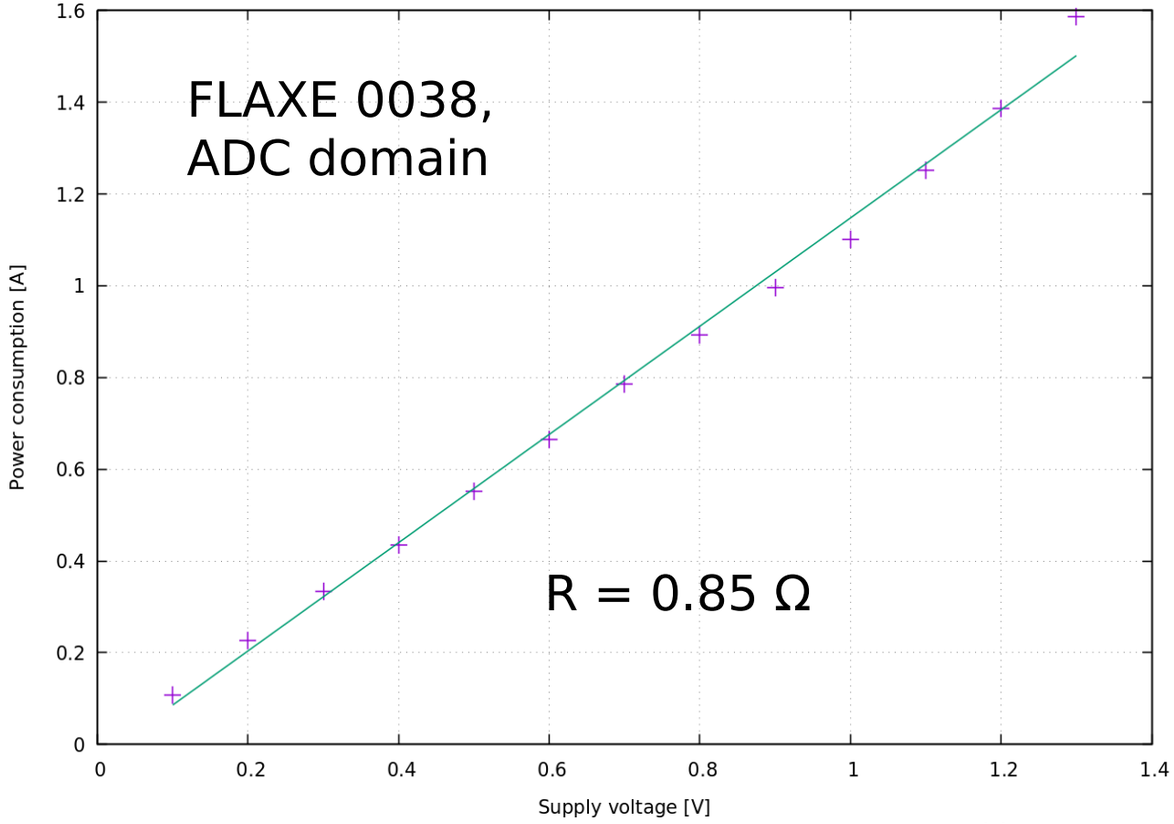
9) Measure nominal pedestal and noise
10) Measure trimDAC response
11) Inject signal, measure pulse shape and peaking time
12) Measure front-end gain using synchronous mode (ADC sample taken directly at pulse maximum, without need for deconvolution)

FLAXE ASIC – power consumption

- 35% of the ASICs have shorts in at least one of the power supply domains
- 54% have extremely large power consumption (>10 times the expected)
- It is **not** related to packaging – we tested two bare dies and both showed shorts
  - One die viewed via IR camera – short clearly located in one of ADC channels

- Shorts are either fully resistive, or shows two resistive components
- Issue not yet understood...



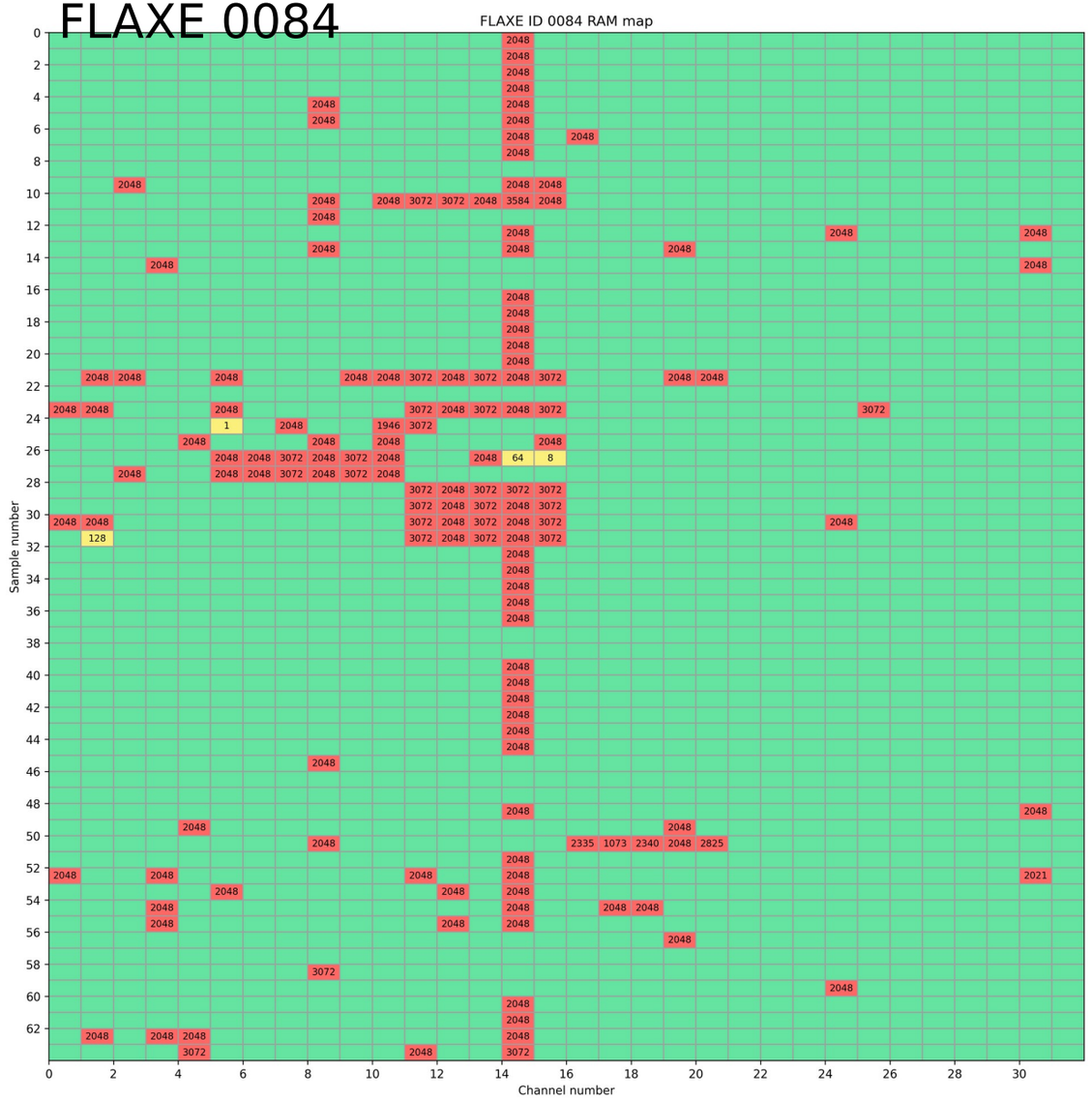


FLAXE qualification tests – RAM

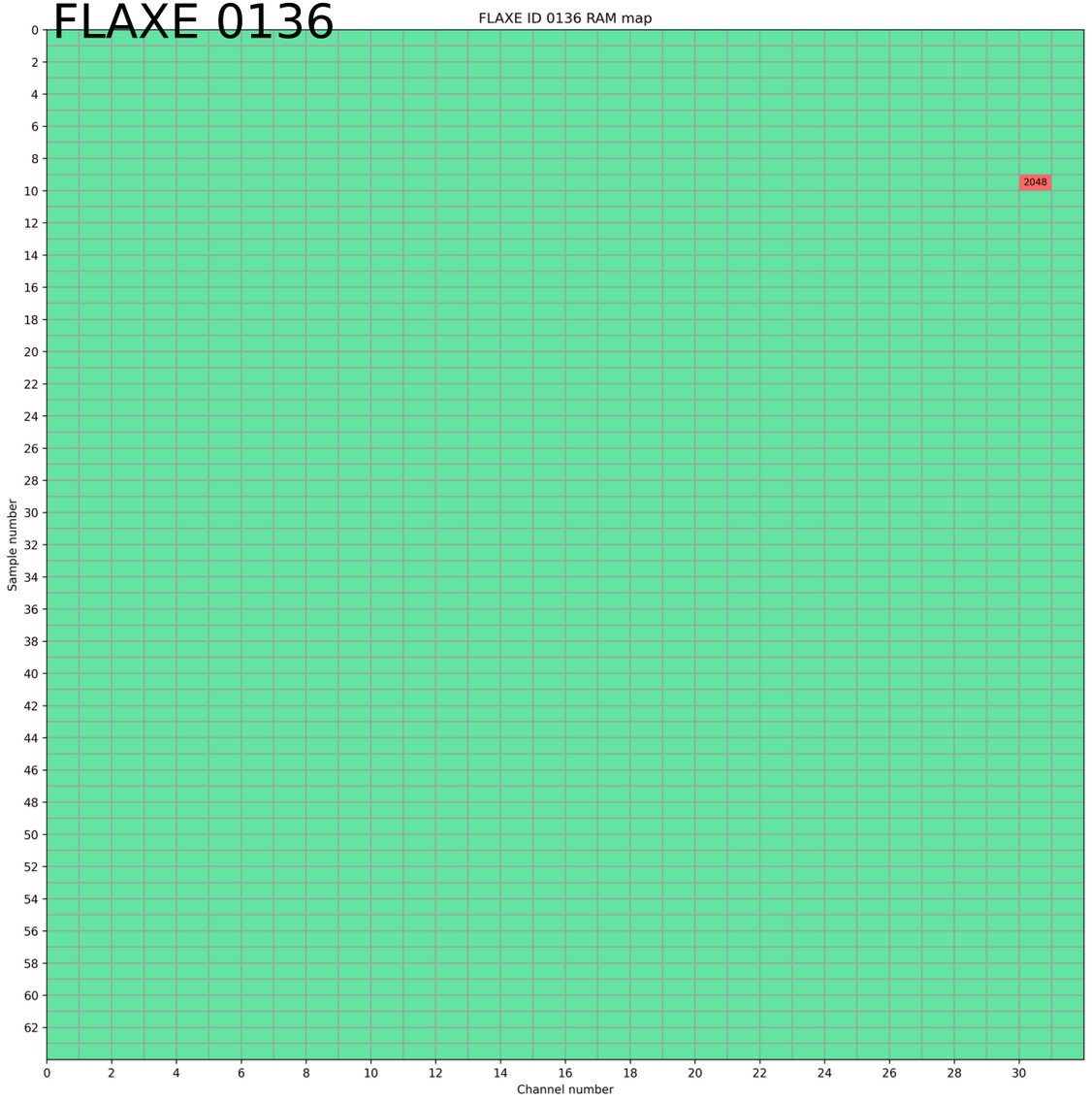
- Sample number = time – vertical axis
- Channel number – horizontal axis

- Green no errors in cell
- Yellow or red – damaged, unusable cell

FLAXE 0084

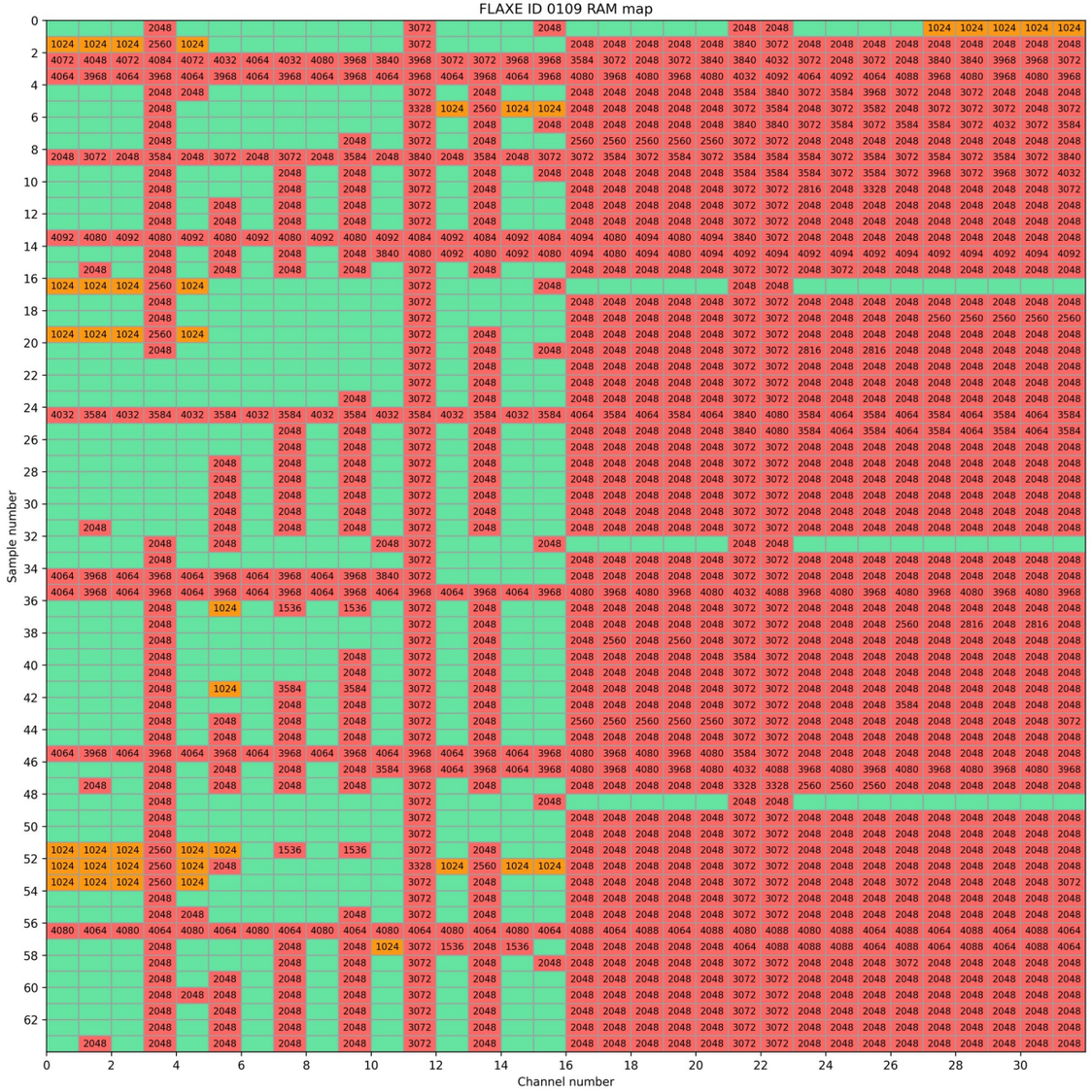


FLAXE 0136



FLAXE qualification tests – RAM

FLAXE 0109



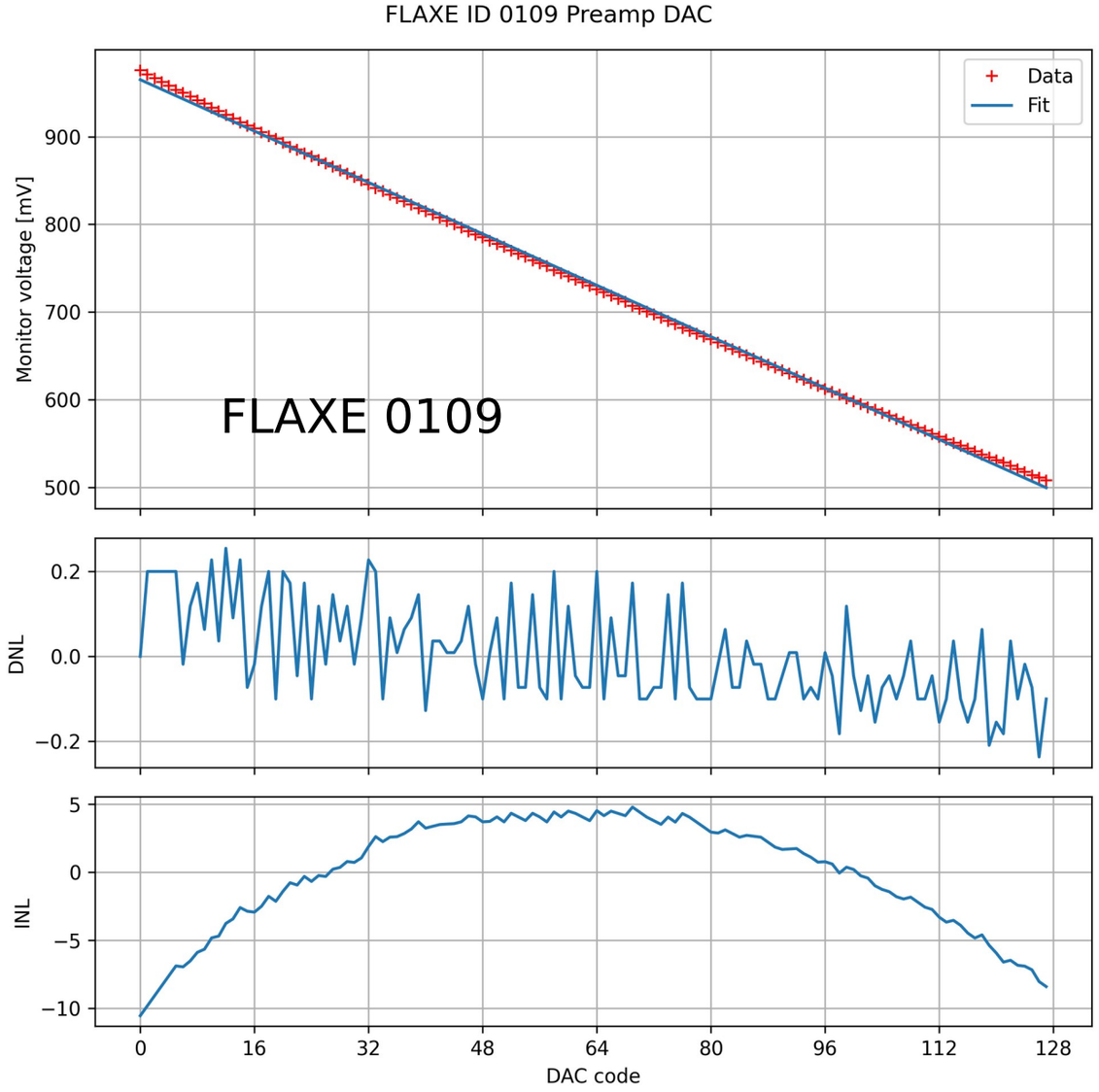
- All ASICs reports errors in RAM
- The best one have 1 damaged cell

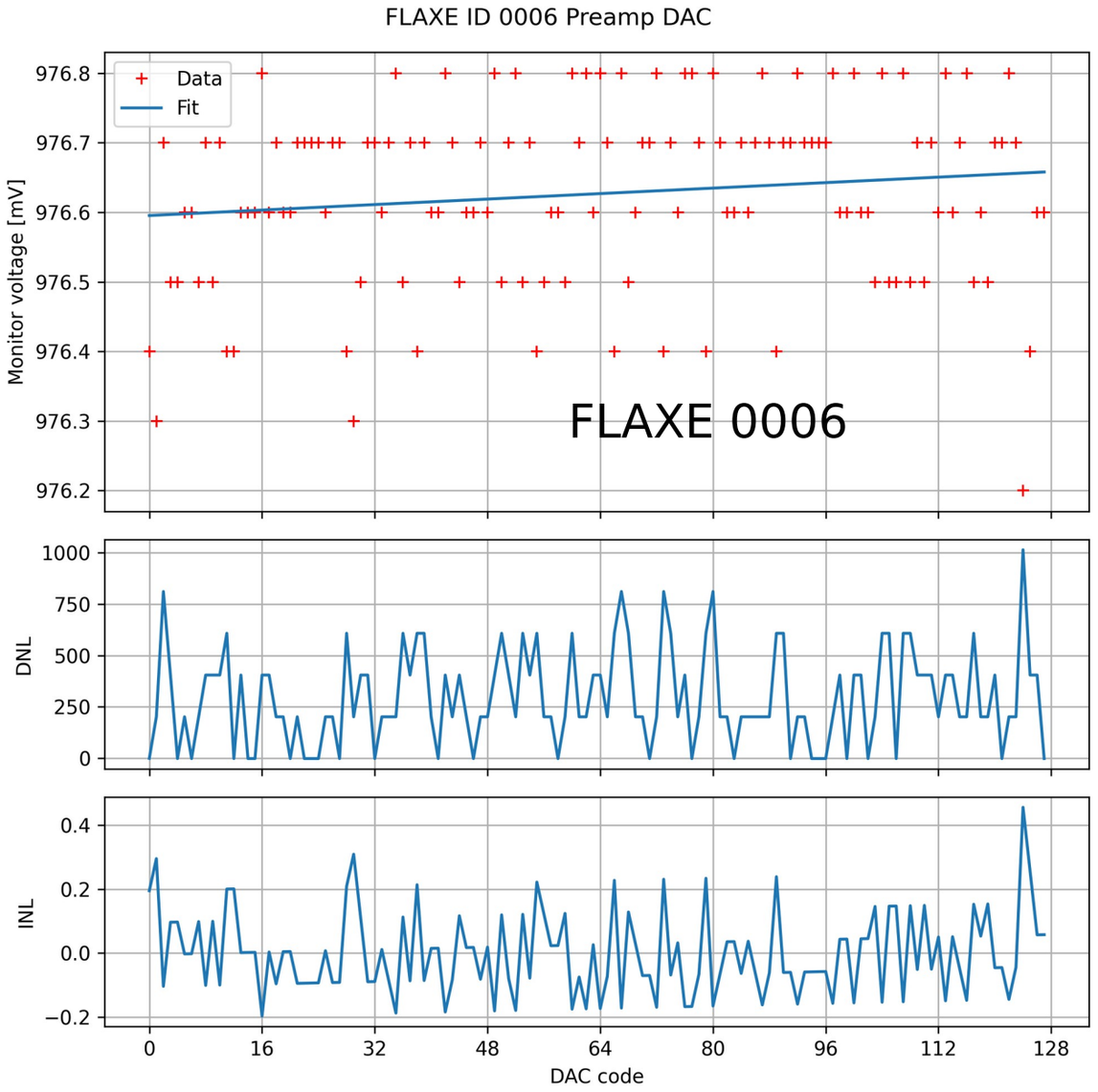
Preliminary conclusions:

- There seems to be correlation between amount of RAM errors and power consumption
- Large power consumption results in voltage drop across digital part affecting the memory (e.g. timing)
- But there are ASICs with expected power consumption and errors in RAM
- This issue have to be resolved before ASIC re-submission

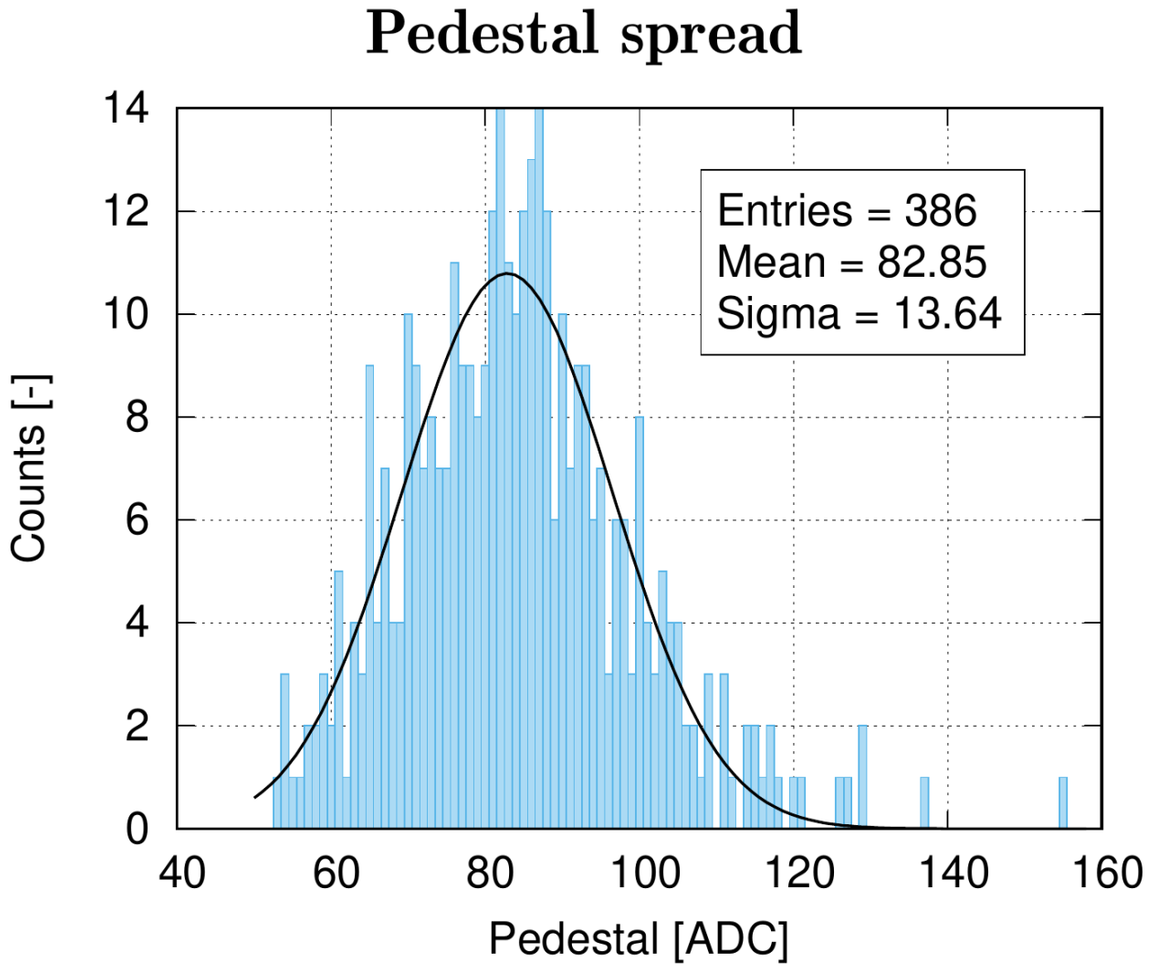
FLAXE ASIC – biasing DACs

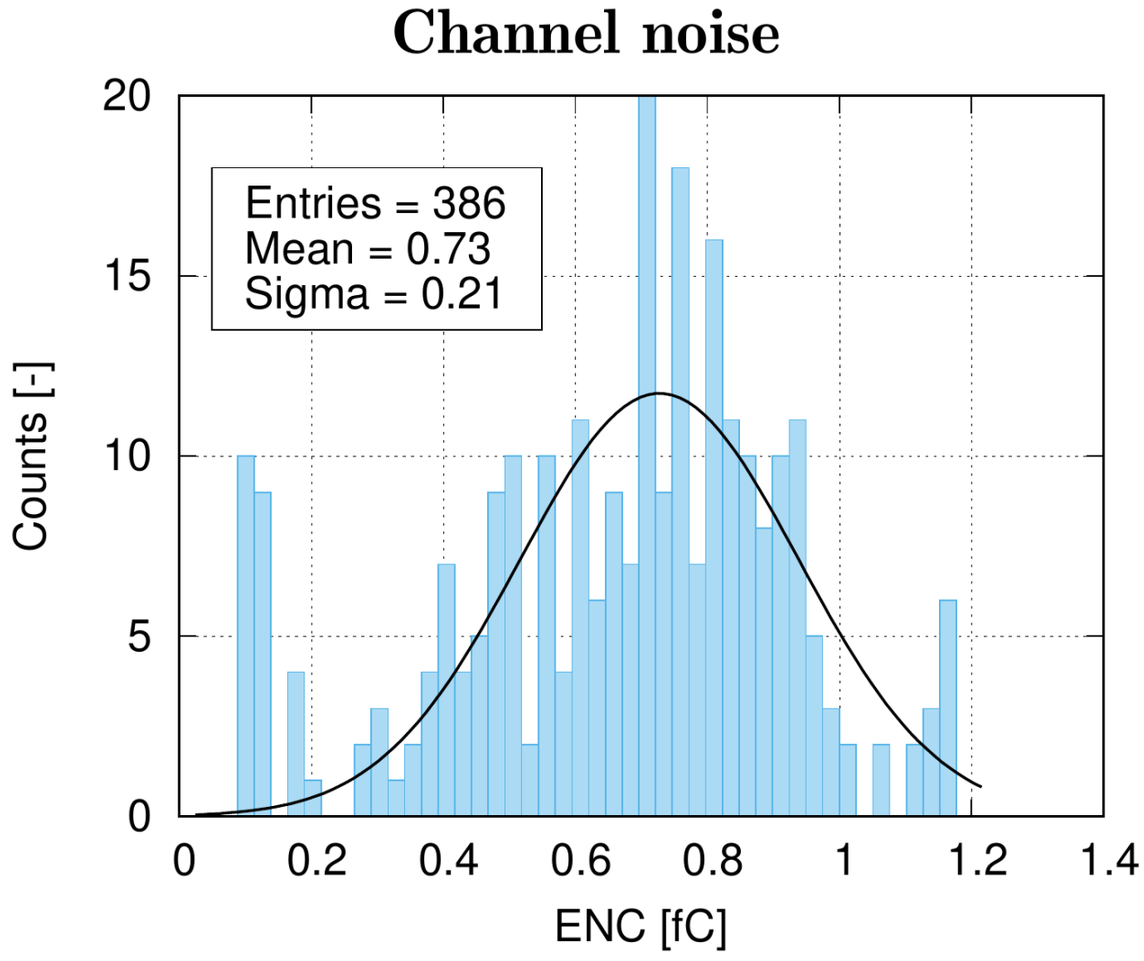
5 DACs measured: preamplifier, shaper, krummenaher, calibration and coarse pedestal





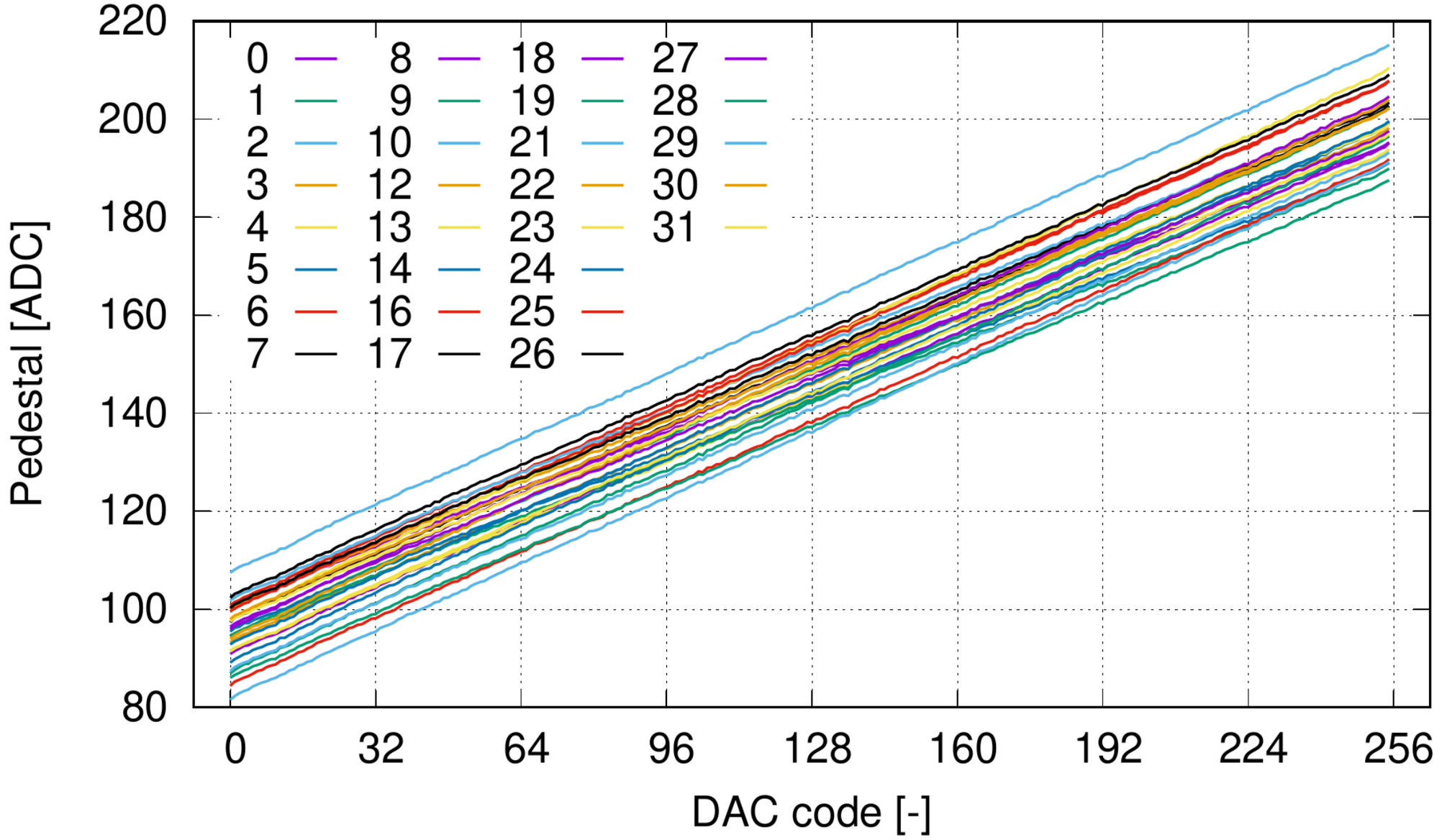
FLAXE ASIC – pedestal and noise





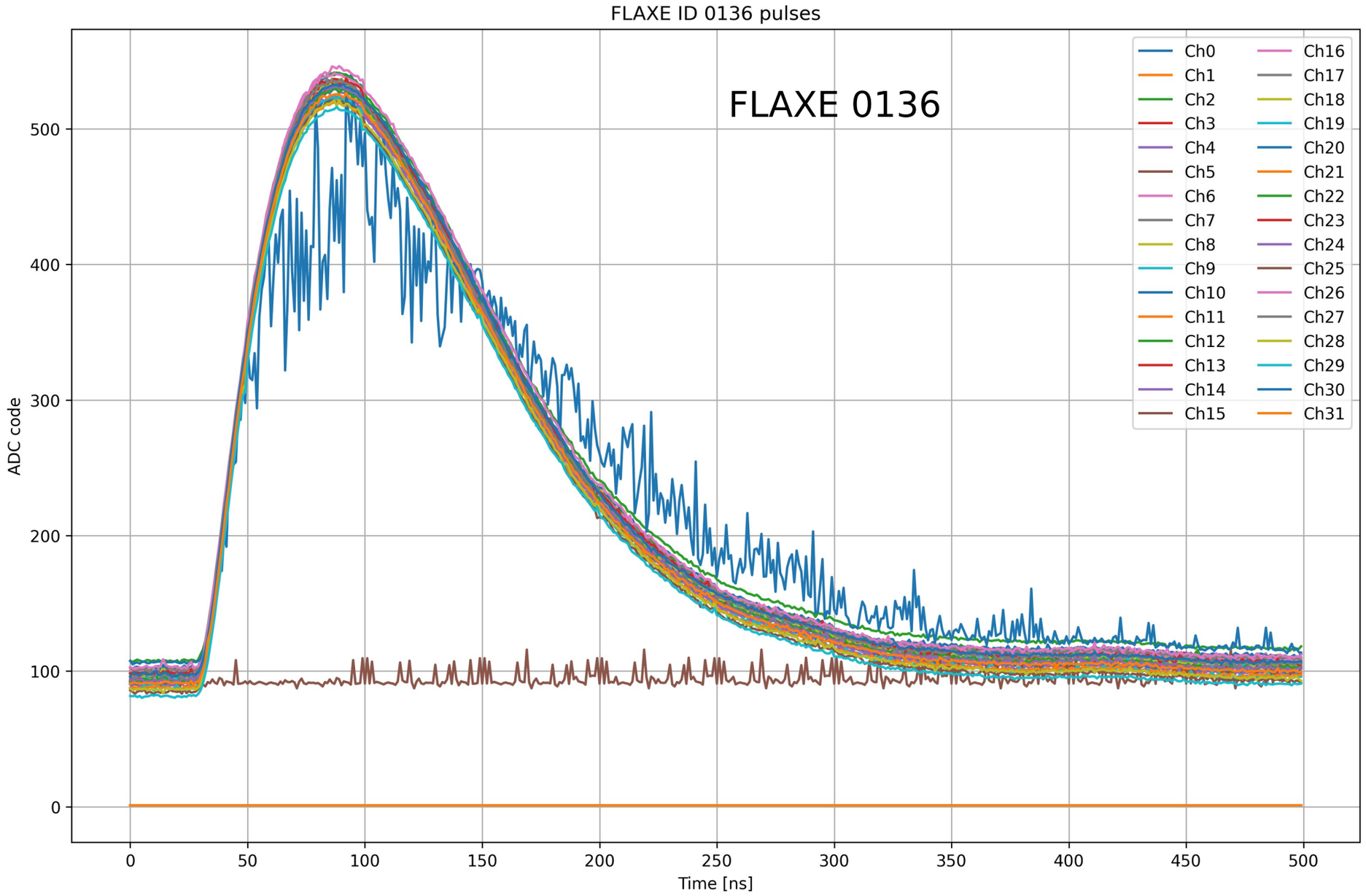
- Pedestal nominal value and spread as expected
- **Setup not optimized for noise measurement** (ENC = 0.73 fC → 2.9 ADC)
  On the last testbeam we were able to reduce the noise to ENC < 0.3 fC !

FLAXE ASIC – channel trimDAC response



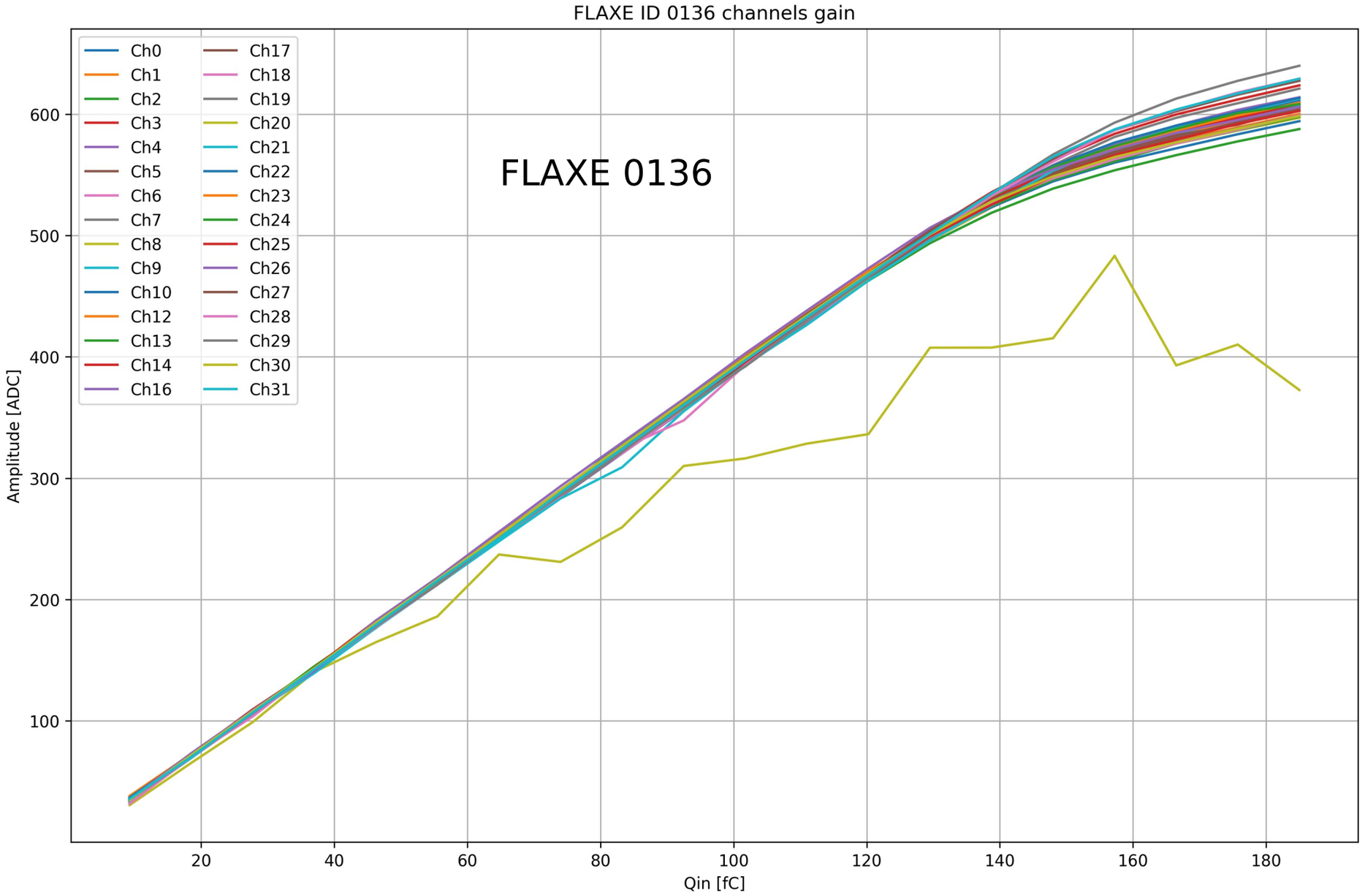
Trimming range sufficient to cover pedestal spread – improvement over FLAME

FLAXE ASIC – channel pulse response



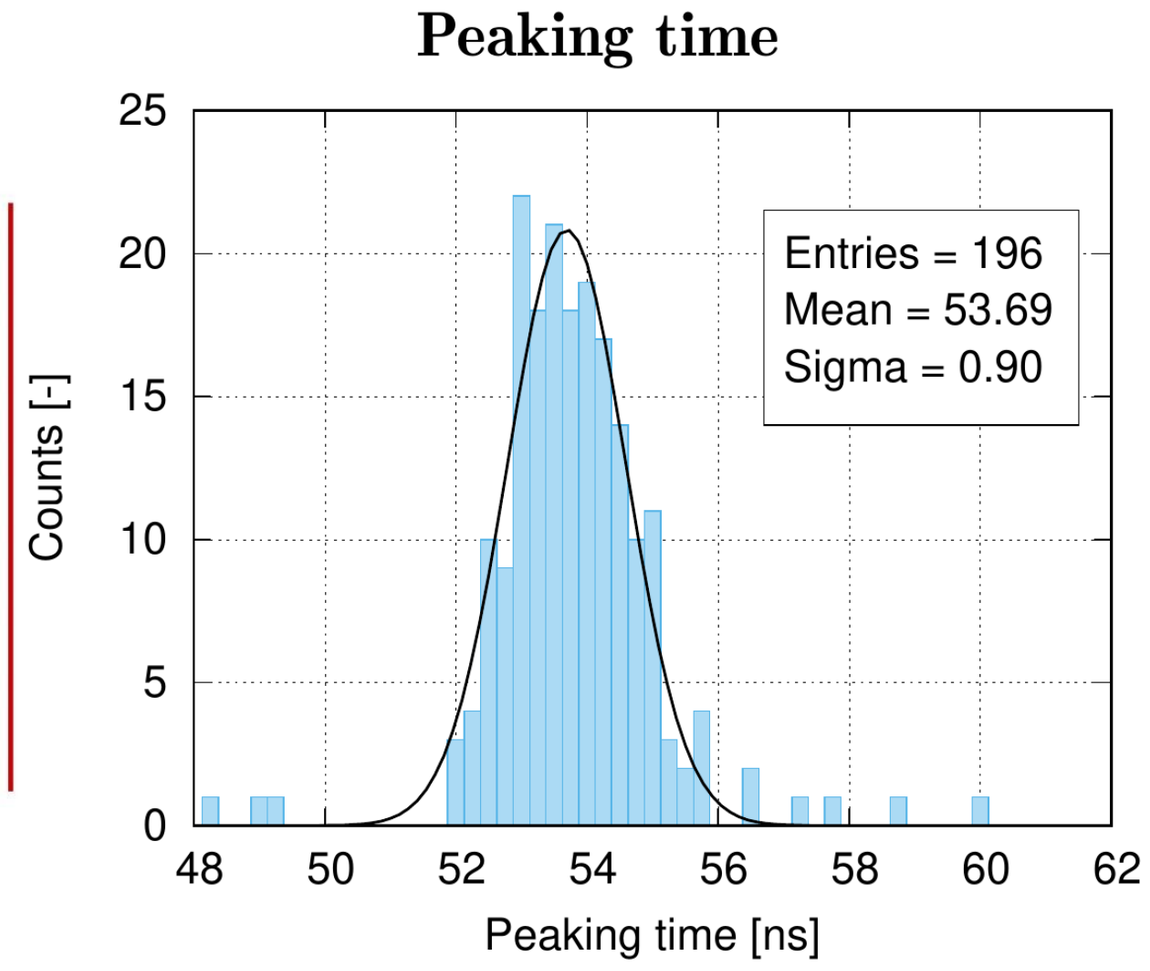
- Good pulse shape with <5% DNL to ideal CR-RC
- Peaking time of 54 ns
- One “noisy” and two dead channels (no response to sensor signal)

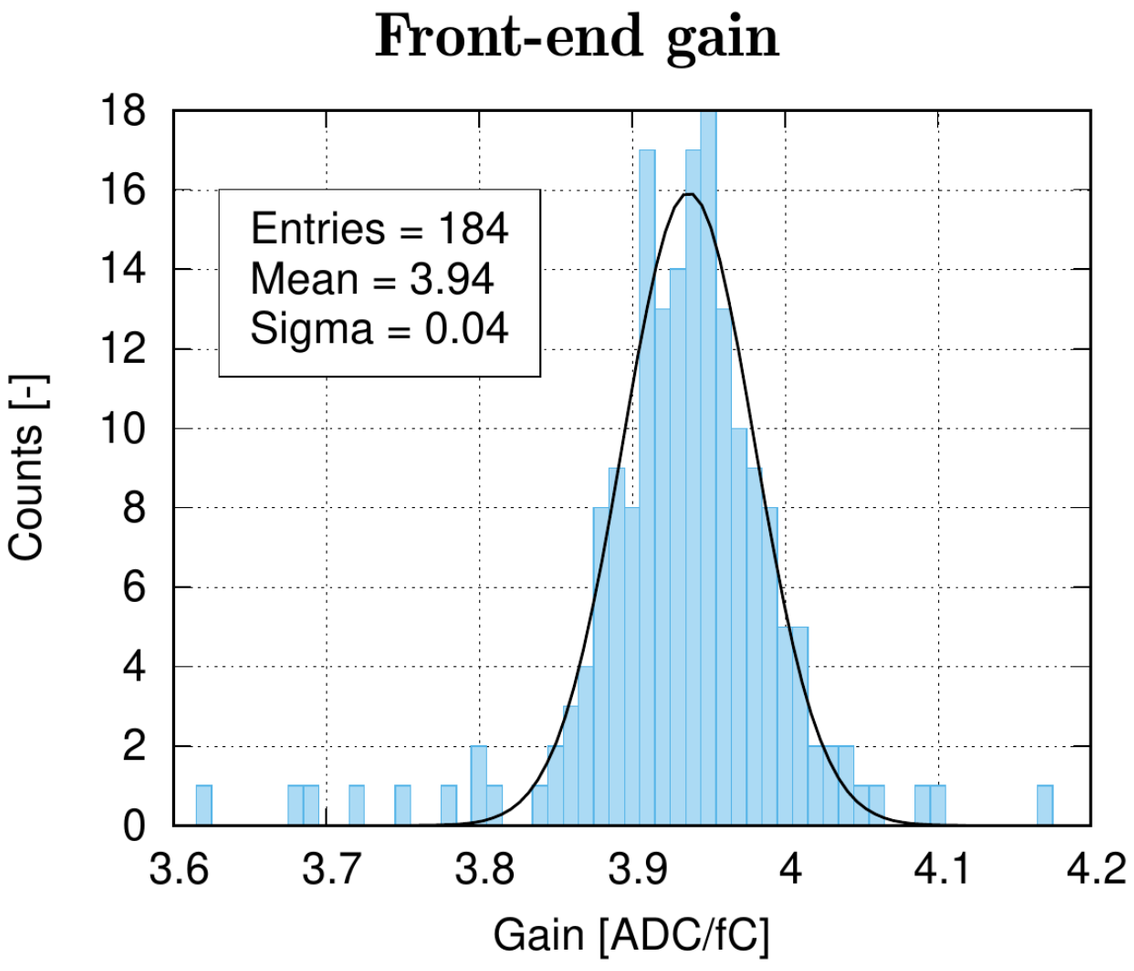
FLAXE ASIC – channel linearity and gain



- Only high gain measured
- Gain 4 ADC/fC exactly as designed
- Linear range up to 150 fC
- One “strange” channel (needs further investigation)

FLAXE ASIC – channel response





- Channels in working ASICs behaves exactly as expected with all parameters well within specification
- Only 184 channels passed all tests (4% from 4,544 total channels in 142 ASICs)

FLAXE ASICs summary

- ~1000 ASICs fabricated, 142 packaged and tested
- Manufacturing problem result in catastrophic yield

- **Only 7 ASICs works at all, with 20 – 30 good channels each**

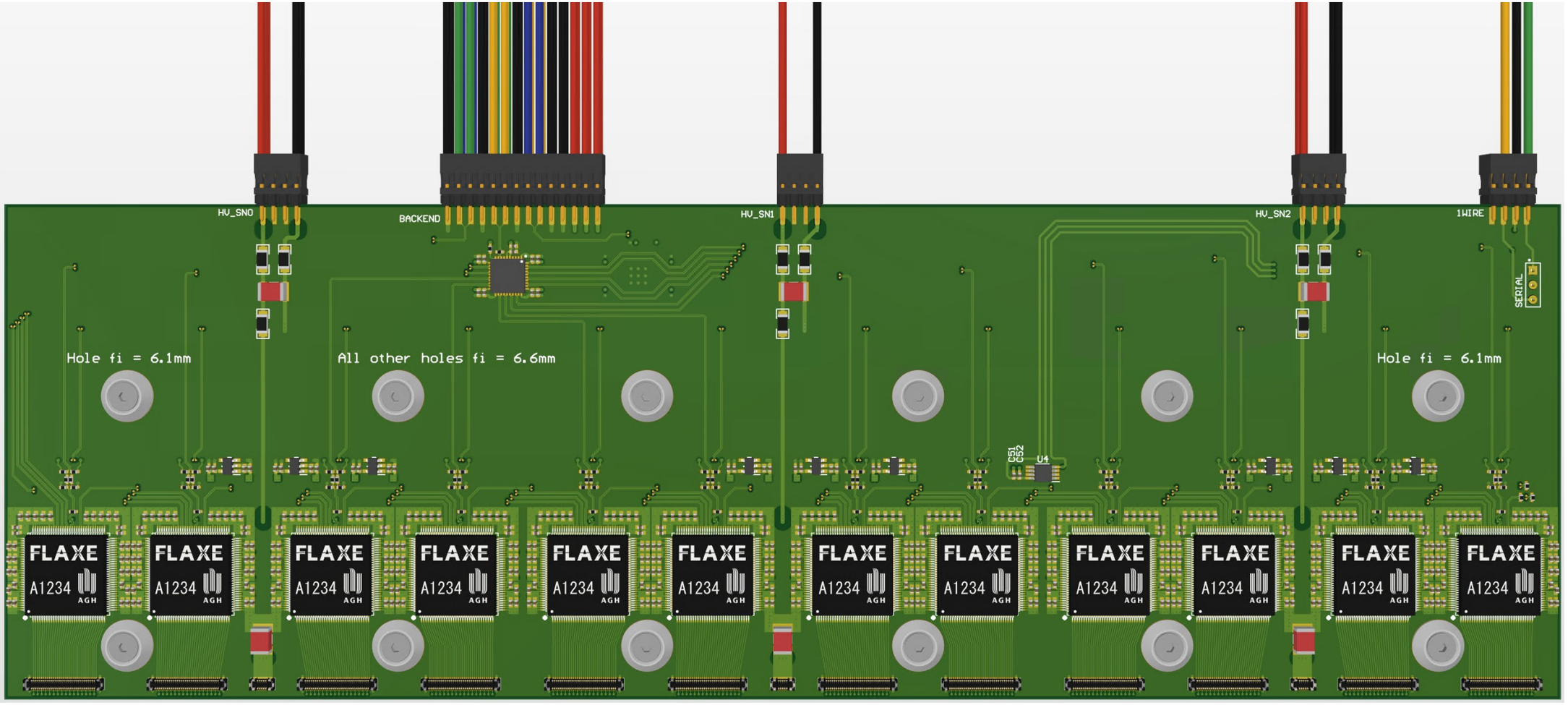
- It seems to be enough to read one (maybe two) sensors (but only part of each)

- **Does it make any sense to organize testbeam with one sensor plane?**

- We are going to re-submit FLAXE for another engineering run, most likely at the end of this year
  - First, we need to be sure that design itself is errorless
- Realistically, looking at this production process, we can expect packaged ASICs somewhere in mid-2025

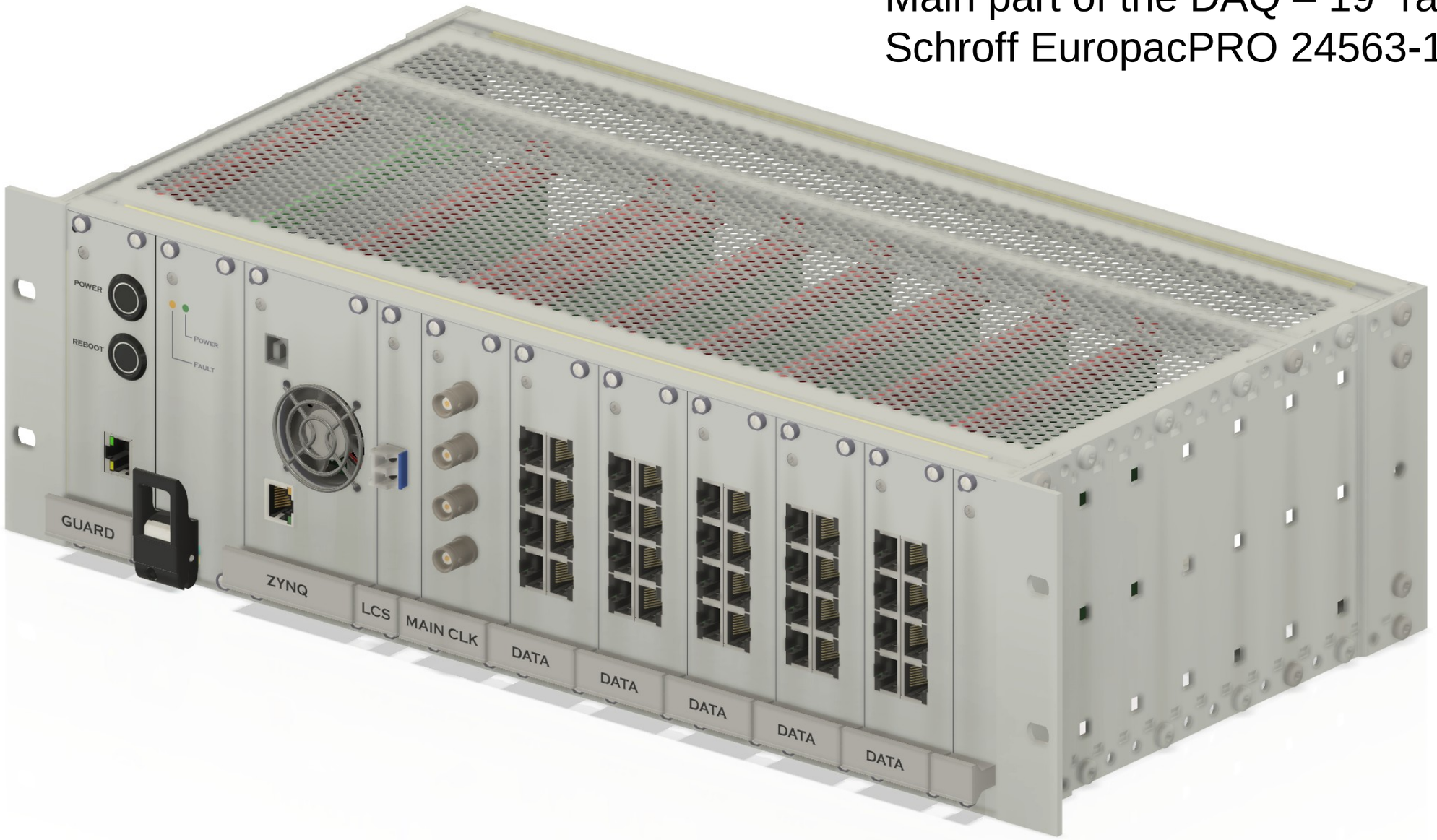
PCB status – FEB

- FEB designed (but for FLAXE with “normal” power consumption)
- For TB with current ASICs some modifications may be needed
- “Dummy” version for mechanical integration postponed due to administrative problems first, later due to test setup preparation and ASICs debug

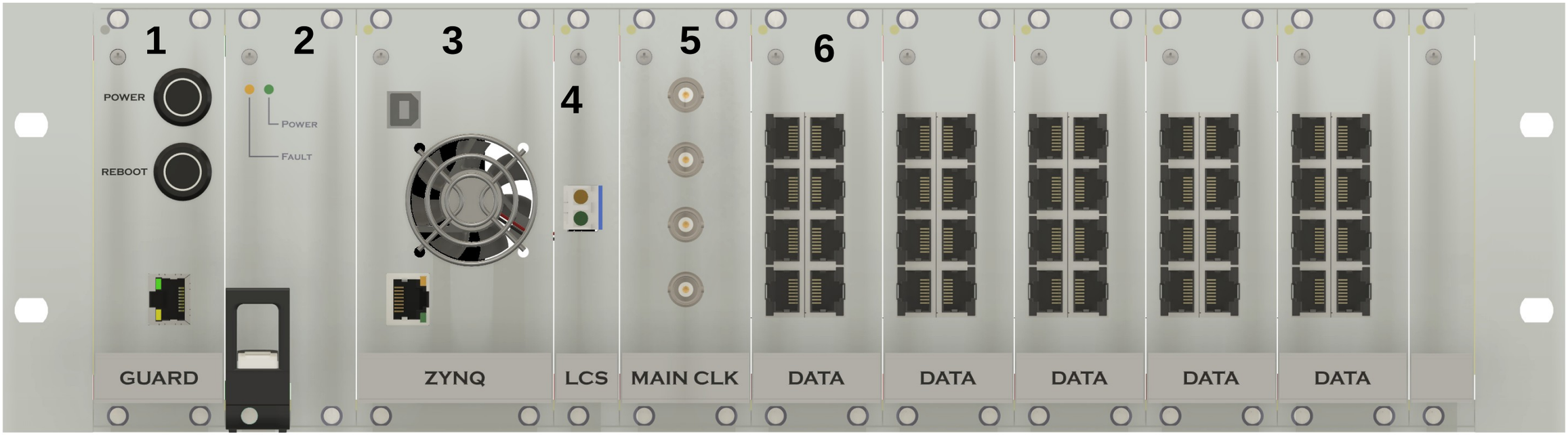


Readout hardware – DAQ rack

Main part of the DAQ – 19” rack
Schroff EuropacPRO 24563-142

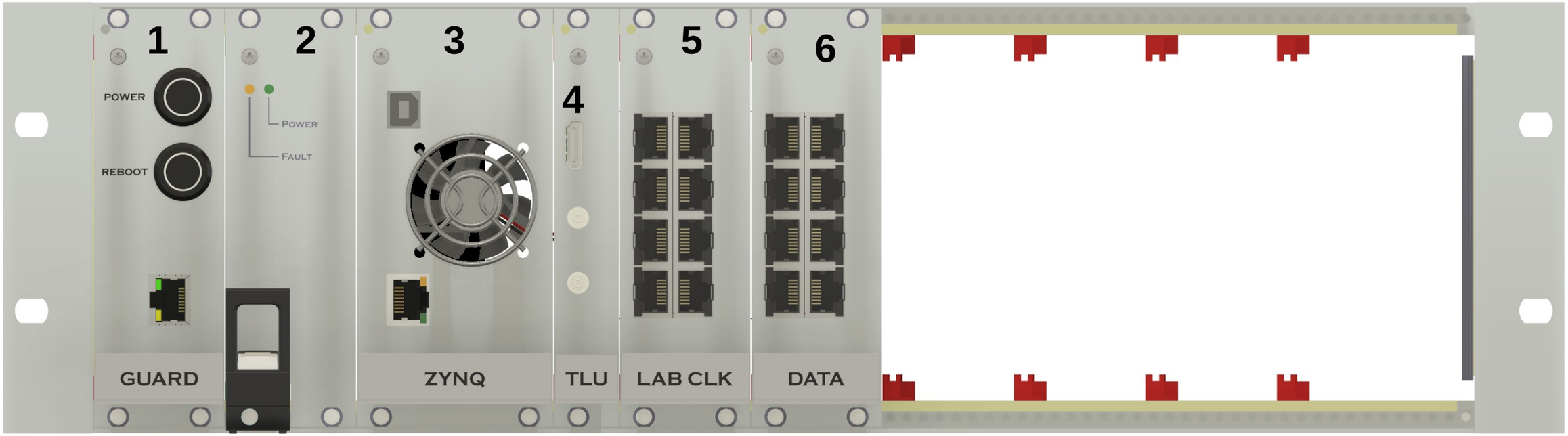


Readout hardware – DAQ rack – experiment configuration



1) Remote power supply control and DAQ health monitor
2) Rack power supply – Schroff CompactPCI 250W, 13100-141
3) Main DAQ card with Zynq Ultrascale+ FPGA on a Trenz TE-0808 module
4) LUXE Control System (LCS) slave card – *not defined yet by LUXE DAQ group…*
   Receives LUXE system clock (45MHz) and pre-trigger from the main DAQ system
5) Main FLAXE clock (20MHz) and acquisition control signals 50Ω coaxial driver
6) FEB data and reset interface. Each card serves eight FEBs → 5 cards in total for full-stack calorimeter

Readout hardware – DAQ rack – laboratory configuration



1) Remote power supply control and DAQ health monitor

2) Rack power supply – Schroff CompactPCI 250W, 13100-141

3) Main DAQ card with Zynq Ultrascale+ FPGA on a Trenz TE-0808 module

4) TLU interface card (for testbeam) with external trigger inputs (for laboratory)

5) Main FLAXE clock (20MHz) and acquisition control distributor for laboratory tests. Serves eight FEBs at the same time, but without <1ns precision (no synchronous sampling)

6) FEB data and reset interface. Each card serves eight FEBs

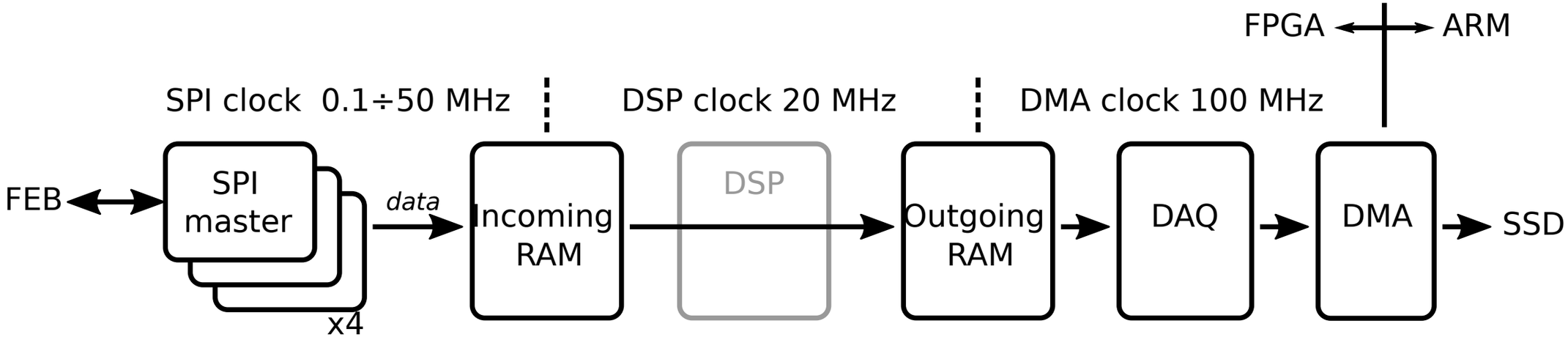
PCB status

- Test setup for FLAXE: designed and fabricated (done)
- FEB: design done
- Rack-based DAQ:
  - Backplane done
  - Guard card done
  - Remaining cards – in progress

- PCB development suspended from March till now in favor of test setup hardware and DAQ preparation and ASICs debug

- I am going back again to PCB design, with the only interruptions from ASIC re-verification before next submission

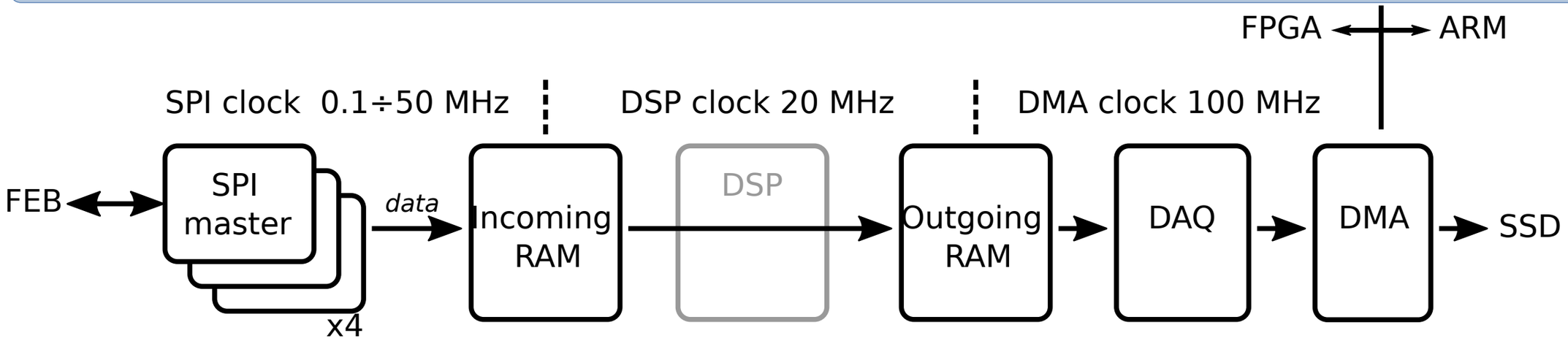
DAQ



First version for the DAQ developed for test setup

- Four SPI master modules – one for each FEB (up to 4 FEBs supported right now, easily scalable for more)
- No DSP yet – only raw data can be collected.
  DSP can be taken from FLAME DAQ, but requires some work and adjustments
- Data saved currently on the SSD drive local to the DAQ board.
  Kernel driver for UDP data transmission in progress (also a userspace software developed for FLAME DAQ can be used here)
- Three clock domains for more flexibility:
  - Variable SPI clock (throughput versus signal integrity)
  - DSP clock matching the existing design for FLAME (simplified DSP development)
  - Fast DMA clock for highest throughput

DAQ



Outgoing package can now contain data from any stage of signal processing:

- Raw ADC data from ASIC (*only one currently available*)
- Pedestal subtraction
- CMS
- FIR deconvolution filter
- TOA and amplitude reconstruction for all 64 samples from given trigger

Huge improvement in DAQ verification from the FLAME DAQ

Event rate depends on number of FEBs and number of ASICs per FEB:

- From 2 kev/s (up to 7 FEBs, one ASIC per FEB)
- To 15 ev/s for fully instrumented ECALp (40 FEBs, 24 ASICs each)

Enormous amount of data produced in full debug mode (with all data): ~1 TB/day for setup with 8 FEBs, 8 ASICs (one sensor) each

DAQ maximal event rate

	Number of ASICs per FEB																							
Number of FEBs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
1	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
2	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
3	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
4	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
5	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
6	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
7	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
8	1792	896	597	448	358	298	256	224	199	179	162	149	137	128	119	112	105	99	94	89	85	81	77	74
9	1592	796	530	398	318	265	227	199	176	159	144	132	122	113	106	99	93	88	83	79	75	72	69	66
10	1433	716	477	358	286	238	204	179	159	143	130	119	110	102	95	89	84	79	75	71	68	65	62	59
11	1303	651	434	325	260	217	186	162	144	130	118	108	100	93	86	81	76	72	68	65	62	59	56	54
12	1194	597	398	298	238	199	170	149	132	119	108	99	91	85	79	74	70	66	62	59	56	54	51	49
13	1102	551	367	275	220	183	157	137	122	110	100	91	84	78	73	68	64	61	58	55	52	50	47	45
14	1024	512	341	256	204	170	146	128	113	102	93	85	78	73	68	64	60	56	53	51	48	46	44	42
15	955	477	318	238	191	159	136	119	106	95	86	79	73	68	63	59	56	53	50	47	45	43	41	39
16	896	448	298	224	179	149	128	112	99	89	81	74	68	64	59	56	52	49	47	44	42	40	38	37
17	843	421	281	210	168	140	120	105	93	84	76	70	64	60	56	52	49	46	44	42	40	38	36	35
18	796	398	265	199	159	132	113	99	88	79	72	66	61	56	53	49	46	44	41	39	37	36	34	33
19	754	377	251	188	150	125	107	94	83	75	68	62	58	53	50	47	44	41	39	37	35	34	32	31
20	716	358	238	179	143	119	102	89	79	71	65	59	55	51	47	44	42	39	37	35	34	32	31	29

ev/s for given configuration

Only main data (raw + amplitude)

Real data rate will be most likely ~20% lower!

DAQ maximal event rate

	Number of ASICs per FEB																							
Number of FEBs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
21	682	341	227	170	136	113	97	85	75	68	62	56	52	48	45	42	40	37	35	34	32	31	29	28
22	651	325	217	162	130	108	93	81	72	65	59	54	50	46	43	40	38	36	34	32	31	29	28	27
23	623	311	207	155	124	103	89	77	69	62	56	51	47	44	41	38	36	34	32	31	29	28	27	25
24	597	298	199	149	119	99	85	74	66	59	54	49	45	42	39	37	35	33	31	29	28	27	25	24
25	573	286	191	143	114	95	81	71	63	57	52	47	44	40	38	35	33	31	30	28	27	26	24	23
26	551	275	183	137	110	91	78	68	61	55	50	45	42	39	36	34	32	30	29	27	26	25	23	22
27	530	265	176	132	106	88	75	66	58	53	48	44	40	37	35	33	31	29	27	26	25	24	23	22
28	512	256	170	128	102	85	73	64	56	51	46	42	39	36	34	32	30	28	26	25	24	23	22	21
29	494	247	164	123	98	82	70	61	54	49	44	41	38	35	32	30	29	27	26	24	23	22	21	20
30	477	238	159	119	95	79	68	59	53	47	43	39	36	34	31	29	28	26	25	23	22	21	20	19
31	462	231	154	115	92	77	66	57	51	46	42	38	35	33	30	28	27	25	24	23	22	21	20	19
32	448	224	149	112	89	74	64	56	49	44	40	37	34	32	29	28	26	24	23	22	21	20	19	18
33	434	217	144	108	86	72	62	54	48	43	39	36	33	31	28	27	25	24	22	21	20	19	18	18
34	421	210	140	105	84	70	60	52	46	42	38	35	32	30	28	26	24	23	22	21	20	19	18	17
35	409	204	136	102	81	68	58	51	45	40	37	34	31	29	27	25	24	22	21	20	19	18	17	17
36	398	199	132	99	79	66	56	49	44	39	36	33	30	28	26	24	23	22	20	19	18	18	17	16
37	387	193	129	96	77	64	55	48	43	38	35	32	29	27	25	24	22	21	20	19	18	17	16	16
38	377	188	125	94	75	62	53	47	41	37	34	31	29	26	25	23	22	20	19	18	17	17	16	15
39	367	183	122	91	73	61	52	45	40	36	33	30	28	26	24	22	21	20	19	18	17	16	15	15
40	358	179	119	89	71	59	51	44	39	35	32	29	27	25	23	22	21	19	18	17	17	16	15	14

ev/s for given configuration

Only main data (raw + amplitude)

Real data rate will be most likely ~20% lower!

DAQ maximal event rate

	Number of ASICs per FEB																							
Number of FEBs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
1	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
2	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
3	2000	1000	666	500	400	333	285	250	222	200	181	166	153	142	133	125	117	111	105	100	95	90	86	83
4	1629	814	543	407	325	271	232	203	181	162	148	135	125	116	108	101	95	90	85	81	77	74	70	67
5	1303	651	434	325	260	217	186	162	144	130	118	108	100	93	86	81	76	72	68	65	62	59	56	54
6	1086	543	362	271	217	181	155	135	120	108	98	90	83	77	72	67	63	60	57	54	51	49	47	45
7	931	465	310	232	186	155	133	116	103	93	84	77	71	66	62	58	54	51	49	46	44	42	40	38
8	814	407	271	203	162	135	116	101	90	81	74	67	62	58	54	50	47	45	42	40	38	37	35	33
9	724	362	241	181	144	120	103	90	80	72	65	60	55	51	48	45	42	40	38	36	34	32	31	30
10	651	325	217	162	130	108	93	81	72	65	59	54	50	46	43	40	38	36	34	32	31	29	28	27
11	592	296	197	148	118	98	84	74	65	59	53	49	45	42	39	37	34	32	31	29	28	26	25	24
12	543	271	181	135	108	90	77	67	60	54	49	45	41	38	36	33	31	30	28	27	25	24	23	22
13	501	250	167	125	100	83	71	62	55	50	45	41	38	35	33	31	29	27	26	25	23	22	21	20
14	465	232	155	116	93	77	66	58	51	46	42	38	35	33	31	29	27	25	24	23	22	21	20	19
15	434	217	144	108	86	72	62	54	48	43	39	36	33	31	28	27	25	24	22	21	20	19	18	18
16	407	203	135	101	81	67	58	50	45	40	37	33	31	29	27	25	23	22	21	20	19	18	17	16
17	383	191	127	95	76	63	54	47	42	38	34	31	29	27	25	23	22	21	20	19	18	17	16	15
18	362	181	120	90	72	60	51	45	40	36	32	30	27	25	24	22	21	20	19	18	17	16	15	15
19	343	171	114	85	68	57	49	42	38	34	31	28	26	24	22	21	20	19	18	17	16	15	14	14
20	325	162	108	81	65	54	46	40	36	32	29	27	25	23	21	20	19	18	17	16	15	14	14	13

ev/s for given configuration

Full data

Real data rate will be most likely ~20% lower!

DAQ maximal event rate

	Number of ASICs per FEB																							
Number of FEBs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
21	310	155	103	77	62	51	44	38	34	31	28	25	23	22	20	19	18	17	16	15	14	14	13	12
22	296	148	98	74	59	49	42	37	32	29	26	24	22	21	19	18	17	16	15	14	14	13	12	12
23	283	141	94	70	56	47	40	35	31	28	25	23	21	20	18	17	16	15	14	14	13	12	12	11
24	271	135	90	67	54	45	38	33	30	27	24	22	20	19	18	16	15	15	14	13	12	12	11	11
25	260	130	86	65	52	43	37	32	28	26	23	21	20	18	17	16	15	14	13	13	12	11	11	10
26	250	125	83	62	50	41	35	31	27	25	22	20	19	17	16	15	14	13	13	12	11	11	10	10
27	241	120	80	60	48	40	34	30	26	24	21	20	18	17	16	15	14	13	12	12	11	10	10	10
28	232	116	77	58	46	38	33	29	25	23	21	19	17	16	15	14	13	12	12	11	11	10	10	9
29	224	112	74	56	44	37	32	28	24	22	20	18	17	16	14	14	13	12	11	11	10	10	9	9
30	217	108	72	54	43	36	31	27	24	21	19	18	16	15	14	13	12	12	11	10	10	9	9	9
31	210	105	70	52	42	35	30	26	23	21	19	17	16	15	14	13	12	11	11	10	10	9	9	8
32	203	101	67	50	40	33	29	25	22	20	18	16	15	14	13	12	11	11	10	10	9	9	8	8
33	197	98	65	49	39	32	28	24	21	19	17	16	15	14	13	12	11	10	10	9	9	8	8	8
34	191	95	63	47	38	31	27	23	21	19	17	15	14	13	12	11	11	10	10	9	9	8	8	7
35	186	93	62	46	37	31	26	23	20	18	16	15	14	13	12	11	10	10	9	9	8	8	8	7
36	181	90	60	45	36	30	25	22	20	18	16	15	13	12	12	11	10	10	9	9	8	8	7	7
37	176	88	58	44	35	29	25	22	19	17	16	14	13	12	11	11	10	9	9	8	8	8	7	7
38	171	85	57	42	34	28	24	21	19	17	15	14	13	12	11	10	10	9	9	8	8	7	7	7
39	167	83	55	41	33	27	23	20	18	16	15	13	12	11	11	10	9	9	8	8	7	7	7	6
40	162	81	54	40	32	27	23	20	18	16	14	13	12	11	10	10	9	9	8	8	7	7	7	6

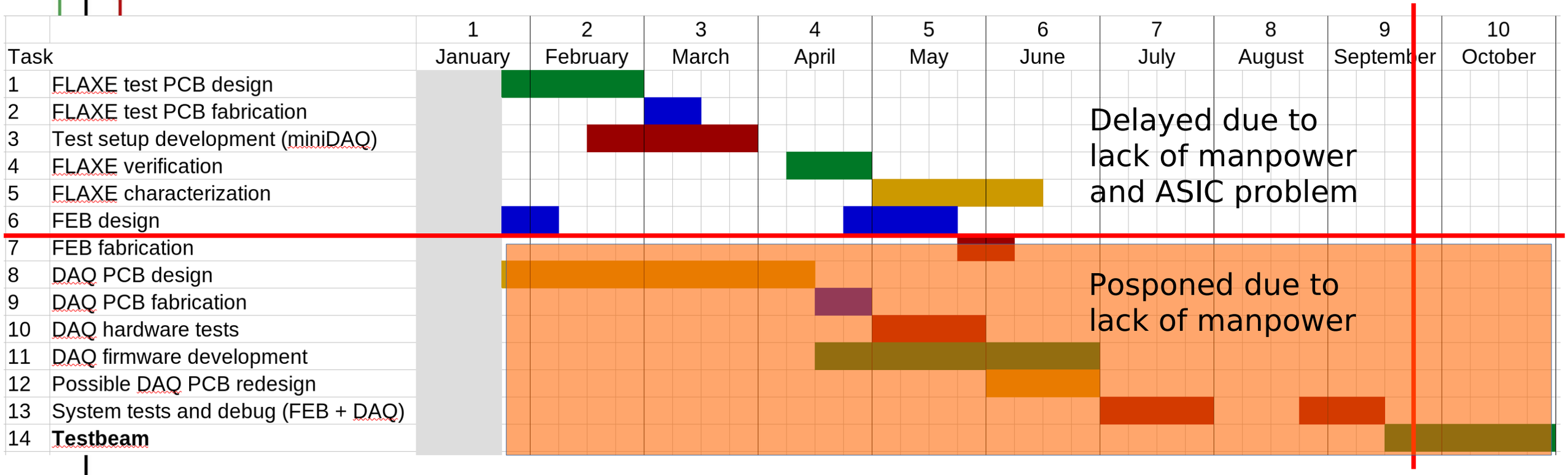
ev/s for given configuration

Only main data (raw + amplitude)

Real data rate will be most likely ~20% lower!

Schedule

- **Absolute lack of manpower:**
  - My best student accepted as technical student at CERN – till 09.2025
  - No postdoc



Schedule update depends on the FLAXE submission date, which is not yet determined...

Summary

- FLAXE ASICs fabricated, packaged and tested, but unfortunately with the worst scenario that could happened…
- We have only 7 working ASICs (20 – 30 channels each) – does it have any sense to make a testbeam with them?
- Re-submission of the ASIC somewhere at the end of this year – not yet decided
- Initial version of the DAQ prepared – good enough for testbeam
- Hardware (PCB) design heavily delayed due to:
  - Lack of manpower (one person instead of three-four planned)
  - ASIC manufacturing problem (~2 months long debug)
- Software for testbeam DAQ (EUDAC based) not even started