2nd PUNCH4NFDI TA5 Workshop on Machine Learning and Data Processing on FPGAs

Report of Contributions

https://indico.desy.de/e/45348

Contribution ID: **18** Type: **not specified**

Welcome to the Workshop

Wednesday 18 September 2024 14:00 (10 minutes)

Session Classification: Session 1

Contribution ID: **19** Type: **not specified**

Hands-on Tutorial: Running Machine Learning models on an Alveo card using hls4ml

Wednesday 18 September 2024 16:40 (1h 20m)

Presenter: MEN, Yunpeng (MPIfR)

Session Classification: Session 2

Contribution ID: **20** Type: **not specified**

Deep Learning for Real-time Classification of Astronomical Radio Signals: Current Status

Wednesday 18 September 2024 14:35 (25 minutes)

Presenter: KAZANTSEV, Andrei (MPIfR)

Session Classification: Session 1

Contribution ID: **21** Type: **not specified**

Experience with Xilinx Versal AI and status and news from Mainz group

Wednesday 18 September 2024 14:10 (25 minutes)

Presenter: KAHRA, Christian (Johannes Gutenberg - Universitaet Mainz)

Session Classification: Session 1

Contribution ID: **22** Type: **not specified**

Track reconstruction for the ATLAS Phase-II Event Filter using Graph Neural Networks on FPGAs

Wednesday 18 September 2024 15:00 (30 minutes)

Presenter: DITTMEIER, Sebastian (Physikalisches Institut, University of Heidelberg)

Session Classification: Session 1

Contribution ID: **23** Type: **not specified**

Comparison of massively parallel and fully serial sorting on FPGAs

Wednesday 18 September 2024 16:00 (20 minutes)

Presenter: MEUSER, Emanuel (JGU Mainz)

Session Classification: Session 2

Contribution ID: **24** Type: **not specified**

CNNs for real time signal reconstruction in ATLAS LAr: Status and news from TU Dresden group

Wednesday 18 September 2024 16:20 (20 minutes)

Presenter: VOIGT, Johann Christoph

Session Classification: Session 2

Contribution ID: **25** Type: **not specified**

IPbus for FPGA slow control

Thursday 19 September 2024 11:30 (20 minutes)

Presenter: HENTGES, Rainer (TU Dresden)

Session Classification: Session 4

Contribution ID: **26** Type: **not specified**

High Level Synthesis with Siemens Catapult: Experience in ATLAS LAr

Thursday 19 September 2024 09:05 (30 minutes)

Presenter: FRITZSCHE, Nick (CERN)

Session Classification: Session 3

Contribution ID: **27** Type: **not specified**

OneAPI for Intel FPGAs

Thursday 19 September 2024 09:35 (20 minutes)

Presenter: VOIGT, Johann Christoph

Session Classification: Session 3

Contribution ID: **28** Type: **not specified**

CLAppED: A Design Framework for Implementing Cross-Layer Approximation in FPGA-based Embedded System

Thursday 19 September 2024 09:55 (30 minutes)

Presenter: Dr ULLAH, Salim (Ruhr-Universität Bochum)

Session Classification: Session 3

Contribution ID: **29** Type: **not specified**

Machine Learning on FPGAs for the CMS Level-1 Trigger

Thursday 19 September 2024 11:00 (30 minutes)

Presenter: LABE, Finn Jonathan (Universität Hamburg)

Session Classification: Session 4

Contribution ID: **30** Type: **not specified**

Summary discussion

Thursday 19 September 2024 11:50 (30 minutes)

Session Classification: Session 4

Contribution ID: **31** Type: **not specified**

Dinner at a Dresden Restaurant (L'Osteria, Prager Strasse 1c)

Wednesday 18 September 2024 19:30 (1h 30m)