Artificial Intelligence

in Detector Front-End Electronics

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Lots of info/inspiration from T. Heim (LBL), D. Braga (FNAL), and many more (CPAD, 4D-Tracking US Workshop, etc..)

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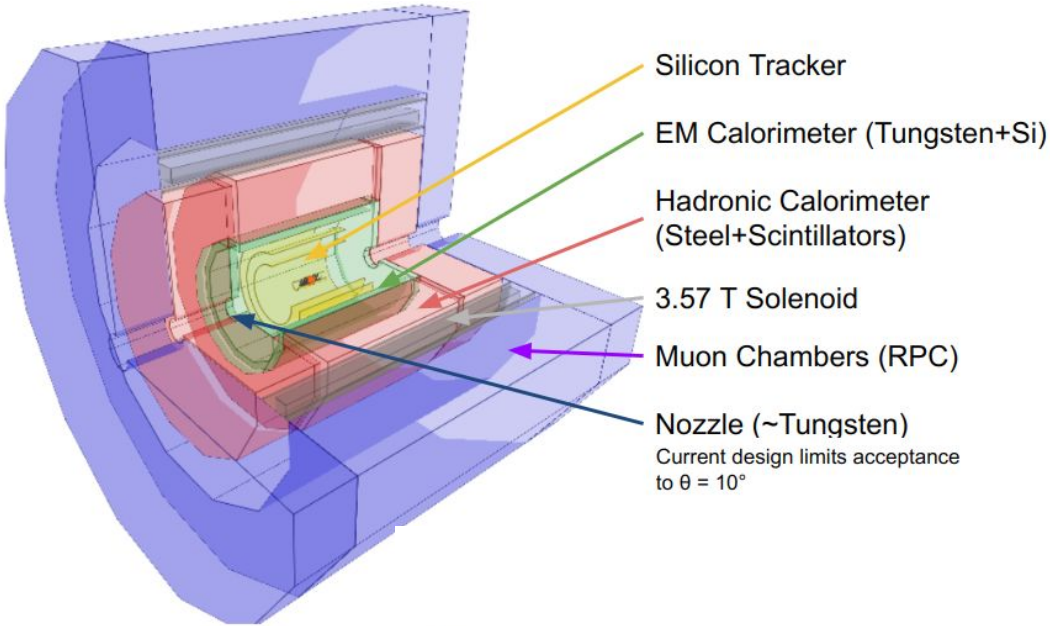
DESY
IMCC Annual Meeting

ASICs in HEP Detectors

Front-End electronics is the first component that handles the electric signal generated by the active detectors components.

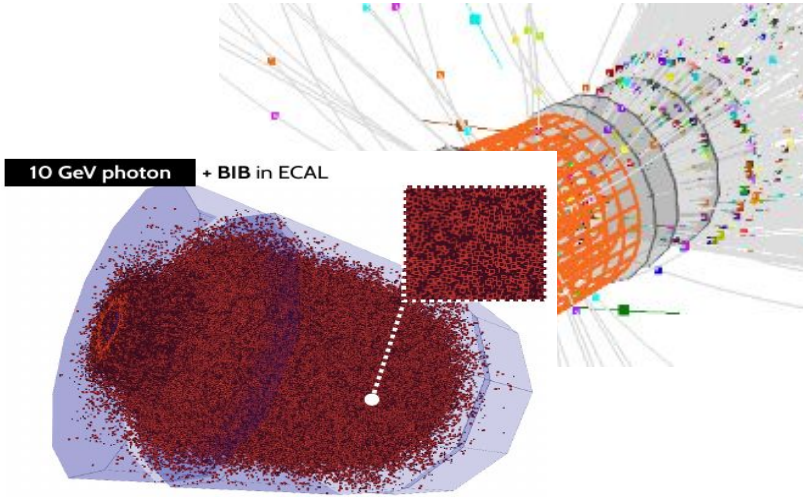
- amplify input signals (analog)
- digitize
- process/output signal (digital)

Custom Application-Specific Integrated Circuits (ASICs) are designed for this purpose for the majority of particle physics (sub-)detectors.

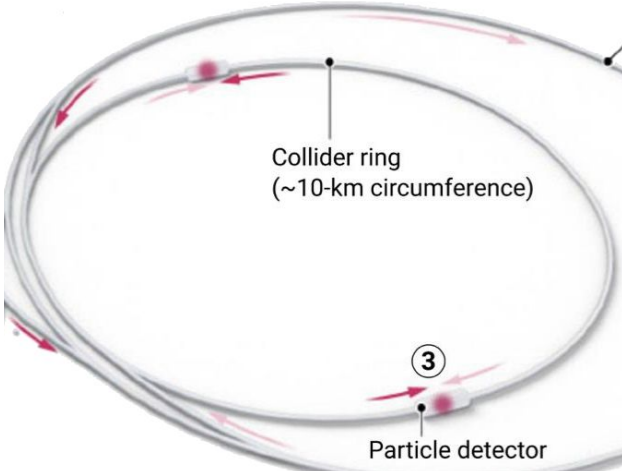


Why is Muon Collider different from LHC?

While details are many, two big highlights:



BIB: amount of raw information in key parts of the detector can be overwhelming



100kHz vs 40MHz bunch crossing, but large fraction of the events have interesting physics!

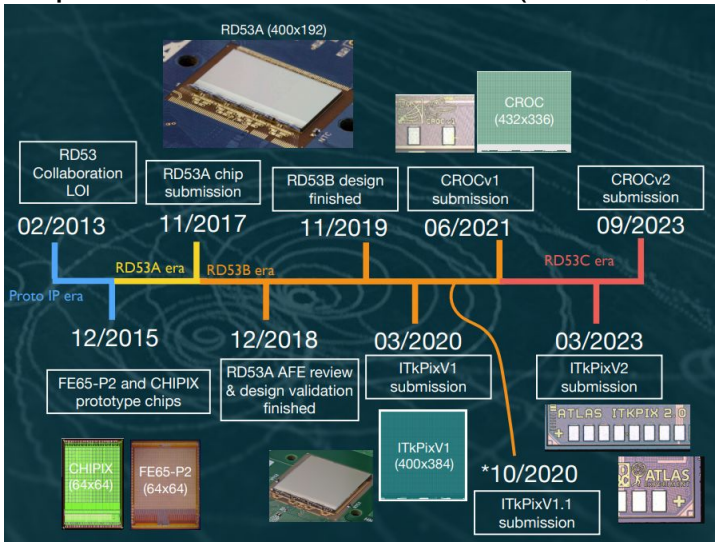
In addition, we want more information (e.g. timing) and more granularity for many of our sub-detectors and those requirements have direct implications on FE ASICs.

Timeline for ASIC design and production

Timeline strongly depends on complexity, can easily take > 10 years!

- from when requirements/specifications are set
- R&D for feature exploration started earlier

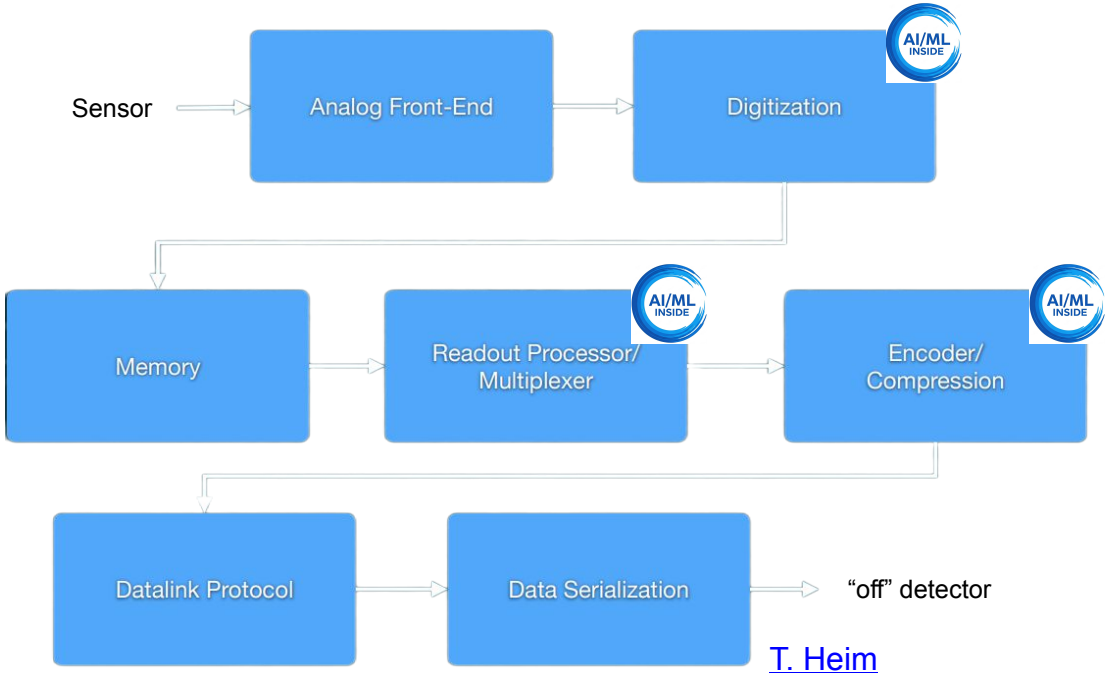
Example: HL-LHC Pixel FE ASIC (ATLAS, CMS)



Highlighted in the EU Strategy submission R&D needs as critical:

> Among all tasks that have been considered, ASICs and detector magnets have been identified as critical components requiring extended development timelines and should therefore be prioritised to ensure readiness for detector construction.

Where can AI help?



T. Heim

Smarter FE electronics

- better extracting relevant information
- reducing data size

- power consumption, cooling
- flexibility (vs offline processing)

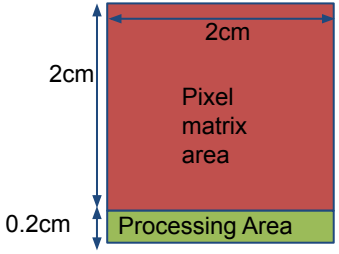
In the following, I'll try to give a few more specific examples

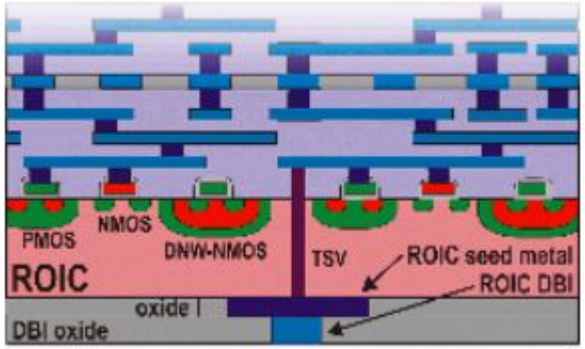
- non-exhaustive, focus on what I'm most familiar with, many similar developments
- will also try to highlight some questions I think we should ask/answer

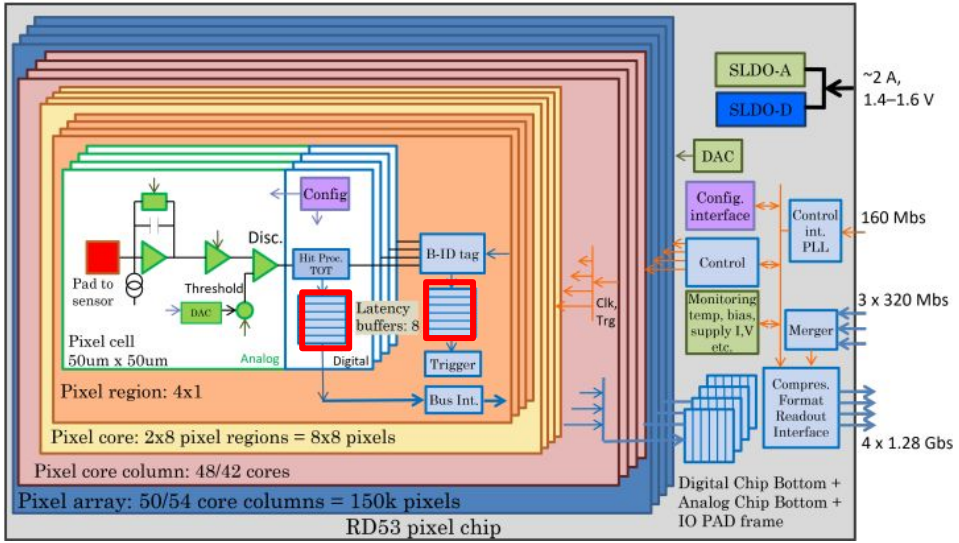
Making room for new functionalities

Modern ASIC are very dense, packed with lots of logical components!!
How to make room for smarter functionalities?
Ex. for the pixel tracker FE

- going to smaller feature sizes: 65nm -> 28nm
- remove need of data buffering for several BXs
- employ new 3D structures within ASIC



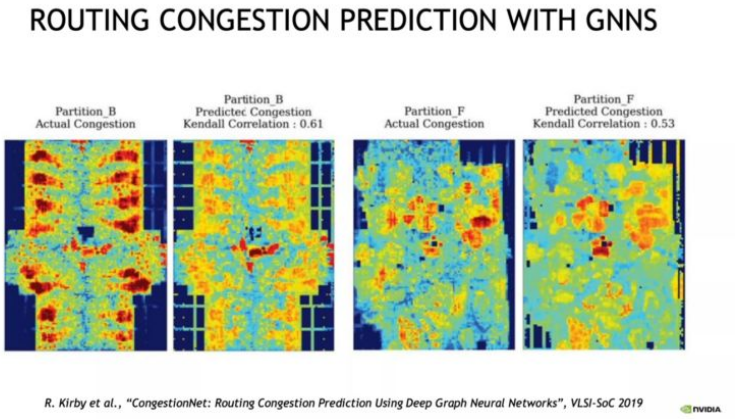


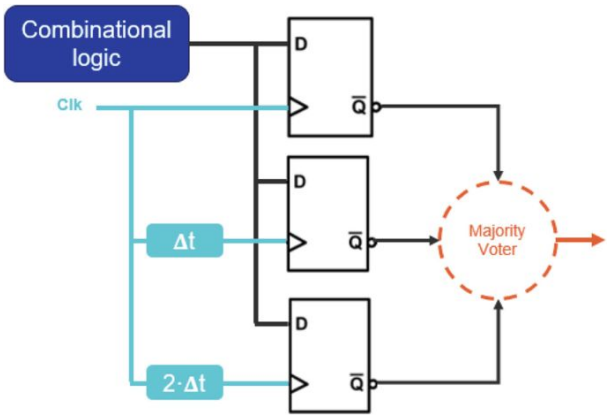


AI in design

AI ~~can~~ will help in the actual ASIC design

- optimal routing on silicon, driven by industry
- ensure optimal and efficient radiation hardness
  - manufacturing techniques, but also traditionally through “triplication” of logic/memory
  - but often can’t afford for everything and optimal choices require complex simulations, harder as chip becomes more complex.
    Can ML help approximating an optimal solution and speed up simulations?
  - radiation hardness (~ error correction) in ML models. *How?*



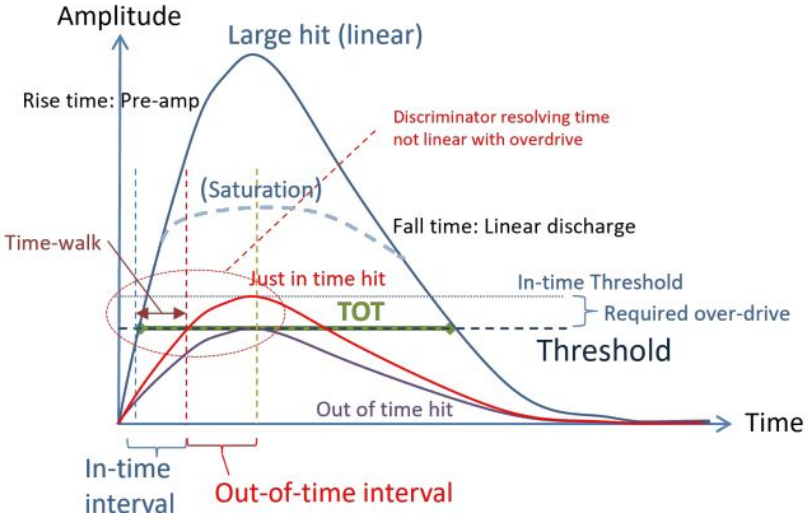


Signal digitization

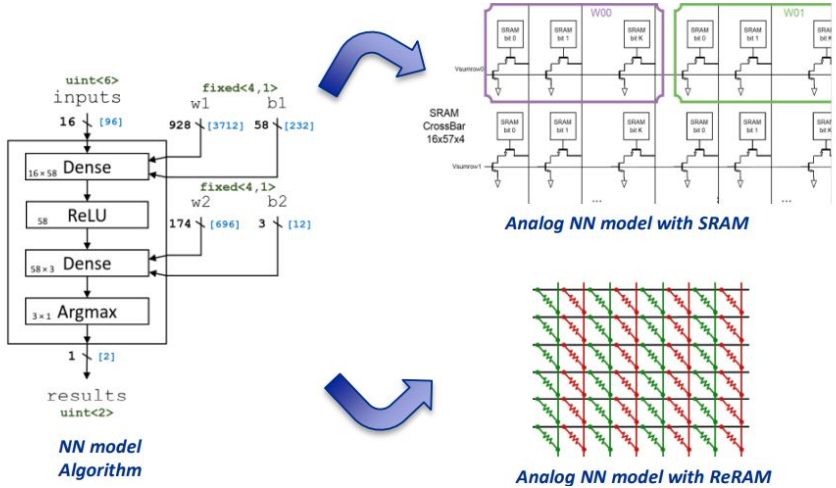
Extract information from pre-amplified signal and condense in digital format.
Example (for tracker):

- amplitude (right now through signal time-over-threshold)
- time-of-arrival

BIB can significantly differ in time, energy deposit, …



ML connected with analog part (D. Braga)

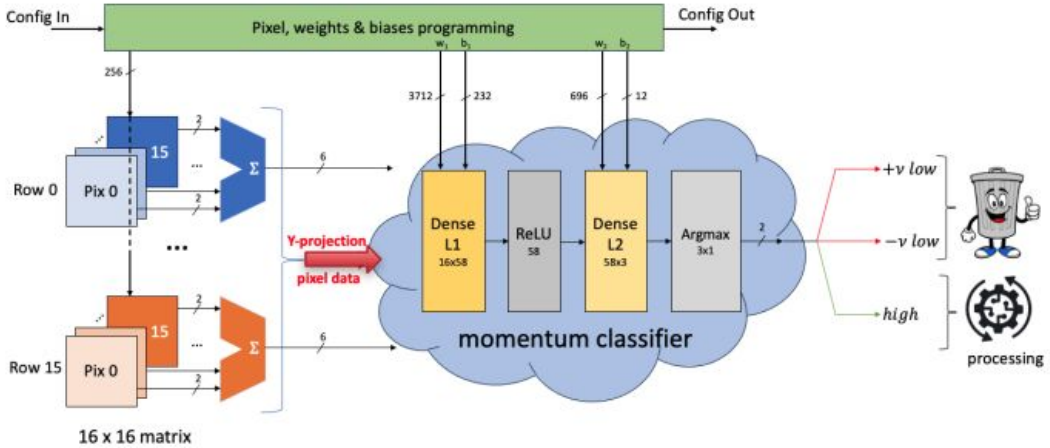


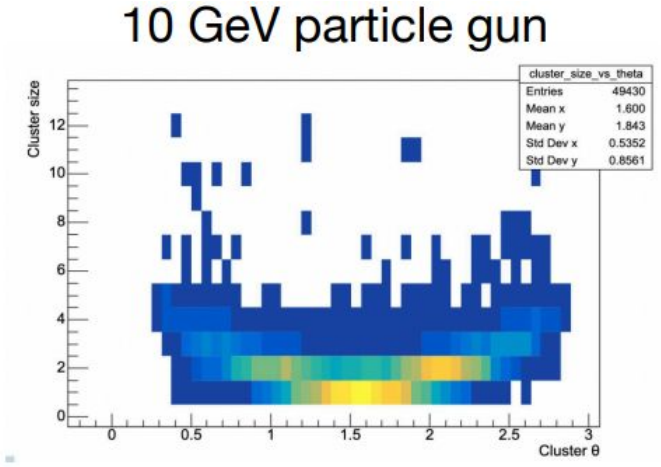
Signal digitization: properties extraction

Pattern of contiguous channels in trackers significantly differ for BIB:

- can use to perform on-chip data filtering
- can extract higher-level properties (e.g. position, incident angle)

One can envision similar approaches in other detectors.



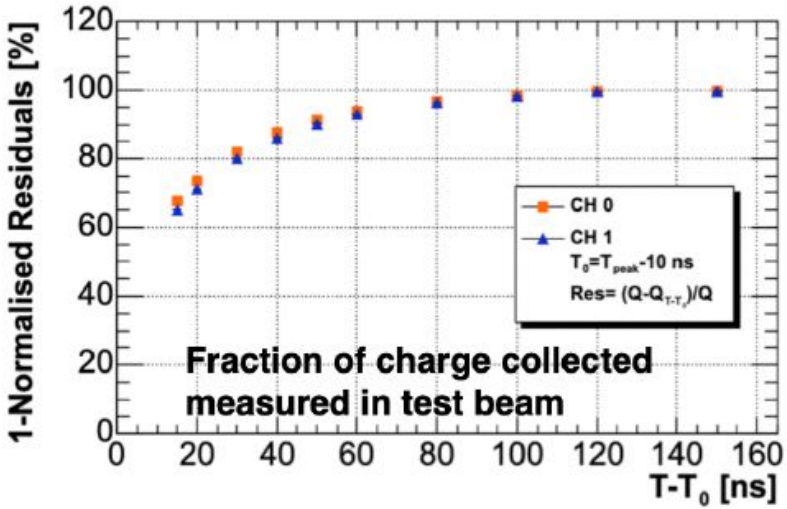


e.g. smart-pixel project (e.g. here)

BIB “pile-up” on signal

In critical places of the tracker and EM calorimeter, BIB will overlap with signal from particles from the interaction-point.

- gating in time to avoid unnecessary overlap
- reducing integration time
- waveform analysis / dynamic subtraction would be desirable
- *Can ML help extracting correct features?*



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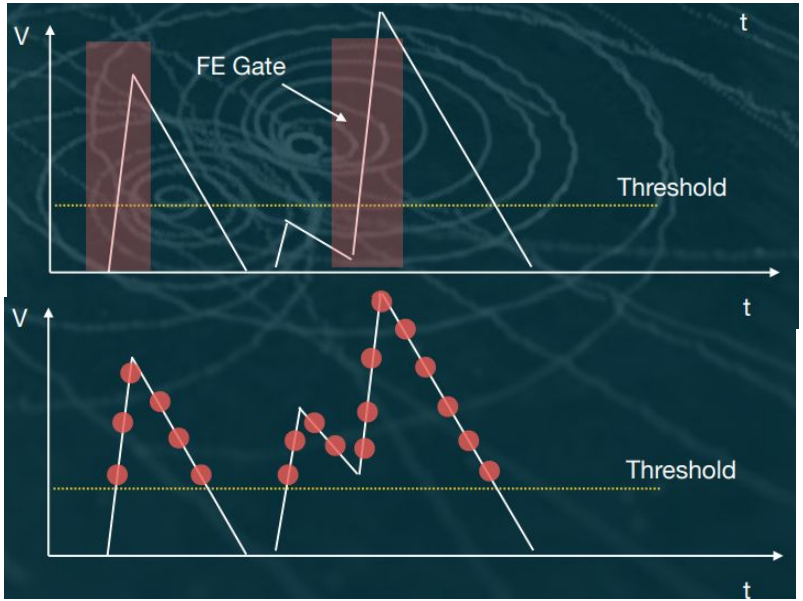
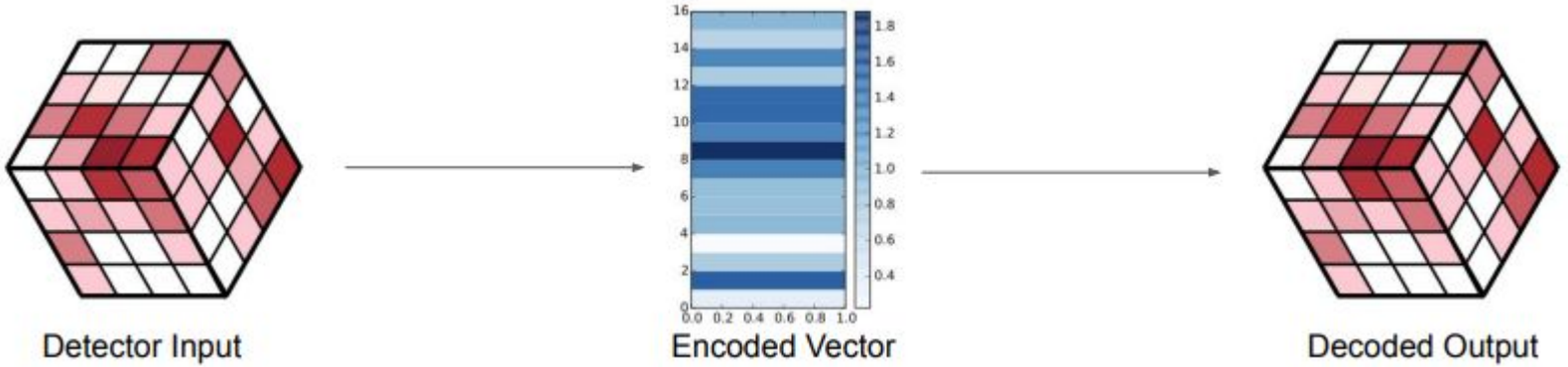


Data compression

Large bandwidth requirements expected on some FE electronics.
ML techniques can also be used to compress information

- beyond feature extraction, but connected problem
- important to understand *when it's necessary*
  - e.g. HL-LHC Pixel FE chip already employs an optimal lossless compression, but drawbacks in resources needed to "un-pack"



see e.g. ECON project (FNAL et al.) and many more

ML from hyper-local to “global”

Use when patterns might not be trivial and might require adjustments

Within the channels of the FE itself

- accurate time-of-reference determination within FE chip
- feature extractions (as in previous slide)
- …

Across FEs in the detector

- coincidence of signals
  - double-layers
  - through wireless communication
- reference time synchronization
- …

not a great example… thanks Gemini

Flexibility

Whenever we think of using any ML technique in Silicon, we need to balance

- optimizing for small resource usage
- flexibility in adapting to conditions that change, or are not perfectly known

How to design in Silicon ML techniques that are:

- robust
- flexible
- redundant in architecture and error-resistant

Many of these questions can start to be answered by detailed simulations!

Design systems that can output a great level of debug information

- even on the final FE chip, a mix of full information and condensed information at different rates are likely a requirement

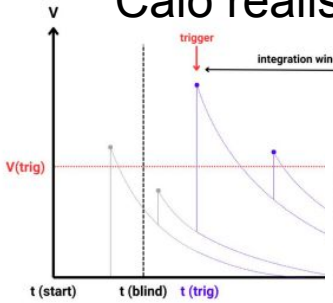
Simulation, Simulation, Simulation…

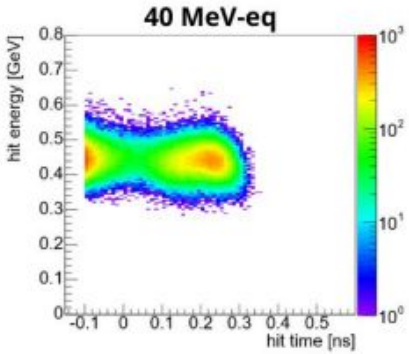
Understanding what approximation we do is key in answering many of these questions and ensuring we can trust what we learn from them.

- Realistic digitization code developed for tracker, calorimeter
- Significant work still needs to be done, depending on what features we're most interested in!

see Angira's talk

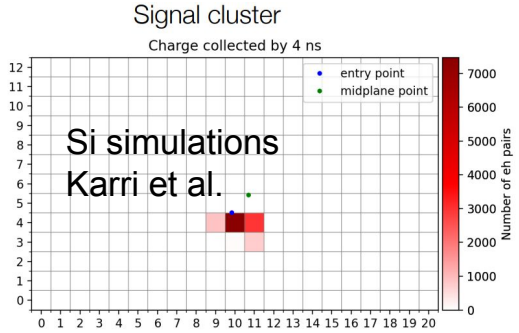
Calo realistic digi for Crilin (EM-Calo)



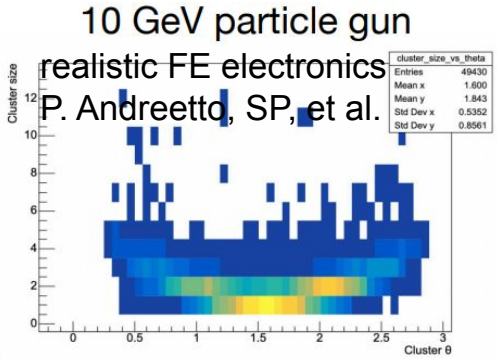


Calo realistic digi
L. Sestini et al.

Silicon tracker realistic digitization



Si simulations
Karri et al.



Scalability and Testing

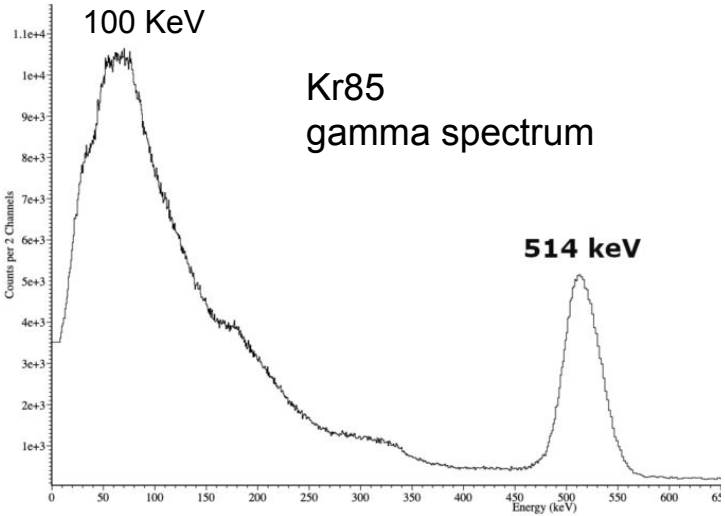
Important to start early prototyping, however

- what is done for a small prototype is not trivial to scale to a full-size chip
- a production-ready ASIC requires lots of testing, validation, bug-fixes, …

Important to start early with small system-like prototypes!

Imperative to create mid-size prototypes
to test together with real sensors in conditions
as realistic as possibles

- *how to recreate a BIB-like background*
  - see e.g. here, different application
- test beam
- irradiation
- *what facilities?*



Conclusions

AI/ML will be part of the design and likely some functionalities of future FE ASICs

- close loop with developing detailed simulations to study what features are needed, desirable or not practical. Explore widely (architecture, features, etc..)
- create small prototypes and test them in realistic conditions
- small system-tests to prove scalability of concepts
- create small system-tests to ensure scalability
- create collaboration for final FE ASICs as soon as experiment is approved

At all stages, engage early with DRD/RDC groups to create collaborations

- ensure knowledge sharing
- ensure affordability, given the high costs of prototyping ASICs

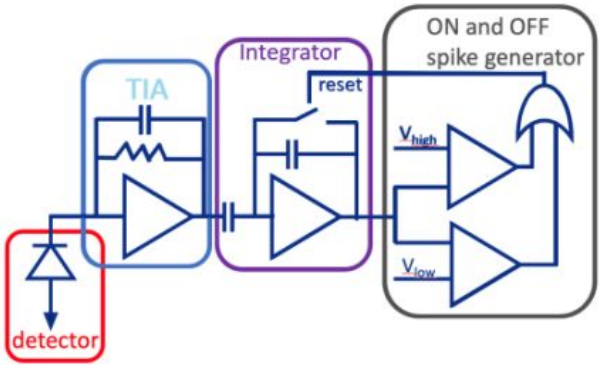
BACKUP

Architecture

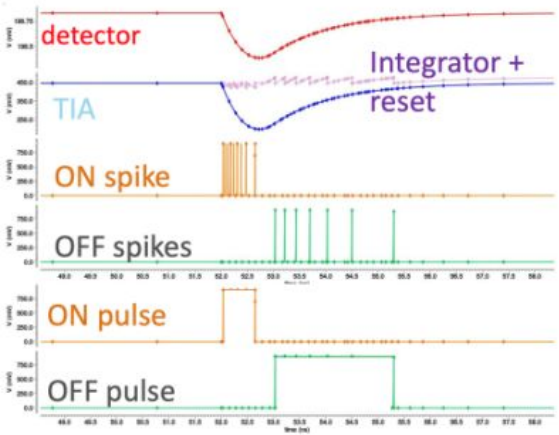
Employ/optimize non-traditional architectures.
Just one example: neuromorphic chips

- achieve very low power consumptions, active only when needed
- usually limited/advantageous for “low” event rate*, but could be ok for 100 kHz.

  * potentially controversial statement, but I haven’t been convinced otherwise yet
- *How to best integrate them? is there any real advantage?*



Pulse shape encoded in spike train
Ultra-fast signal processing ~ 100ps
Digital processing – power constraints
Analog processing – device constraints (speed)



M. Braga (FNAL)

Detailed Outline

- Introduction and General Considerations
  - where ASIC electronics is in the detector
  - key general aspects that differ from LHC (esp. BIB, bunch crossing rate, processing requirements), spirit of the talk
  - why AI on FE electronics?
  - timelines for ASIC design, prototype and production. Show resources and highlight priority given to ASIC design
  - ASIC architecture, feature sizes, radiation hardness, neuromorphic chip given the lower bunch x-ing rate (but need to be gated)
  - Link also to Murtaza's talk on Thursday (link) on timing detector ASIC
- Tracker
  - current state-of-the-art
  - where AI can help?
  - BIB in tracker: all time vs gated, in-pixel pile-up
  - Digitization ToT/ToA vs waveform analysis for in-pixel pile-up suppression and timing measurement
  - Time synchronization and corrections also within the chip. Overall t0 determination (could also be done on-chip? AI driven?)
  - Analysis of clusters on-chip. From corrections to discrimination to position-determination
  - Compression for output given the different nature of clusters on-chip. Shape-analysis, NN-based, sim vs reality, smart-pixels, etc..
- Calorimeters (esp. EM)
  - New electronics developments for HL-LHC, e.g. ECON with auto-encoders for compression
  - BIB and charge integration time
  - current assumptions, possible strategies to mitigate BIB
  - Shape analysis, when? digi and/or analysis on FE? or both?
- Other detectors
  - Muons, PID?, etc..
- Flexibility
  - new environment, need to be ready for the unexpected
  - allow "debug" information or a mix of raw and highly bandwidth-optimized data flow
  - any AI embedded on the chip needs to be conifgurable, but also optimized for reducing power consumption
  - trade-off between advantages of local processing and increase in power/cooling requirements
- System tests
  - importance of early prototyping and system tests (one feature vs scaling up)
  - Dependence on testing with sensors, coordinate prototyping with sensor technology developments
  - Recreation of muC conditions? how? e.g. Kr-85 source studies (link proceeding, paper coming)
  - Test beams
- Conclusions