DAMC-DS5014DR

A High-Speed and High-Performance RFSoC-Based Platform for Diverse Scientific Applications

13th MicroTCA Workshop for Industry and Research

Behzad Boghrati, Burak Dursun, Michael Fenner, Cagil Gümüs, Szymon Jablonski, Johannes Zink
Hamburg, 12.12.2024

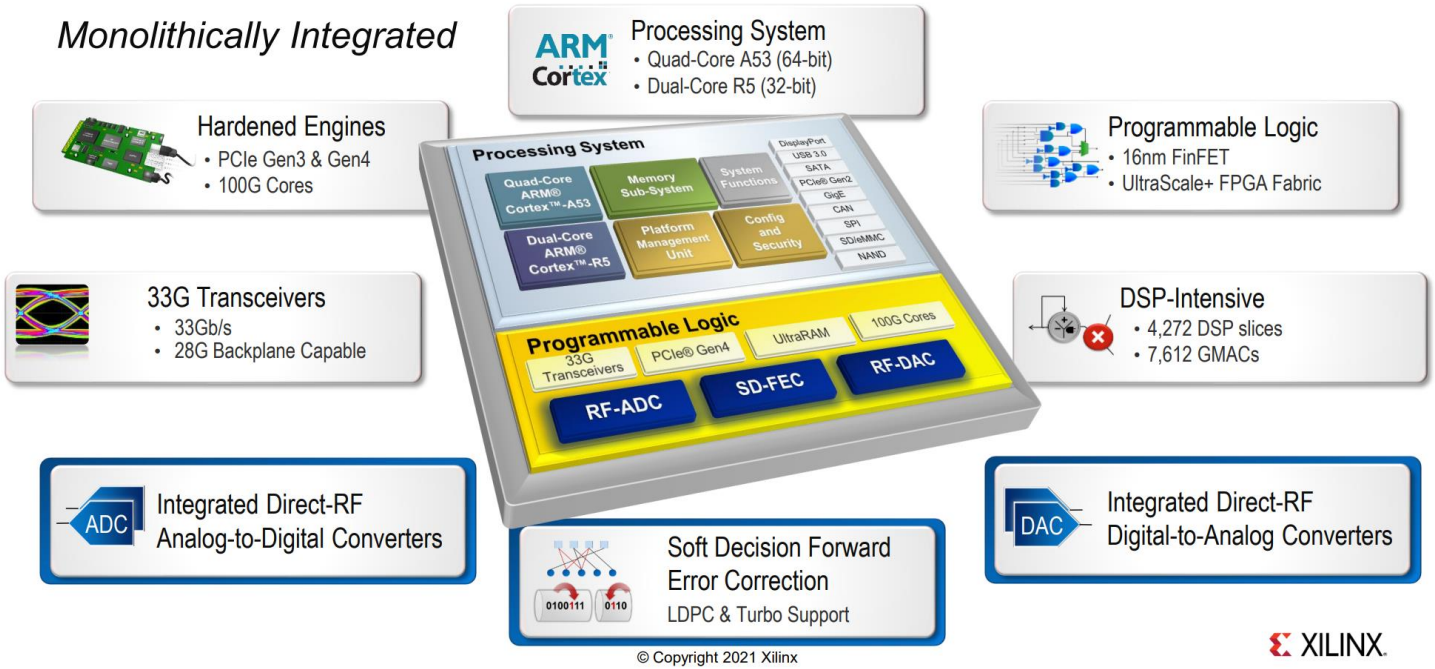
HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

DESY.

Radio Frequency System-on-Chip

Why using the RFSOC?

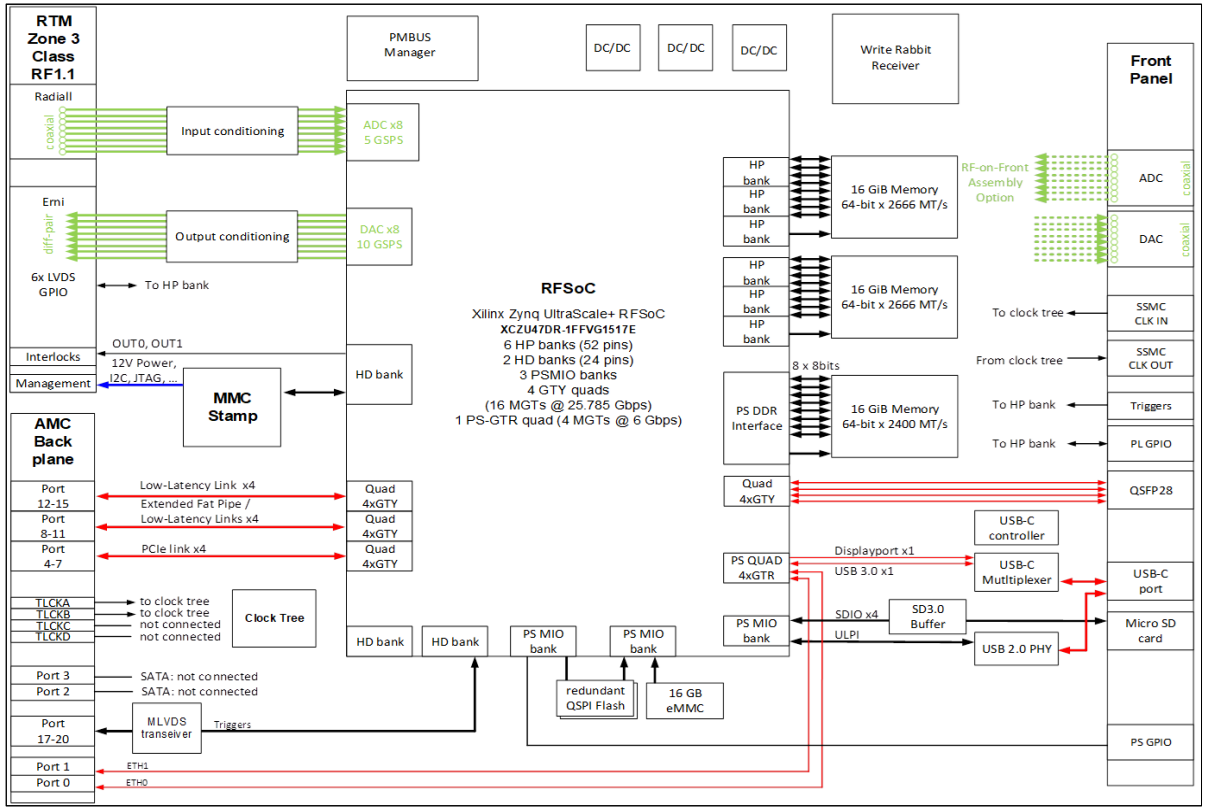
- **RFSoC offers significant advantages in applications demand:**
  - High integration,
  - Enhanced bandwidth,
  - Flexibility and reconfigurability,
  - Reduced power consumption,
  - High performance in RF signal processing,
  - Improve software interface, and
  - Cost



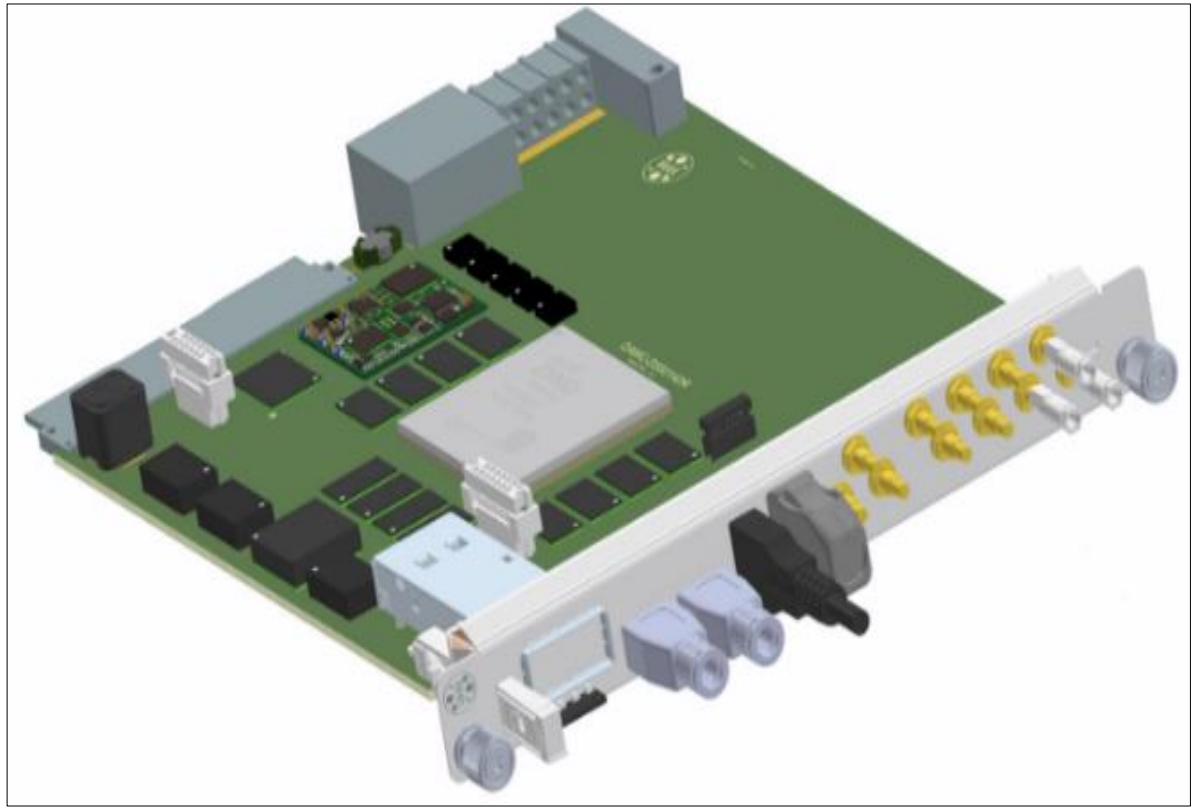
- **High Integration:**
  - RFSoC integrate ADCs, DACs, FPGAs, and Processing Systems into a single chip.
  - This monolithic integration not only reduces system size, weight, power consumption, and cost but also minimizes signal losses, delays, and interface complexities associated with multi-chip solutions.
  - The integration also eliminates high-speed serial interfaces, further contributing to power savings and simplified board design.

Review of the DS5014DR Specifications

High-speed digitizer



Block Diagram

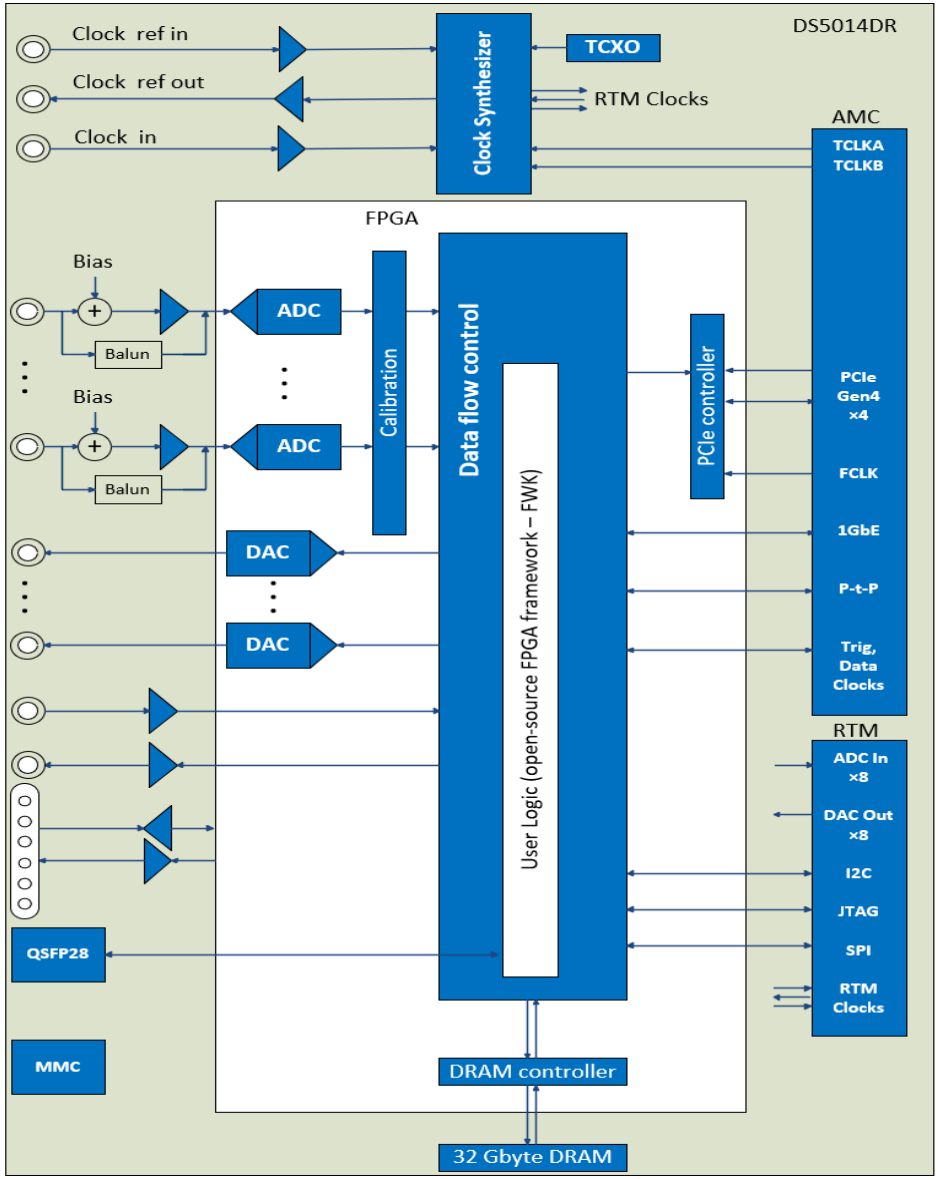


3D Layout

Review of the DS5014DR Specifications

Highlights

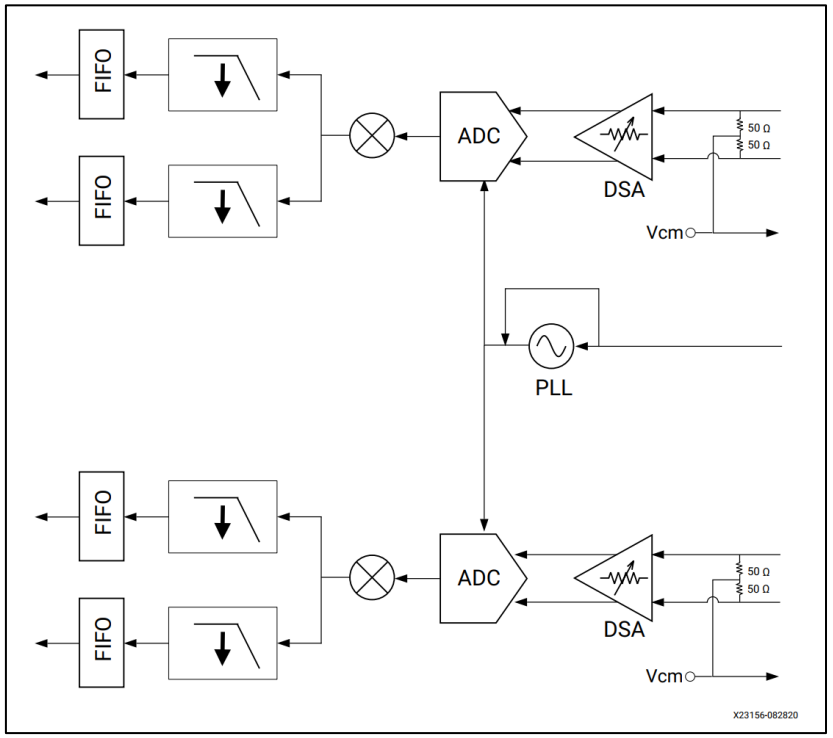
- 6.0 GHz analog bandwidth (-3 dB)
- Single-ended analog RTM connection (Class RF1.1)
- 8 analog inputs and 8 analog outputs via RTM
- Alternatively up to 8 analog inputs and/or outputs on front panel via coaxial SSMC connector
- 5.0 GSPS per channels ADC sampling rate
- 3x DDR4 banks with up to 48 GB DRAM
- 8.92 GSPS per channels DAC data rate
- Up to 12 Trigger inputs and one Trigger output
- AC or DC coupling, depending upon assembly variant
- Internal or external clock reference and ref. output
- PCIe Gen.4 x 8 and 100G Ethernet data interfaces
- Fully customized firmware code available for fast data processing
- FPGA open for custom application (open-source BSP)
- Yocto Linux support
- Standalone mode (can run without AMC CPU module)



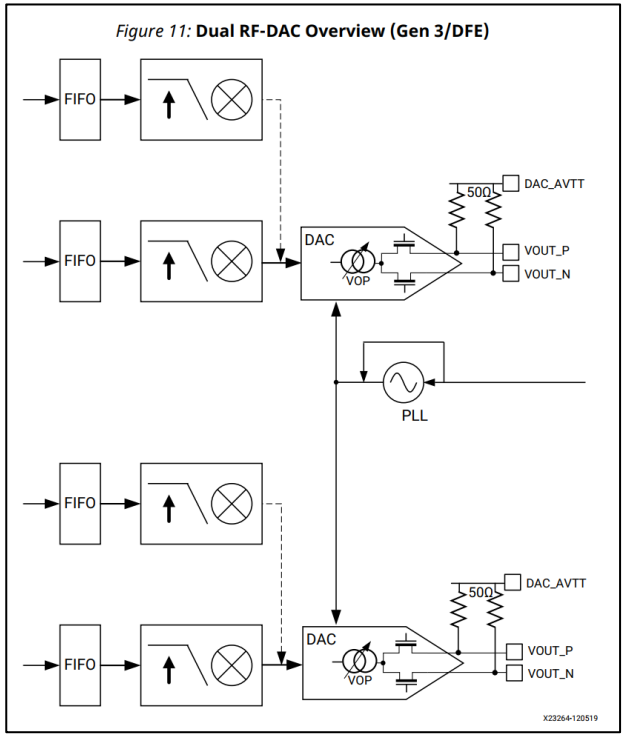
Review of the DS5014DR Specifications

XCZU47DR-1FFVG1517E

Dual RF-ADC Tile



Dual RF-DAC Tile



DAMC-DS5014DR

Analog Input and Output Configuration

	Analog Input (ADC)				Analog Output (DAC)			
	Channels	Location / Connector	Coupling	Bandwidth (GHz)	Channels	Location & Connector	Coupling	Bandwidth (GHz)
MBFB / MSK	8 Single-ended	Zone 3 / Radiall	AC	0.06 – 2.6	8 Differential	Zone 3 / ERNI	DC	DC – 2.5
LLRF-MINERVA / SCK-CEN	6 Single-ended	Zone 3 / Radiall	AC	< 1	2 Single-ended	Zone 3 / Radiall	AC	Default - Ok
BAC / MSK	4 Single-ended	Zone 3 / Radiall	AC	0.01 – 0.05	4 Single-ended	Zone 3 / Radiall	AC	Default - Ok
iDAS / Uni-HH	8 Single-ended	Zone 3 / Radiall	AC	Default - Ok	4 Differential	Zone 3 / ERNI	DC	DC – 2.5
XFEL	Default - Ok	Default - Ok	DC	Default - Ok	Default - Ok	Default - Ok	Default - Ok	Default - Ok
Kicker / MIN	Default - Ok	Zone 3 / Radiall	AC (DC is OK)	0.03 - 4	Default - Ok	Default - Ok	Default - Ok	Default - Ok
FLASH	2-8 (or 4) Single-ended	Default - Ok	DC	DC – 6 (1 kHz or 10 kHz - 6 GHz)	Default - Ok	Default - Ok	Default - Ok	Default - Ok

DAMC-DS5014DR

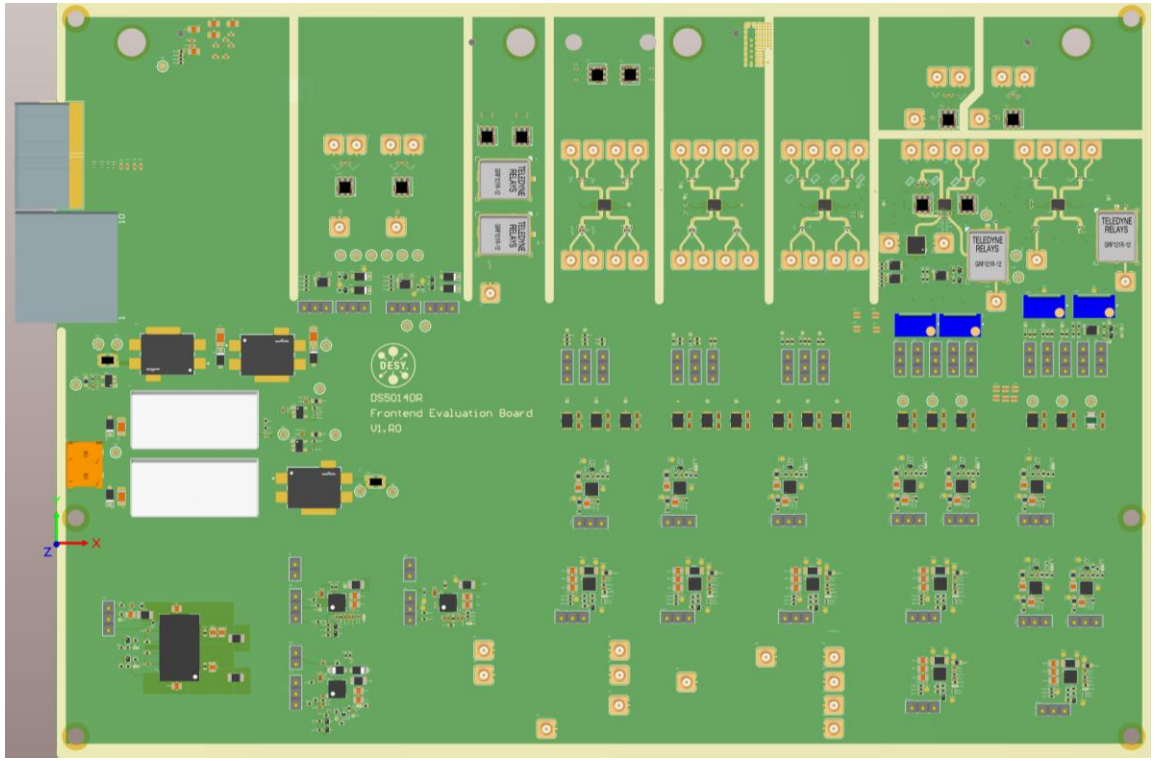
Analog Input and Output Configuration

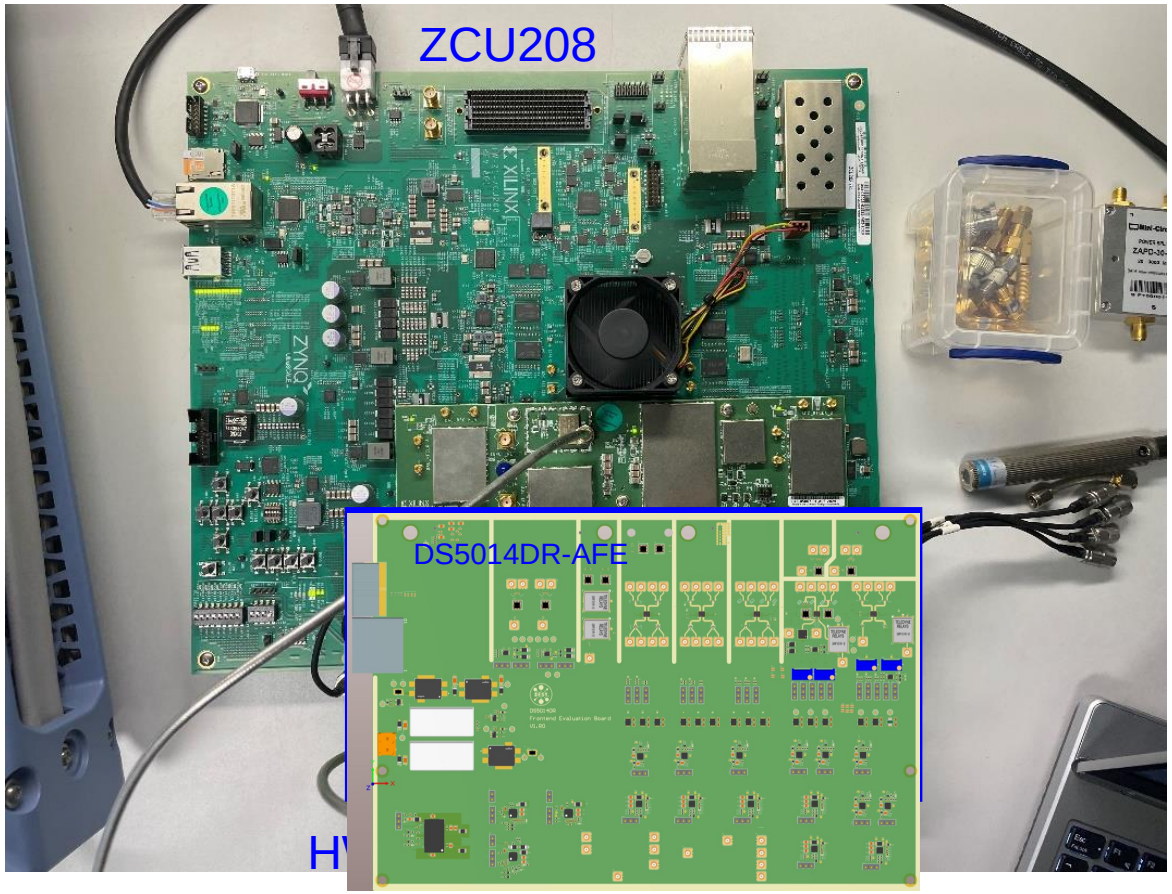
	Analog Input (ADC)				Analog Output (DAC)			
	Channels	Location / Connector	Coupling	Bandwidth (GHz)	Channels	Location & Connector	Coupling	Bandwidth (GHz)
	8 Single-ended	Zone 3 / Radiall	AC	0.06 – 2.6	8 Differential	Zone 3 / ERNI	DC	DC – 2.5
Photon Diag FLASH / FS-FLASH-D								
Photon Diag XFEL (tbd) /XFEL								
Photon Diag PIII /FS-EC								
BPM / MLS								
ICT PIV / MDI								
HV Pulse Diagnostics / MIN								
BT0 Correction for PETRA IV / MSK Timing								

DS5014DR - Front-end Eval Board

Analog Front-end (AFE)

- ✓ Analog Front End and analog signal conditioning
- ✓ Two modes; A) Standalone, B) Mezzanine Board.

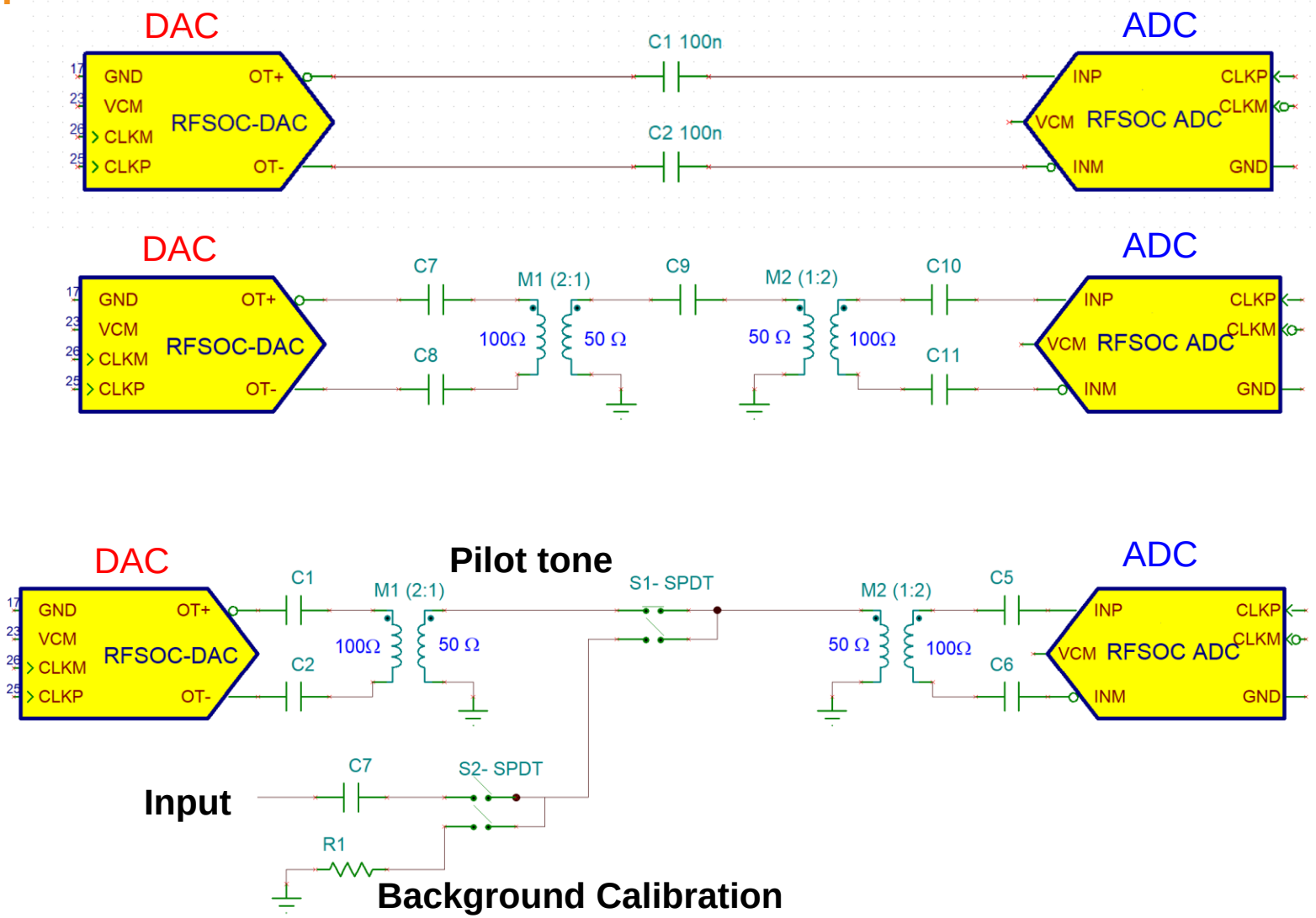




DS5014DR - Front-end Eval Board

ADC Specifications and Calibration

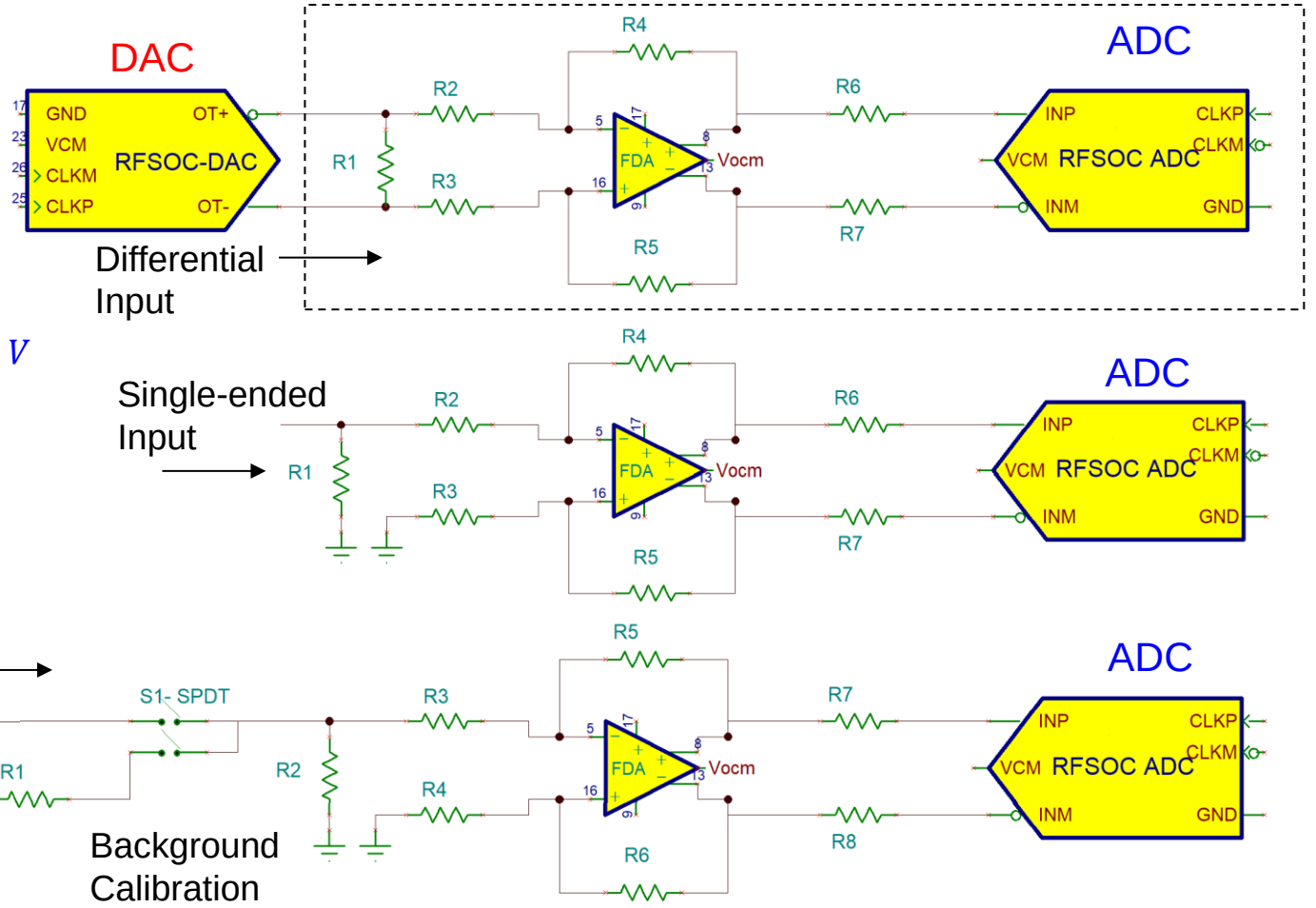
- Measurement of the Analog Converters
  - Noise floor
  - Time latency
  - Other specifications
  - RF switch
- RF-ADC has interleaving architecture
  - Needs to Calibration



DS5014DR - Front-end Eval Board

ADC DC Coupling Input

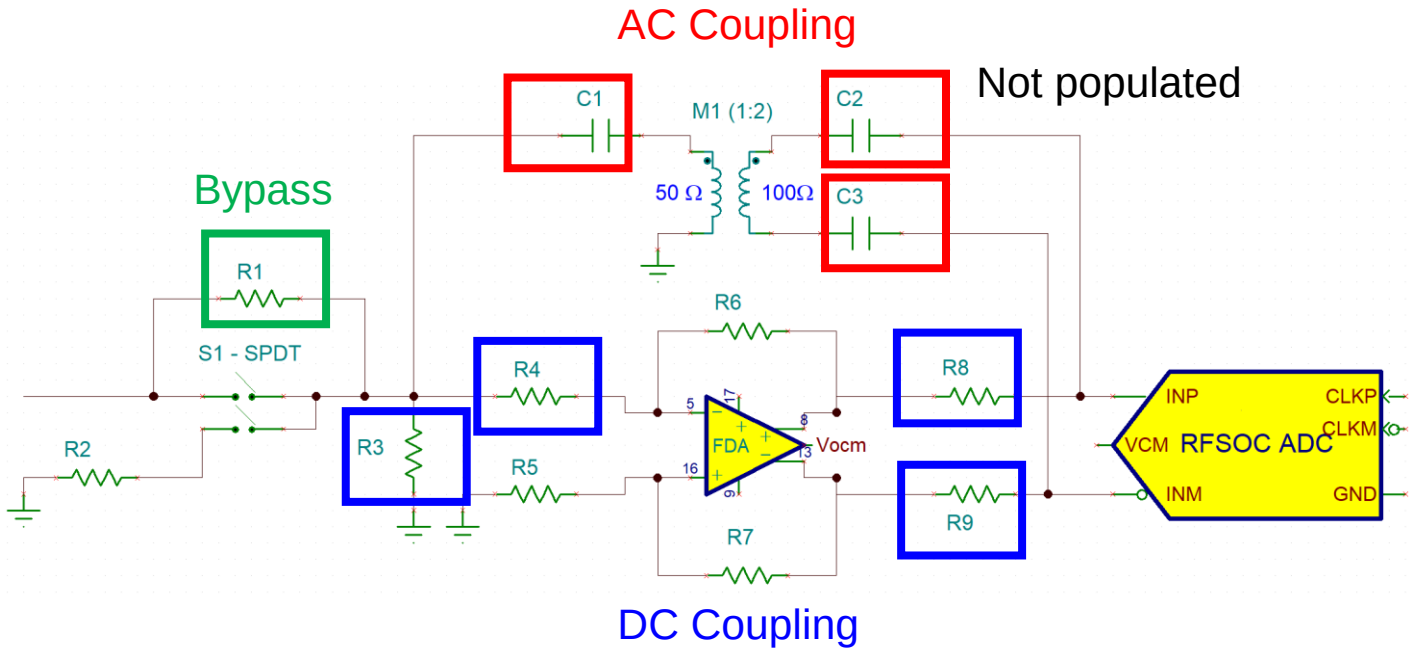
- ADC input has 0.7 V common mode input voltage
- Maximum ADC input voltage swing 1 Vpp (±500 mV)
- DAC output common voltage is 2.1 V to 2.81 V
- DAC output swing voltage $V_{OUT} = \pm 0.32\ V$ to $V_{OUT} = \pm 1.6\ V$



DS5014DR - Front-end Eval Board

ADC Hybrid Coupling Input

- In Hybrid Coupling, assembly option, is used to select between the AC or DC coupling.
- Performance of the input channels need to be evaluated
- Two different RF Switch will be evaluated
  - Mechanical Relay (Expensive and Wideband range DC – 18 GHz)
  - Semiconductor (Tiny, Chip and DC – 8 GHz)



Assembly options

RF-ADC Electrical Characteristics

DC Coupling characteristics

- Three design rules: 1) Remove unnecessary attenuation resistors from the RF analog chain, 2) Adjust the gain using the different variant of the TRF1305 chip, and 3) keep the RF signal within the 1 Vpp.

- Use an amplifier version that requires minimal attenuation to achieve the overall gain:

1. 5 dB (TRF1305A2)
2. ✓ 10 dB (TRF1305B2)
3. 15 dB (TRF1305C2)

Device Information

PART NUMBER(1)	D2D POWER GAIN	PACKAGE(2)
TRF1305A2 (3)	5 dB	RYP (WQFN-FCRLF, 16)
TRF1305B2	10 dB	
TRF1305C2 (3)	15 dB	

(1) See the Device Comparison Table.
(2) For more information, see Section 11.
(3) Preview information (not Production Data).

- In DC coupling input, single-ended mode,

1. The dynamic range of the input signal is 1 Vpp (±0.5 V)
2. The DC common mode input voltage is 0 V.

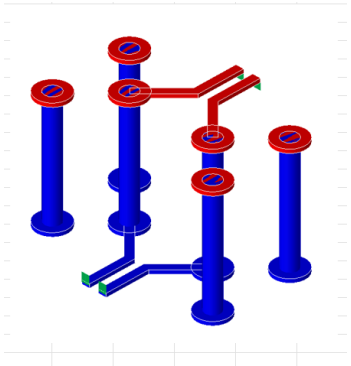
- In DC coupling input, differential mode,

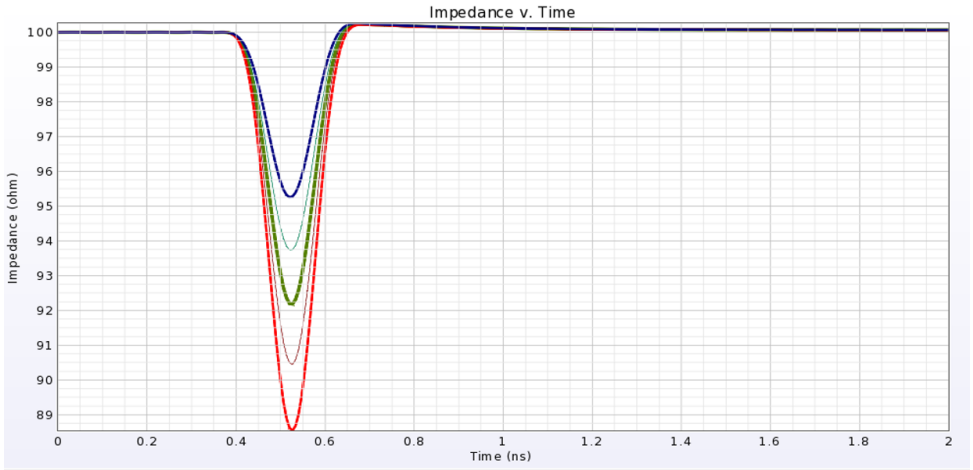
1. The dynamic range of the input signal is 1 Vpp (±0.5 V)

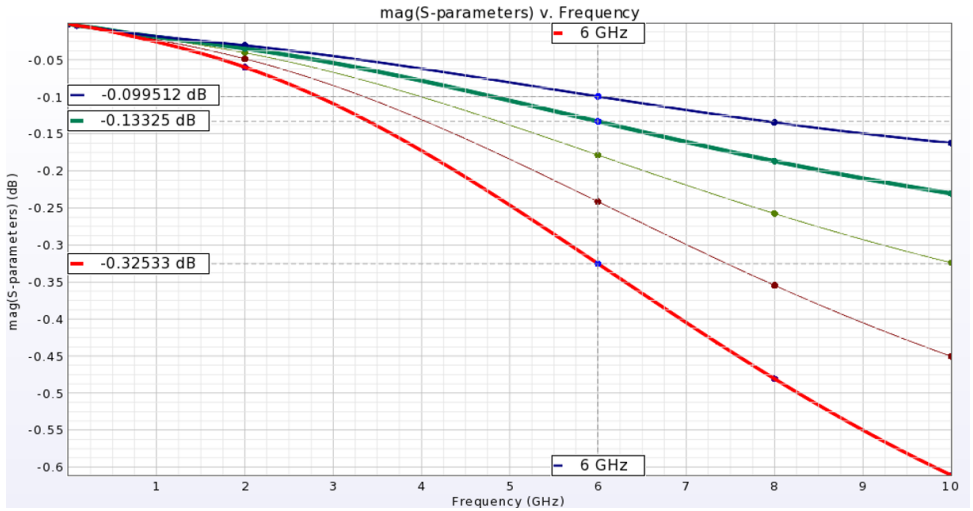
- The DC common mode input voltage range is $0.25 \leq V_{ICM} \leq 2.25\,V$.

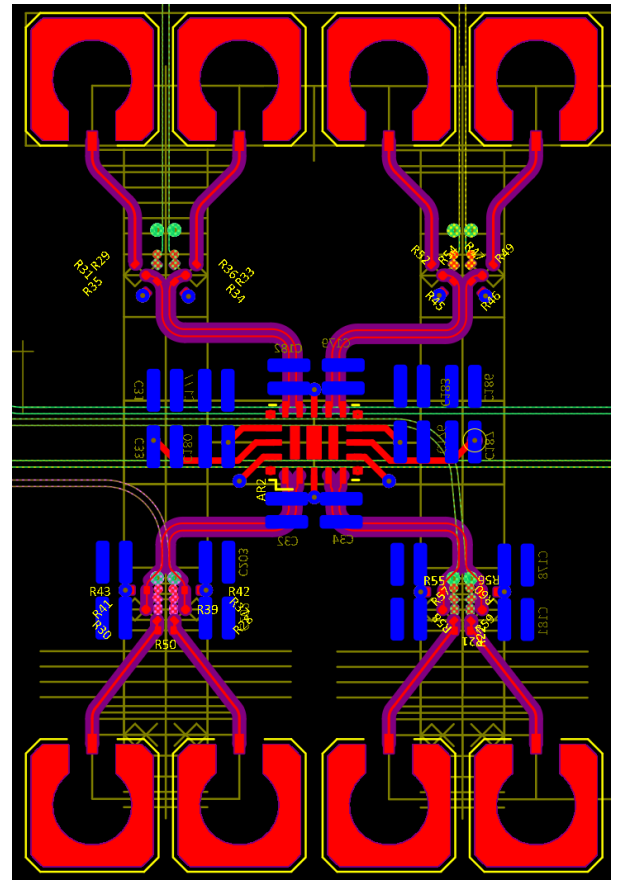
RF PCB layout

Pre-layout validation







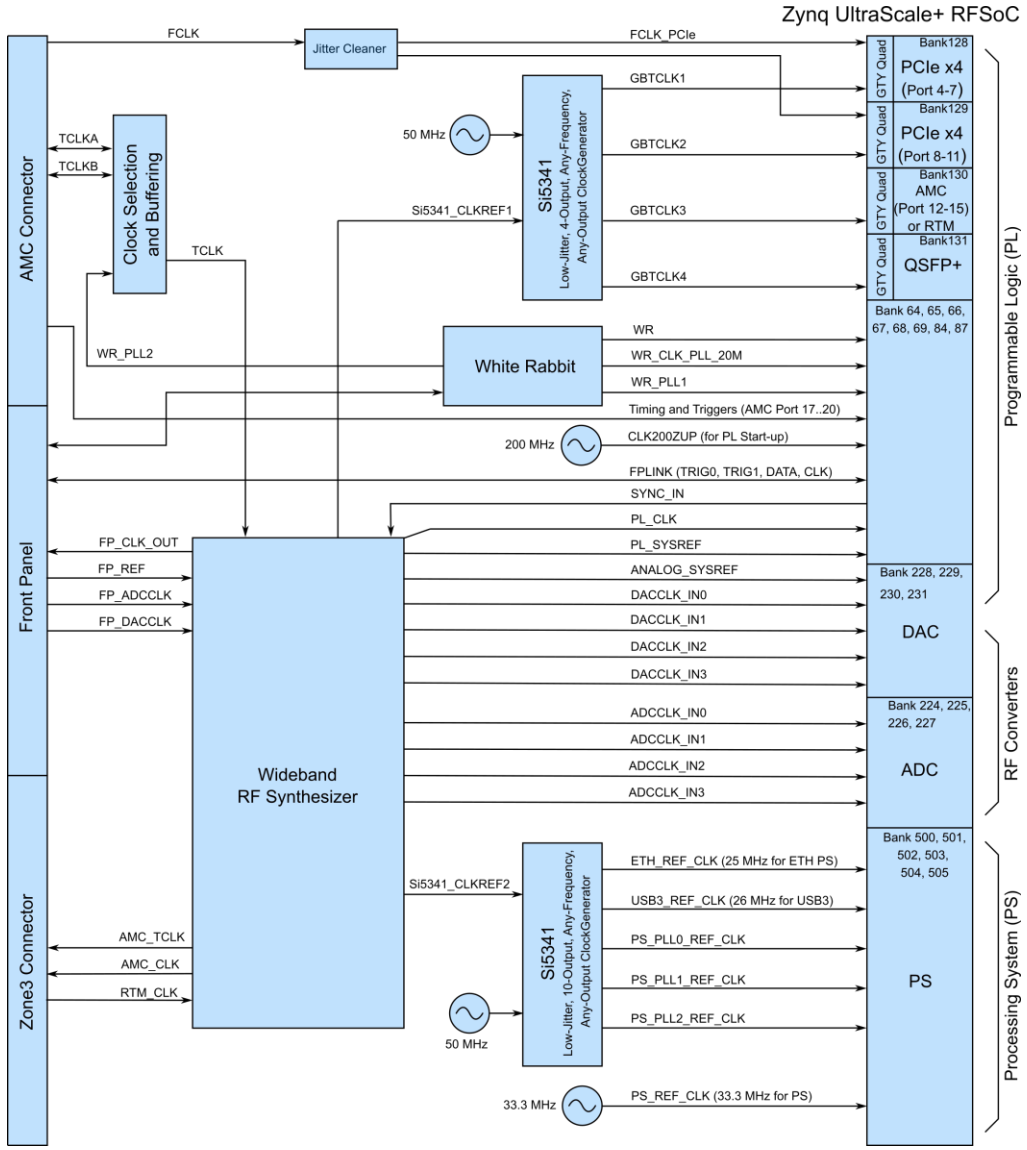


Differential, Start=1 MHz, Stop=10 GHz, Param Sweep=on, Nominal Params: drill_ctc=1.08 mm, pad_drill=0.18 mm: | S(D(1,2) , D(3,4)) | =
Differential, Start=1 MHz, Stop=10 GHz, Param Sweep=on, Nominal Params: drill_ctc=1.08 mm, pad_drill=0.1975 mm: | S(D(1,2) , D(3,4)) |
Differential, Start=1 MHz, Stop=10 GHz, Param Sweep=on, Nominal Params: drill_ctc=1.08 mm, pad_drill=0.215 mm: | S(D(1,2) , D(3,4)) | =
Differential, Start=1 MHz, Stop=10 GHz, Param Sweep=on, Nominal Params: drill_ctc=1.08 mm, pad_drill=0.2325 mm: | S(D(1,2) , D(3,4)) |
Differential, Start=1 MHz, Stop=10 GHz, Param Sweep=on, Nominal Params: drill_ctc=1.08 mm, pad_drill=0.25 mm: | S(D(1,2) , D(3,4)) | =

ZU47DR ADC/DAC converter Clocking Characteristics

Szymon Jabłoński and Michael Fenner

106				
107	Tile clock input frequency range (FIN)	102.40625 - 10000	MHz	FREF range restrictions apply when the PLL is used. The FS range restriction applies when PLL is bypassed.
108	Frequency input division ratio (R)	1	-	Possible values are 1, 2, 3, 4 Only available when using internal PLL
109	Reference input frequency (FREF = FIN/R)	102.40625 - 615	MHz	On-chip PLL activated
110	ADC Input sampling frequency (Fs)	1) 0.5 - 2.5 2) 0.5 - 5.0	GHz	1) PLL bypassed, quad ADC tile configuration 2) PLL bypassed, dual ADC tile configuration
111	DAC Input sampling frequency (Fs)	0.5 - 10.0	GHz	PLL bypassed
112	PLL output frequency (Fout)	1) 0.5 - 5.000 2) 0.5 - 6.882 3) 0.5 - 10.00	GHz	1) RF-ADC PLL output frequency range, 2) RF-DAC PLL output Low frequency range, 3) RF-DAC PLL output High frequency range.
113	Phase noise for the RF-ADC (PN_ADC)	-124, -128; -135, -143.	dBc/Hz	Offset = 100 kHz, Offset = 1 MHz, Offset = 2.5 MHz, Offset = 10 MHz.
114	Phase noise for the RF-DAC (PN_DAC)	-121, -128, -135, -144.	dBc/Hz	Offset = 100 kHz, Offset = 1 MHz, Offset = 2.5 MHz, Offset = 10 MHz.
115	Reference spur (RS)	-70	dBc	
116	Reference harmonic spur (RHS)	-70 -80	dBc	Offset from carrier <800 MHz Offset from carrier >800 MHz



ZONE 3 - Class RF1.1

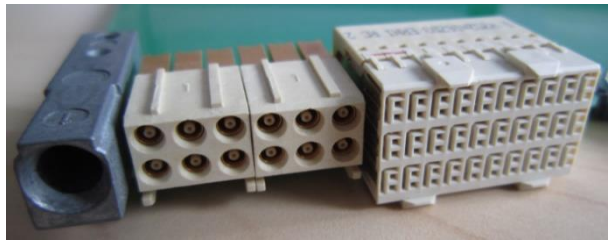
TE Connectivity (ERNI) and Radiall Connectors – Johannes Zink

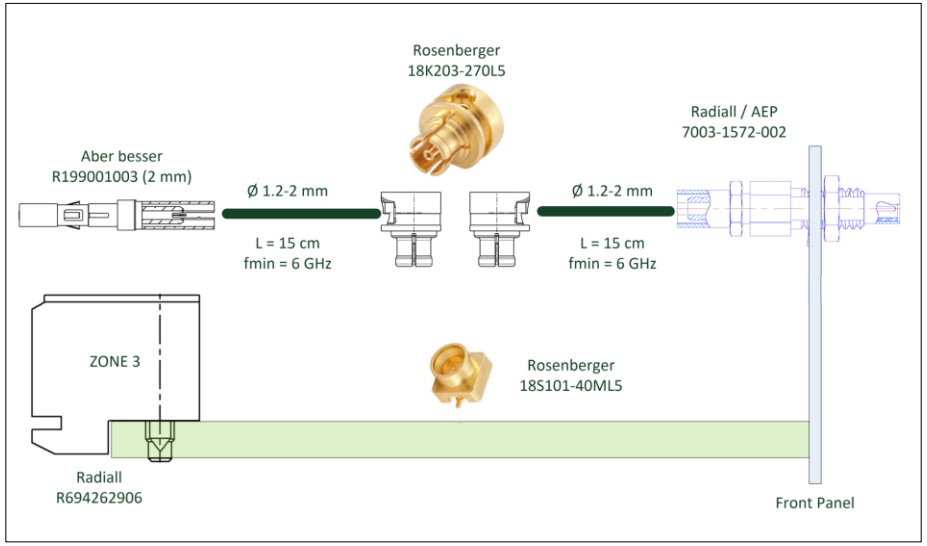
		Digital Clock IO	Digital Fixed IO	Digital Clock Input	Digital User IO		Differential DACs			MTCA.4 Management	
J30		10	9	8	7	6	5	4	3	2	1
-	F	AMC-CLK-	OUT1-/D8-	RF-CLK3-	DAC7-	D5-	DAC4-	D2-	DAC1-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D8+	RF-CLK3+	DAC7+	D5+	DAC4+	D2+	DAC1+	TDI	TCK
-	d	RF-CLK2-	OUT0-/D7-	RF-CLK1-	D6-	DAC5-	D3-	DAC2-	D0-CC-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D7+	RF-CLK1+	D6+	DAC5+	D3+	DAC2+	D0-CC+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-	DAC6-	D4-	DAC3-	D1-	DAC0-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+	DAC6+	D4+	DAC3+	D1+	DAC0+	PWRA2	PWRA1

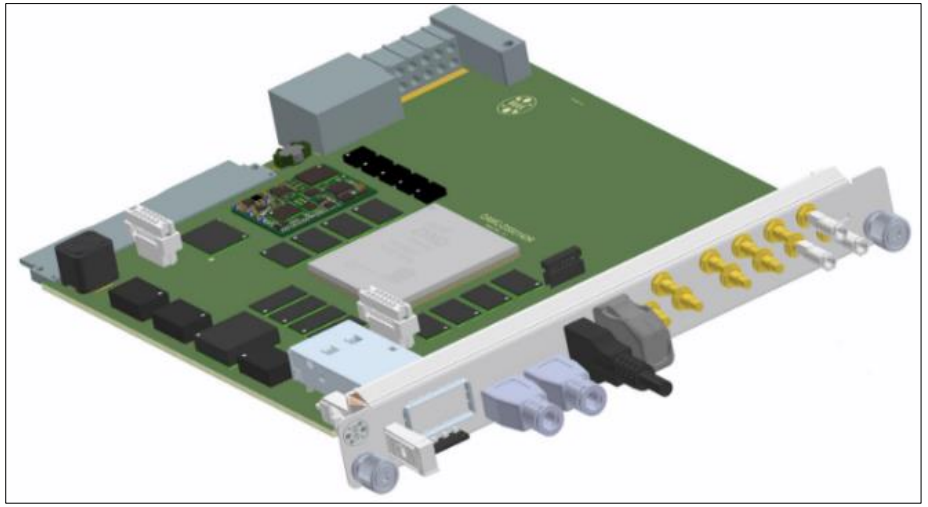
Single Ended Analog Signals

J31		3	2	1
	B	ADC-IN7	DAC-OUT1	DAC-OUT3
	A	ADC-IN6	DAC-OUT0	DAC-OUT2
J32		3	2	1
	B	ADC-IN1	ADC-IN3	ADC-IN5
	A	ADC-IN0	ADC-IN2	ADC-IN4

Zone 3 – Class RF1.1 pin assignment J30, J31, and J32 Connector, AMC side View.







Project Status and Updates

Project timeline

1) Schematics is completed and reviewed on 10 August 2024.

2) PCB routing will start on 9 September 2024.

3) We expect the PCB routing to be finished in two months.

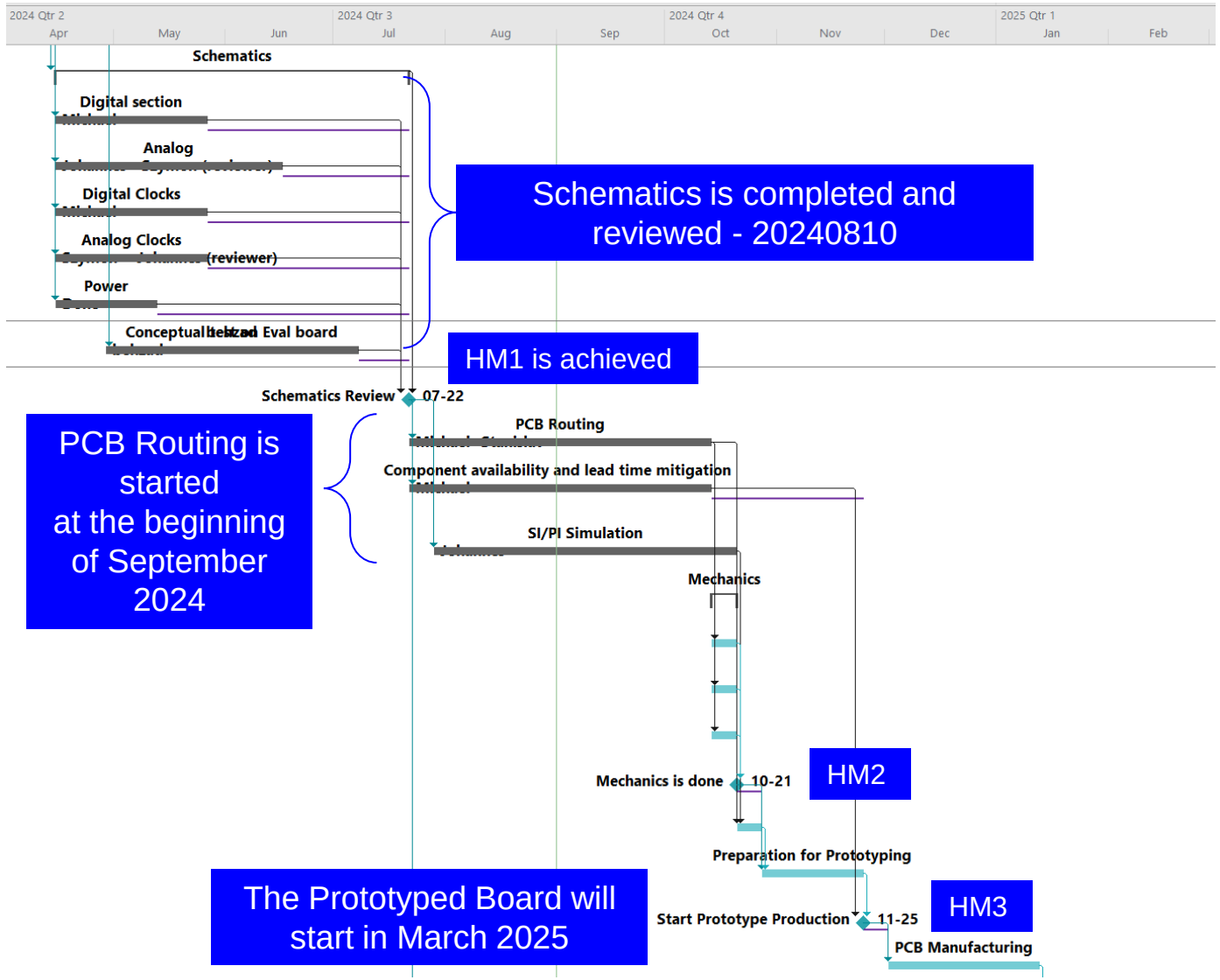
4) To mitigate the project risk, two sensitive sections, i.e., analog front-end and clock synthesizer, will be prototyped on separate evaluation boards fully compatible with Xilinx RFSoC Eval Board ZCU208.

   a) The Analog Front-end eval board will be sent to the manufacturing company in the middle of October. We expect to receive the AFE By the end of 2024.

   b) The Clock Synthesizer eval board will be sent to the manufacturing company at the beginning of December 2024. The Clock Synthesizer eval board will be received in February 2025.

5) The analysis of these two eval boards will be used to justify the design of the main DAMC-DS5014 board.

6) By the end of March 2025, DS5014DR will be ready for prototyping and in June 2025, the prototyped board will be ready.



Summary

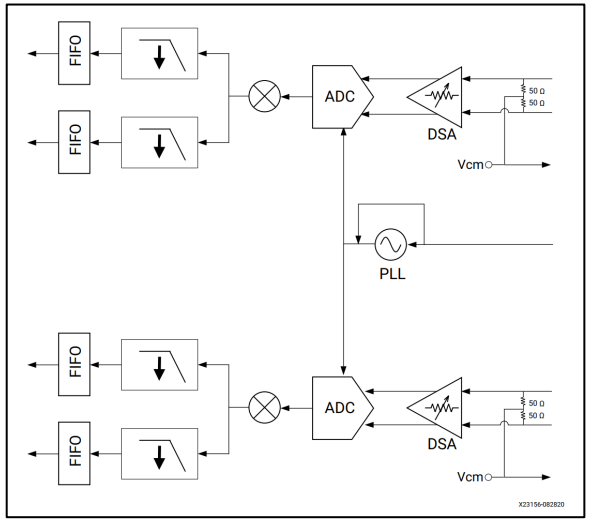
- The DAMC-DS5014DR project progress is well advanced.
- The first high-level milestone of the project has been achieved based on the plan.
- The PCB routing of the board has been started, and the board PCB stackup has already been defined.
- The project's risk has been mitigated by prototyping two crucial sections of the electronics in advance to ensure that these electronics boards meet all design aspects.
- As a result of this mitigation, the prototyping was shifted from 25 November 2024 to the June 2025.

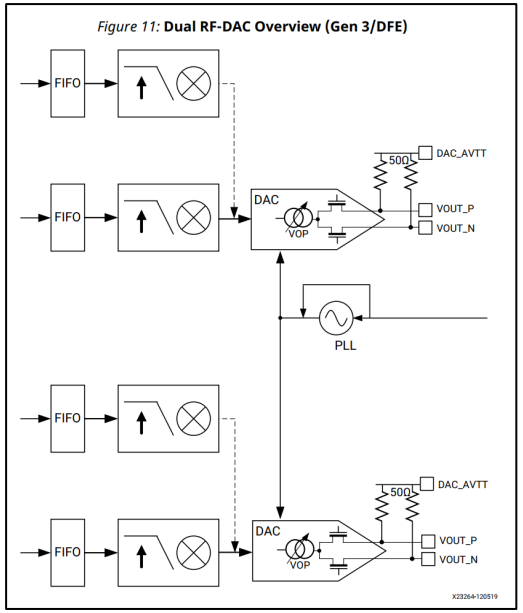
Thank You for your attention!

Backup Slides

Review of the DS5014DR Specifications

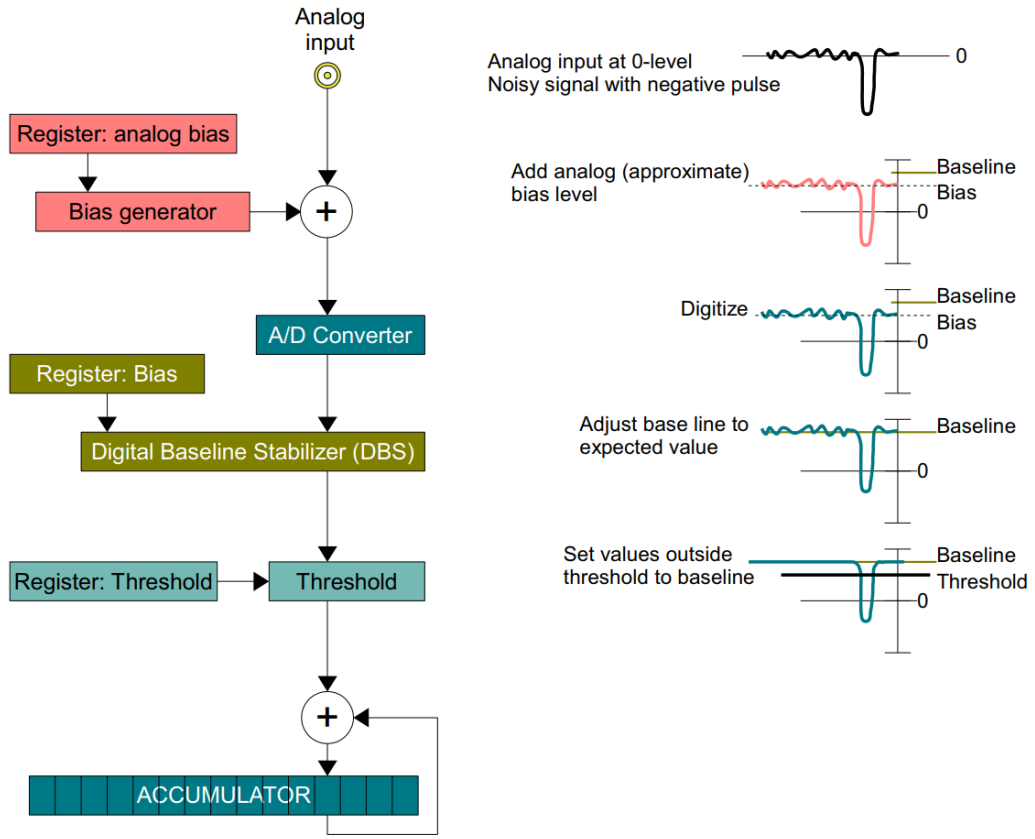
FPGA Resources	Parameter	Value	Scale	Condition
Part Number	XCZU47DR-1FFVG1517E			
	ADC Tile Configuration	Dual		14-bit RF-ADC with DDC
	Number of ADC Tiles	4		
	Number of ADC Channels	8		
	ADC Max Rate	5	GSPS	
	DAC Tile Configuration	Dual		14-bit RF-DAC with DUC
	Number of DAC Tiles	4		
	Number of DAC Channels	8	-	
	DAC Max Rate	8.92 (9.85)	GSPS	
	Number of DDCs per RF-ADC	1	-	
	Analog Bandwidth	6	GHz	
	Decimation / Interpolation	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x	-	
	System Logic Cells	930	k	
	CLB LUTs	425	k	
	Max. Dist. RAM	13	Mb	
	Total Block RAM	38	Mb	
	UltraRAM	22.5	Mb	
	DSP Slices	4272	-	
	GTY Transceivers(32.75Gb/s)	16	-	
	PCIe Gen3 x16	-	-	
	PCIeGen3 x16/Gen4 x8 / CCIX	2	-	
	150G Interlaken	1	-	
	et MAC/PCS w/RS-FEC	2	-	
	System Monitor	2	-	
	Speed Grades	-1E	-	
	PSIO	214	-	
	HDIO	48	-	
	HPIO	299	-	
	GTR (6.0Gb/s)	4	-	
	GTY	16	-	
	Package Footprint	FFVG1517	-	
	Package size	40 x 40	mm^2	





DS5014DR - Front-end Eval Board

DC Signal flow



Courtesy of TELEDYNE SP Devices
Waveform averaging Application Note 11-0699-C 2017-10-04

RF-ADC Electrical Characteristics

ZU4xDR

Figure 17: **RF-ADC Analog Input (Gen 3/DFE)**

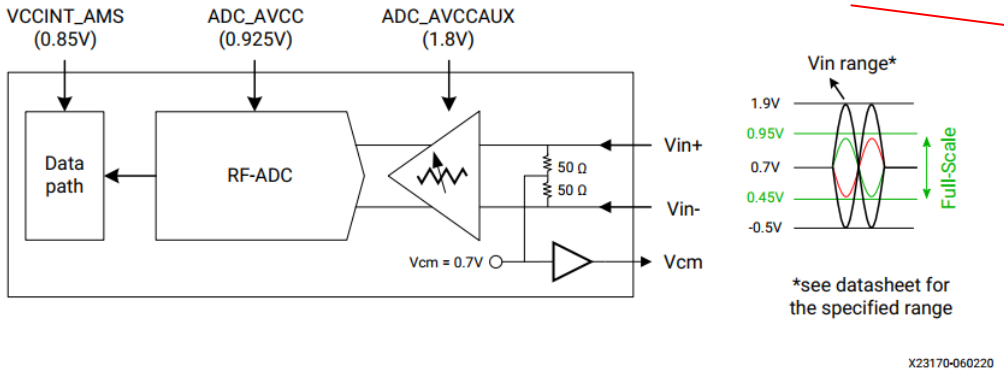
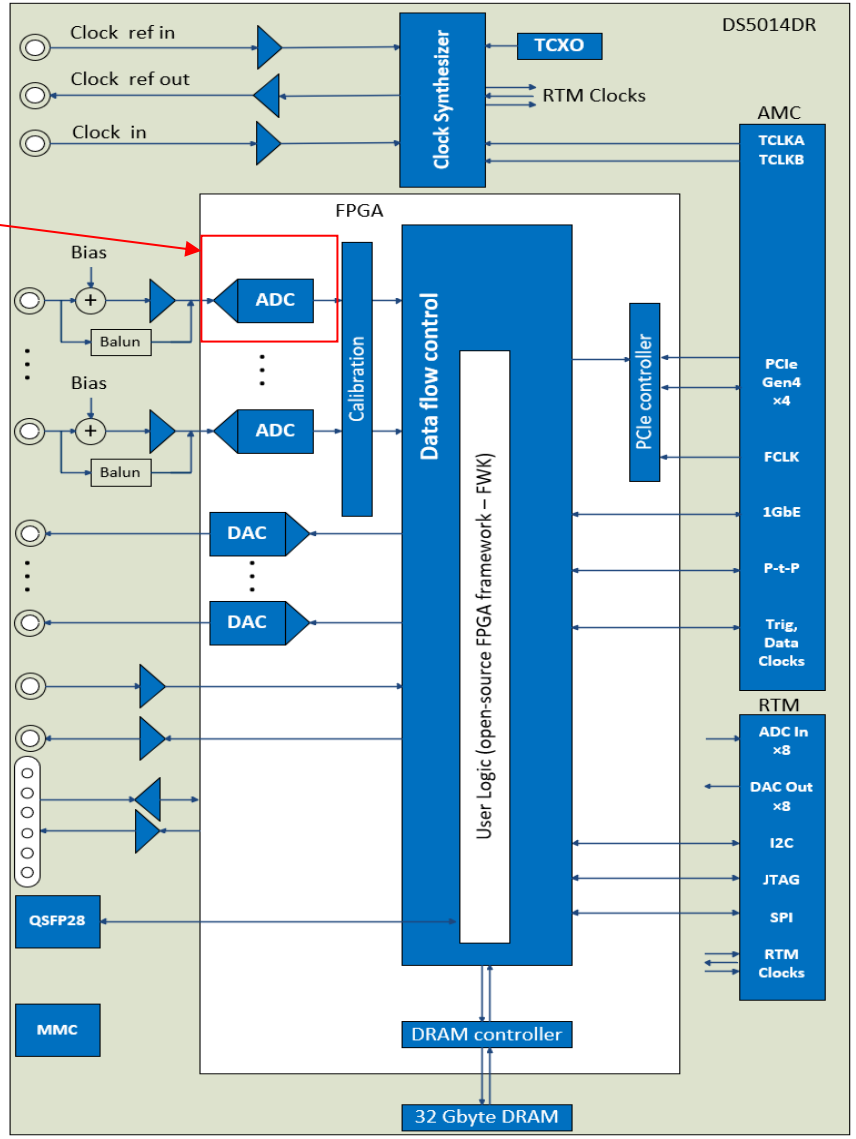


Table 117: **RF-ADC Electrical Characteristics for ZU4xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog inputs					
Resolution		14	–	–	Bits
Sample Rate	Devices using quad ADC tile channel	0.5	–	2.5	GS/s
	Devices using dual ADC tile channel	1	–	5	GS/s
Full-scale input[3]	Input 100Ω on-die termination when DSA attenuation = 0 dB	–	1	–	V_{PPD}
		–	1	–	dBm
Maximum allowed input power	Input 100Ω on-die termination when DSA attenuation ≥ 15 dB	–	4.8	–	V_{PPD}
		–	14.6	–	dBm
Digital Attenuation Range		0	–	27	dB
Attenuator step size		–	1	–	dB



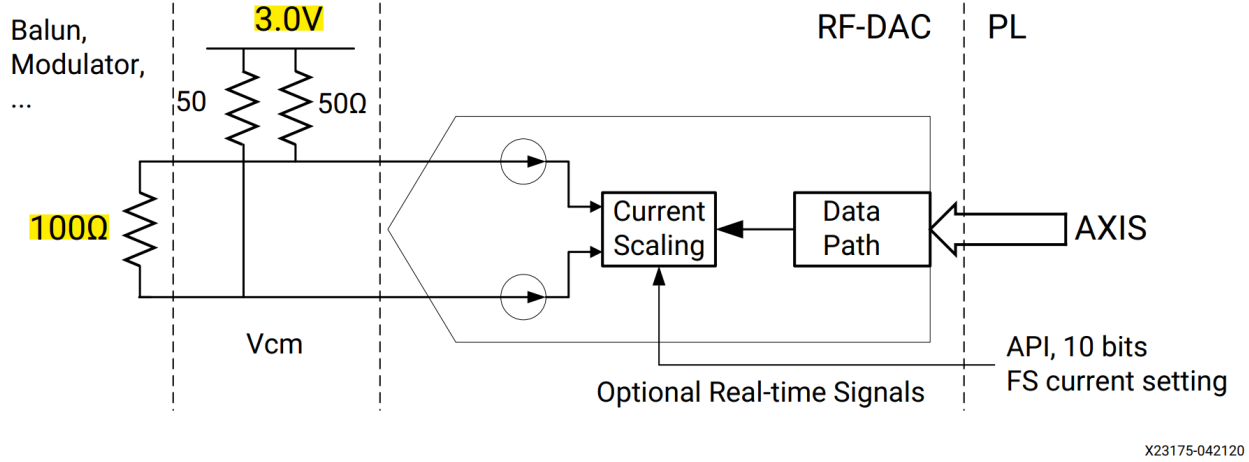
RF-DAC Electrical Characteristics

DAC_{AVTT}

- ***Variable Output Power (VOP) (Gen 3/DFE)***

  - Many transmitter systems include variable gain amplifier (VGA) stages that allow signals to be amplified or attenuated in the analog domain. The RF-DAC analog circuitry supports the ability to adjust the output power and is combined with digital control to implement the RF-DAC Variable Output Power (VOP) feature.

$$DAC_{AVTT} = 3.0\ V$$



CAUTION! *To use the VOP feature, the DAC_AVTT must be 3.0V.*

  - The variable output power is achieved by varying the full-scale current in fine steps defined in datasheet DS926.
  - RF-DAC full scale current can be derived as follows:

$$I_{OUTFS}\ (\mu A) = \text{Minimum VOP Current} + \text{N} * \text{VOP step size}\ (\mu\text{A})$$

RF-DAC Electrical Characteristics

DAC output Swing

- ***DAC Transmit Transfer Function***
- The differential output provides the maximum output current when all digital input bits are High.
- The output current (using binary format) is shown in the following equations:

  - $I_{OUTP} = \pm \frac{Bin\ Data\ In}{2^N} \times I_{OUTFS}$
  - $I_{OUTN} = I_{OUTFS}$ - I_{OUTP}
  - $V_{CM} = DAC_{AVTT} - I_{OUTFS} \times (0.5 + 0.08) \times 50\ \Omega$

    where:

    1. $Bin\ Data\ In = Signed\ 14 - bit$ Number
    2. I_{OUTFS} = Full-scale output current
    3. V_{CM} is the common-mode voltage on each $VI_{OUTP/N}$ leg

RF-DAC Electrical Characteristics

Common Mode Voltage

- $I_{OUTFS}\ (\mu A) = \text{Minimum VOP Current} + \text{M} \times \text{VOP step size (µA)}$

  $= 6.4\ \text{mA} + \ \text{M}\ \times 43.75\ \mu A \qquad (M: 0, 1, 2, \ldots)$

  $I_{OUTFS}\ (\mu A) = 6.4\ mA \sim 32\ mA$

- $V_{CM\_Max} = DAC_{AVTT} - I_{OUTFS} \times (0.5 + 0.08) \times 50\ \Omega =$

  $3.0\ V - 6.4\ mA \times (0.5 + 0.08) \times 50\ \Omega = 2.81\ \text{V}$

- $V_{CM\_Min} = DAC_{AVTT} - I_{OUTFS} \times (0.5 + 0.08) \times 50\ \Omega =$

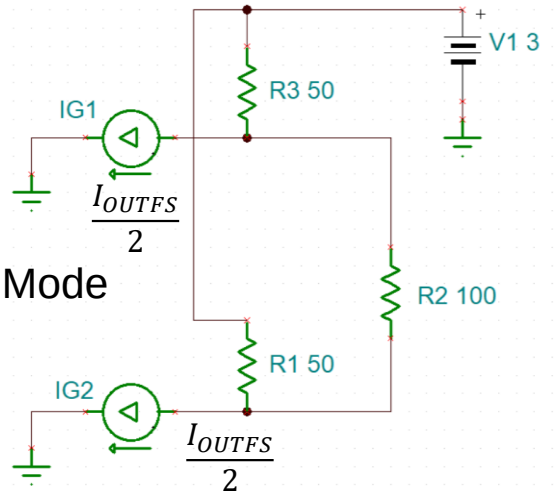
  $3.0\ V - 32\ mA \times (0.5 + 0.08) \times 50\ \Omega = 2.1\ \text{V}$

- $I_{OUTP} = \frac{Bin\ Data\ In}{2^N} \times I_{OUTFS} \qquad Bin\ Data\ In = 14 - bit\ signed$

  $N = 14$

Table 132: **RF-DAC Electrical Characteristics for ZU4xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog Outputs					
Resolution		14	–	–	Bits
Sample rate[3]	-2E, -2I, -2LI speed grade without clock forwarding, datapath modes 2, 3, and 4	0.5	–	9.85	GS/s
	-2E, -2I, -2LI speed grade with clock forwarding, datapath modes 2, 3, and 4	0.5	–	9.70	GS/s
	-1E, -1I, -1LI, -1M speed grade, datapath modes 2, 3, and 4	0.5	–	8.92	GS/s
	All speed grades, datapath mode 1	0.5	–	7.0	GS/s
Maximum output power	V_{DAC_AVTT} = 3.0V, 100Ω termination, signal frequency <200 MHz	–18.5	–	6.5	dBm
Output current range	AC coupling: V_{DAC_AVTT} = 3.0V, 100Ω termination, signal frequency <200 MHz	2.25	–	40.5	mA
	DC coupling: V_{DAC_AVTT} = 3.0V, 100Ω termination, signal frequency <200 MHz	6.4	–	32	mA
Variable output current step size		–	43.75	–	µA
Variable output power range	At 240 MHz	24	–	–	dB
Equivalent dynamic range from output current range[4]	At 3500 MHz	20	–	–	dB
	At 4900 MHz	18	–	–	dB
	At 5900 MHz	17	–	–	dB
Analog bandwidth	Full power bandwidth (–3 dB)	–	6	–	GHz
Return loss (R_L)[5]	Up to 4 GHz	–	–12	–	dB
	Up to 6 GHz	–	–10	–	dB
On-die termination	Single-ended on-die termination to external 3V V_{DAC_AVTT}	–	50	–	Ω
Crosstalk isolation between channels[6]	F_{OUT} = 0–4 GHz	–	–75	–	dBc
	F_{OUT} = 0–6 GHz	–	–70	–	dBc



Common Mode

Radio Frequency System-on-Chip

The main benefit of the RFSoC

- **Multi-Tile Synchronization (MTS)**
  - **MTS** is a crucial feature in the RFSoC architecture that enables the synchronization of multiple ADC tiles to ensure accurate and coherent data acquisition.
  - **ADC Tiles:** RFSoCs feature multiple ADC tiles, each containing a set of ADC channels. These tiles are designed to handle high-speed analog signals and convert them into digital data.
  - **Synchronization Challenges:** Without proper synchronization, each ADC tile operates with its independent clock, leading to timing mismatches between the sampled data from different tiles. These mismatches introduce phase errors and distortions, compromising the coherence and accuracy of the acquired data, especially for high-frequency signals.
  - ***MTS Solution:*** *MTS addresses this synchronization challenge by employing a common reference clock and dedicated circuitry to align the sampling instants of all ADC tiles. This ensures that data from different tiles are sampled at the same time, preserving phase relationships and data integrity.*

Zynq UltraScale+ RFSoC Product Selection Guide

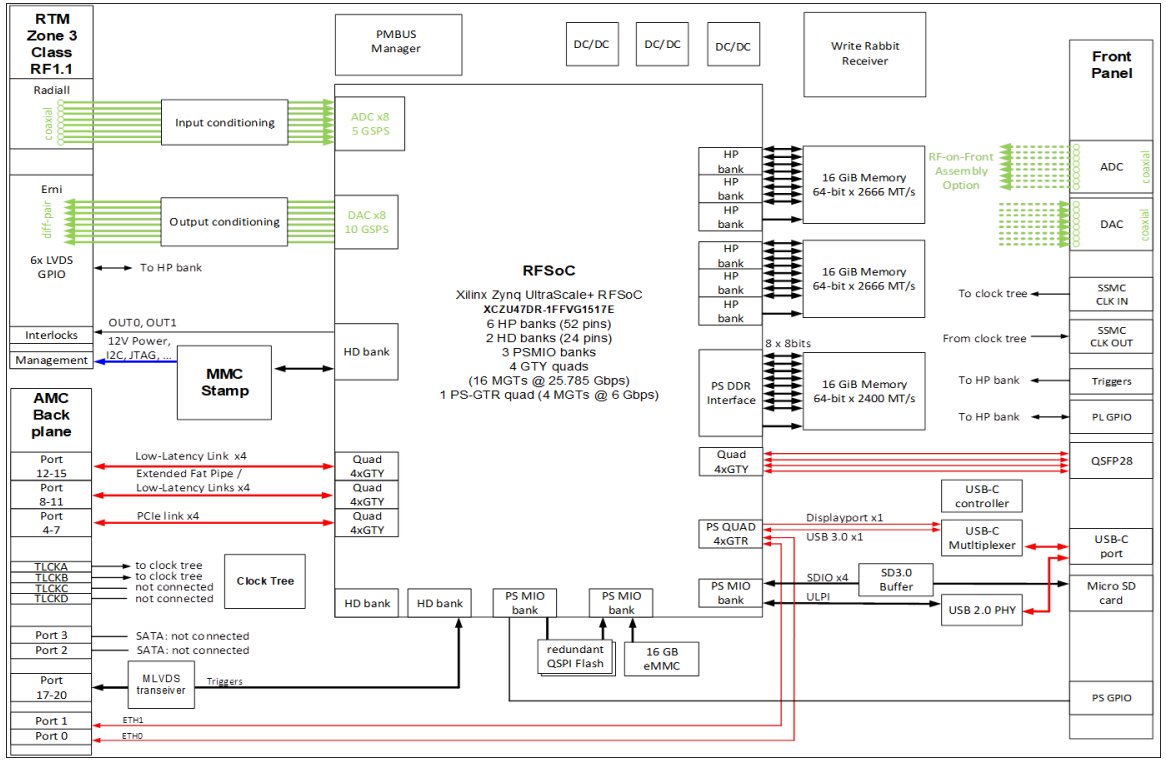
	Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
		Gen 1					Gen 2	Gen 3					
PS		**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz, **Dual-core** Arm Cortex-R5F MPCore up to 533MHz											
RF Data Converter	12-bit RF-ADC w/DDC # of ADCs	0	8	8	8	16	16	–	–	–	–	–	–
RF Data Converter	12-bit RF-ADC w/DDC Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	–	–	–	–	–	–
RF Data Converter	14-bit RF-ADC w/DDC # of ADCs	–	–	–	–	–	–	8 2	4	8 4	8	8	16
RF Data Converter	14-bit RF-ADC w/DDC Max Rate (GSPS)	–	–	–	–	–	–	2.5 5.0	5.0	2.5 5.0	5.0	5.0	2.5
RF Data Converter	14-bit RF-DAC w/DUC # of DACs	0	8	8	8	16	16	8	4	12	8	8	16
RF Data Converter	14-bit RF-DAC w/DUC Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	9.85[3]	9.85[3]	9.85[3]	9.85[3]	9.85[3]	9.85[3]
RF Data Converter	SD-FEC	8	0	0	8	0	0	0	0	8	0	8	0
RF Data Converter	Digital Front-End (DFE)	–	–	–	–	–	–	–	–	–	–	–	–
RF Data Converter	Number of DDCs per RF-ADC[1]	0	1	1	1	1	1	1	2	1	1	1	1
RF Data Converter	RF input Freq max. GHz	4					5	6					
RF Data Converter	Decimation / Interpolation	1x, 2x, 4x, 8x					1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x					
Programmable Logic (PL)	System Logic Cells (K)	930	678	930	930	930	930	489	930	930	930	930	930
Programmable Logic (PL)	CLB LUTs (K)	425	310	425	425	425	425	224	425	425	425	425	425
Programmable Logic (PL)	Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0
Programmable Logic (PL)	Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0
Programmable Logic (PL)	UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5
Programmable Logic (PL)	DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272
Programmable Logic (PL)	GTY Transceivers	16	8	16	16	16	16	8	16	16	16	16	16
Programmable Logic (PL)	PCIe® Gen3 x16	2	1	2	2	2	2	–	–	–	–	–	–
Programmable Logic (PL)	PCIe® Gen3 x16/Gen4 x8 / CCIX[2]	–	–	–	–	–	–	0	2	2	2	2	2
Programmable Logic (PL)	150G Interlaken	1	1	1	1	1	1	0	1	1	1	1	1
Programmable Logic (PL)	100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	0	2	2	2	2	2
Programmable Logic (PL)	System Monitor	2	2	2	2	2	2	2	2	2 2	2	2	2
Programmable Logic (PL)	Speed Grades	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI
Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC
D1156	35x35	214, 72, 208 4, 16 0, 0											
E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 24, 128 4, 8 10, 8	214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	
G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8	
F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16						214, 96, 312 4, 16 16, 16
H1760	42.5x42.5									214, 48, 312 4, 16 12, 12			

Zynq™ UltraScale+™ RFSoCs

1. This value applies when all RF I/O of an RF-ADC tile are used. 2. Operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213. 3. For operation up to 10GSPS, contact your local Xilinx Sales Representative.

Review of the DS5014DR Specifications

FPGA Resources	Parameter	Value	Scale	Condition
Part Number	XCZU47DR-1FFVG1517E			
	ADC Tile Configuration	Dual		14-bit RF-ADC with DDC
	Number of ADC Tiles	4		
	Number of ADC Channels	8		
	ADC Max Rate	5	GSPS	
	DAC Tile Configuration	Dual		14-bit RF-DAC with DUC
	Number of DAC Tiles	4		
	Number of DAC Channels	8	-	
	DAC Max Rate	8.92 (9.85)	GSPS	
	Number of DDCs per RF-ADC	1	-	
	Analog Bandwidth	6	GHz	
	Decimation / Interpolation	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x	-	
	System Logic Cells	930	k	
	CLB LUTs	425	k	
	Max. Dist. RAM	13	Mb	
	Total Block RAM	38	Mb	
	UltraRAM	22.5	Mb	
	DSP Slices	4272	-	
	GTY Transceivers	16	-	
	PCIe Gen3 x16	-	-	
	PCIeGen3 x16/Gen4 x8 / CCIX	2	-	
	150G Interlaken	1	-	
	et MAC/PCS w/RS-FEC	2	-	
	System Monitor	2	-	
	Speed Grades	-1E	-	
	PSIO	214	-	
	HDIO	48	-	
	HPIO	299	-	
	GTR	4	-	
	GTY	16	-	
	Package Footprint	FFVG1517	-	
	Package size	40 x 40	mm^2	



ZONE 3 Interface

ERNI and Radiall Connectors – Johannes Zink

	Zone 3 Interfaces with RTM (Class RF1.1)	Pin Assignment	Pin Number	I/O	Description
209	J30 ERNI Connector	PWRA1, PWRA2, PWRB1, PWRB2	1a, 2a, 1b, 2b	I	RTM supply voltage (12 V, 30 W max.)
210		PS#	1c	O	RTM present signal (connected to GND on RTM)
211		SDA, SCL	1d, 2d	I/O	I2C management interface to- RTM (level 3.3 V)
212		TCK, TDI, TDO, TMS	1e, 2e, 1f, 2f	I/O	JTAG interface to RTM
213		MGT-RX±	3a, 3b	I/O	Gigabit receiver, not implemented
214		DAC0±, DAC1±, DAC2±, DAC3±, DAC4±, DAC5±, DAC6±, DAC7±	3c, 3d, 3e, 3f, 4a, 4b,4c, 4d, 4e, 4f, 5a, 5b, 5c, 5d, 5e, 5f	O	Differential DAC outputs, DC coupling
215		D0-CC±, D1±, D2±, D3±, D4±, D5±	6a, 6b, 6c, 6d, 6e, 6f, 7a, 7b, 7c,7d, 7e, 7f	I/O	LVDS (Vcm 1.2V, Vdiff 350mV, 100R), connected to the PL HP bank (1.8V) Note: This interface is intended to carry a differential SPI Bus with LVDS levels. A CPLD on the RTM can fan out these signals into standard SPI and I2C busses.
216		RTM-CLK±	8a, 8b	I	LVDS/LVPECL clock input from RTM to the RF synthesizer
217		RF-CLK0±, ..., RF-CLK3	10a, 10b, 8c,8d, 10c, 10d,8e, 8f	I	Not implemented
218		AMC-TCLK±	9a, 9b	O	LVDS/LVPECL clock output to RTM derived from TCLK
219		OUT0/D6±, OUT1/D7±	9c, 9d, 9e, 9f	I/O	LVDS (Vcm 1.2V, Vdiff 350mV, 100R) trigger, interlock or user IO connected to the PL HP bank (1.8V)
220		AMC-CLK±	10e, 10f	O	LVDS/LVPECL output clock to RTM from RF synthesizer
221					
222					
223	J31 Radiall Connector	DAC-OUT0, DAC-OUT1, DAC-OUT2, DAC-OUT3	1a, 1b, 2a, 2b	O	Single-ended DAC outputs, AC coupling
224		ADC-IN6, ADC-IN7	3a, 3b	I	Single-ended ADC inputs, AC coupling
225					
226					
227	J32 Radiall Connector	ADC-IN0, ADC-IN1, ADC-IN2, ADC-IN3, ADC-IN4, ADC-IN5	1a, 1b, 2a, 2b, 3a, 3b	I	Single-ended ADC inputs, AC coupling
228					

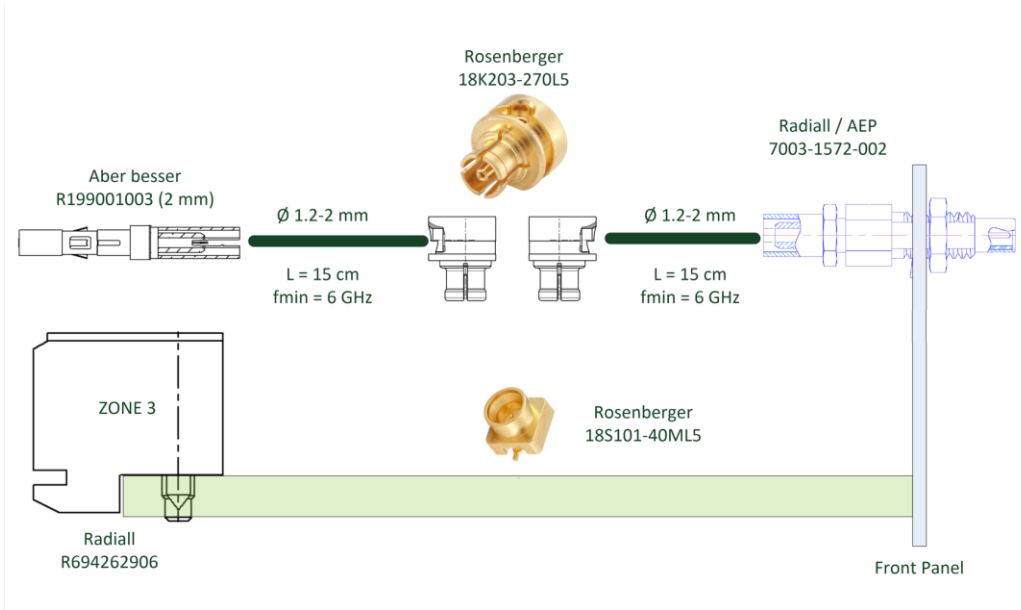
		Digital Clock IO	Digital fixed IO	Digital Clock Input	Digital user IO		Differential DACs			MTCA.4 Management	
J30		10	9	8	7	6	5	4	3	2	1
-	f	AMC-CLK-	OUT1-/D7-	RF-CLK3-	D5-	D2-	DAC7-	DAC4-	DAC1-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D7+	RF-CLK3+	D5+	D2+	DAC7+	DAC4+	DAC1+	TDI	TCK
-	d	RF-CLK2-	OUT0-/D6-	RF-CLK1-	D4-	D1-	DAC6-	DAC3-	DAC0-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D6+	RF-CLK1+	D4+	D1+	DAC6+	DAC3+	DAC0+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-	D3-	D0-CC-	DAC5-	DAC2-	GBT0-RX-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+	D3+	D0-CC+	DAC5+	DAC2+	GBT0-RX+	PWRA2	PWRA1

Single Ended Analog Signals

J31	3	2	1
B	ADC-IN7	DAC-OUT1	DAC-OUT3
A	ADC-IN6	DAC-OUT0	DAC-OUT2

J32	3	2	1
B	ADC-IN1	ADC-IN3	ADC-IN5
A	ADC-IN0	ADC-IN2	ADC-IN4

Table 1: Zone 3 - Class RF1.1 pin assignment J30, J31 and J32 connector, AMC side view

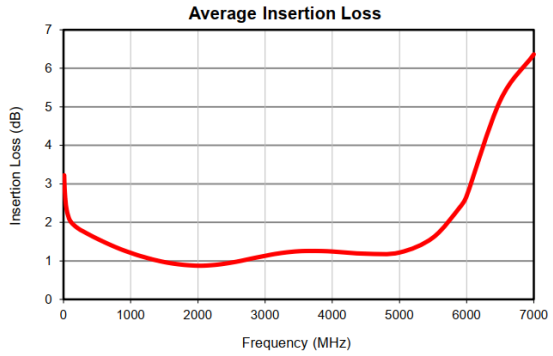


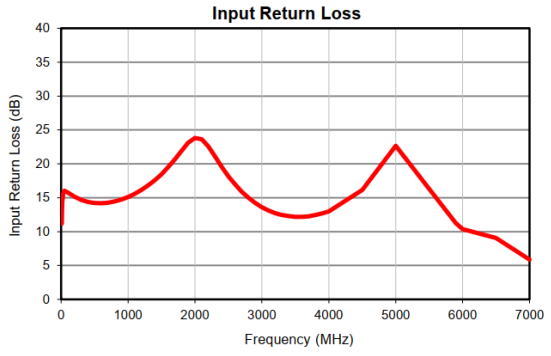
Selected Passive Baluns

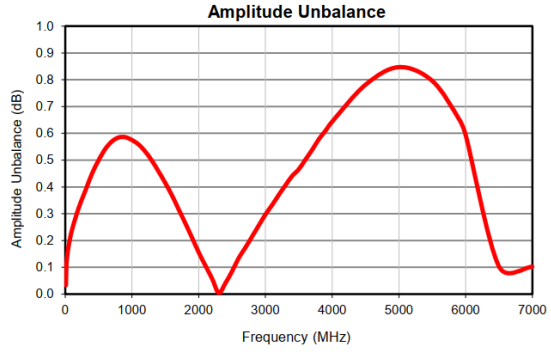
➢ **Passive Balun: TCM2-63WX+**

RF Transformer **TCM2-63WX+**

Typical Performance Data







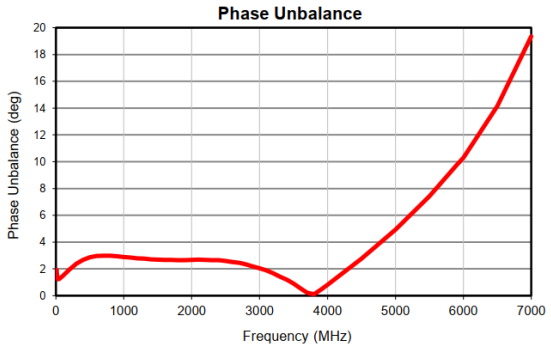
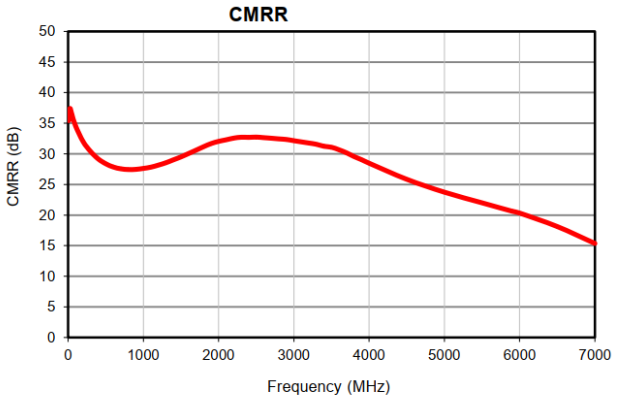


Table 3-2: **Balun Specification Recommendations**

Specification	Typical Result
Impedance ratio	2 or 1
Bandwidth	Application specific
Insertion loss	–1 dB or better
Return loss	–15 dB or better
Common-mode rejection ratio (CMRR)	>30 dB(1)
Amplitude imbalance	<~0.5 dB
Phase imbalance	<~1.5°

Notes:

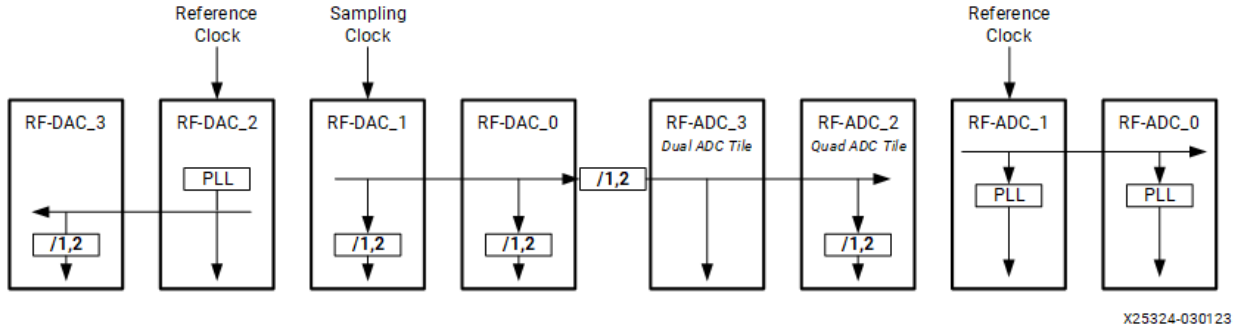
1. CMRR can be relaxed if the system is designed to avoid second harmonic distortion (HD2) by frequency planning.



On-chip Clock Distribution

Szymon Jabłoński

- The clock signal from the source tile can be:
  - External sampling clock
  - External reference clock used with internal PLLs
  - Sampling clock generated by on-chip PLL



- Clock forwarding
  - No individual clock for each tile
  - Skipping over a tile using a different clock is not allowed
  - When a tile group comprise of both RF-DAC tiles and RF-ADC tiles, the source tile must be a RF-DAC tile; forwarding clock from RF-ADC tile to RF-DAC tile is not allowed
  - Any tile can be a source tile to forward its low frequency reference clock within a tile group
  - High frequency sample rate clock from external or generated by in-tile PLL:
    - Only RF-ADC Tile 3 and Tiles 2 are allowed to accept forwarded clock from RF-DAC tiles
    - Either Tile 1 or Tile 2 (the two center tiles) can be a source tile if it has the external clock input pins.

RF Data Converter Subsystem

DS889 (v1.14) June 27, 2023

Table 6: **RF-ADC and RF-DAC Tile Configurations**

	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
	Gen 1				Gen 2	Gen 3					
RF Transceiver	**8x8**	**8x8**	**8x8**	**16x16**	**16x16**	**8x10**	**4x4**	**12x12**	**8x8**	**8x8**	**16x16**
14-bit Quad DAC Tile	2	2	2	4	4	2		2			4
14-bit Dual DAC Tile								2	4	4	
14-bit Single DAC Tile							4				
12-bit Quad ADC Tile				4	4						
14-bit Quad ADC Tile						2		2			4
12-bit Dual ADC Tile	4	4	4								
14-bit Dual ADC Tile						1		2	4	4	
14-bit Single ADC Tile							4				