Development of a new AMC card for the Diamond-II EBPM Upgrade

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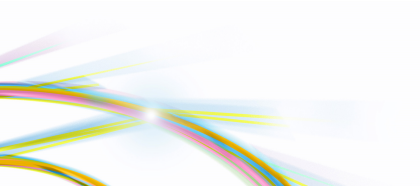


Overview

Diamond-II upgrade requires rebuild of EBPM and FOFB systems

- New Electron Beam Position Monitoring (EBPM) and Fast Orbit FeedBack (FOFB) system needed as part of Diamond-II upgrade
- New EBPM system design based on FMC ADCs and MTCA based FPGA signal processing
- Initial system development with Vadatech AMC525 and AMC561 cards
- Design now moving to IOxOS IFC_1412 card (in final stages of development)

Diamond-II Upgrade

New Requirements for Beam Position Stability

During 2028 the entire Diamond-II storage ring will be upgraded. Goals include:

- Increase of beam Brightness by between 10- and 100-fold
- Reduction of horizontal emittance from 2.7 to 0.16 nm radian (substantial reduction of beam size delivered to users)

Combined with faster detectors this increases the demands on the electron beam stability:

- The required Fast Orbit FeedBack (FOFB) closed loop bandwidth increases from 100 Hz to 1 kHz

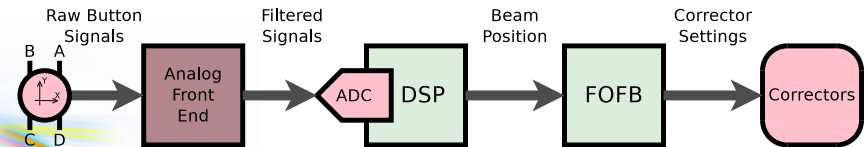
This requires the following changes to the Electron Beam Position Monitoring (EBPM) system:

- Increase beam position readout rate from 10 kHz to 100 kHz
- Reduce closed loop delay from 800 µs to 100 µs

Diamond-II EBPM and FOFB Digital Architecture

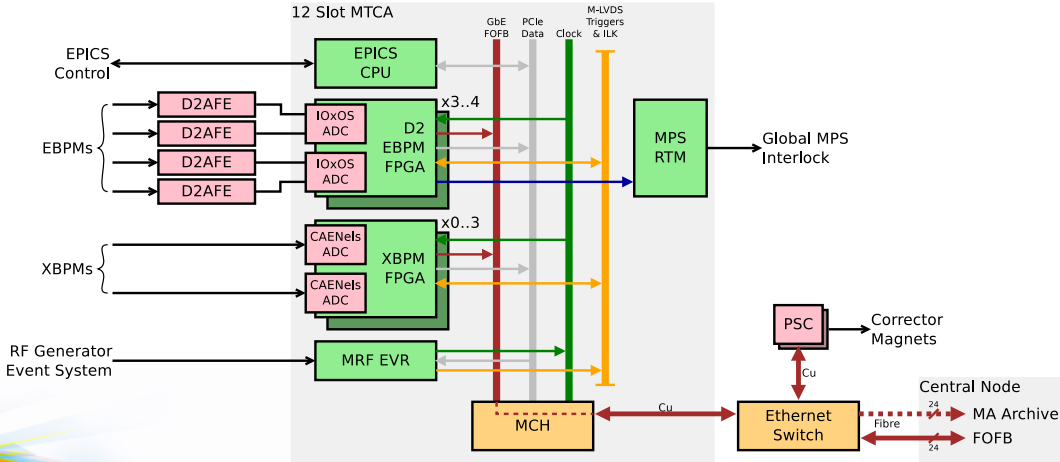
Overview of Signal Processing Chain

- Four RF signals from each of around 250 EBPM button blocks are digitised at around 217 MS/s
- FPGA signal processing extracts the RF component from each signal
- The four signal levels are used to compute the beam position at a variety of data rates
- The beam position is communicated (over Gigabit Ethernet) to a central Fast Orbit FeedBack computation node (network switch latencies looking larger than expected)
- Settings are then communicated back to corrector magnets distributed around the storage ring



One of 24 Storage Ring Cells

MTCA system with up to 7 FPGA processing cards



Requirements for AMC FPGA cards

The extra requirements turn out to be unexpectedly demanding!

Core requirements:

- Capable Xilinx FPGA: at least 1,000 DSPs (existing design currently uses 750 so far). Baseline is Virtex-7 690 (3,600 DSPs) on Vadatech AMC525
- At least 1 GB of on-board storage with at least 4 GB/s transfer capability
- Dual High Pin Count (HPC) FMC slots (to carry IOxOS ADC_3110 ADCs)
- Connectivity: AMC 0 (GigE), AMC 4:7 (PCIe), AMC 17:20 (type 2 M-LVDS)
- Clock distribution: TCLKA to FMCs (and TCLKB to FPGA, optional)
- RTM connector (no special requirements)

Extra requirements arising:

- The ADC_3110 FMC appears to have particularly demanding power requirements
- Half-duplex dynamic multiplexing of some M-LVDS is required

Initial Implementation with the Vadatech AMC525

A good platform for firmware development, but fatal power management issues

Initial development was done with the Vadatech AMC525 and AMC561. The following problems arose:

- The AMC525 cannot handle the power demands of the ADC_3110, and the failure mode is extremely ungraceful (the card simply resets). The AMC561 is worse.
- The power handling issue was never satisfactorily resolved. A fix from IOxOS (moving some load from 3.3V to 1.8V rail) still fails on the AMC561
- M-LVDS support on the AMC561 is not designed for half-duplex operation: drive direction is set over I2C, which is too slow for our application
- We would need a different card for RTM support in the end

During this time IOxOS proposed development of the IFC_1412 AMC carrier.

A new AMC FMC Carrier

Surprisingly limited options available for AMC with HPC FMC

There are surprisingly few AMC cards with High Pin Count FMC and a modern FPGA

Improvements offered by proposed IFC_1412 over the IFC_1410 are

- Improved clock distribution
- Upgraded FPGA
- Upgraded memory (4 GB at 16 GB/s)
- Memory interface would use AXI instead of TOSCA (IOxOS proprietary)
- FMC+
- Improved MMC and firmware management

Both Diamond and BESSY agreed to participate in the development of the IFC_1412

IFC_1412 Development Timeline

Everything always takes longer than expected

May 2020	Start of firmware development of D2EBPM on AMC525 with ADC_3110 FMCs
Sep 2020	Overloading of AMC by FMC first observed, fix from IOxOS received by Dec
Jan 2021	IFC_1412 development first proposed by IOxOS
Mar 2021	Start of development with DLS and BESSY as partners, initial design by IOxOS
Dec 2021	IOxOS reports hardware design of prototype (schematics and layout) in progress
Dec 2022	IFC_1412 prototype delivered Intensive testing at Diamond during this period
Sep 2023	Pre-serial schematic review
May 2024	Delivery of second prototype
Aug 2024	Final revisions of pre-serial
Jan 2025	Expected delivery of final pre-serial

Issues Addressed During Board Development

MMC, Clocking, Power Management

Development of the board was an interactive process between myself and Emilio Perez Juarez at Diamond and Ralph Hoffmann at IOxOS with some input from Günther Rehm's group at BESSY.

- The Vadatech MCH is *much* more fussy than the NAT MCH. To get power to the board the IFC MMC needed to implement many extra commands
- Extensive rework of clock distribution network to ensure proper distribution and termination of clocking with good signal integrity
- Improvements to power handling and overload handling
- Numerous small changes across the whole design
- Memory controller firmware

Measurement of the VADJ current turns out to have been unexpectedly difficult, still waiting for final card version to complete this measurement!

Memory Controller Firmware

An unexpected extra task

Goals for Memory Interface

- AXI compliant interface capable of supporting full memory bandwidth
- Easy instantiation into Xilinx IP Integrator ("Block Design") tool
- Reliable long term operation and maintainability

The external memory hardware (SG GDDR6) is not supported by existing Xilinx memory controller IP, so a specialised controller needed to be written.

A snapshot from IOxOS last summer of their work in progress did not seem to meet our requirements, so over the last year I have written a new memory controller. This is available from Github at

https://github.com/DiamondLightSource/IFC_1412