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CMS

June 16, 2025

CMS ETROC testing and Constellation for DAQ

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Link to Indico

U.S. DEPARTMENT of ENERGY

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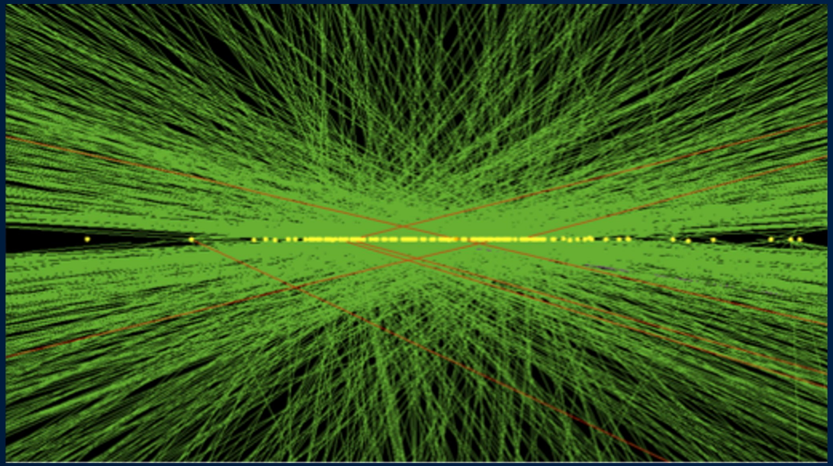
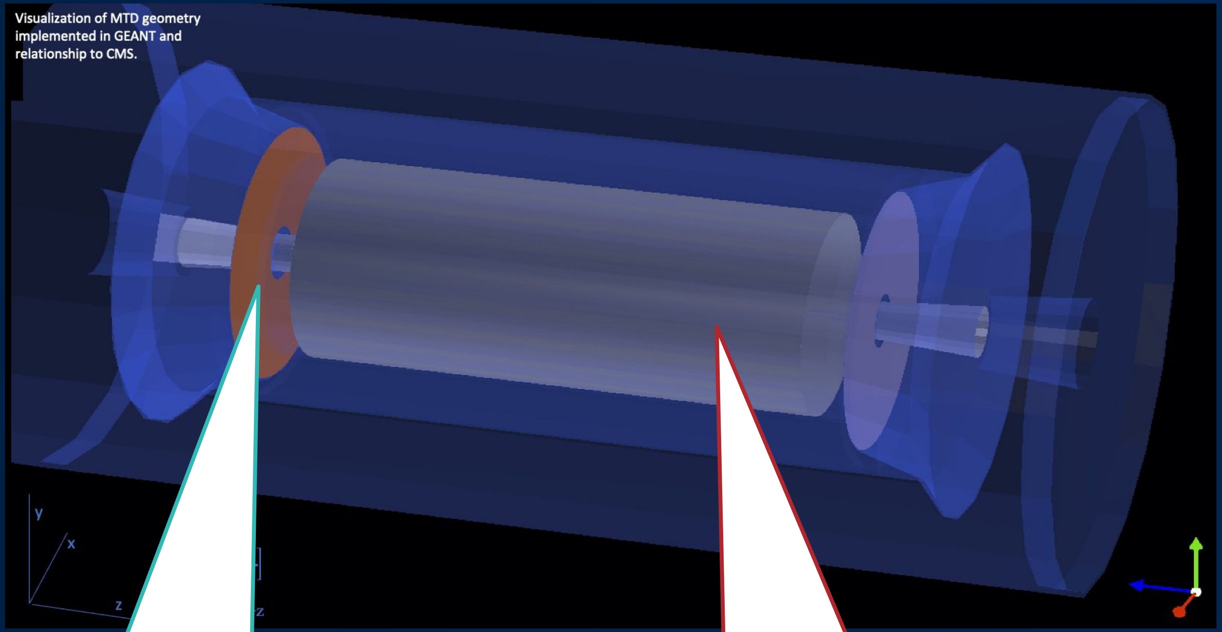
FERMI NATIONAL ACCELERATOR LABORATORY

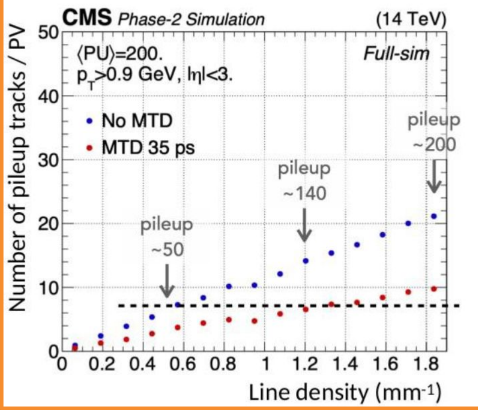
HL-LHC: First generation timing detectors

CMS Minimum Ionizing Particle Timing Detector





MIP Timing Detector (MTD) by CMS



The MTD will exploit timing information to reduce pile-up to current LHC level in both the forward and barrel regions.

Endcap Timing Layer (ETL)

Si with internal gain (LGAD):

- On the CE nose: $1.6 < |\eta| < 3.0$
- Radius: 315 < R < 1200 mm
- Position: z = ±3.0 m
- 1.3x1.3 mm^2 pixels
- ~14 m^2: 8.5M channels
- Fluence: up to 2E15 neq/cm^2

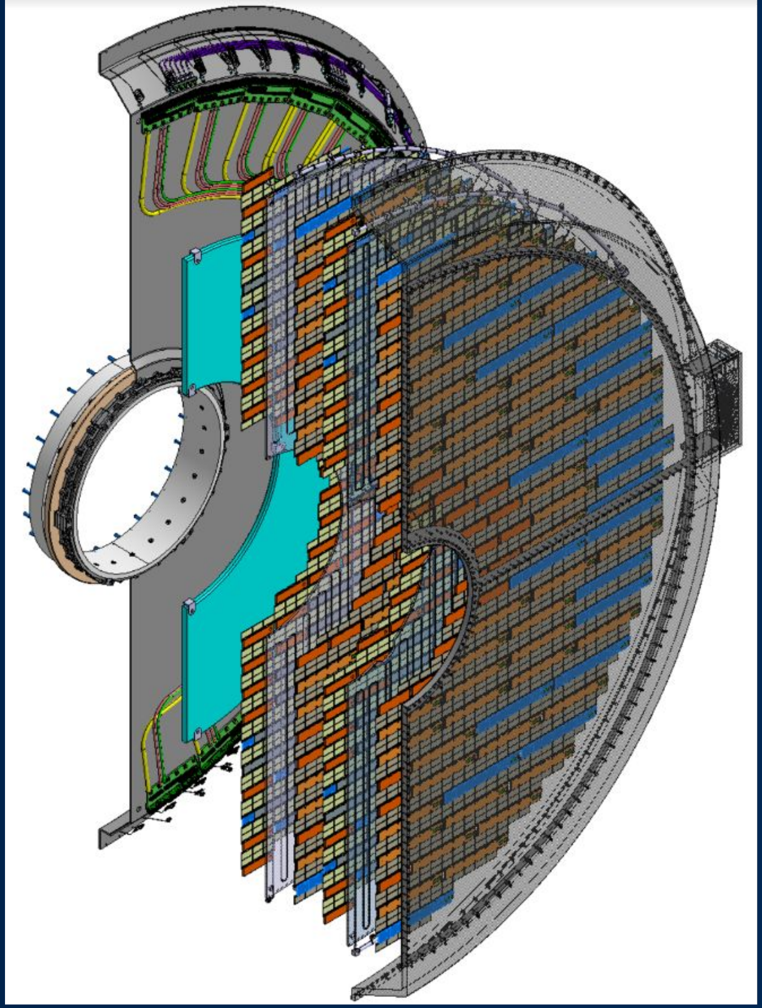
Barrel Timing Layer (BTL)

LYSO bars + SiPM readout:

- TK/ECAL interface: $|\eta| < 1.45$
- Inner radius: 1148 mm
- Thickness: 40 mm
- Length: ±2.6 m along z
- Area: 38 m2
- 332k channels

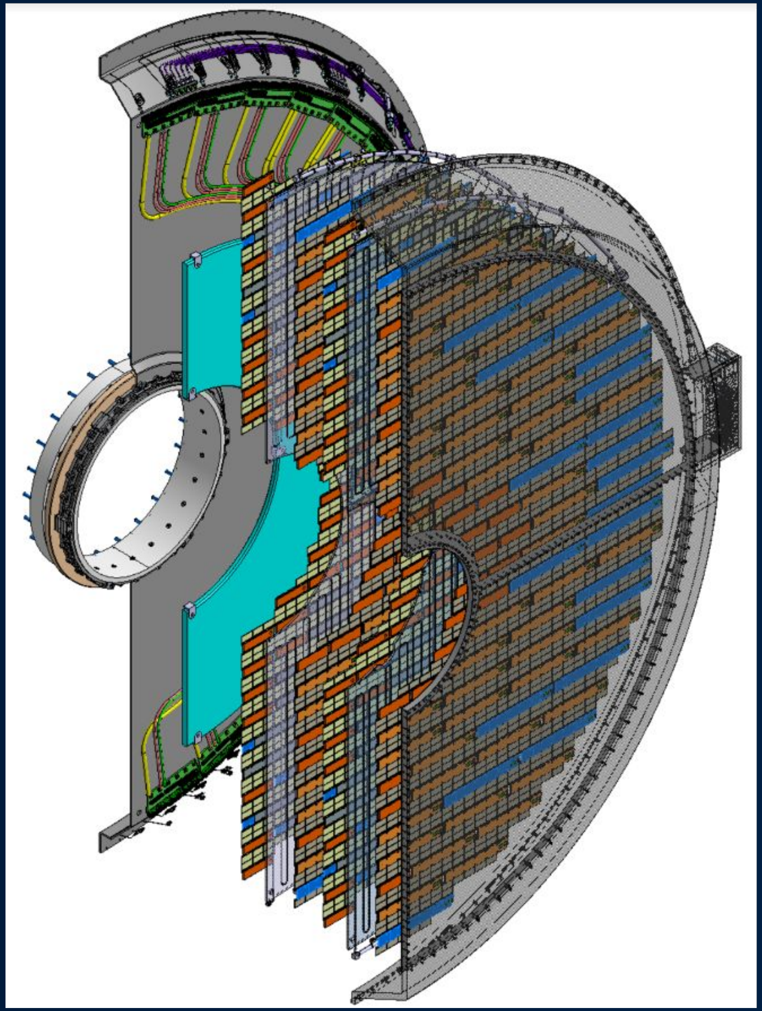
CMS Endcap Timing Layer

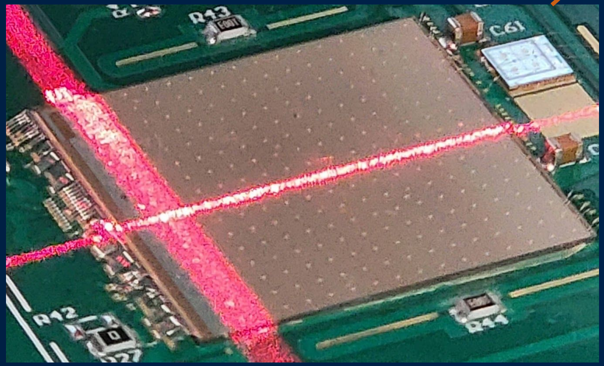
315 < R < 1200 mm, z = ±3.0 m, $1.6 < |\eta| < 3.0$, 1.3mm pixels, 14 m^2: 8.5M channels

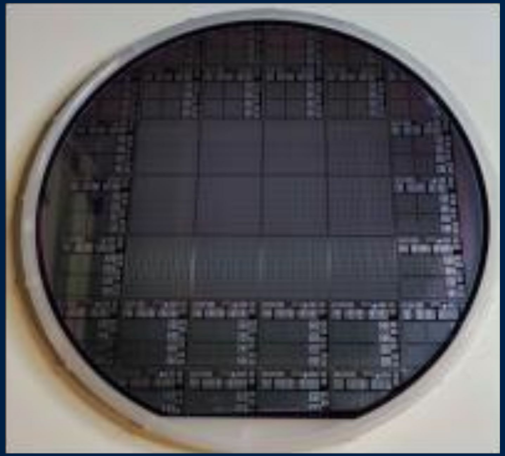


CMS Endcap Timing Layer

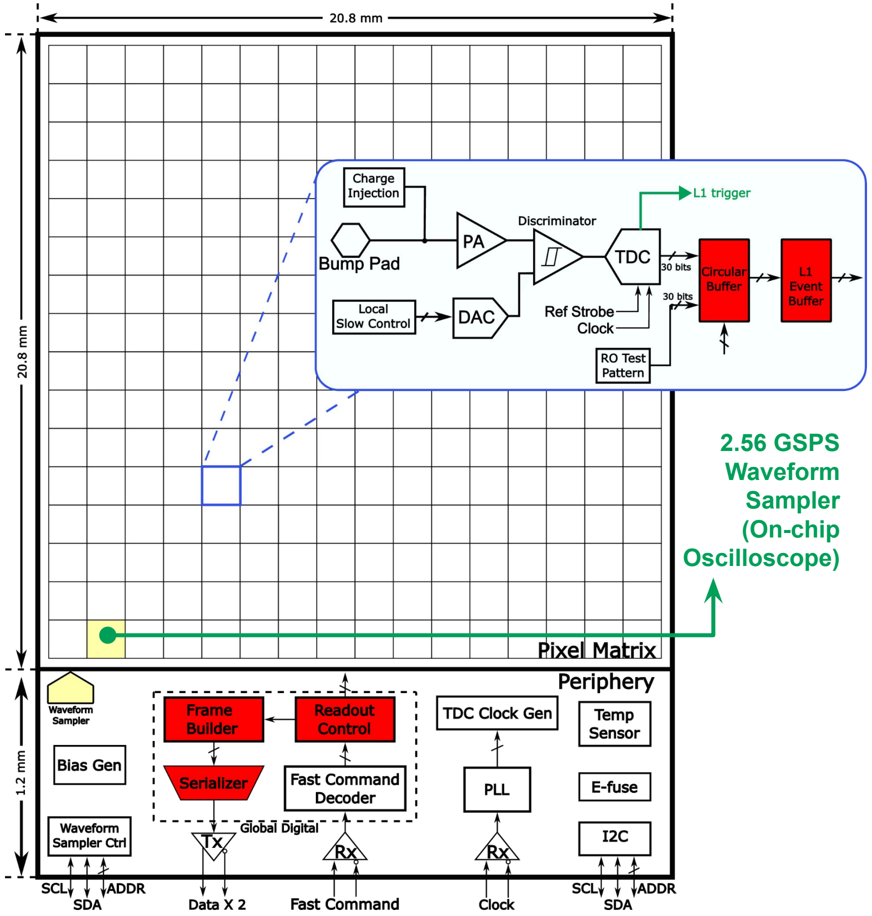
~33k chips, 2.3 x 2.1cm chips, 1.3 mm pixels, 16x16 px







ETL Read Out Chip (ETROC)



2.56 GSPS Waveform Sampler (On-chip Oscilloscope)

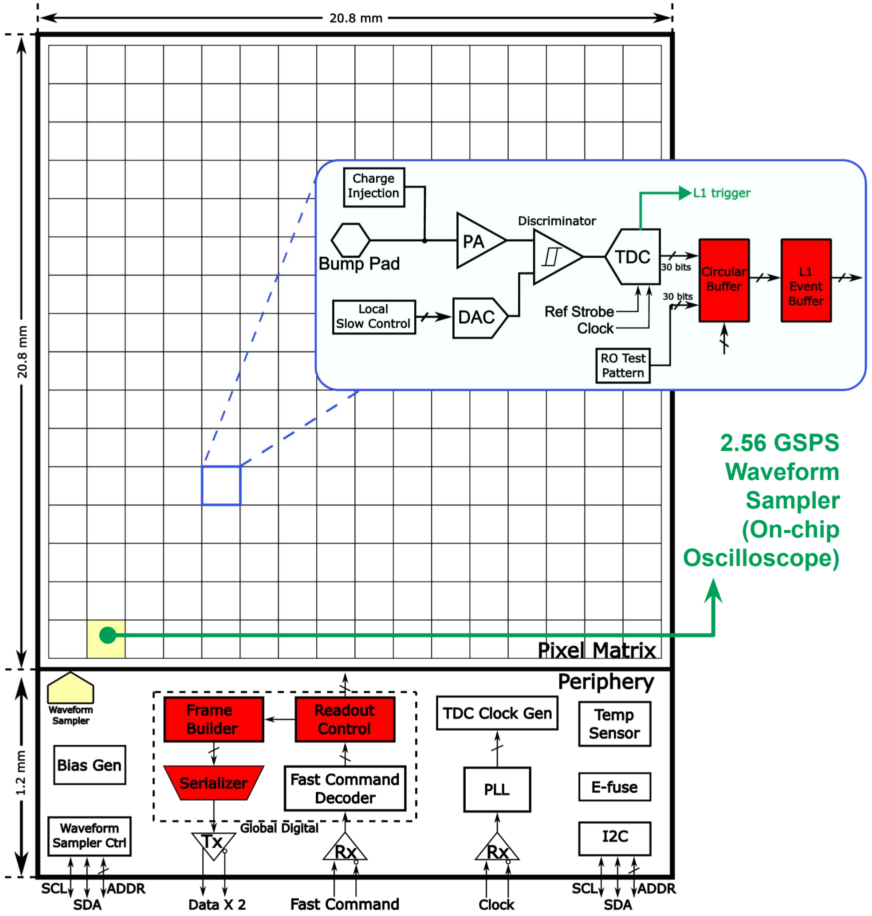
CMS Endcap Timing Layer

2 hits per track, 50ps res. per hit, 35ps res. per track

What are the main constraints on this design?

1. Low Noise
   - This is crucial! 30ps intrinsic (Landau) resolution from LGADs means **ASIC noise contribution < 40ps**
2. Low Power
   - Thou shall not fry your detector! Cooling capacity limits power consumption to **< 1W per chip, 4mW per pixel, 240mW/cm^2**
3. Radiation Hardness
   - Must withstand 100MRad over the 3000fb^{-1} of HL-LHC
4. Sensitive to small LGAD signals
   - Around 10fC per MIP towards end of lifetime of LGADs in ETL
5. Synchronized precision timing over ~33k chips, ~8.5M channels...

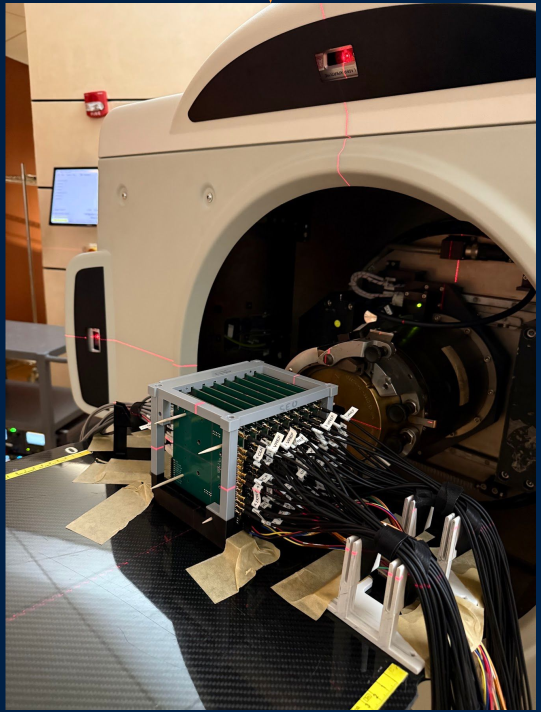
ETL Read Out Chip (ETROC)

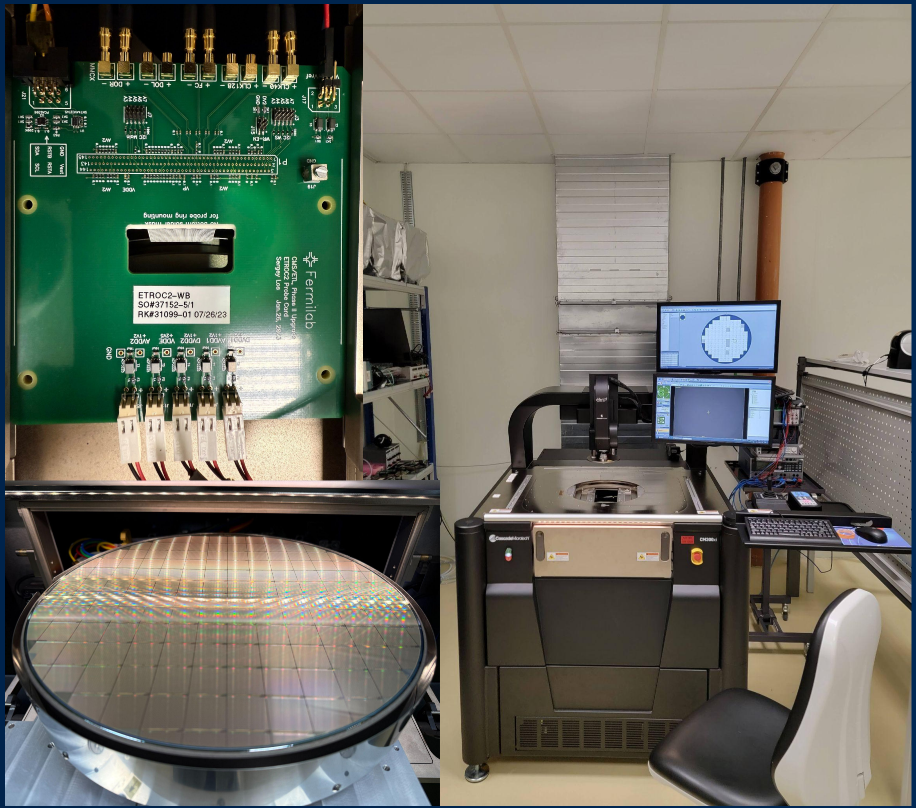


ETROC2 Heterogeneous Testing Campaign

Test beams and live DAQ with real particles or laser pulses

Simulated DAQ under TID / SEU testing conditions





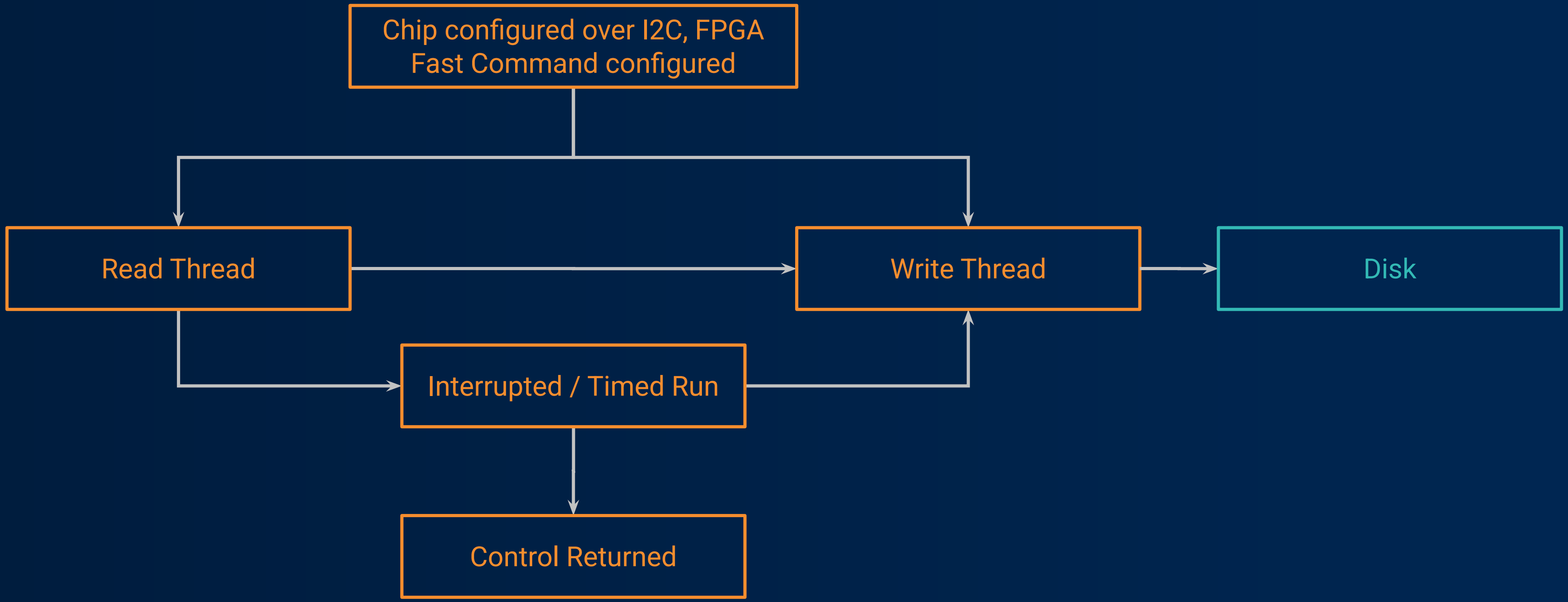
Basic config and simulated DAQ during wafer probe testing

ETROC1 to ETROC2

Simple DAQ Schema

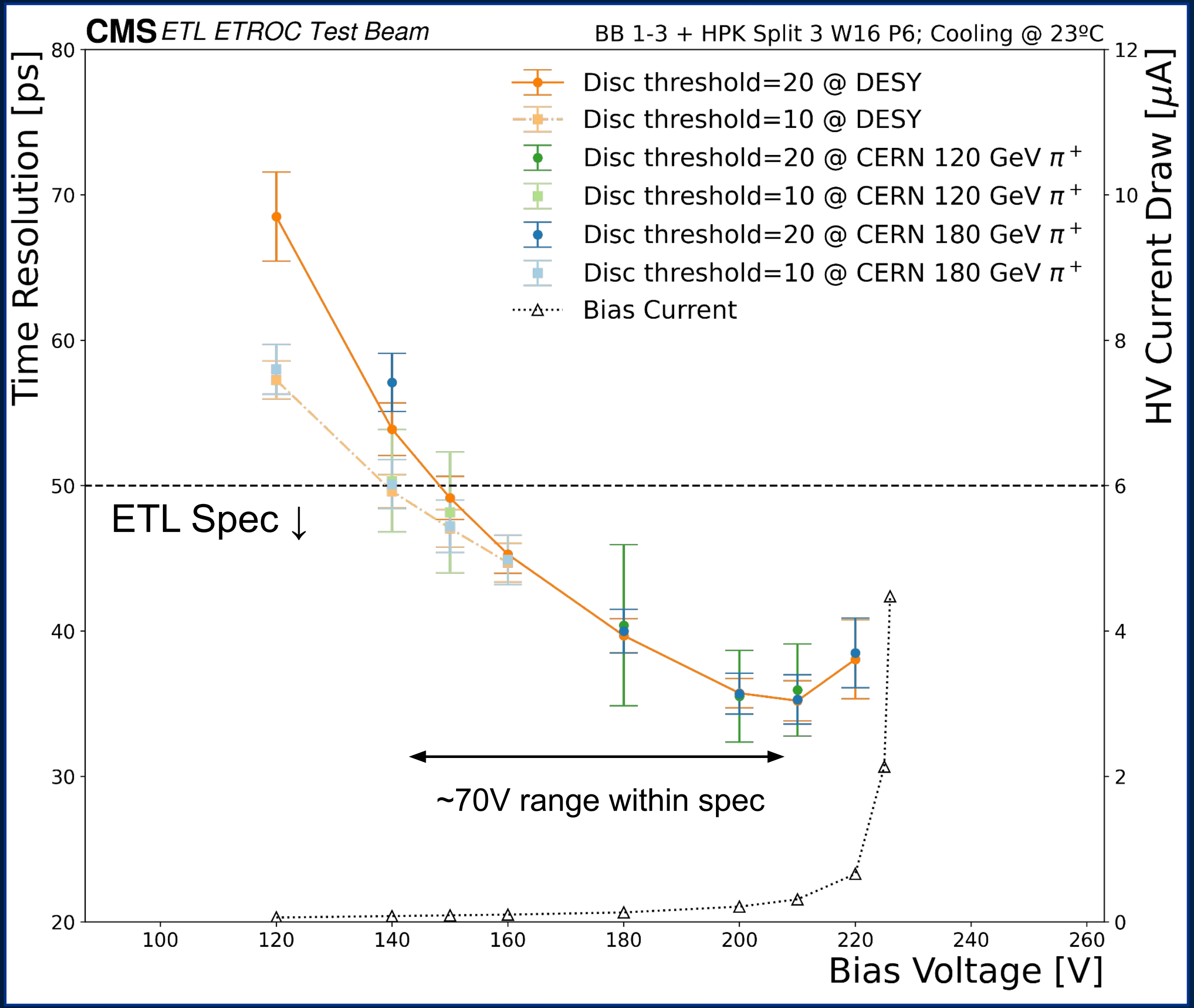
No State Machines for DAQ

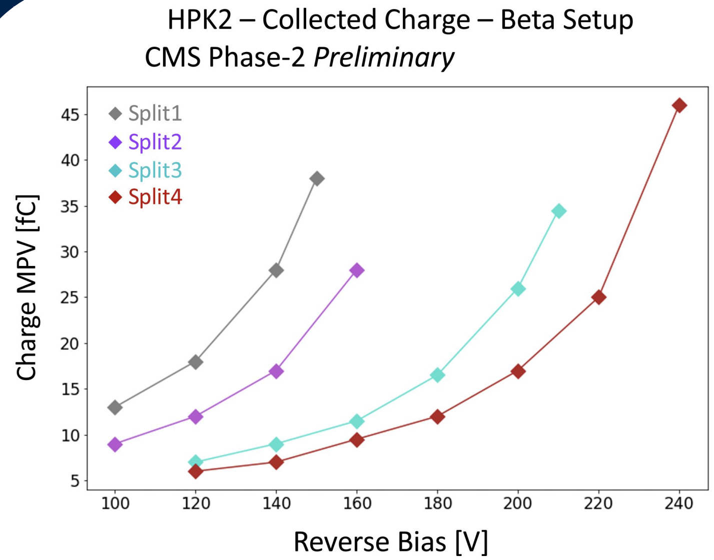
Entirely Sequential DAQ stack



ETROC2 testing with simple DAQ

Limited DAQ flexibility, good for a lot of early results



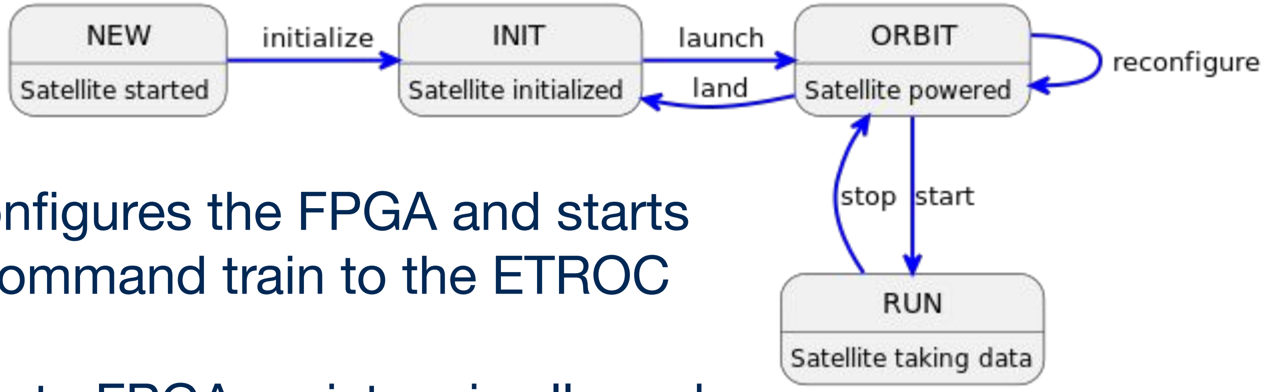


Sensor under consideration here is HPK2 **Split 3**

Successfully reproduced ~35ps res. *with this board. Results from CERN 120-180 GeV π^+ agree with those from DESY 4 GeV e^- beam*

ETROC2 with Constellation

Flexible DAQ!



The ORBIT state allows us to monitor the state of the chips, check DAQ without reading/writing any data

Launch configures the FPGA and starts the Fast Command train to the ETROC Chips

Read/Write to FPGA registers is allowed

All I2C / Slow Control Config is currently done separately.

This can be folded into the Launch transition in the future

The RUN State is simple for the (Sender) Satellite that talks to the FPGA, the Receiver can perform Online translation upon request.

Constellation networking infrastructure has been seamless!

2.56 GSps Waveform Sampler

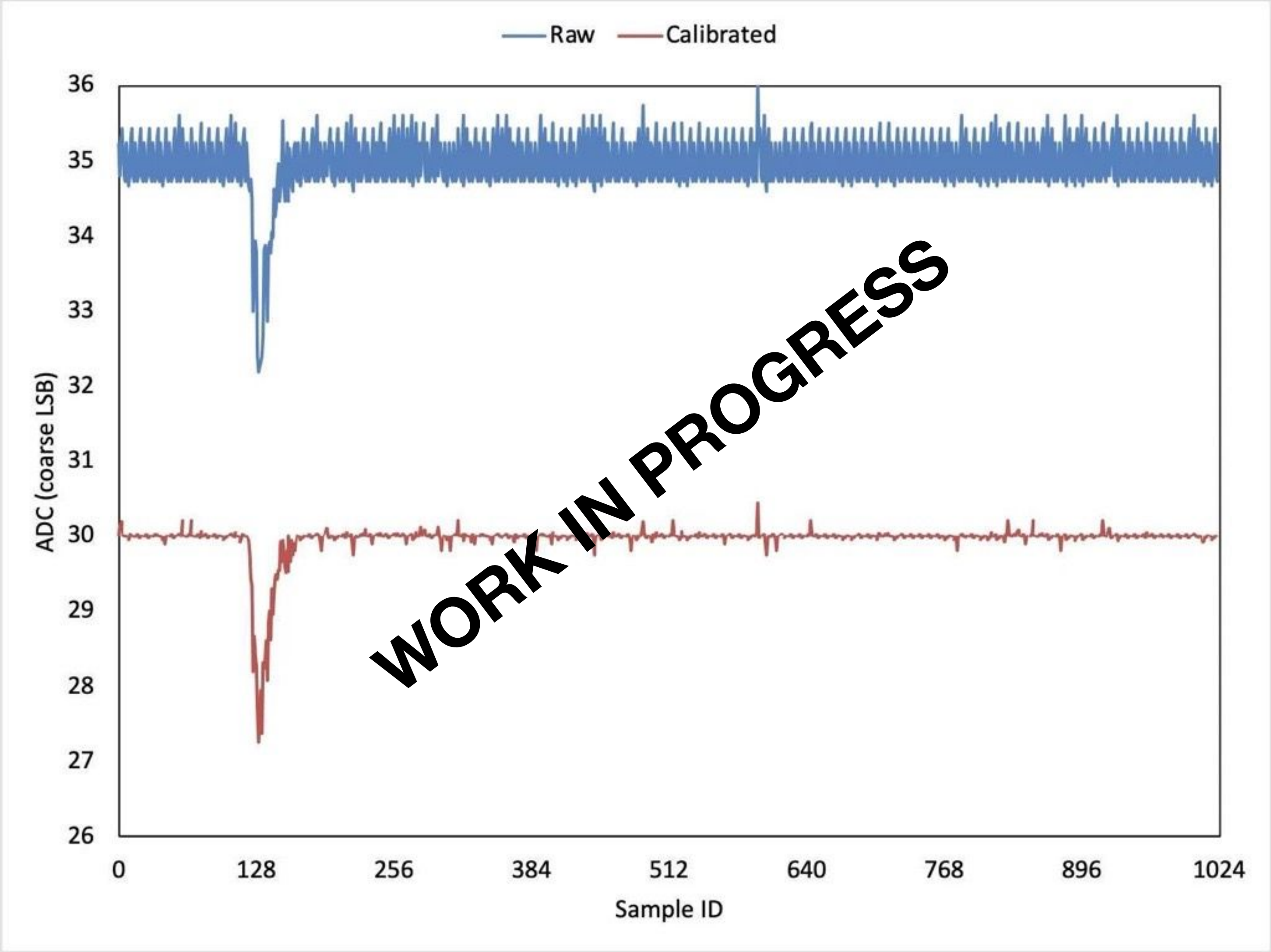
Utilizing multiple Satellites talking to the same Chip / FPGA

The chip must be configured via I2C, but the Fast Command to the chip (WS Stop / Start) requires FPGA config and Run Start - Stop logic.

Waveform Sampler can only be read out via I2C / Slow Control

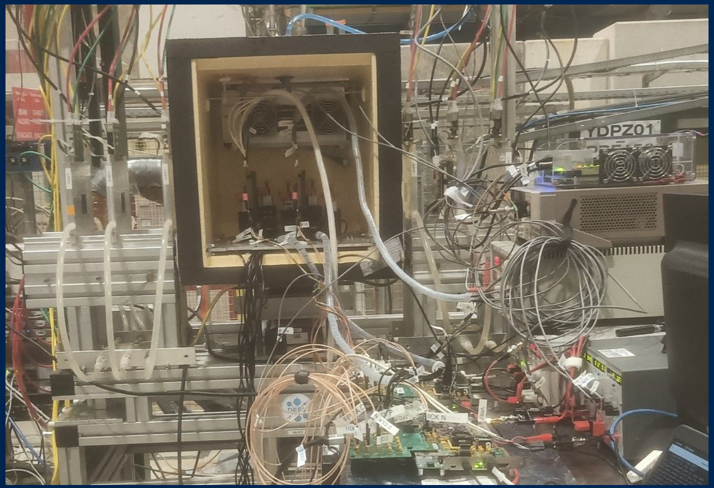
Custom WS Satellite needed for FC and I2C WS Reading.

Reading the TDC data also requires the usual DAQ over ethernet.



AIDA Integration

Testing full stack, AIDA + CROC + **2 ETROC Setups**



One ETROC was used as input for the TLU to create the trigger for the whole system (in yellow, AIDA telescope + 2 ETROC planes + 1 CROC plane).

The two signals (green and pink) are the copies of the trigger sent from the TLU to all the systems, in particular to each ETROC2 plane

Summary

- ETROC2 Testing campaign is fairly heterogeneous and requires some flexibility on the DAQ
  - Beam DAQ
  - QInj based testing (TID/SEU)
  - System DAQ monitoring without read/write during wafer testing
  - Waveform Sampler operation using FC and Slow Control

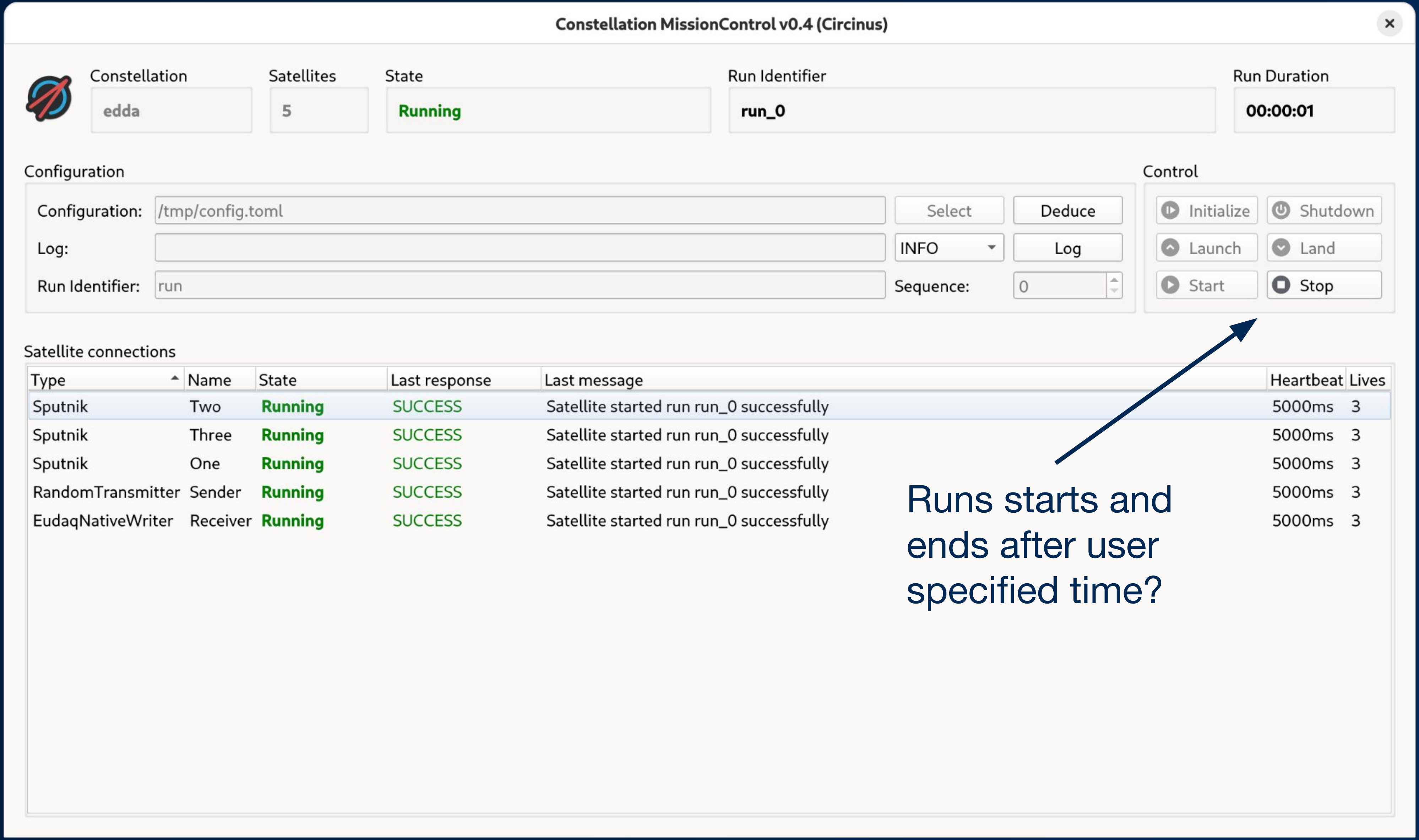
- Transition from older DAQ infrastructure to Constellation was relatively straight forward!

- New DAQ Stack has already been deployed successfully since the start of this year
  a. Data taking efficiency has improved in DESY and CERN beam tests when compared with earlier campaigns
  b. TID / SEU / Wafer / WS Testing success

- AIDA Integration testing underway
  a. In Collaboration with IFCA
  b. Done with EUDAQ/EUDET atm

- Several improvements being explored
  a. VTemp monitoring Satellite
  b. Trigger rate extraction in the Receiver Satellite

Maybe Timed Runs?



Runs starts and ends after user specified time?

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