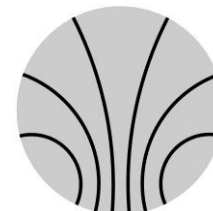


Heidelberg plans for AHCAL

Konrad BriggI
DESY Marzipan meeting 12/2024



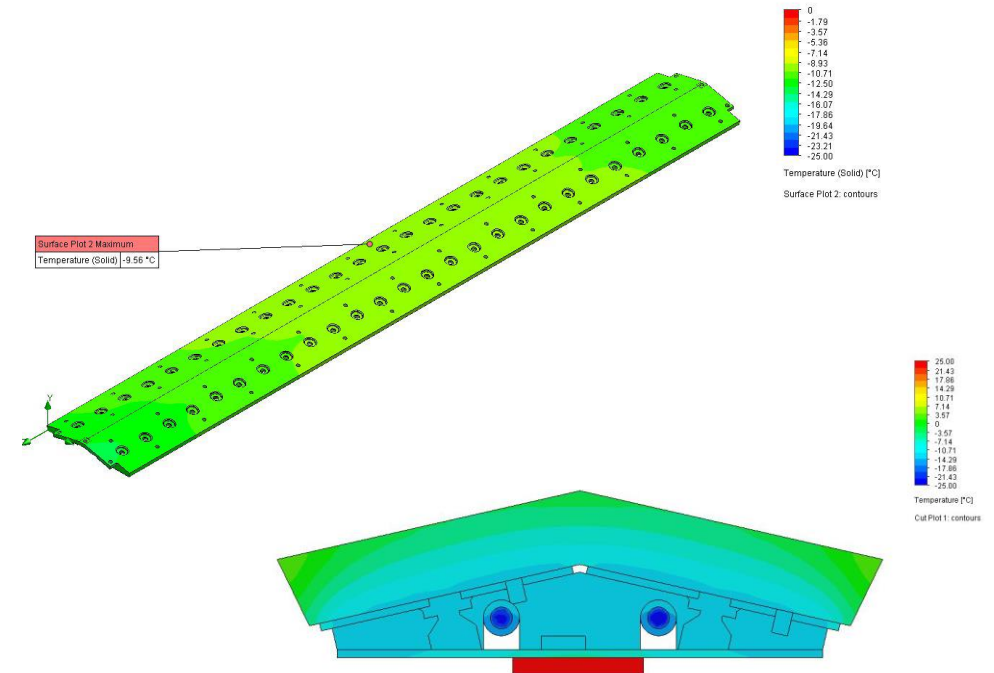
UNIVERSITÄT
HEIDELBERG
ZUKUNFT
SEIT 1386



With funding from
 Bundesministerium
für Bildung
und Forschung

AHCAL Cooling – in collaboration with JGU

- Current cooling system for AHCAL
 - Only cooling of Power board
 - Does not allow for continuous running (... with larger slabs)
- Study of Cooling solutions for next generation prototypes
 - Production of a cooling mock-up
 - Commissioning of a AHCAL cooling system
 - small stacks ; long slab
 - Fluid and Thermal Simulation
 - Verification of simulation results
- Simulation frameworks
 - Licences for Fluid and Thermal simulations in Solidworks CAD available
 - Experience in setup and verification of Simulation ; Commissioning and integration of such a system (Mu3e Tile detector).



Simulation of Mu3e Tile detector Cooling system

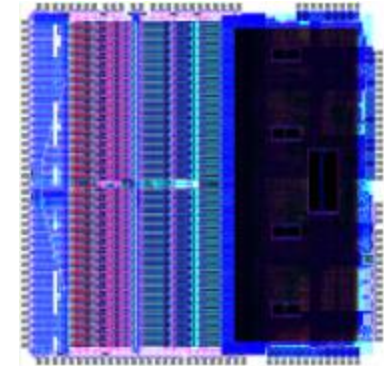
First discussions with JGU have already started

KLauS ASIC Developments - Status

- SiPM readout solution developed for AHCAL and ScECAL
Main target $O(1\text{mm}^2)$; low gain SiPMs (10um pixel and above tested)
- UMC 180nm mixed-mode CMOS technology
- Low power, Power pulsing capable ($\sim 25\mu\text{W}$ @ 0.5% duty cycle)
- Current version KLauS6b with 36 channels
 - Analog front-end + ADC + TDC + Digital circuits
 - Capable of running in continuous readout mode
 - I²C (Slow) or LVDS (160Mbit/s) readout
- KLauS5 was Integrated and successfully run in a HBU
- Timing performance of KLauS6b studied in dedicated testbeam

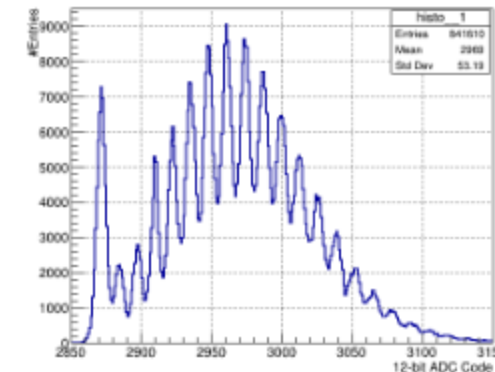


KLauS5 (BGA Packaged) on a HBU

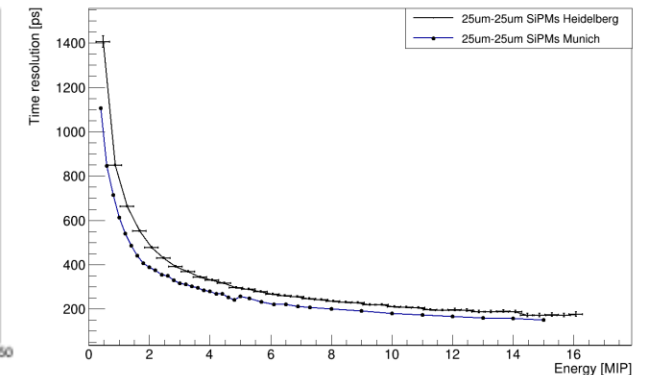


KLauS6 Layout (5x5 mm²)

SPS spectrum of 10um pixel MPPC



KLauS Timing performance



KLauS ASIC Developments - Plans

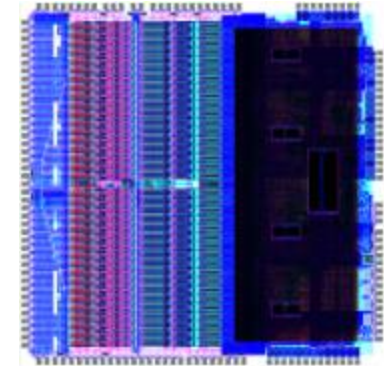
- KLauS is already capable of continuous running
 - Minor changes on analog parts foreseen
- I2C interface too slow to handle high rates with many ASICs
- Increase speed and efficiency of LVDS link
 - More efficient protocol (Hit sizes, Frames)
 - 1.25Gbit transceivers available on the Sister-Chip MuTriG for the Mu3e experiment
- Reduce IO lines to improve integration on HBU
 - Configuration interface
 - External trigger / test lines & Reset -> Fast command link
- New Package & Pad layout for packaging
 - A QFN socket was produced, will be tested with existing KLauS6

A PhD student (Willy Chang) will start end of this week

... discussions on Interfaces, Pinout and additional specs should start early 2025

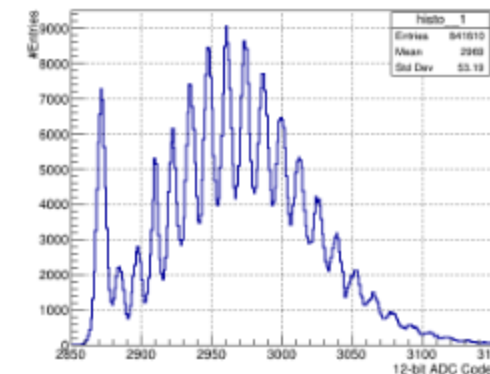


KLauS5 (BGA Packaged) on a HBU

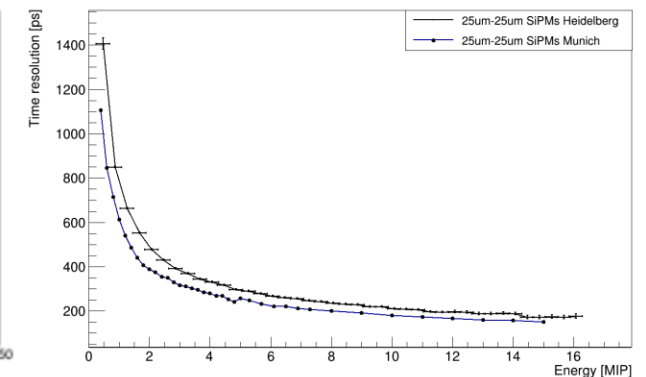


KLauS6 Layout (5x5 mm²)

SPS spectrum of 10um pixel MPPC



KLauS Timing performance



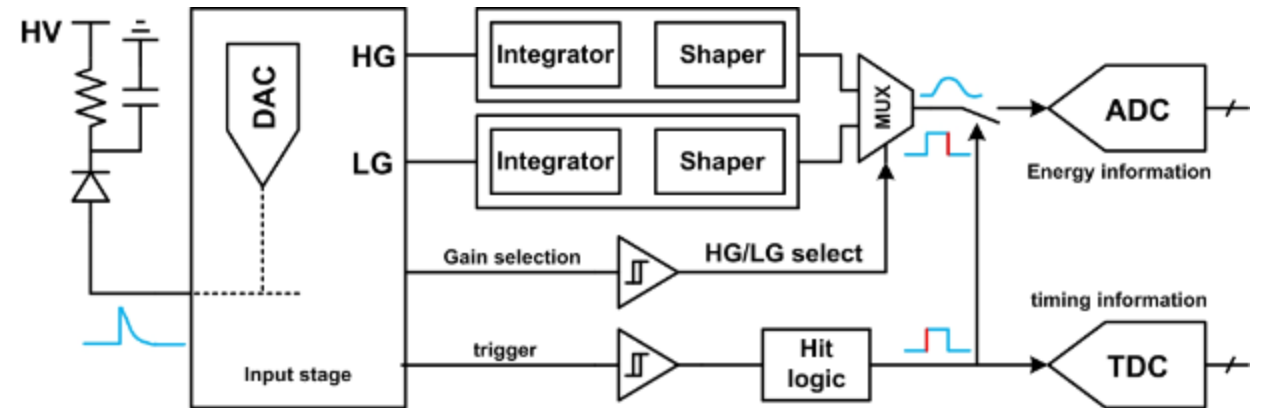
Summary

- **Work on AHCAL cooling**
 - Simulation ; dresign and verification
 - Manufacturing of Test systems and Prototypes (until Q4 2026)
- **KLAuS ASIC**
 - Prepare KLAuS6 asic for HBU
until Q4 2025
 - validate existing DAQ; participate in Test beams
 - Update and extension of design optimized for continous running (KLAuS6c)
 - **Submission planned for Q1/2026**

Backup slides

KLauS ASIC - Channel

- Input stage
Buffer & distribute signal current, SiPM bias voltage tuning ($\sim 2\text{V}$ range)
- 2 integration branches with automatic gain selection
Different charge range (HG, LG) ; Scaling configuration bits for signal range
- 2 comparators blocks
Timestamp & ADC start, charge range selection (auto-gain)
- Integrated ADC per channel
 - 10-bit mode – SiPM spectra for $25\mu\text{m}$ pixels and above; MIP quantization
 - 12-bit ADC – Single pixel spectra for small gain SiPMs (pipelined 8b SAR stage)
- TDC for time stamp recording
- Since KLauS6: $\sim 195\text{ps}$ bins , $\sim 3.3\text{ms}$ dynamic range (@nominal 40MHz clock input)



KLauS ASIC – Charge measurement

Branches and gain scale settings

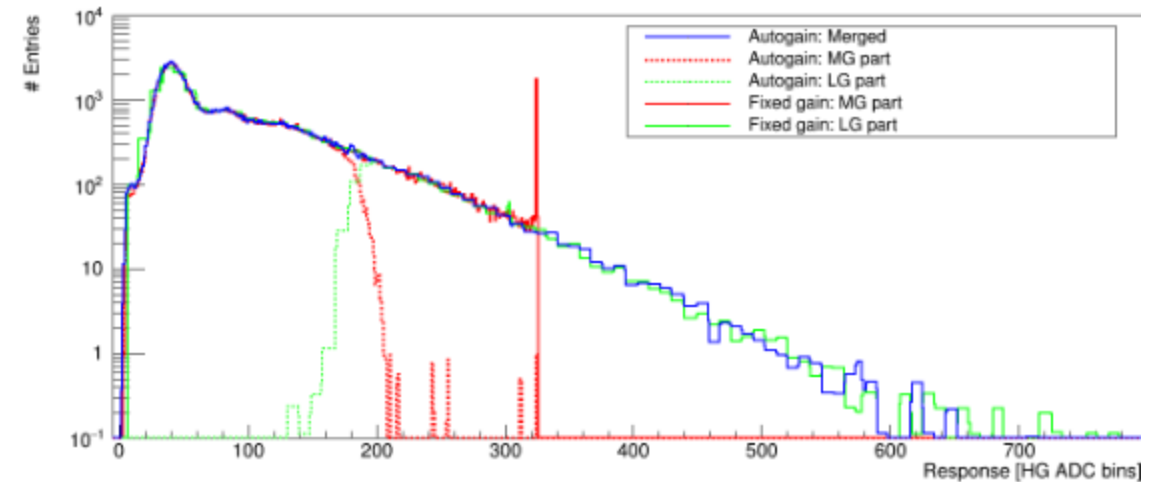
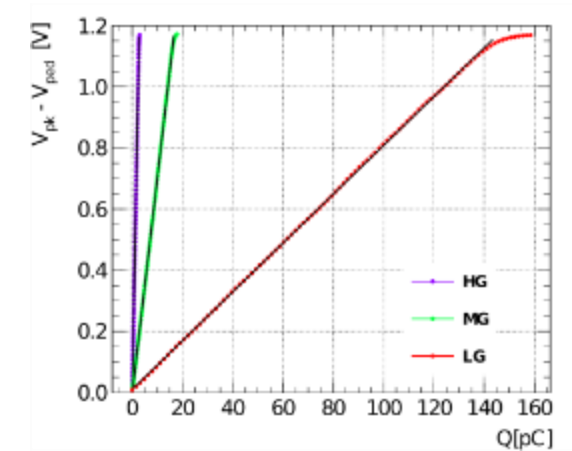
- HG branch \rightarrow 1:1(HG) or 1:7(MG)
- LG branch \rightarrow 1:48 & Scaling option for 3x3mm²

Dynamic range at 1% Full Scale Range (Front-end)

- High Gain scale \rightarrow 2.7pC
- Medium Gain scale \rightarrow 16pC
- Low Gain branch \rightarrow 140pC

Noise in High gain branch

- ENC \sim 4.5fF for O(1mm²) SiPMs



KLauS ASIC – Hit digitization

- Conversion started after time-comparator fires
- Sample time stamp in TDC latches
- Configurable hold delay ($\sim 100\text{ns}$) to sample peak voltage
- ADC conversion, gain bit sampling
- Busy released after conversion is finished, ready for new hit
dead time $\sim 500\text{ns}$ (10b ADC mode)

