Tileboard QC

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AHCAL

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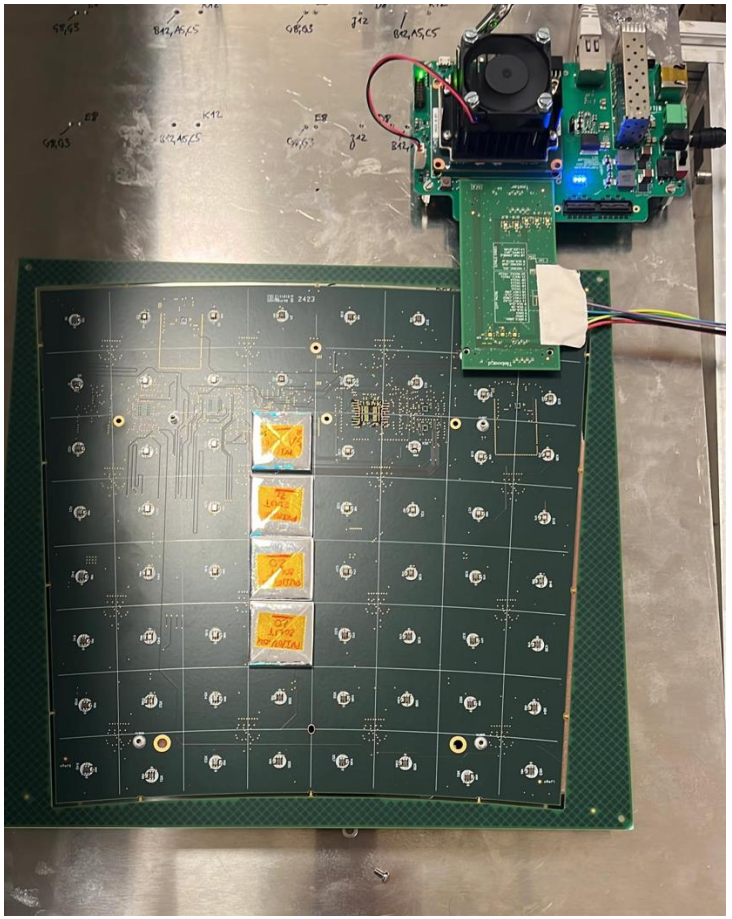
DESY.

Introduction

- Summer student at DESY 2023.
- Worked on SPS measurements with the group
- Now I am a PhD student working with the same group
- My first task is the Tileboard QC procedure

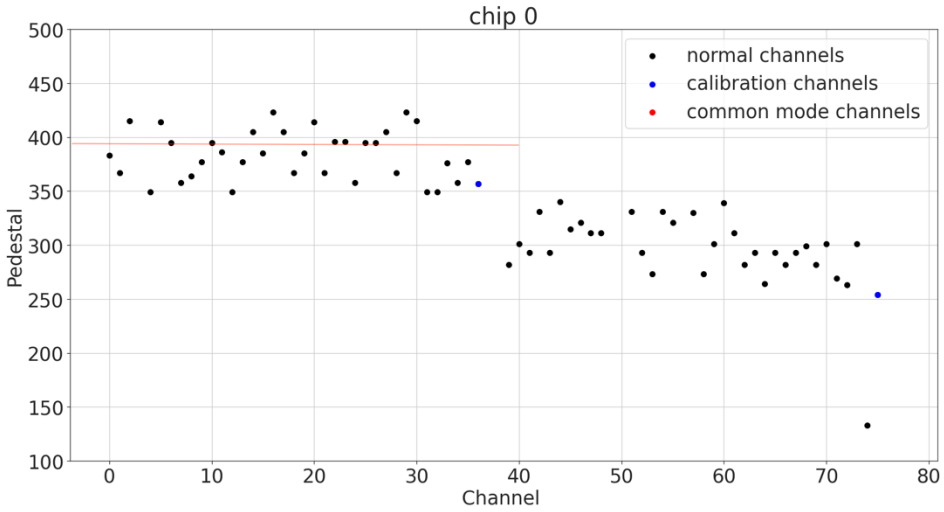
Tileboard QC procedure

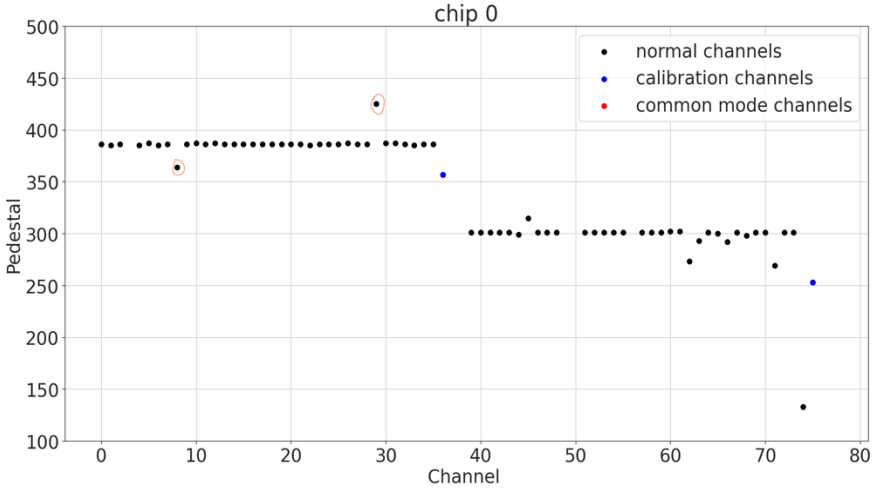
- We will be moving into the production phase with production boards (~2000 boards at DESY)
- Need a robust QC procedure
- Certify the board as well as the HGCROCs (1 or 2 on each board) on them
- Done by checking if we can tune various parameters

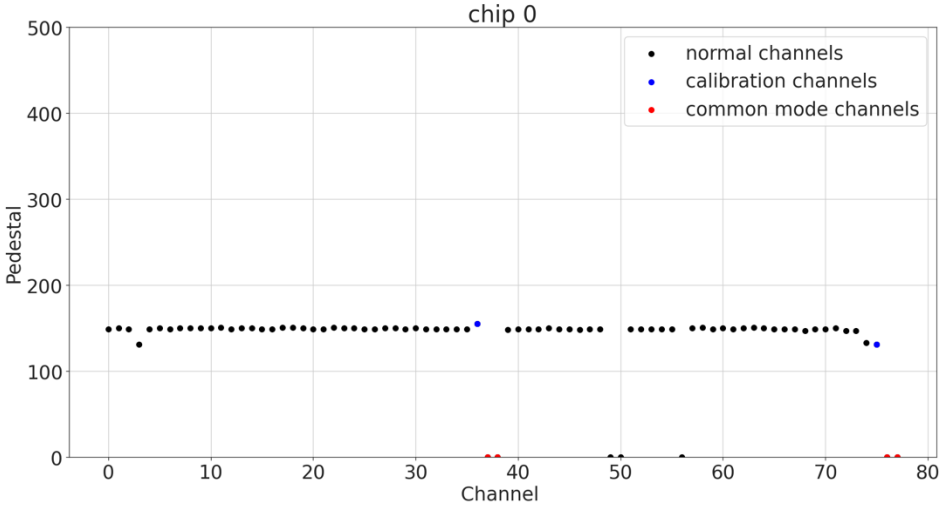


An example procedure: pedestal alignment

- Pedestal is the baseline or noise when we have no signal.
- Tune the pedestal for the channels to get an equal response to a signal.

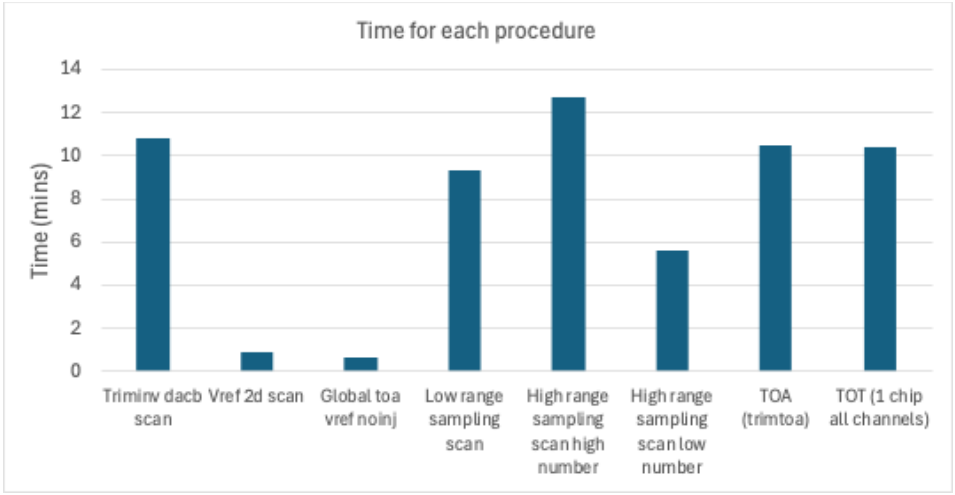


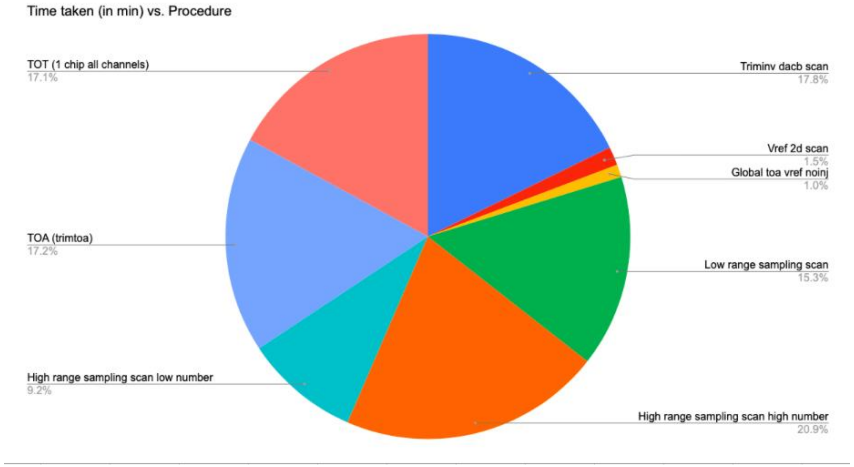




Time for execution of data taking for most steps

- We want to get the runtime for the procedure down to ~30 mins
- These are for boards that have 1 chip, not yet done for 2 chip boards





Remarks and conclusions

- There are ~10 procedures for the full QC
- We also want a modular design with regular checks for the procedure
- Developing a github repo with all the scripts and a sort of GUI.

Thank you