DESY beam test of CMS pixel detectors

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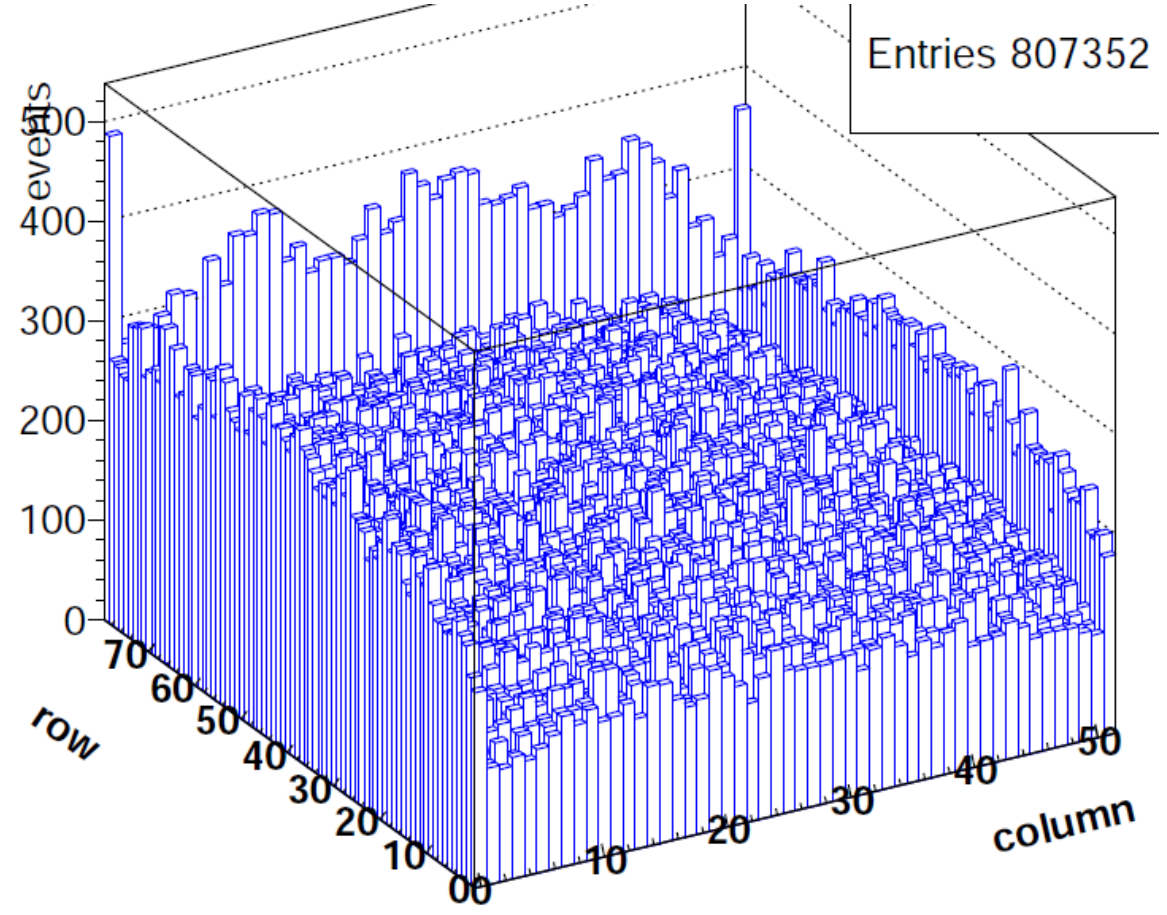
DESY CMS tracker upgrade meeting, 6.9.2011



- setup
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- summary

DESY II


http://adweb.desy.de/~testbeam/
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DESY II
(positrons)
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DESY III
(protons)
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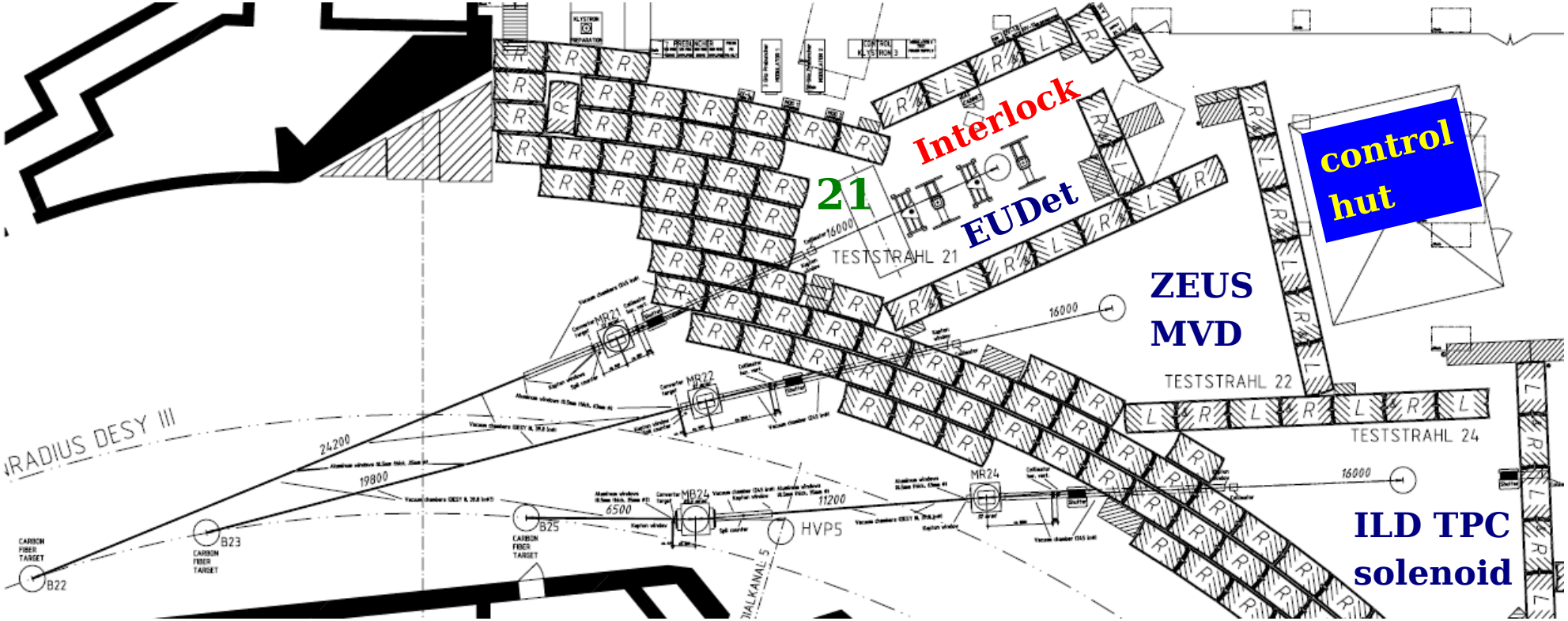
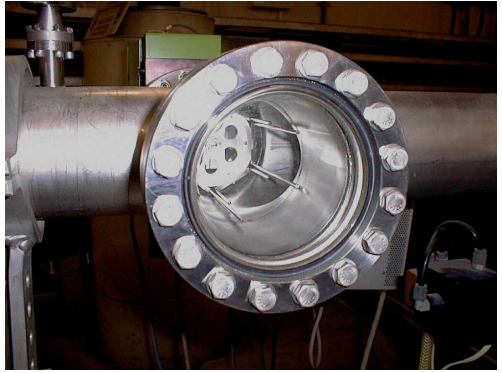
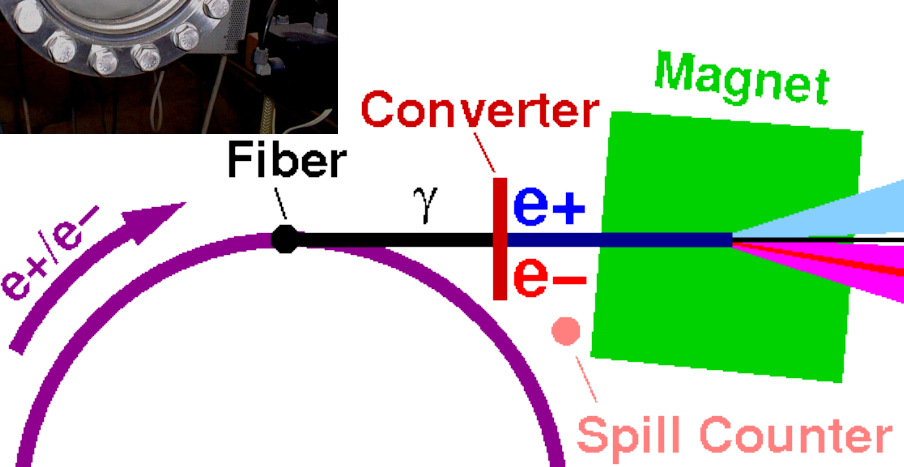
DESY II test beams

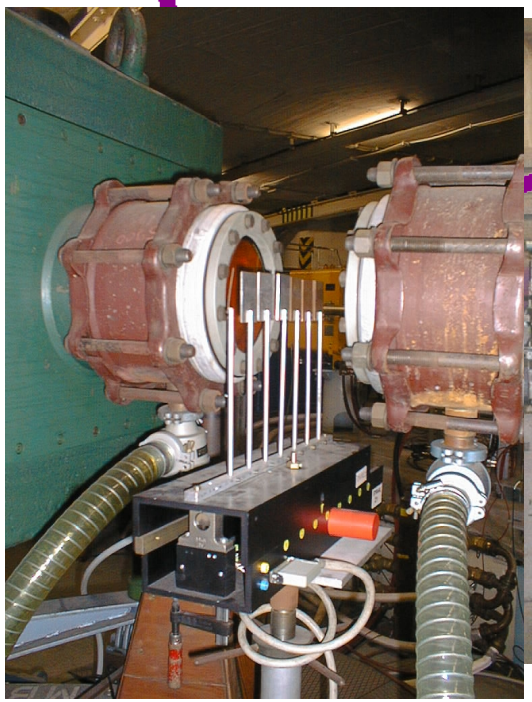


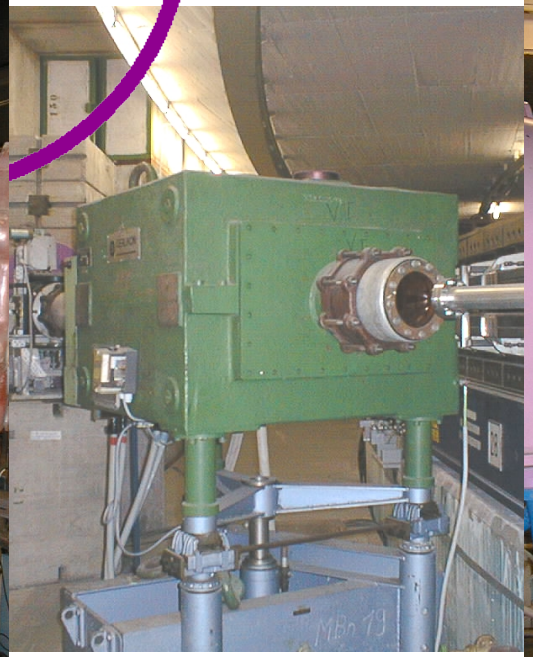
http://adweb.desy.de/~testbeam/

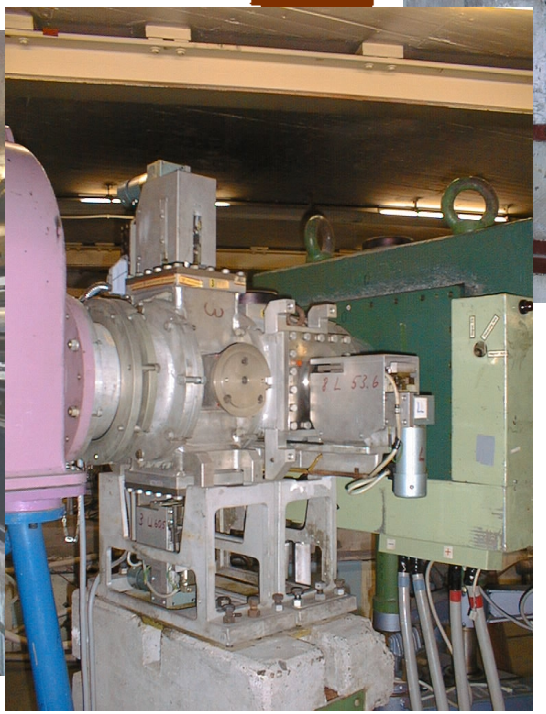
test beam extraction



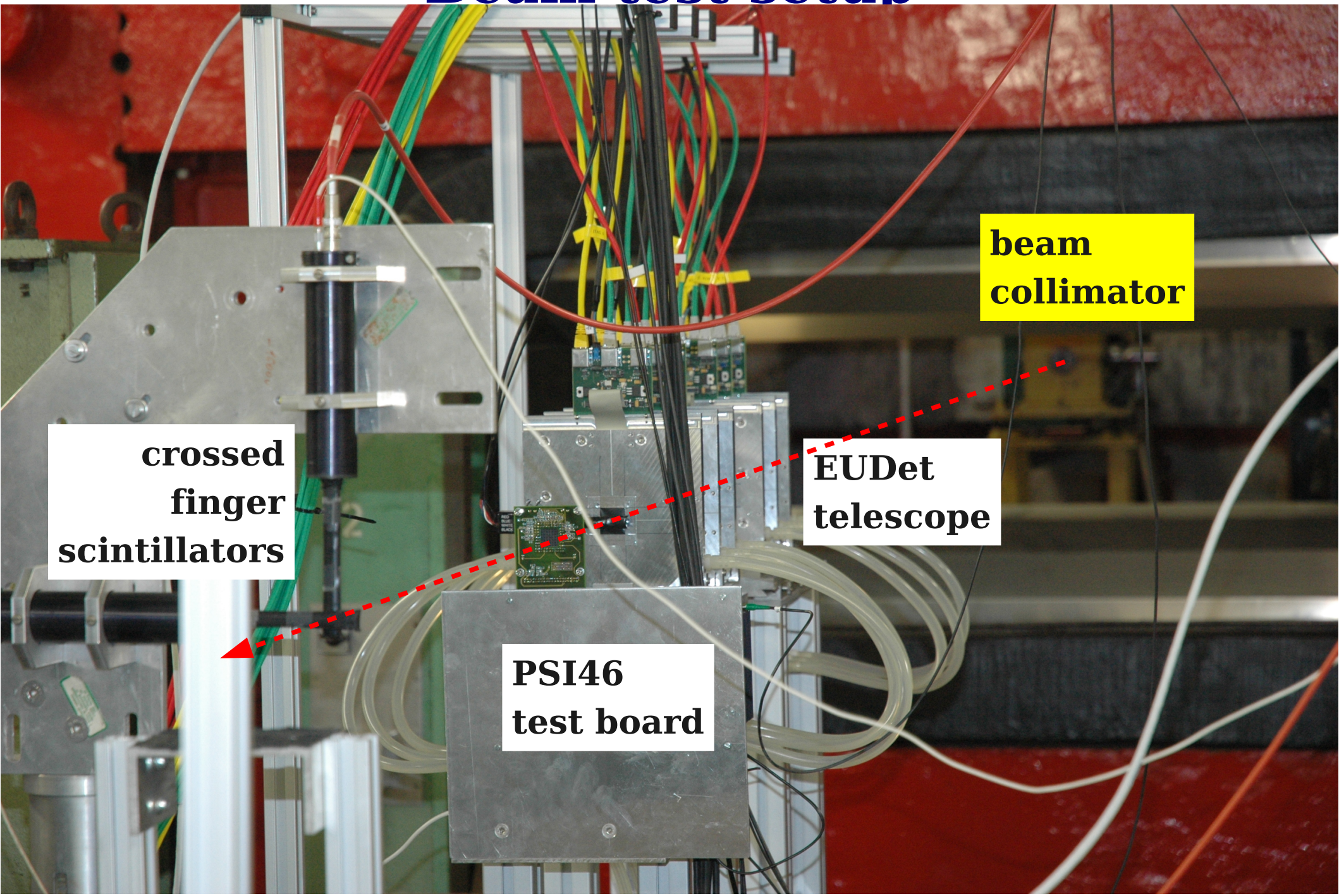




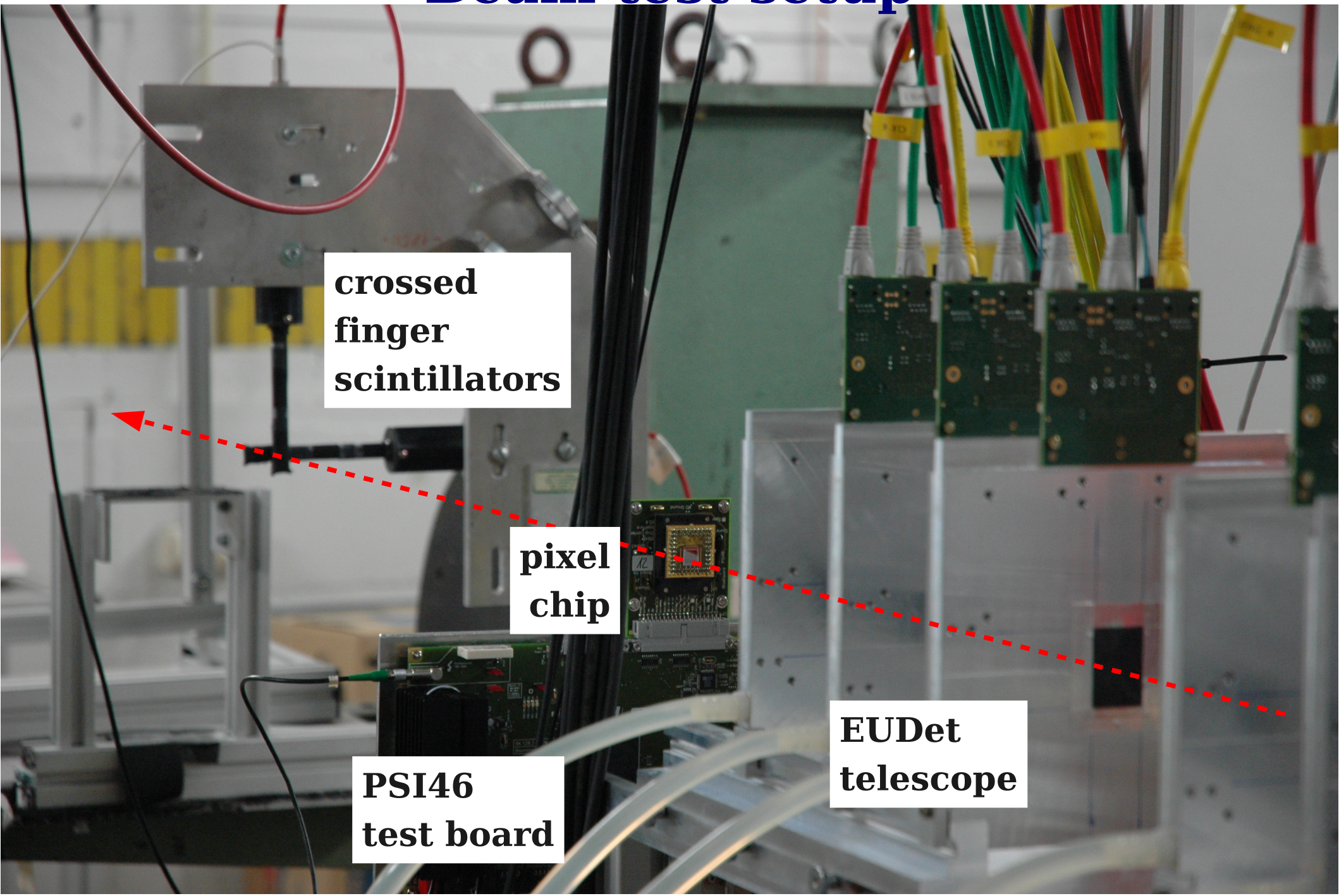




Beam test setup



Beam test setup

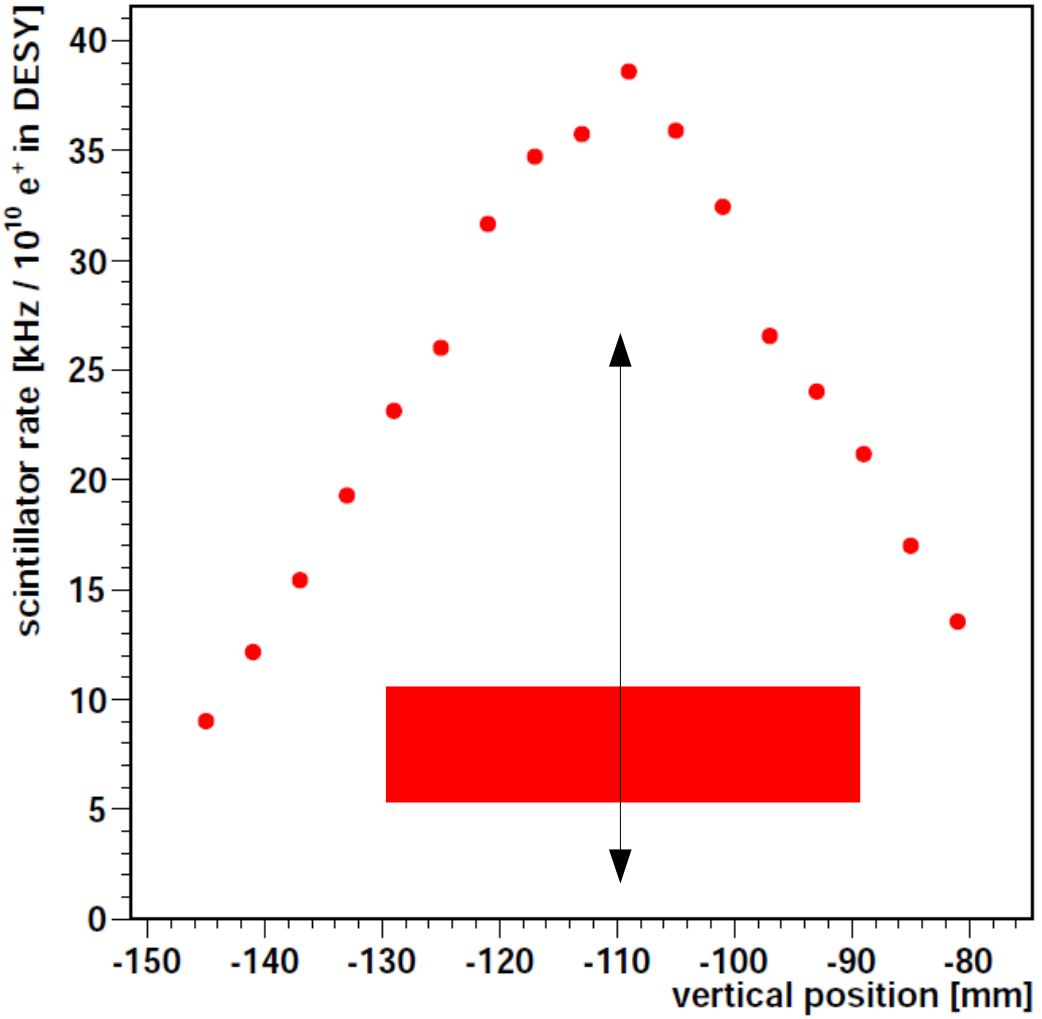


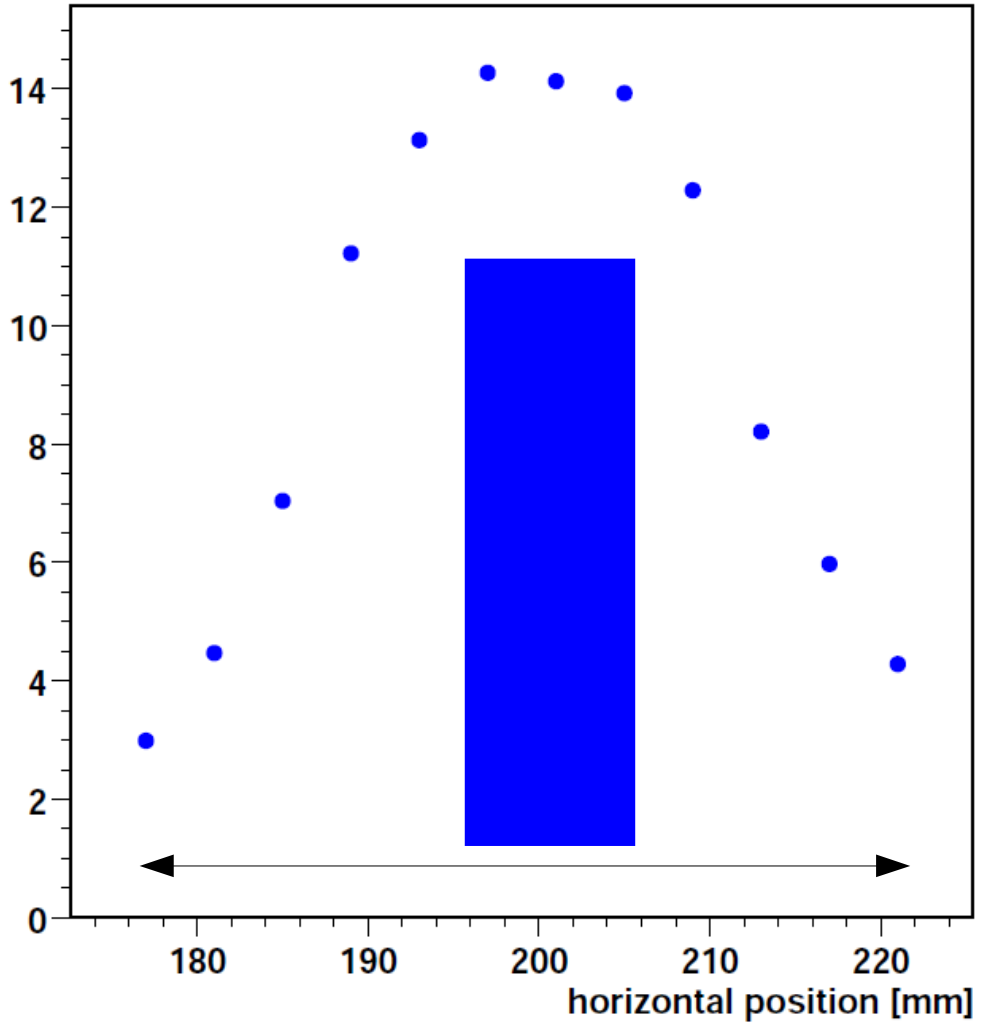
beam setup

- Crossed finger scintillators (~1 cm^2 overlap area) as trigger:
  - Mounted on movable support (x-y stage with step motors, remote)
  - CAEN HV supply (-1700 V) outside in the control hut.
  - NIM trigger logic inside interlock, and mirrored in the control hut.
  - HP trigger delay and level adapter (NIM → TTL) in control hut.
  - Up to 7 kHz scintillator coincidence rate (at 2 GeV e^+).
- PSI46 test board with single-chip sensor:
  - Mounted after EUDet telescope.
  - Keithley bias voltage supply outside in the control hut.
  - Board control and readout via USB from computer inside interlock.
  - LAN connection to a computer outside in the control hut.
- All worked well...

Scintillator position scan

Scintillators on movable support, remote control, ~0.2 mm precision

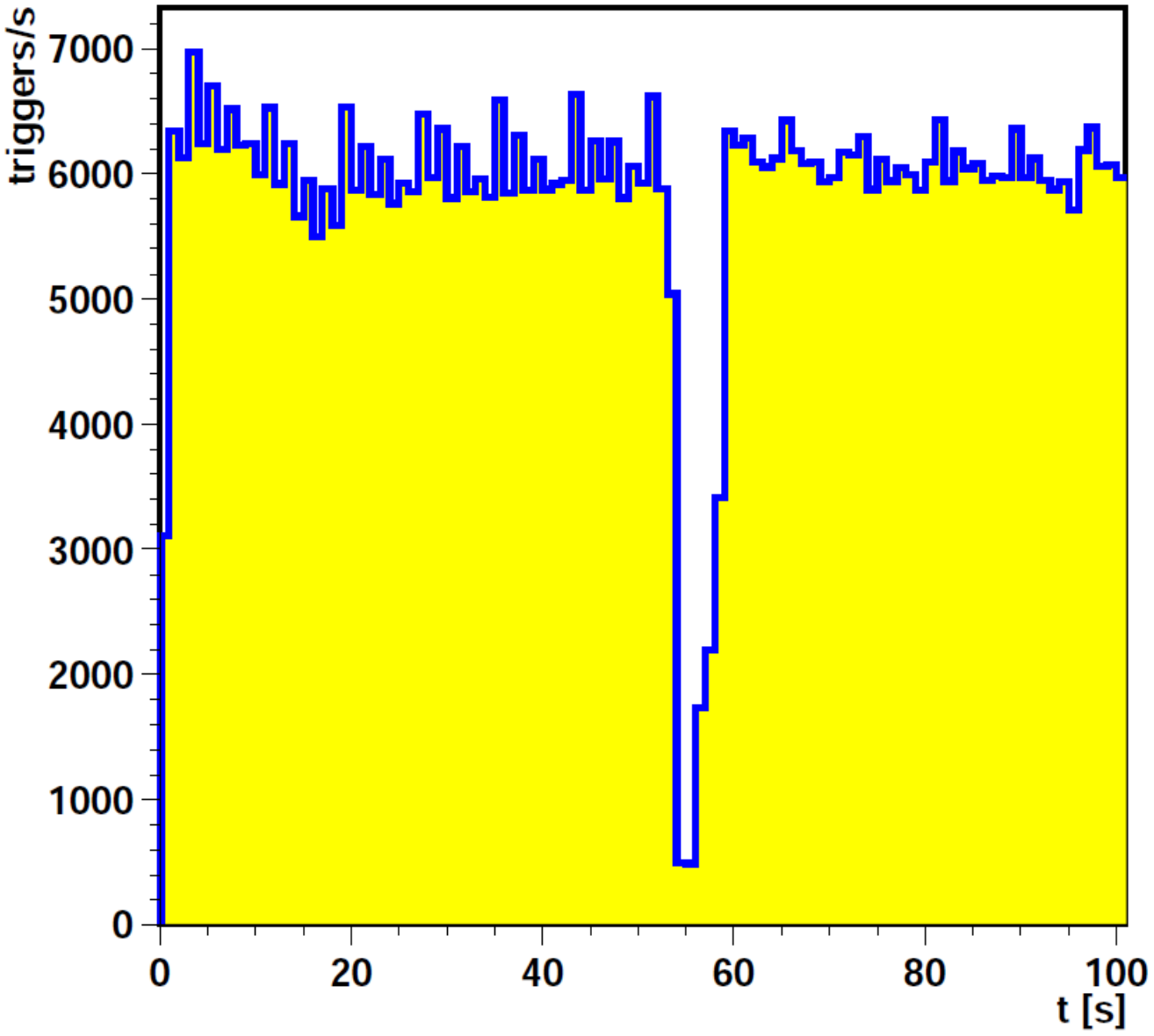




vertical FWHM ≈ 45 mm

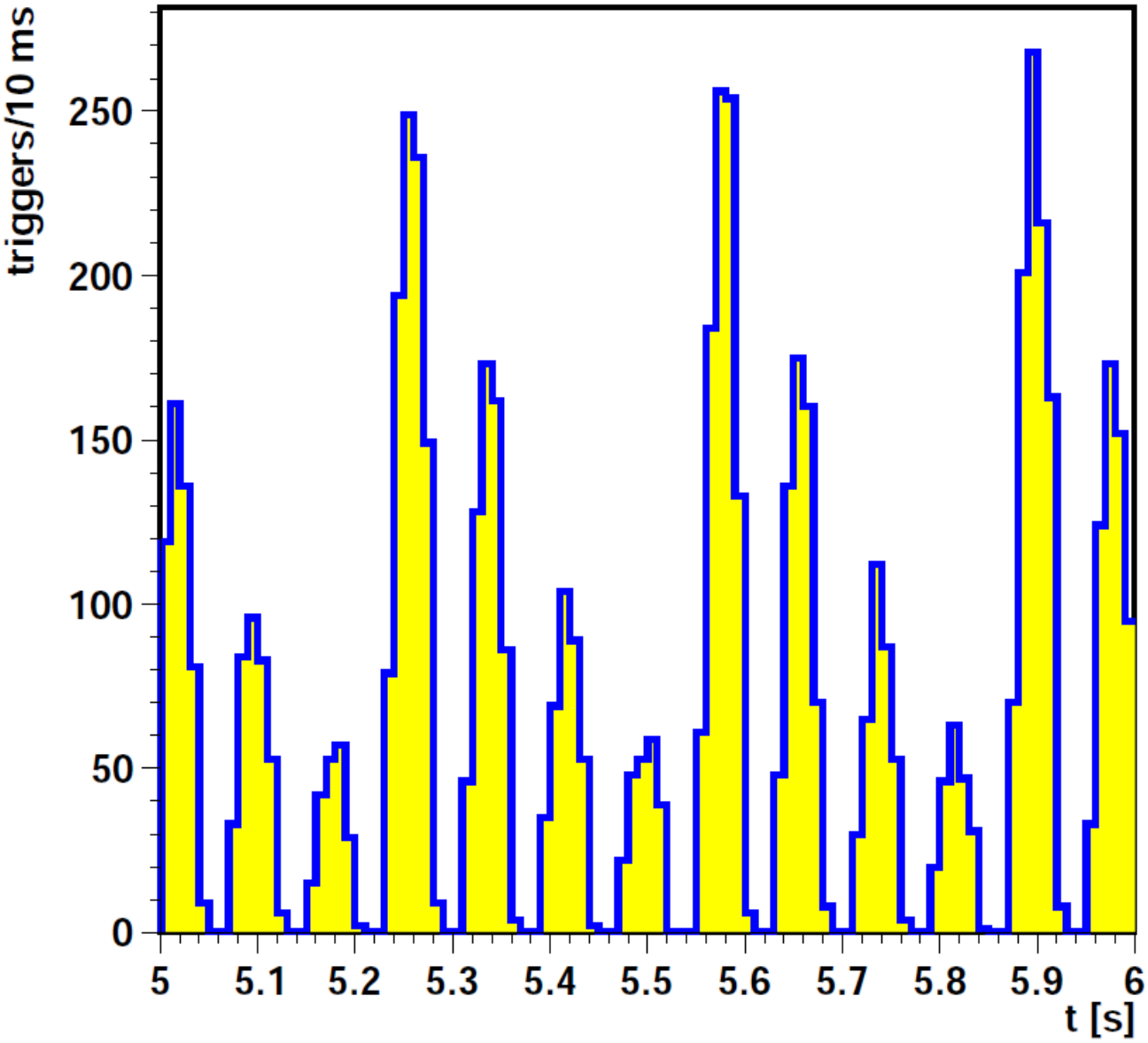
horizontal FWHM ≈ 30 mm

Data taking



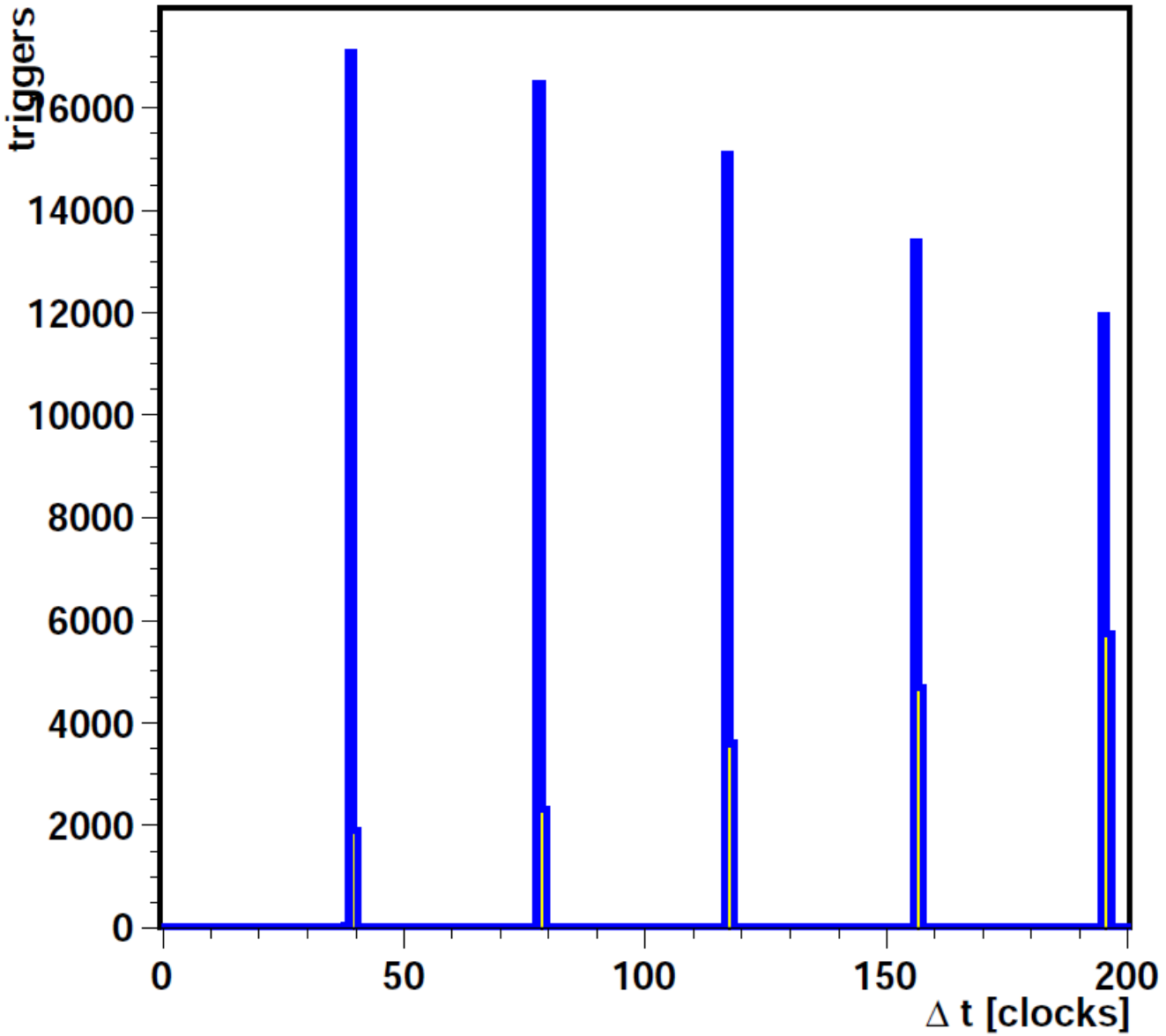
- FPGA provides a time stamp for each event by counting 40 MHz clock cycles.
- Typical scintillator coincidence trigger rate:
  - ~6.4 kHz.
- Dips:
  - DESY filling DORIS or PETRA.
- Sometimes the FPGA blocks for many seconds or gives garbage data (filtered out offline).

DESY II time structure



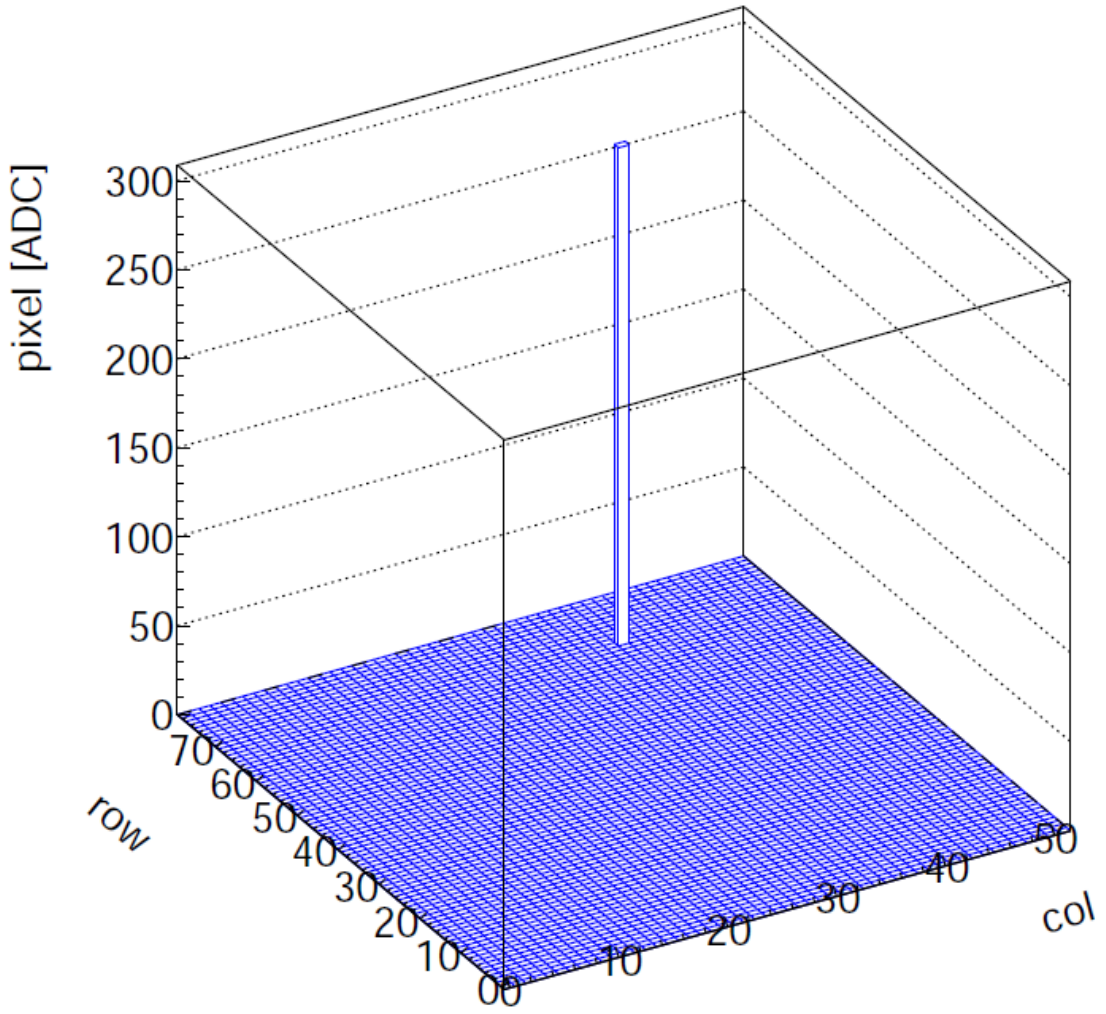
- DESY II has 80 ms cycle (12.5 Hz):
  - ramp down
  - fill one bunch from Linac II (e^-) or PIA (e^+).
  - ramp up
  - eject to DORIS or PETRA
  - or ramp down and dump
  - wire target is always in
  - test beam gets rate as long as DESY energy is above magnet setting.

one bunch in DESY II



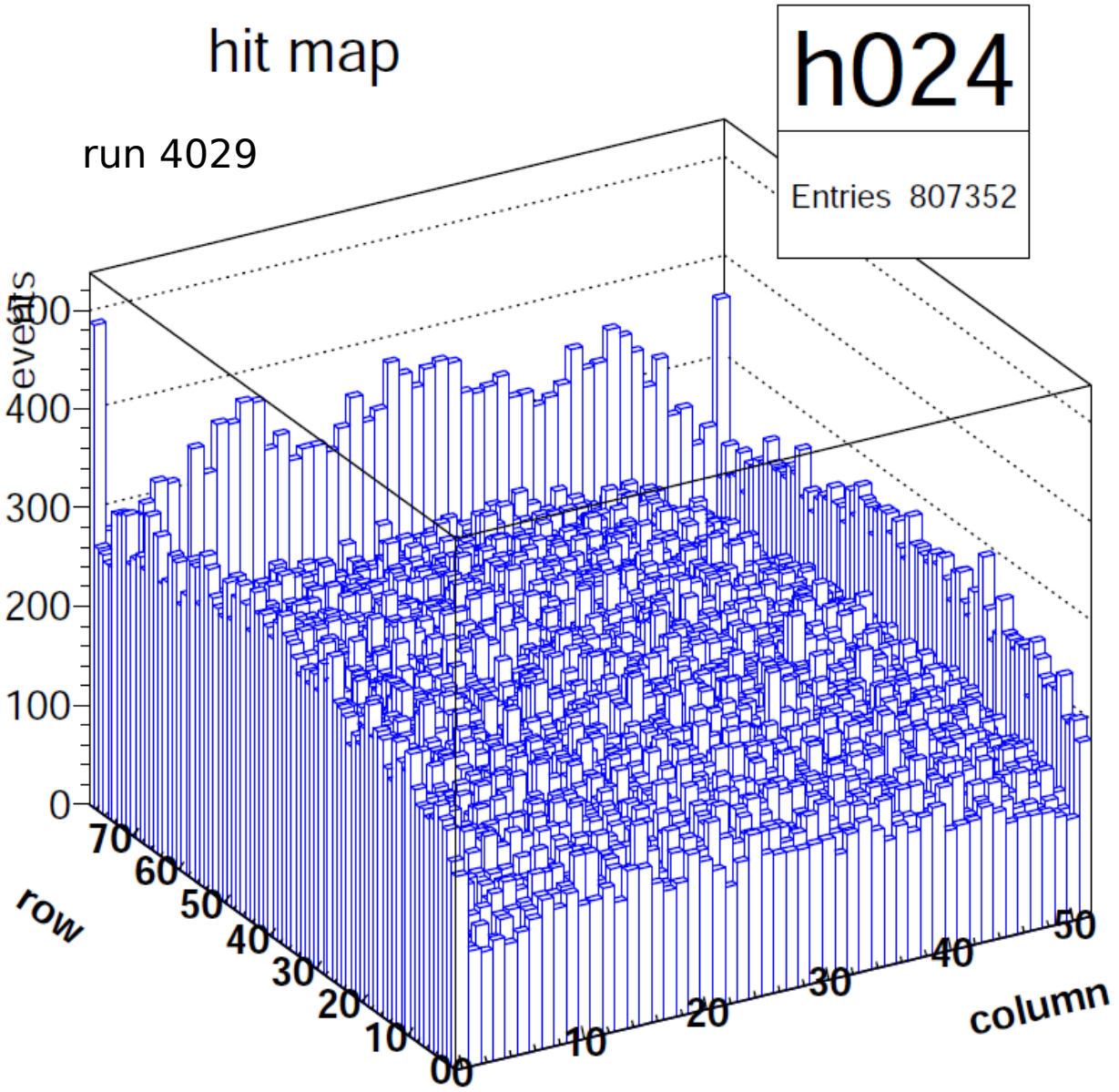
- FPGA counts 40 MHz clock cycles.
- DESY II circumference is 292.8 m
- DESY II has one bunch:
  - repeats every 0.977 µs (1.024 MHz)
  - 1 turn = 39.067 clocks.
- Problem:
  - FPGA clock was not synchronized to DESY
  - Phase of beam to clock was not fixed.

Single event display



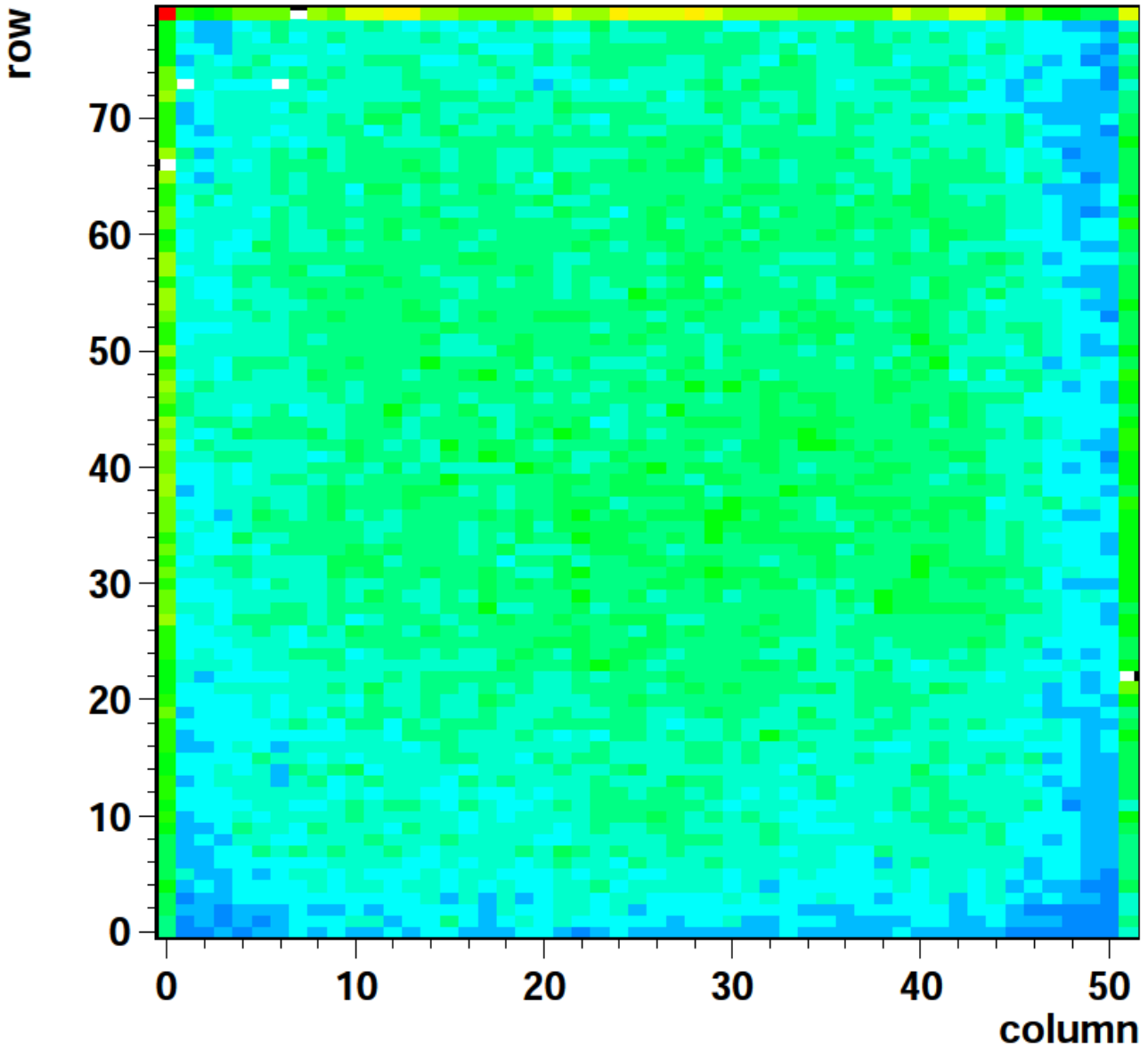
- Sample event:
  - 2 GeV tertiary e^+ beam
  - Scintillator trigger
  - Pixel chip 8
  - -90 V bias
  - optimal clock cycle

Pixel hit map



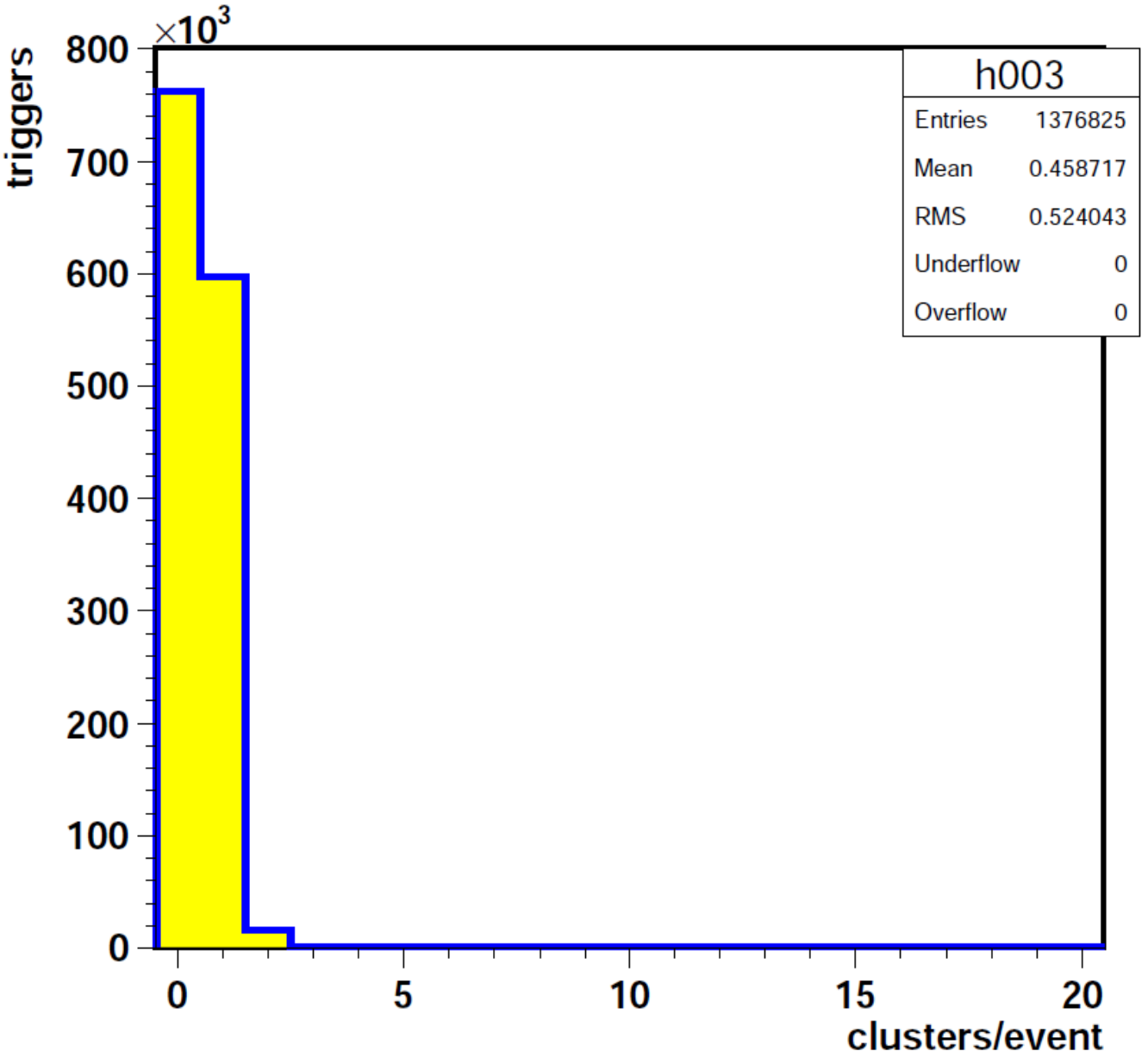
- One run, ~3.5 min
  - Fill test board memory: 60MB
  - USB transfer takes another ~2 min
- Chip 8, optimal settings
- Fully illuminated
- Border pixels have double size and rate
- Corner pixels have quadruple size and rate

Pixel hit map



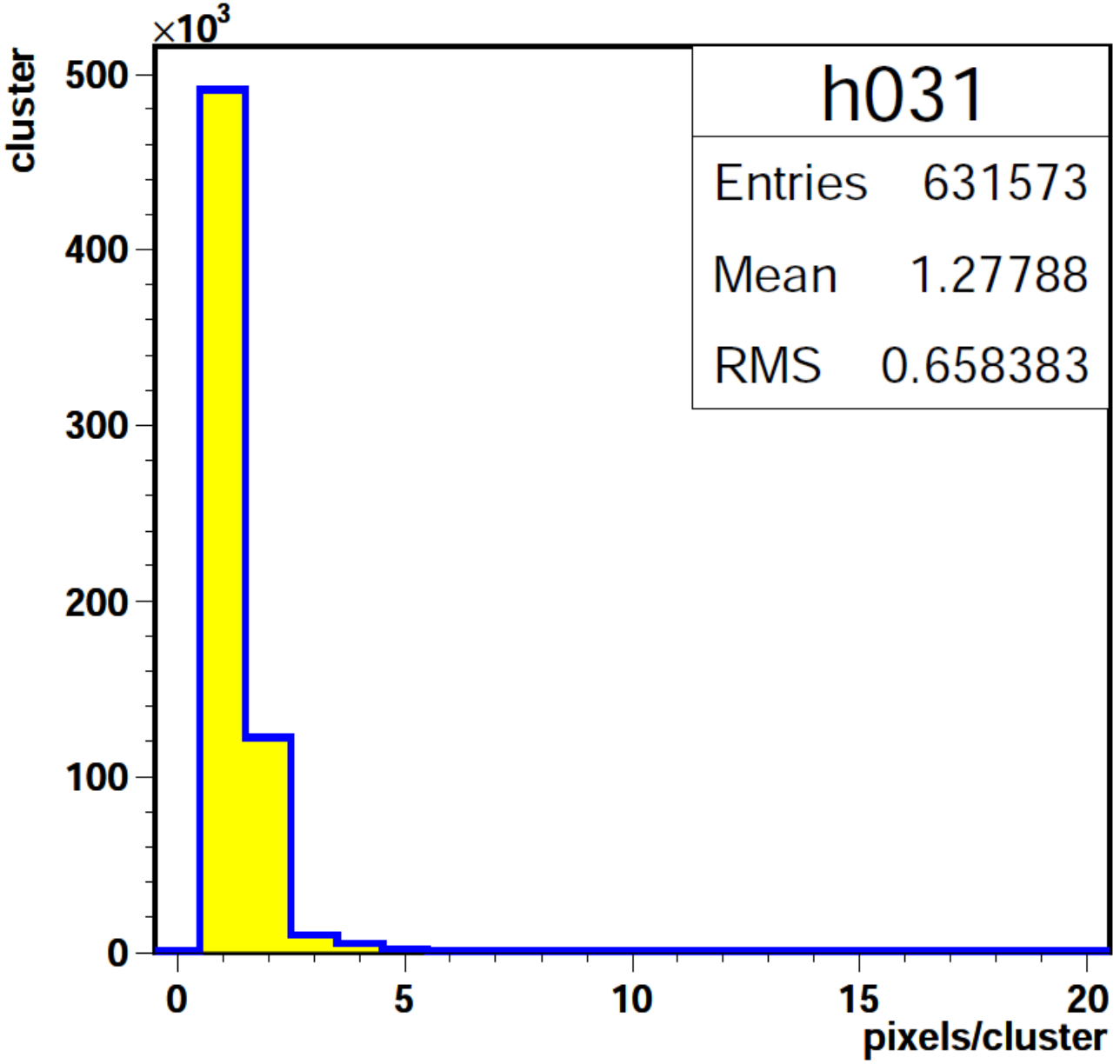
- the same run
- a few dead pixels
- non-uniformity:
  - beam profile,
  - misalignment between sensor and scintillator,
  - limited trigger region (~1 cm^2) just enough to cover 0.8×0.8 cm^2 chip.

Cluster multiplicity



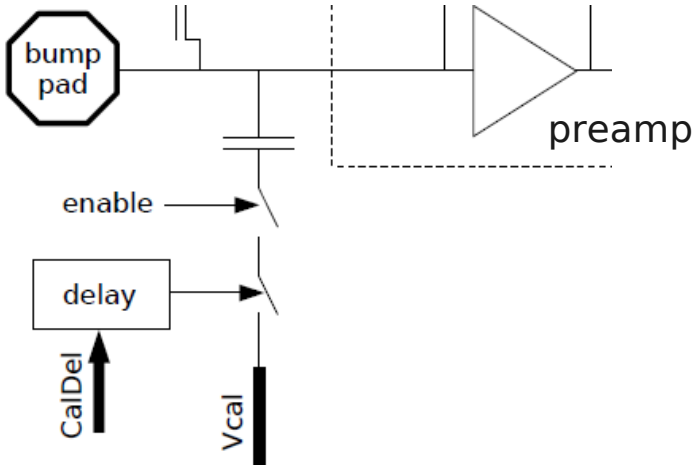
- Pixel chip triggered by crossed finger scintillators:
  - 0.46 clusters/trigger
- Losses:
  - geometric acceptance (trigger area is larger than the pixel chip)
  - wrong timing (clock phase drifts w.r.t. beam)
  - inefficient pixels

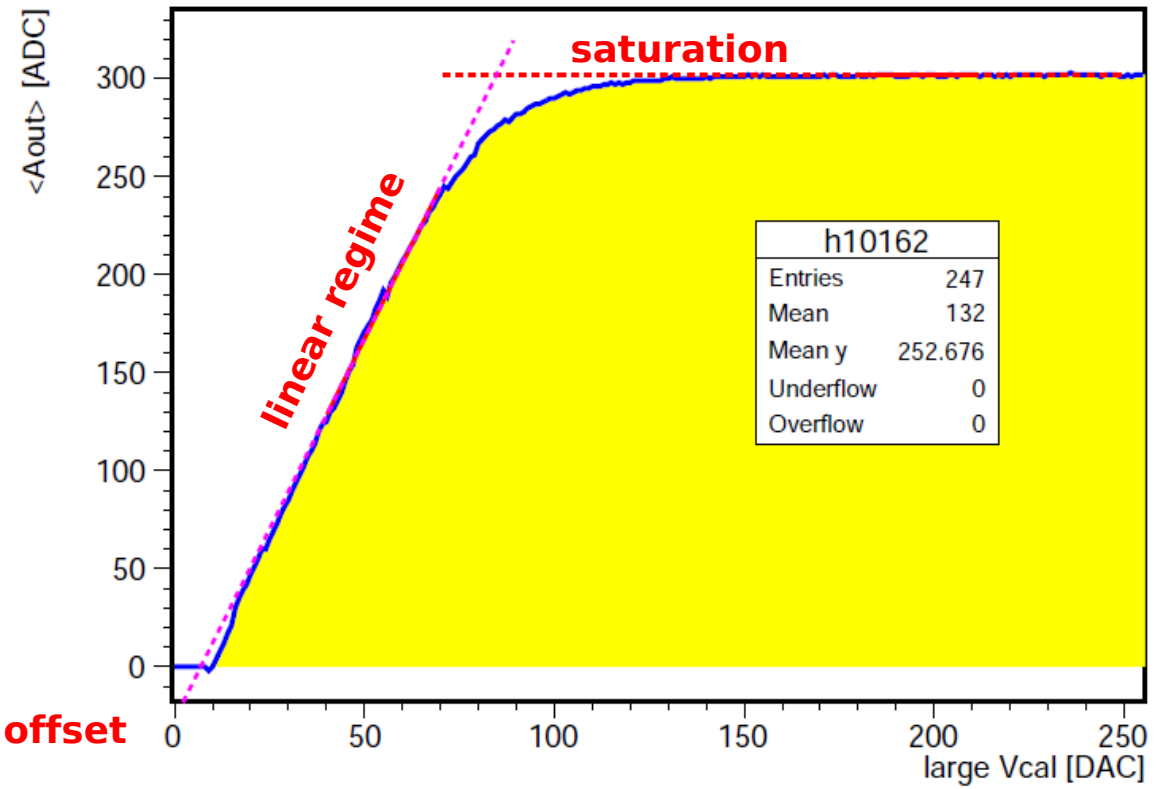
Cluster size



- 2 GeV e+ test beam.
- Pixel detector at vertical incidence, fully depleted (-90V bias).
- No magnetic field.
- Mostly 1-pixel clusters, no charge sharing.
- 2-pixel clusters at pixel edges.
- 3- and 4-pixel clusters at pixel corners.
- 5-pixel clusters?
- mean: 1.3 pixels / cluster

Internal gain calibration



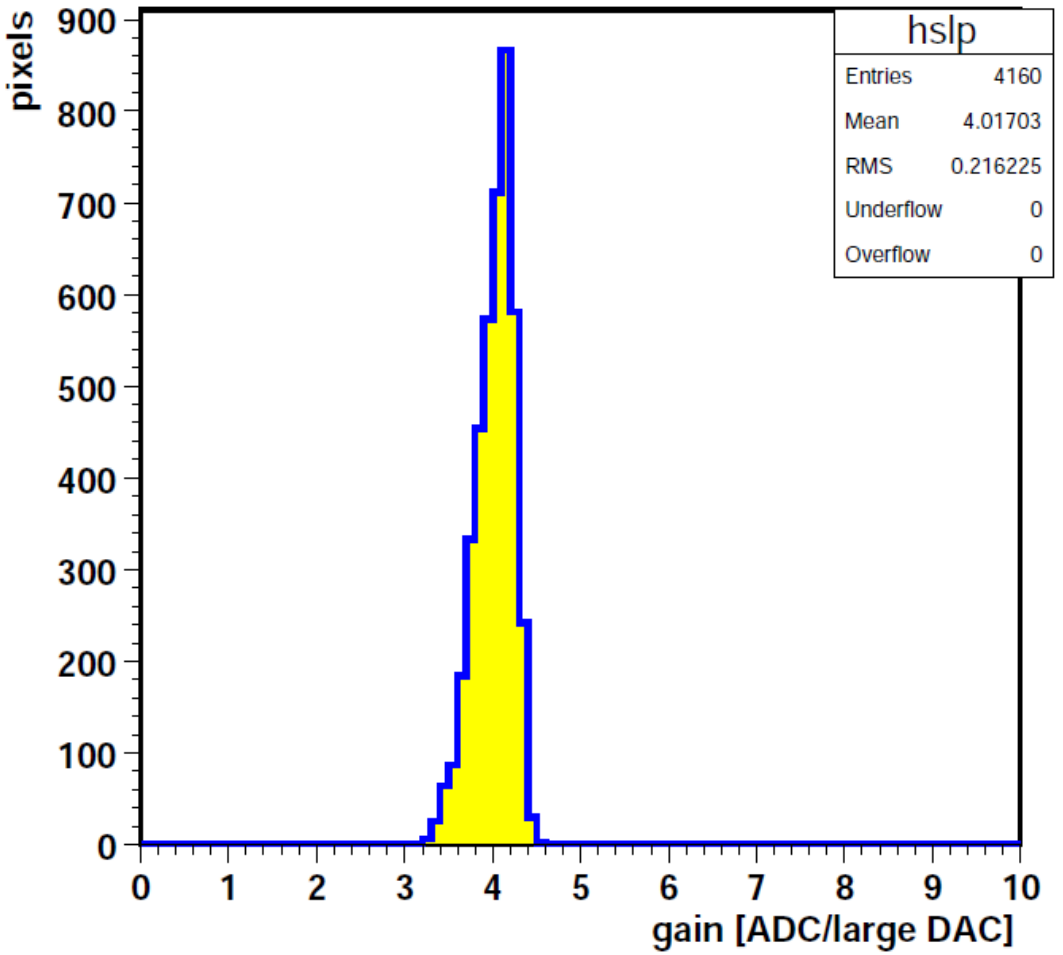


- Scan with internal calibrate pulse
- Linear regime above some threshold:
  - fit gain and offset
- Preamp saturation for large pulses
- Repeat for 4160 pixels

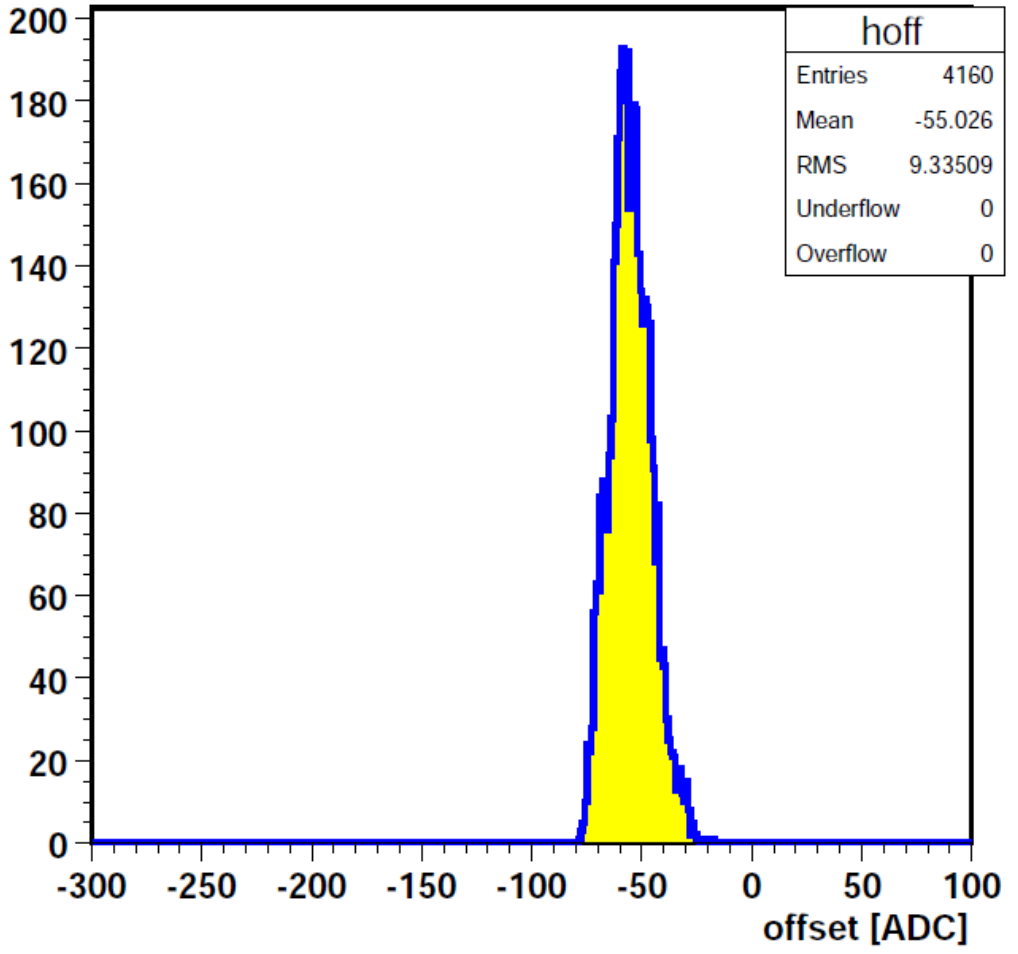
Internal gains

chip 8, Vsf 165 DACs

gains



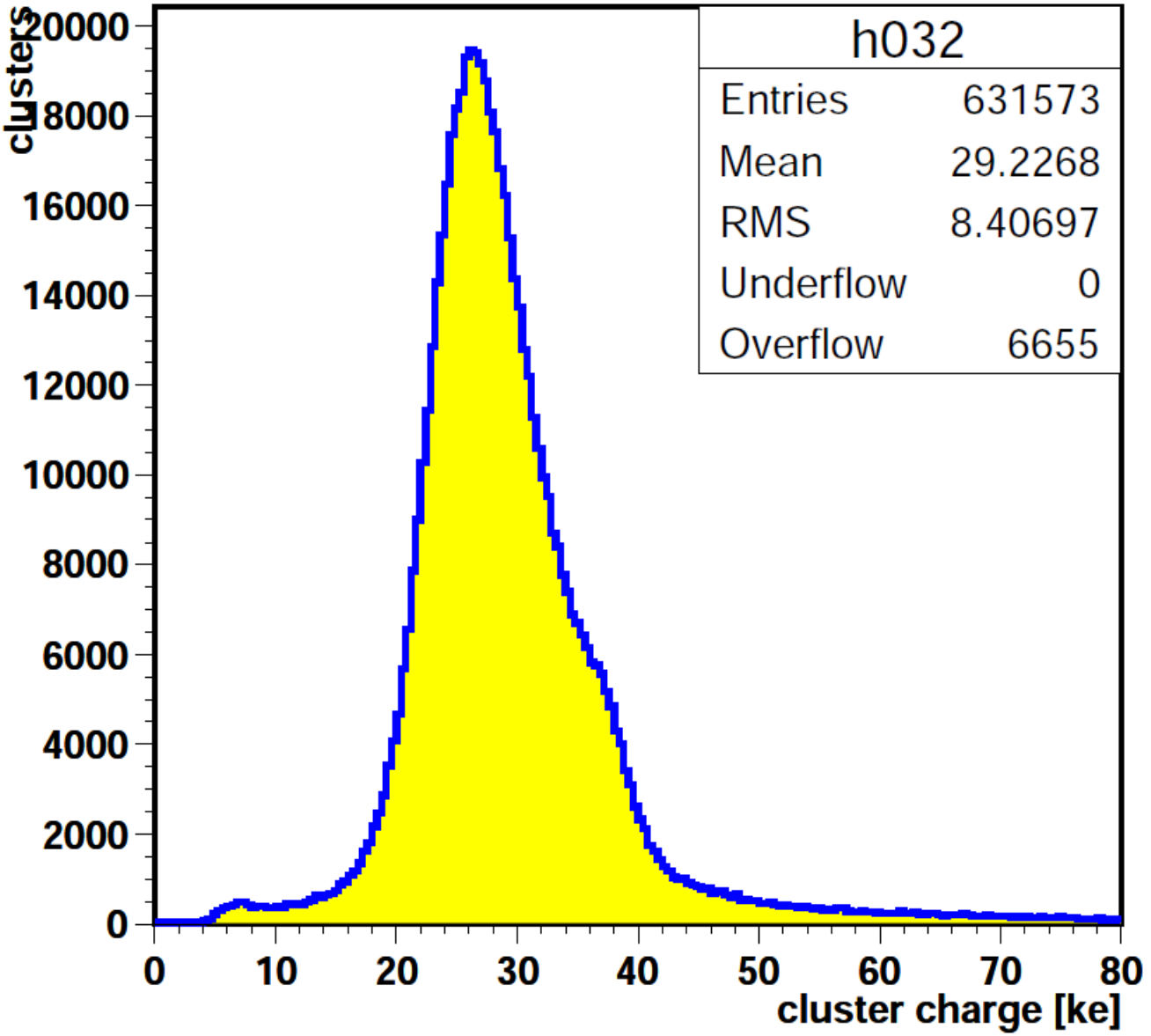
offsets



PSI X-ray source:

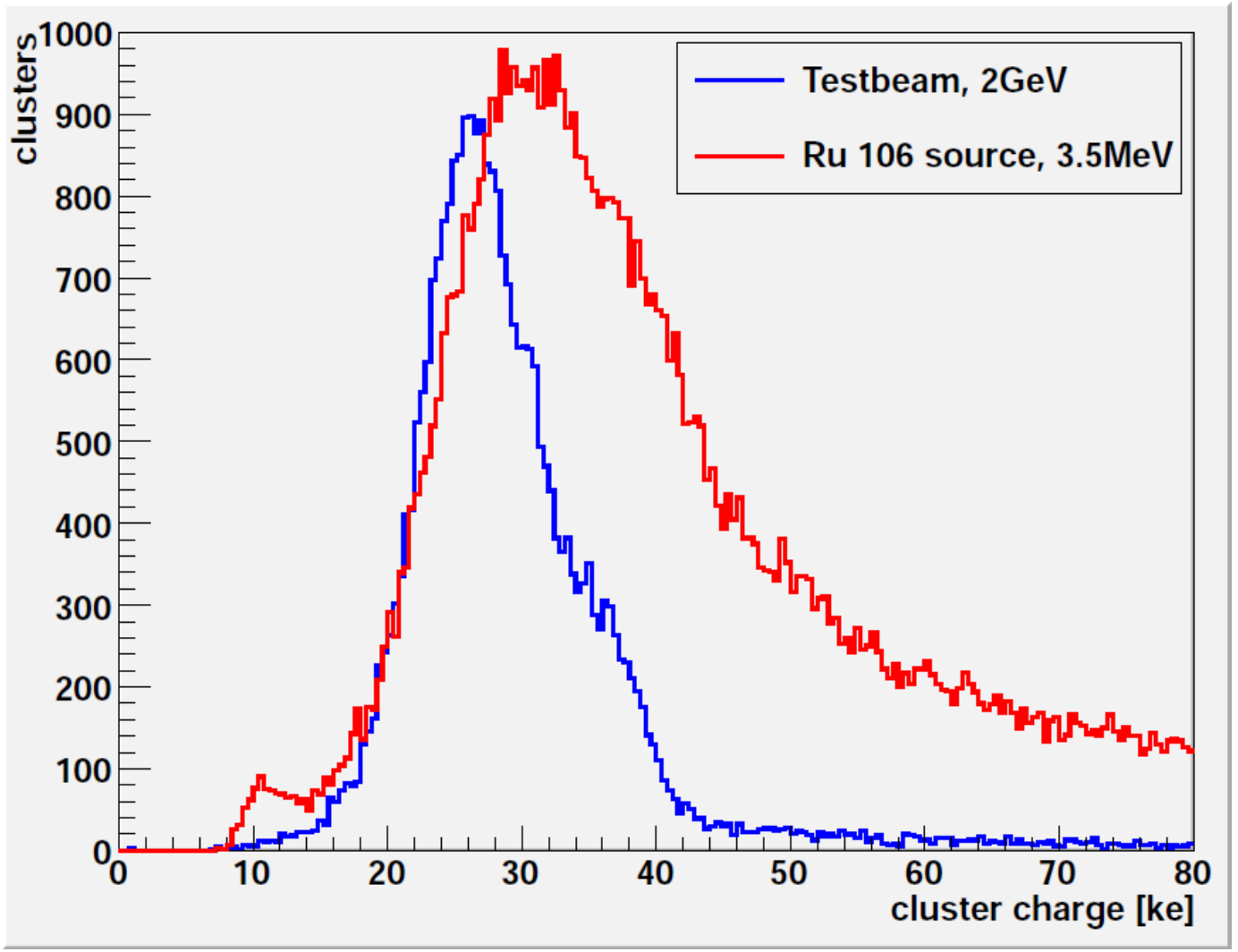
450 e / large Vcal DAC

Cluster charge



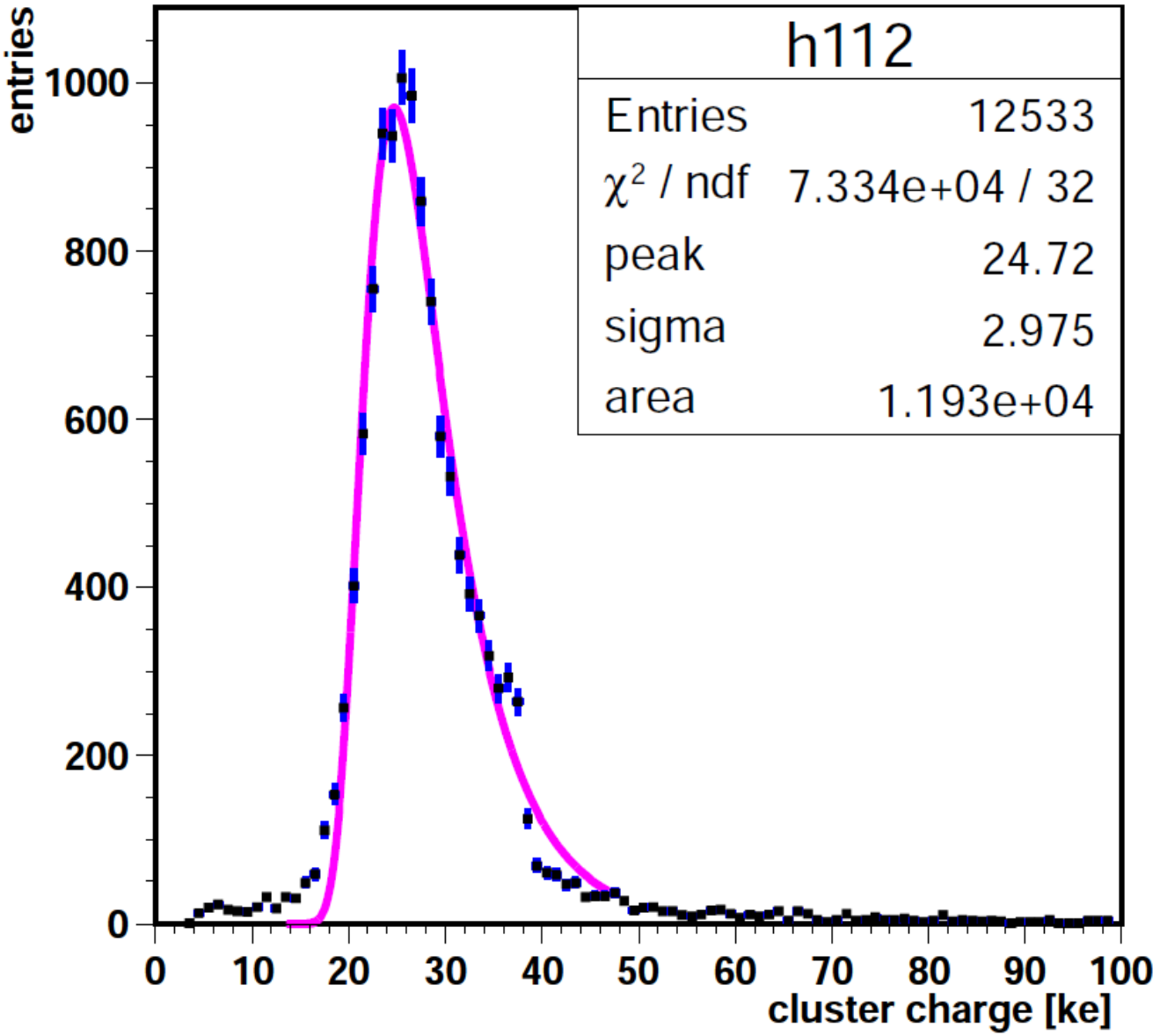
- 2 GeV e+ test beam.
- Pixel detector at vertical incidence, fully depleted (-90V bias).
- No magnetic field.
- Test pulse gain calibration applied.
- Foot of small pulses:
  - wrong timing?
- Peak at 26 ke, OK for MIPs in 285 µm silicon.
- Hump: saturation.
- Tail: multi-pixel clusters.

Cluster charge: Ru source vs beam



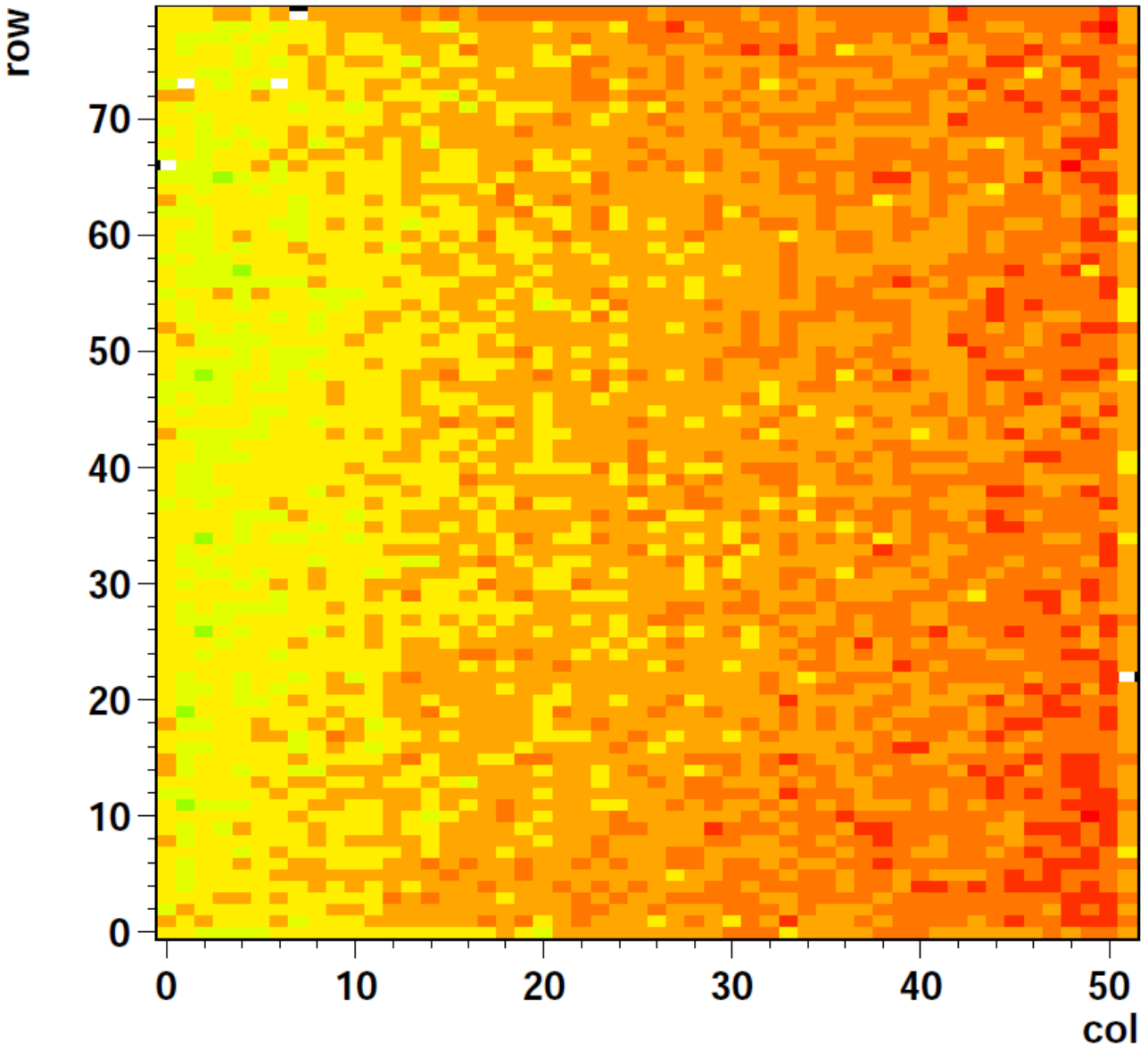
- Chip 8, -90V bias, Vthr 100
- 2 GeV e+ test beam:
  - Minimum ionizing particles
- Ru 106 source:
  - long tail of stronger ionizing electrons (not fully relativistic).

Cluster charge



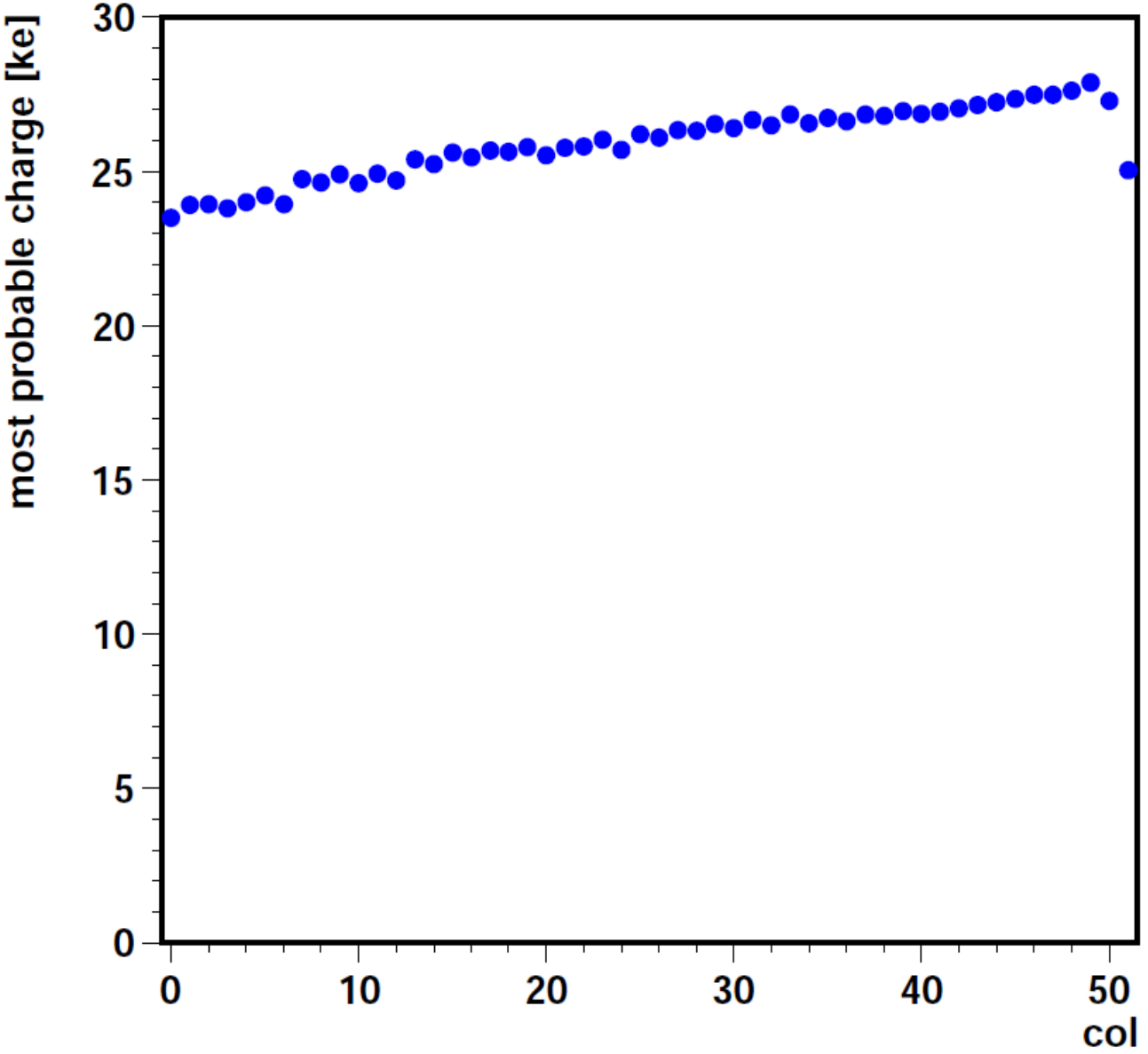
- 2 GeV e+ test beam.
- Pixel detector at vertical incidence, fully depleted (-90V bias).
- No magnetic field.
- Test pulse gain calibration applied.
- Chip 8, column 12.
- Fit by Moyal function:
  - analytic approximation of the Landau integral.
  - suffers from foot and hump in data.

Cluster charge map



- 2 GeV e+ test beam.
- Pixel detector at vertical incidence, fully depleted (-90V bias).
- No magnetic field.
- Test pulse gain calibration applied.
- Trend across the chip
  - test pulse problem?
- Quite uniform along one column.

T

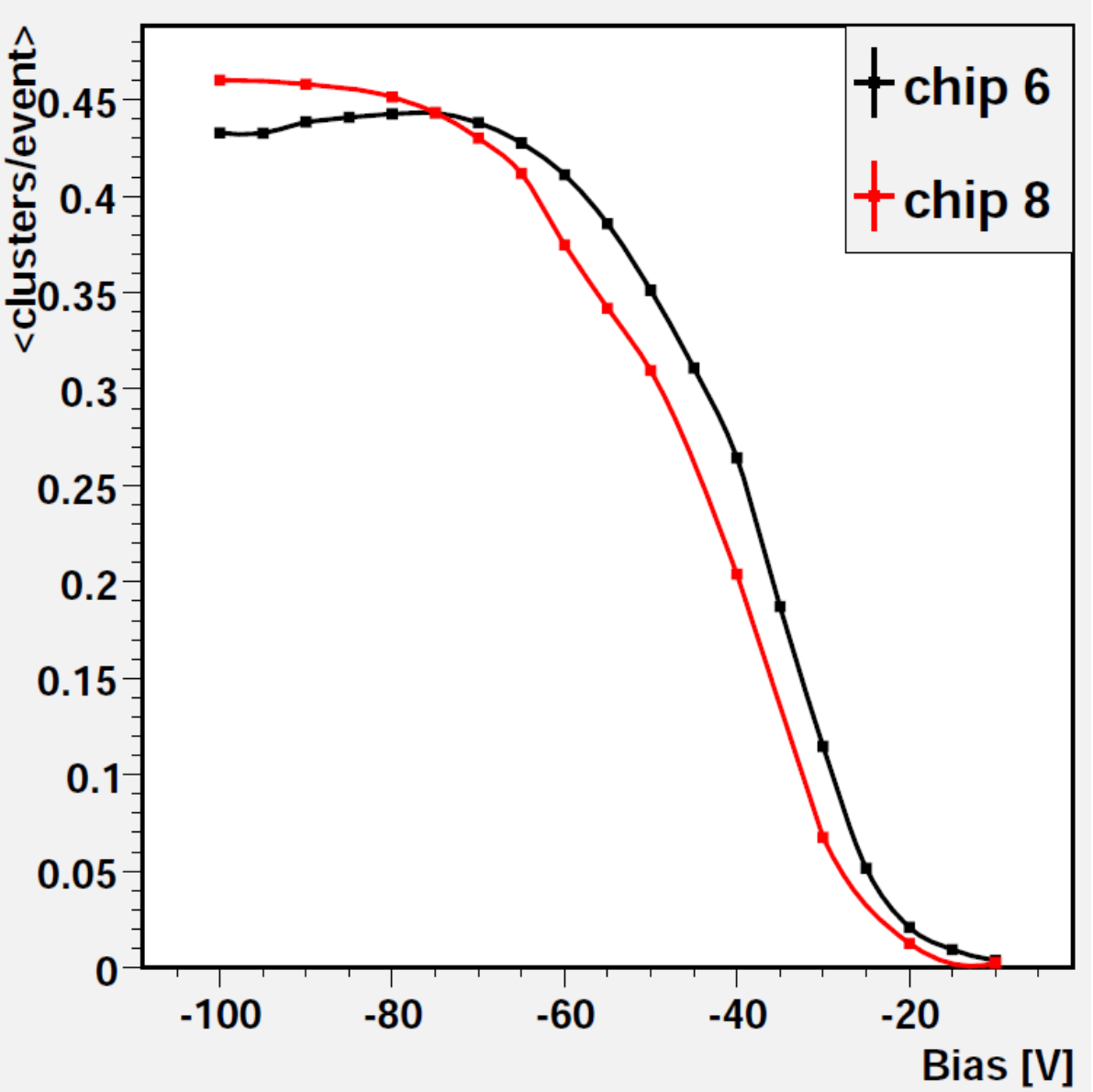


- 2 GeV e+ test beam.
- Pixel detector at vertical incidence, fully depleted.
- Test pulse gain calibration applied.
- Moyal fit to each column.
- Expect ~25 ke from 285 µm silicon.
- Observe ~8% gain variation across the chip:
  - test pulse problem?
  - check with X-ray source!

scans

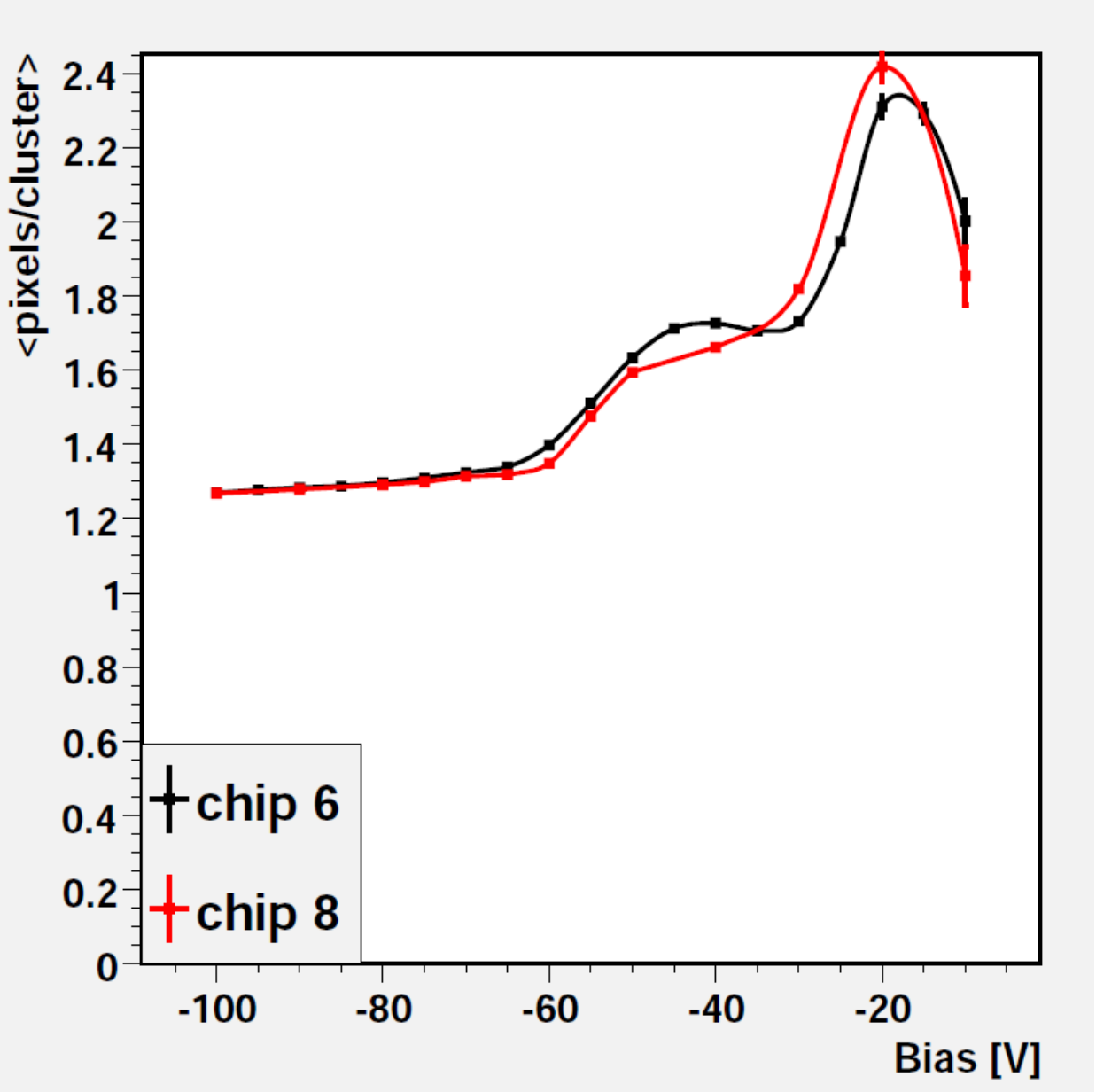
- 2 GeV e^+ beam from DESY II
- scintillator trigger, typically 6.4 kHz.
- chips 6 and 8 with sensor (PSI46 2.0 from 2004)
  - chip 7 gave readout problems (missing token out?)
- DAC settings from test pulse procedure
  - Vsf and VhldDel slightly adjusted compared to March 2011.
- Bias voltage scan
- Threshold scan
- Sample & Hold delay scan
- Trigger delay scan

Cluster multiplicity vs. bias voltage



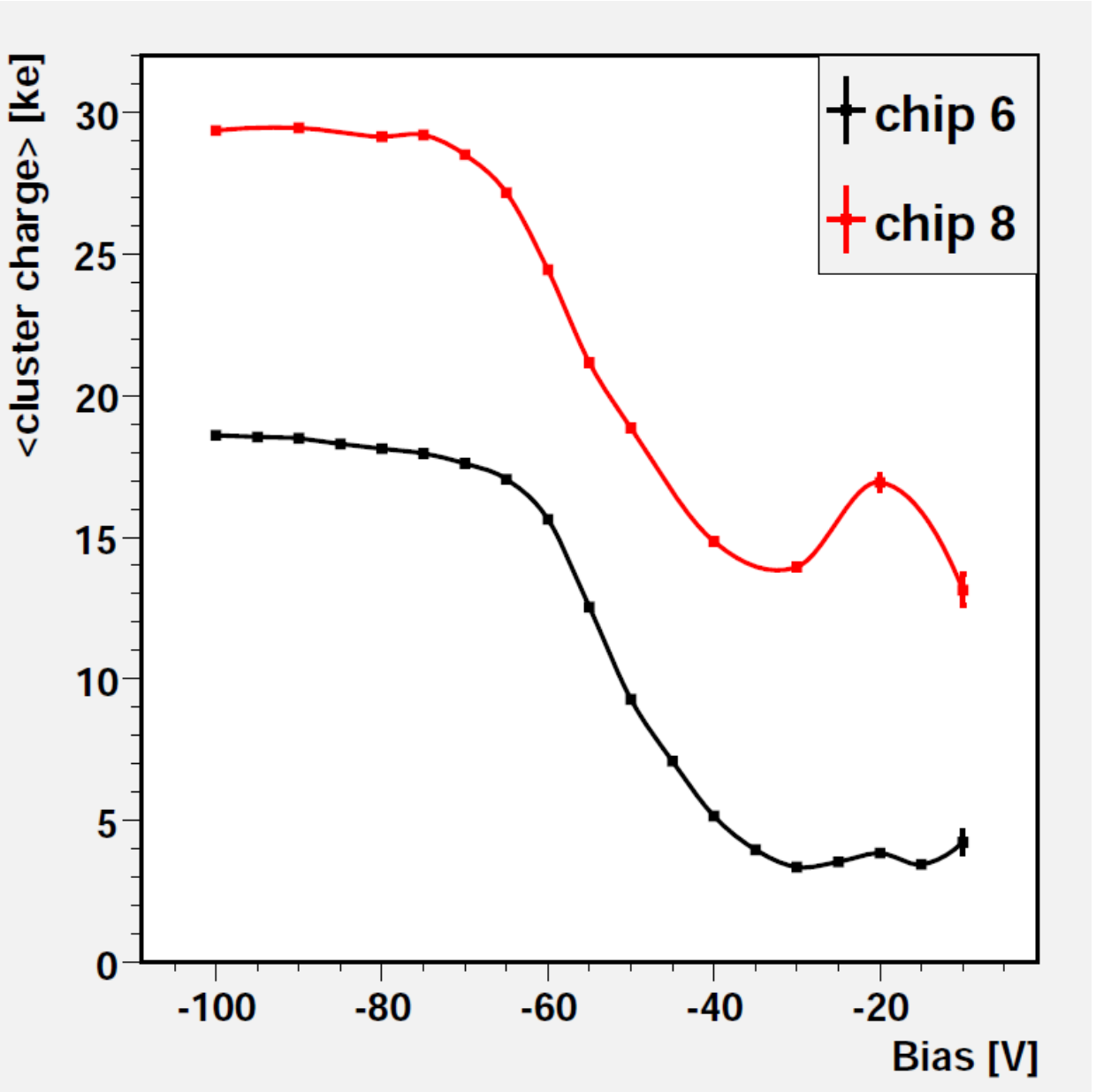
- Cluster efficiency saturates below -80 V

Cluster size vs. bias voltage



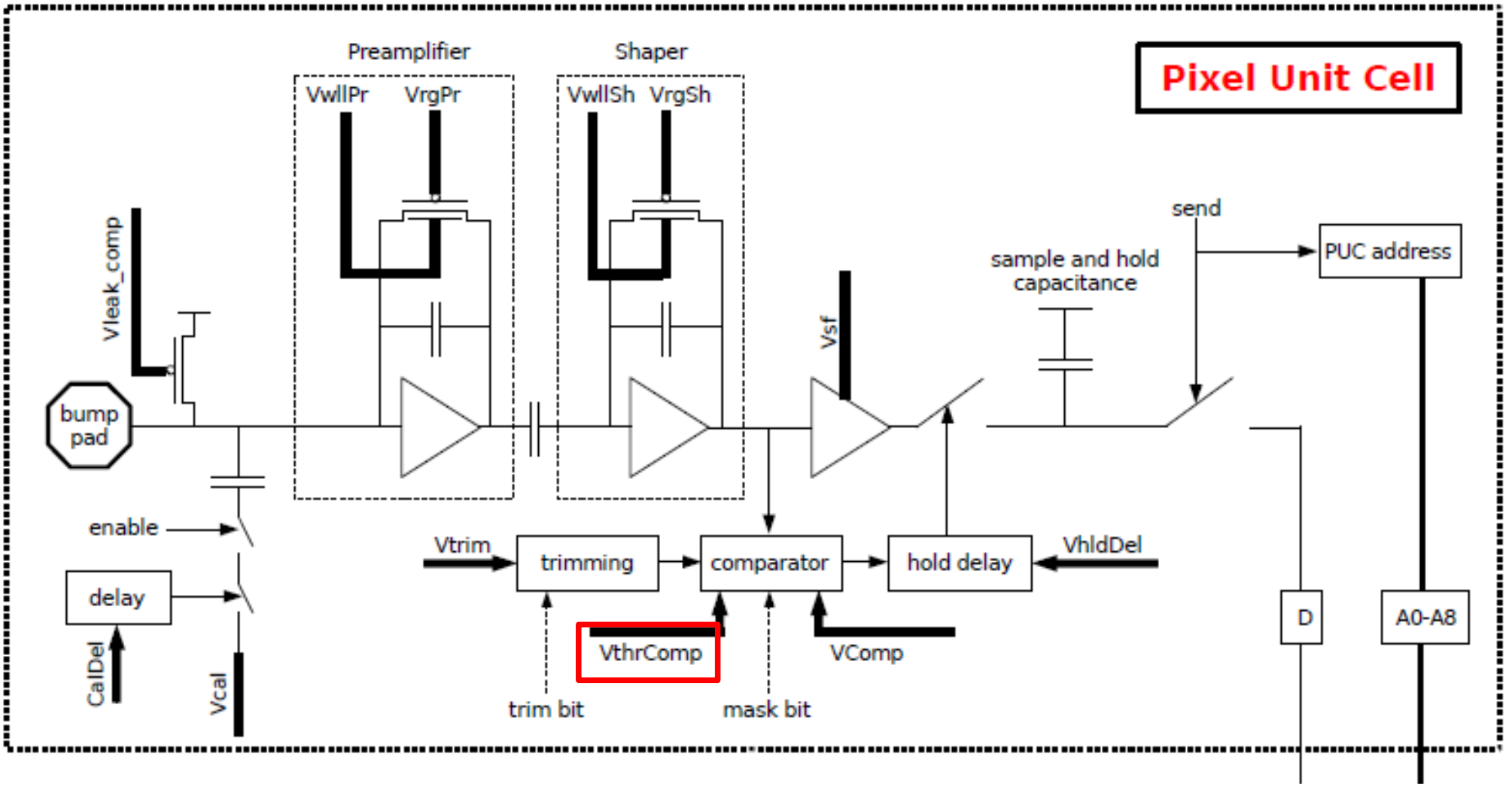
- S

Cluster charge vs. bias voltage



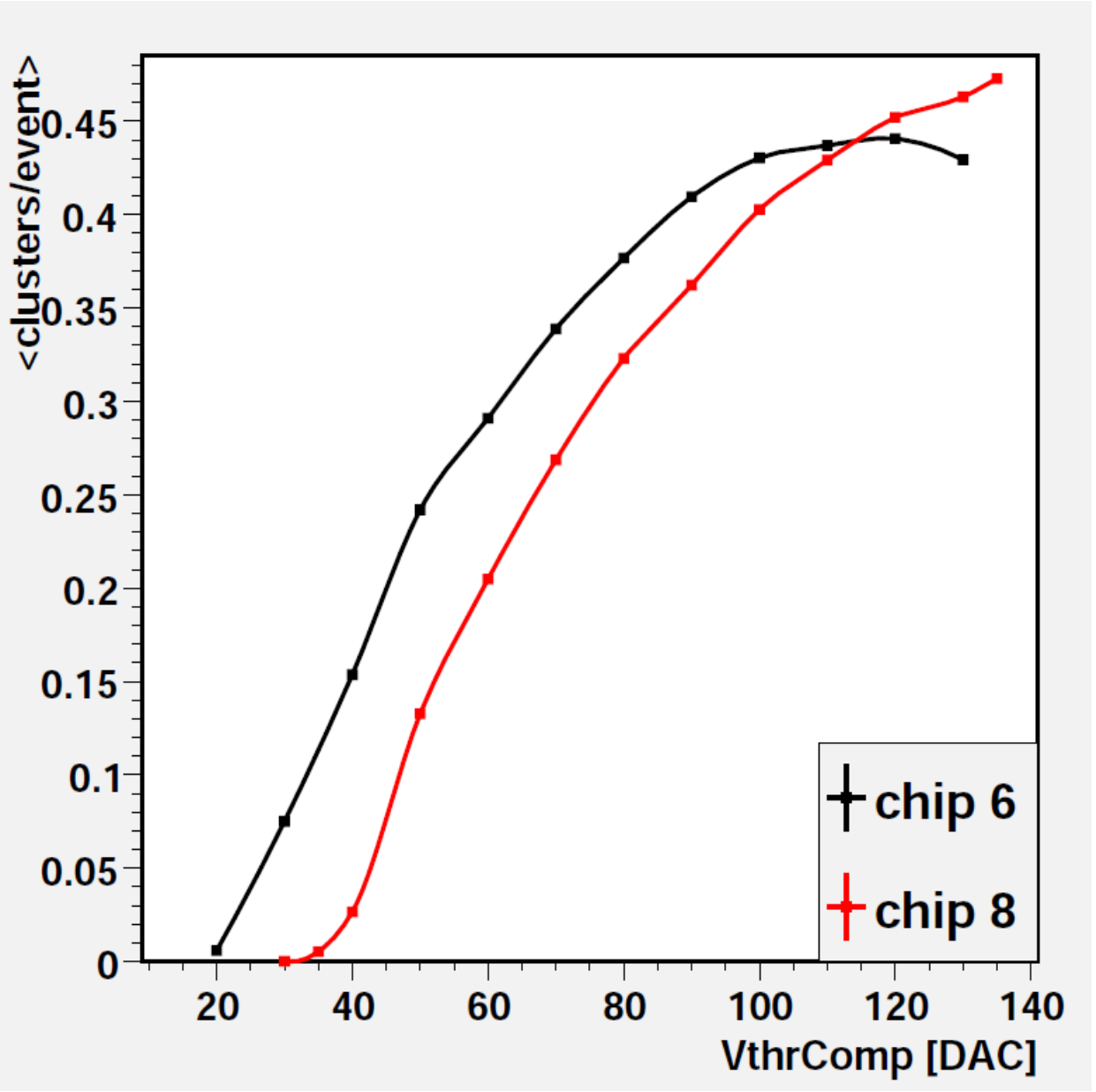
- Analog gain and offset not equalized

Common threshold voltage scan



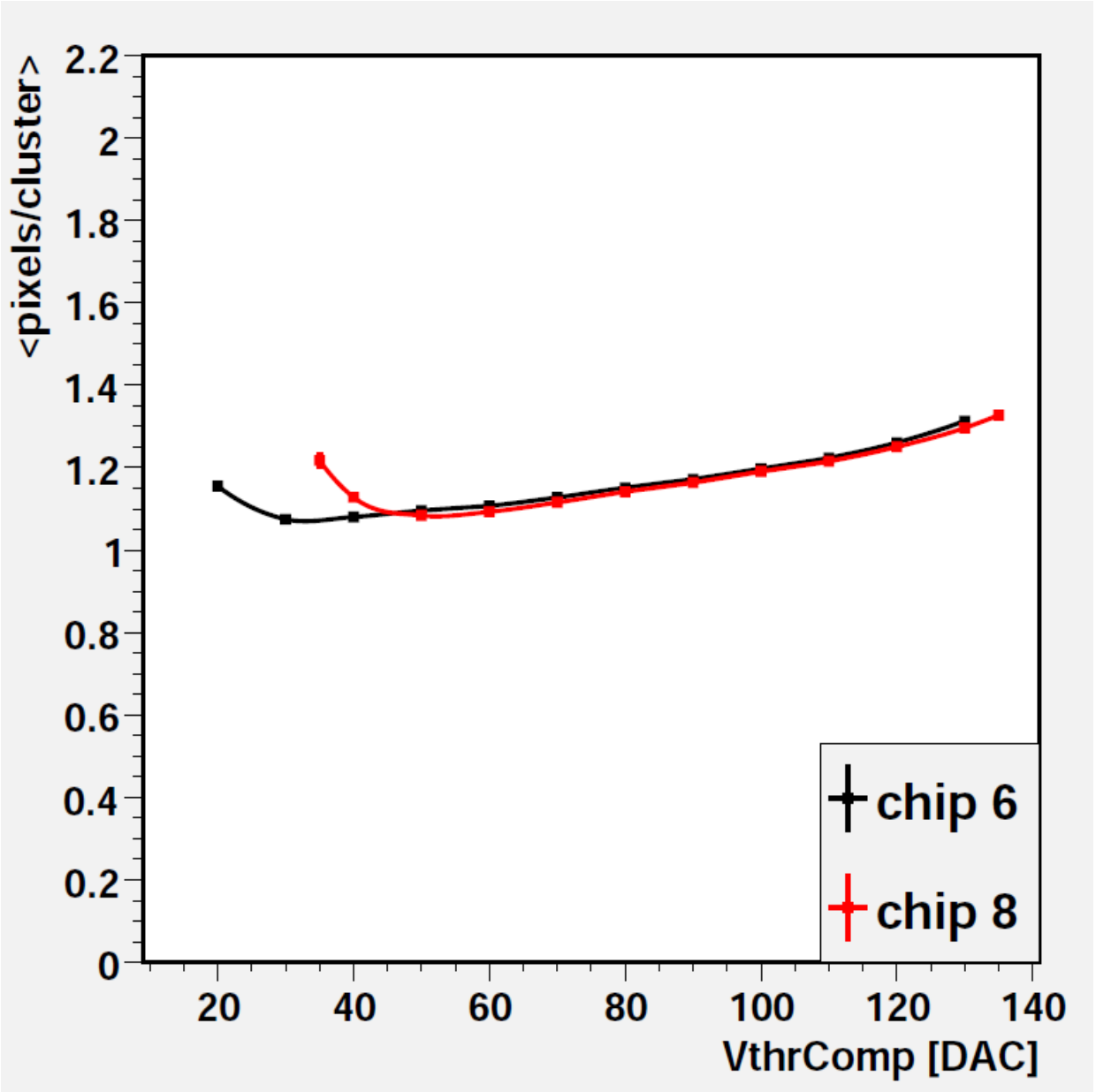
adjustable by programmable DAC, per ROC

Cluster efficiency vs. threshold



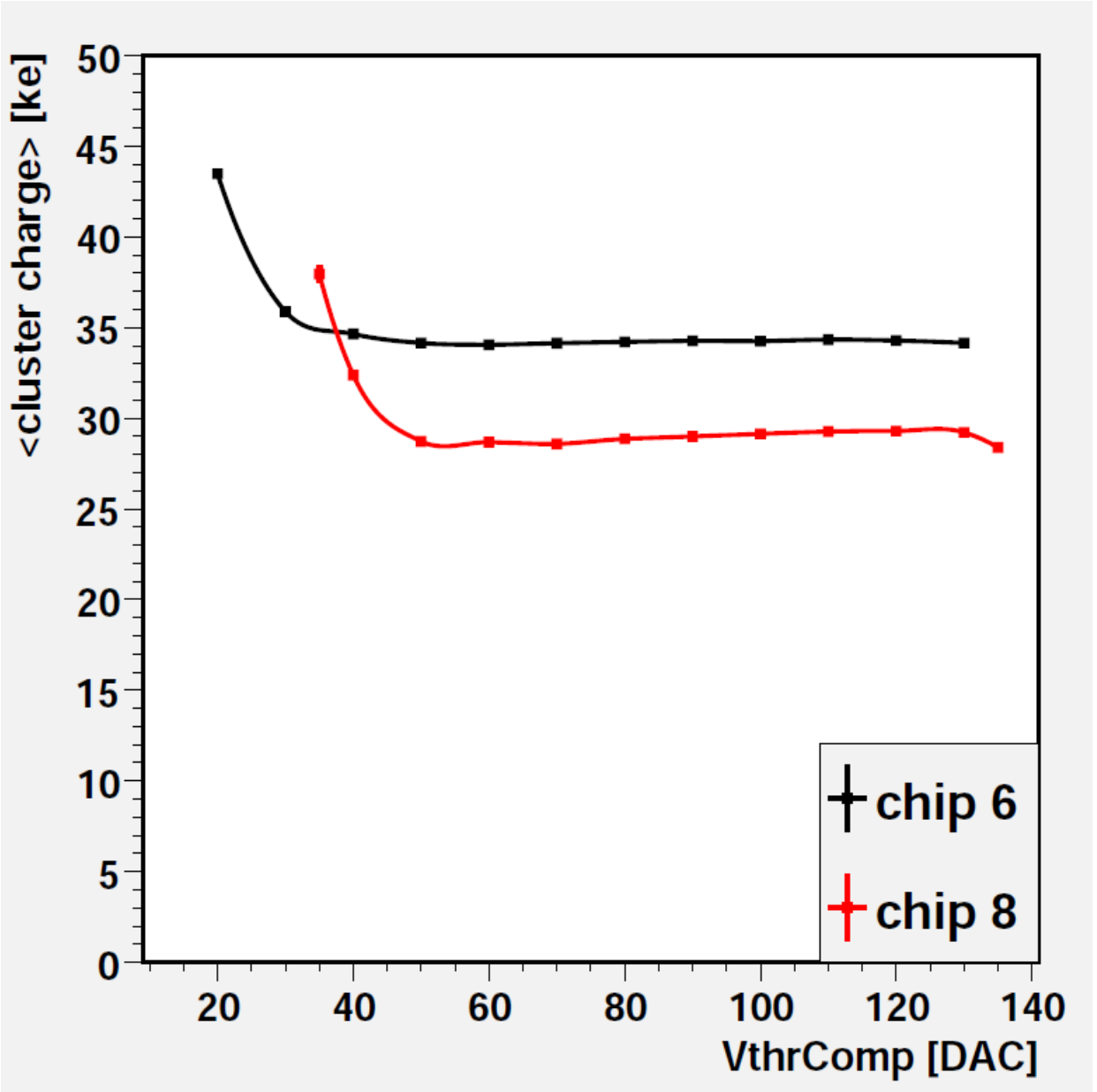
- DESY testbeam:
  - 2 GeV e+
  - Scintillator trigger
  - Vbias -90 V
- VthrComp is inverted:
  - large DAC = soft threshold (close to pedestal).
- Efficiency plateau not reached?
  - timing problem?

Cluster size vs. threshold



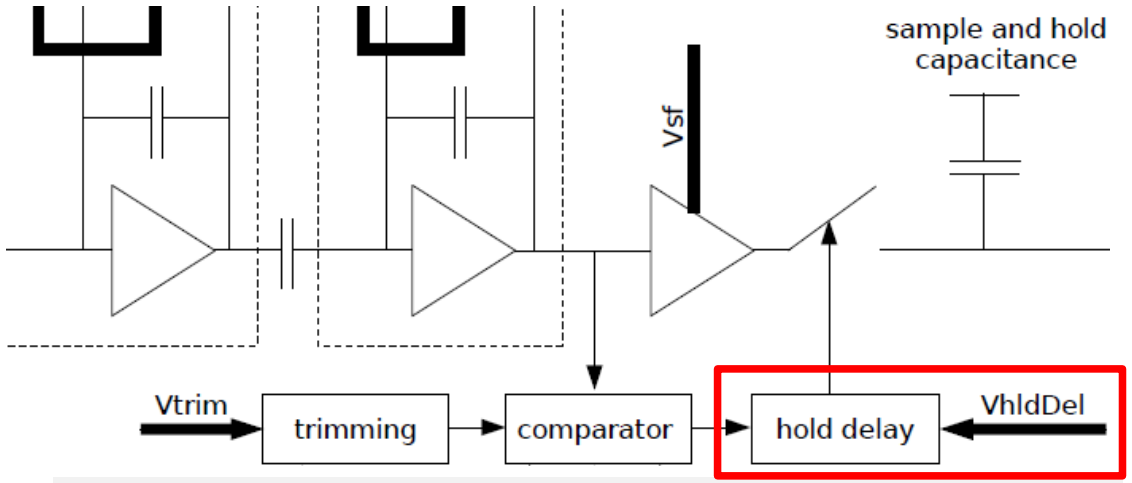
- Strange behavior at hard threshold (small DAC).
- Linear growth of clusters with softer threshold.

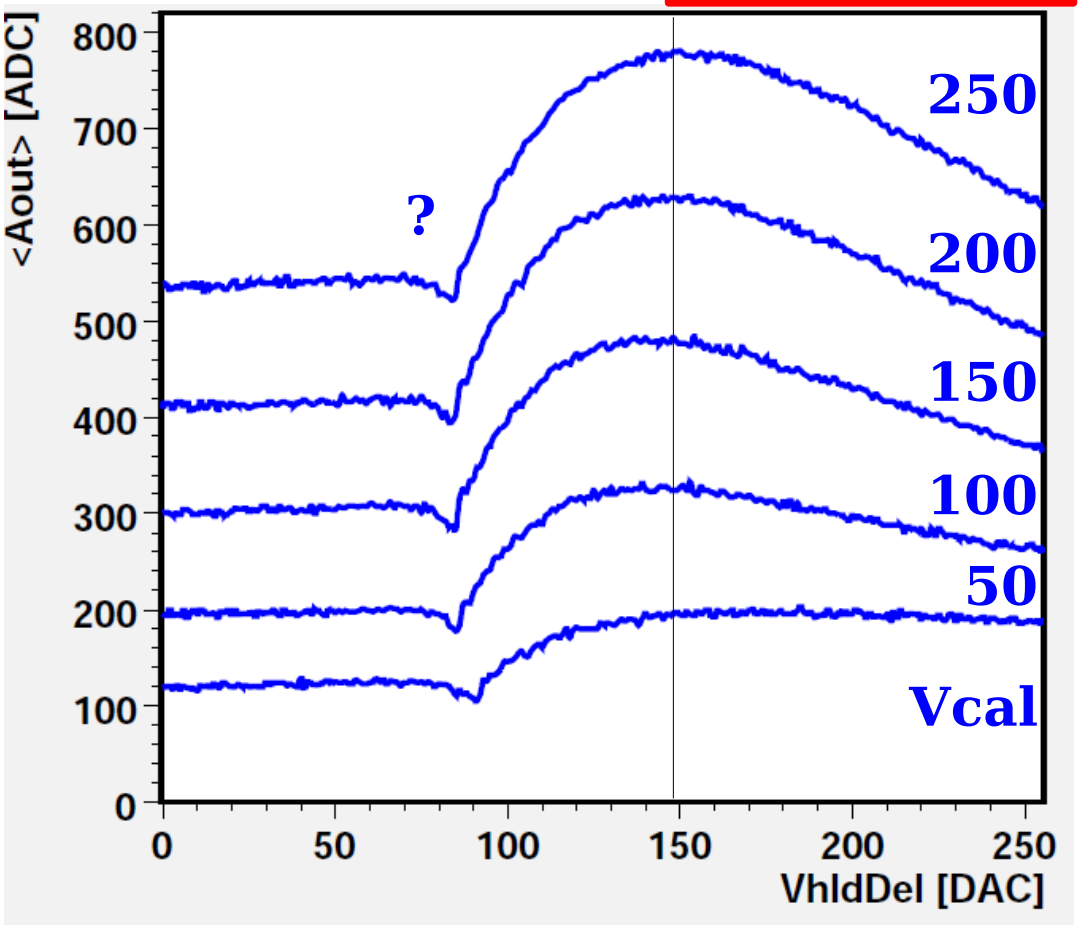
Cluster charge vs. threshold



- softer threshold → clusters gain some pixels
- A small drop at weak threshold?

Sample and hold timing

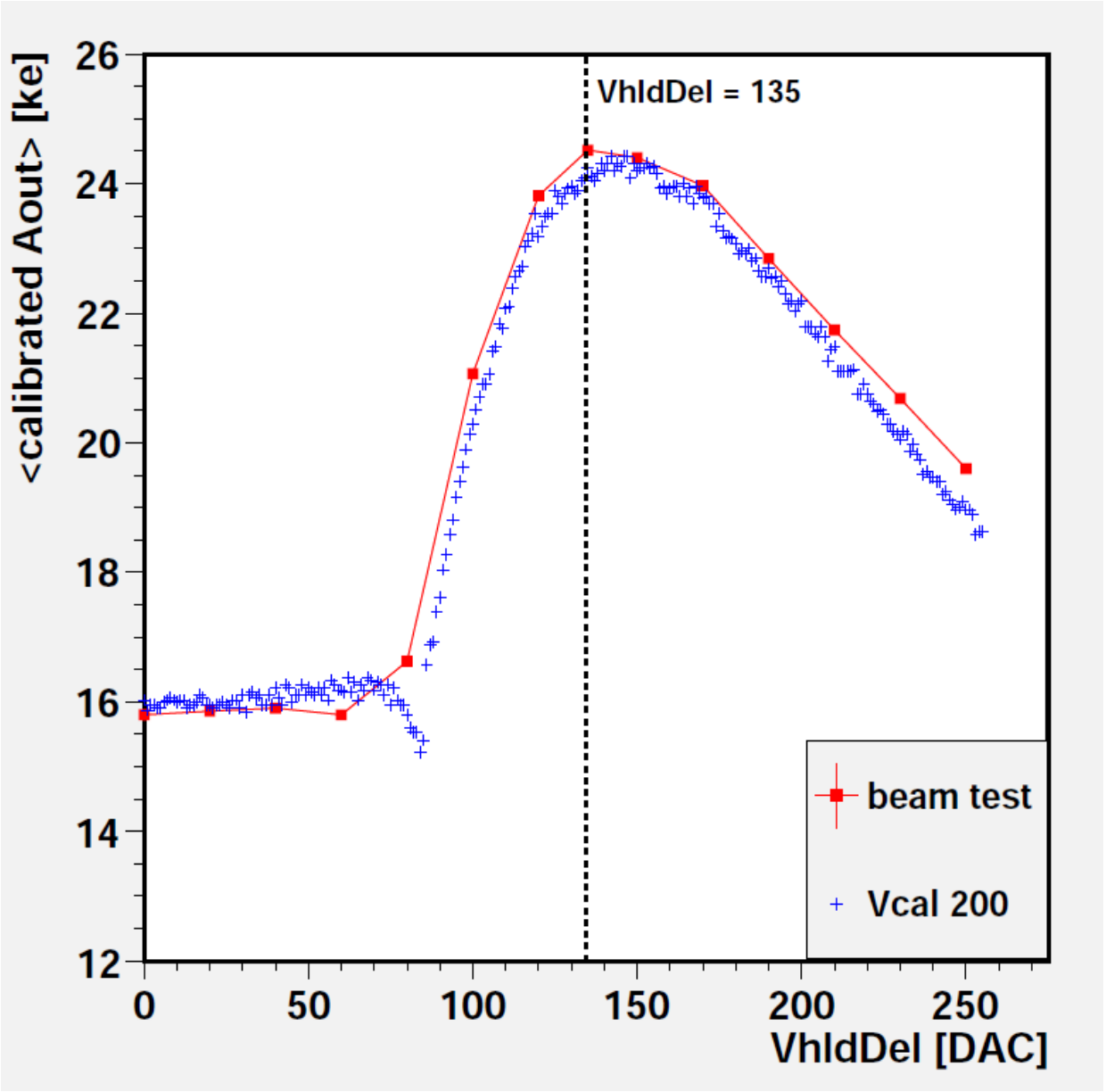




Test pulse study from March 2011 Chip 0

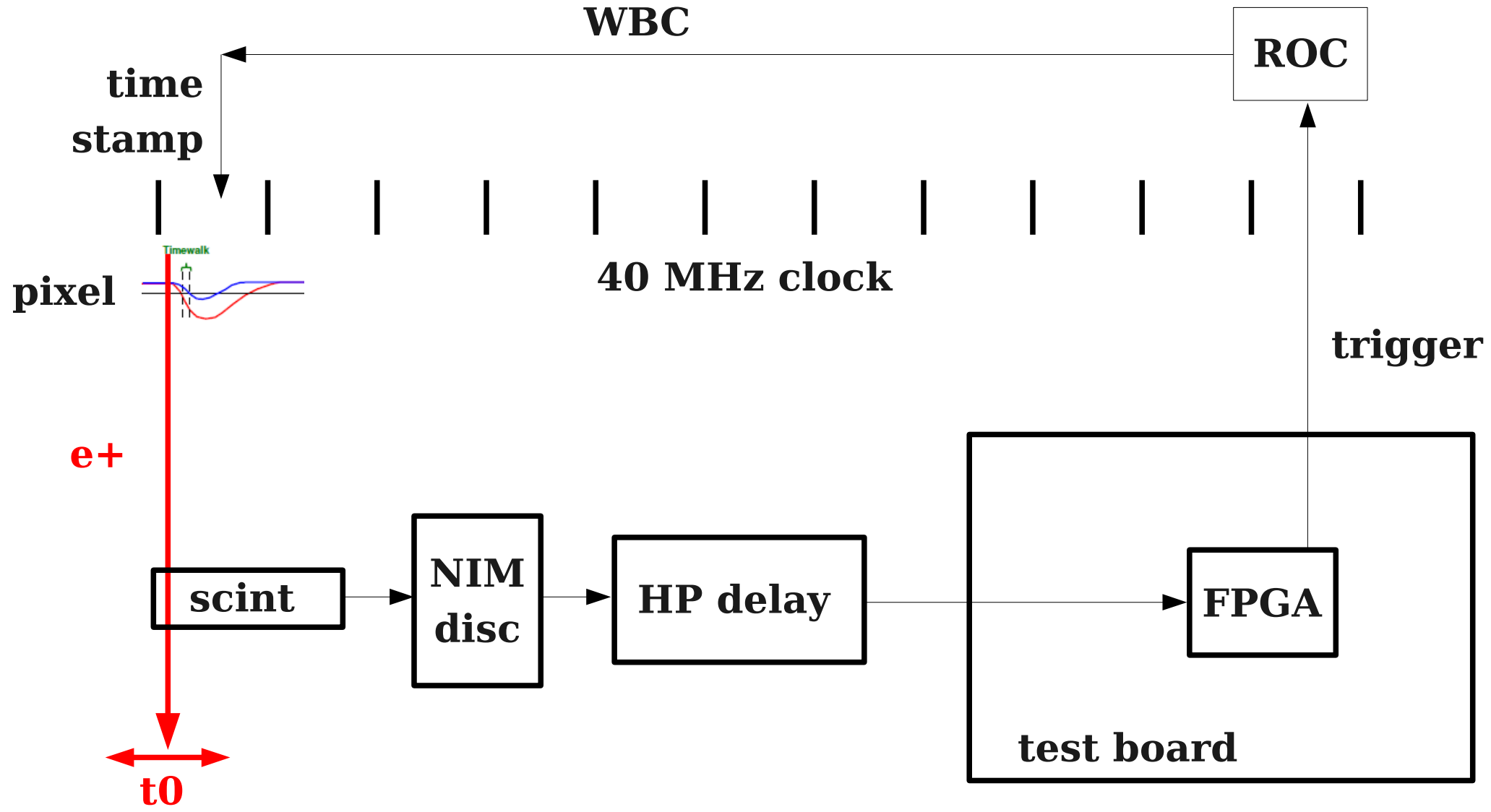
- One pixel.
- Position of maximum depends on pulse height:
  - time walk.
- DAC 150 is compromise

Cluster charge vs. hold delay



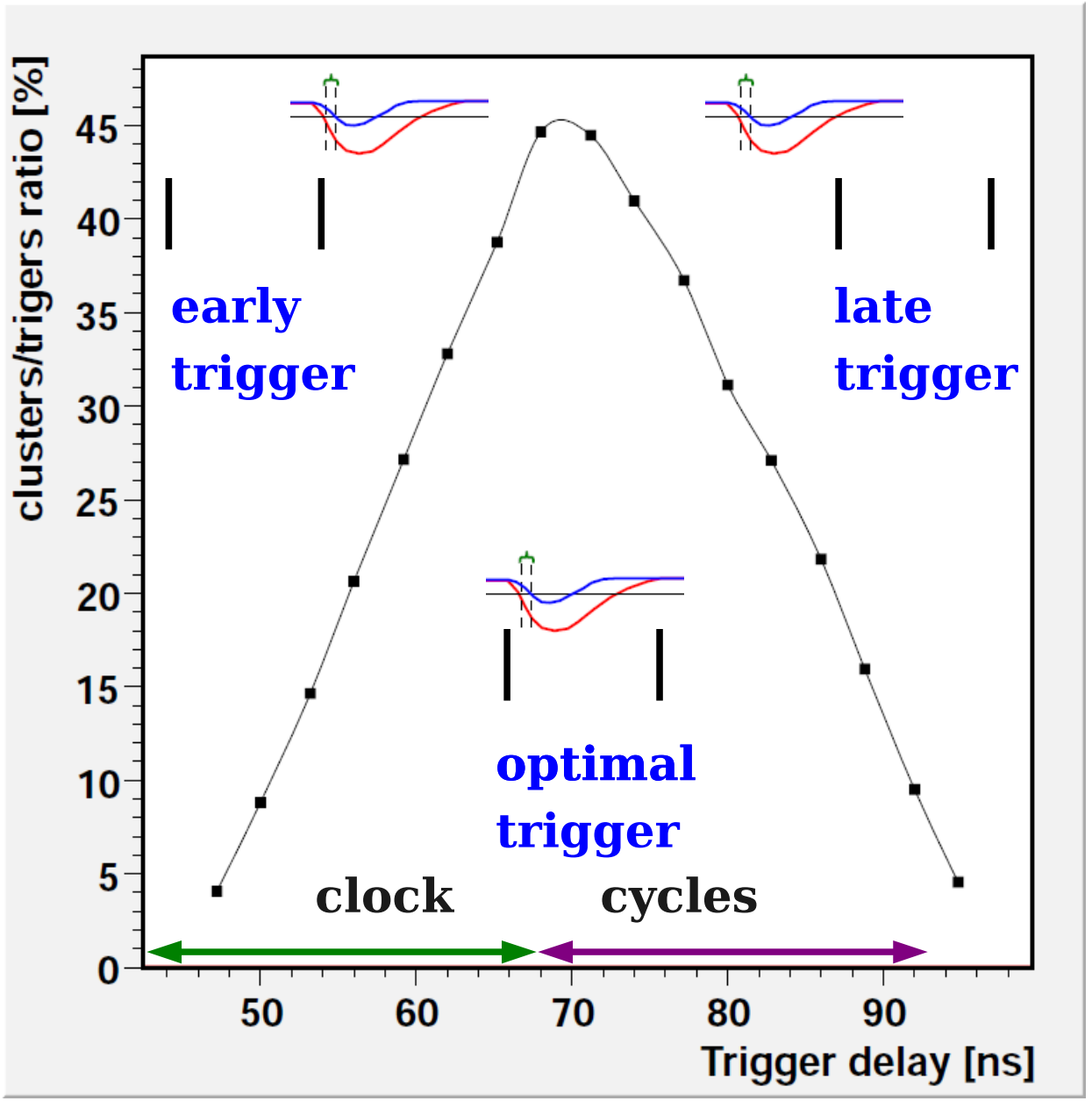
- DESY testbeam:
  - 2 GeV e+
  - Scintillator trigger
  - Chip 8
- similar behavior as with test pulse.
- Chose 135 as working point.

Timing



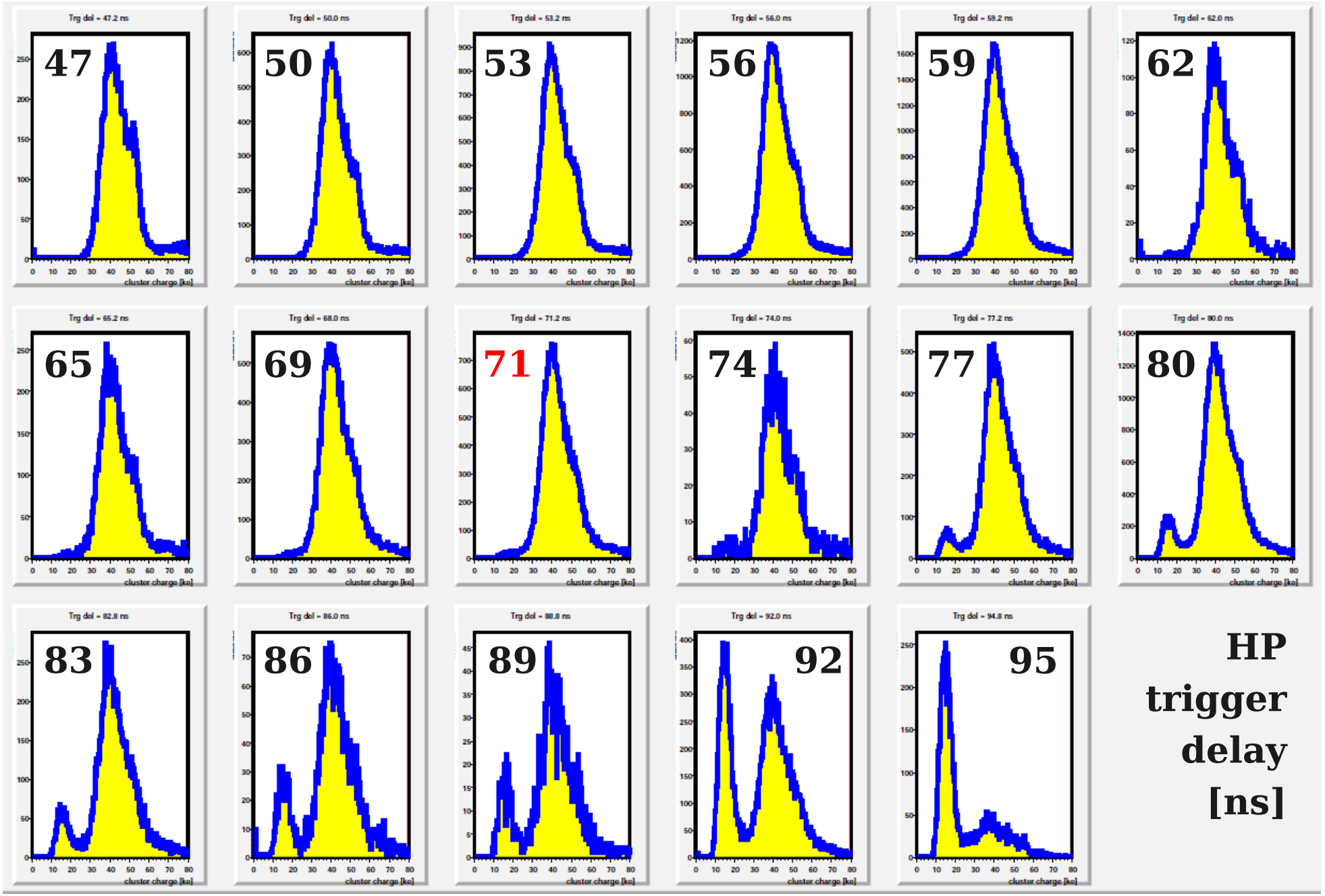
beam not synchronized to clock

Trigger delay scan



- DESY test beam:
  - 2 GeV e+
  - Scintillator trigger
- delay scintillator trigger going to the PSI46test board
- 25 ns clock cycle
- Triangular efficiency curve:
  - flat arrival time distribution (clock not synchronized to beam)
- Chose 70 ns as working point.

Trigger delay scan



Summary

- First experience with pixel detectors in the DESY test beam.
  - up to 7 kHz / cm^2 trigger rate at 2 GeV e+ setting.
  - scans of bias voltage, global threshold, trigger and hold delay done.
  - Results from source test confirmed.
- open issues:
  - corrupt readouts (masked out for analysis).
  - gain variation across chip (~8%).
  - readout problem with chip 7?
- next steps:
  - synchronize clock to beam.
  - apply threshold trimming (progress by Alexey).
  - support that allows for rotation and tilting (vary incidence angle).
  - common readout with the EUDet telescope for resolution studies (Hanno Perrey).

Acknowledgements

- Ingrid Gregor (DESY, test beam coordinator):
  - tolerating us, instructions.
- Norbert Meyners (DESY, test beam coordinator):
  - help with collimator, wire target.
- Samuel Ghazaryan (DESY, test beam support):
  - help with moving system, rate monitor.
- Holger Maser (DESY):
  - building the support frame for the test board.
- Torsten Külper:
  - made the TTL trigger adapter for the test board.
- Erika Garutti (DESY and Uni HH):
  - lent us the finger scintillator and PM.
- BKR machine group:
  - steady beam production, friendly communication

PSI46 test board