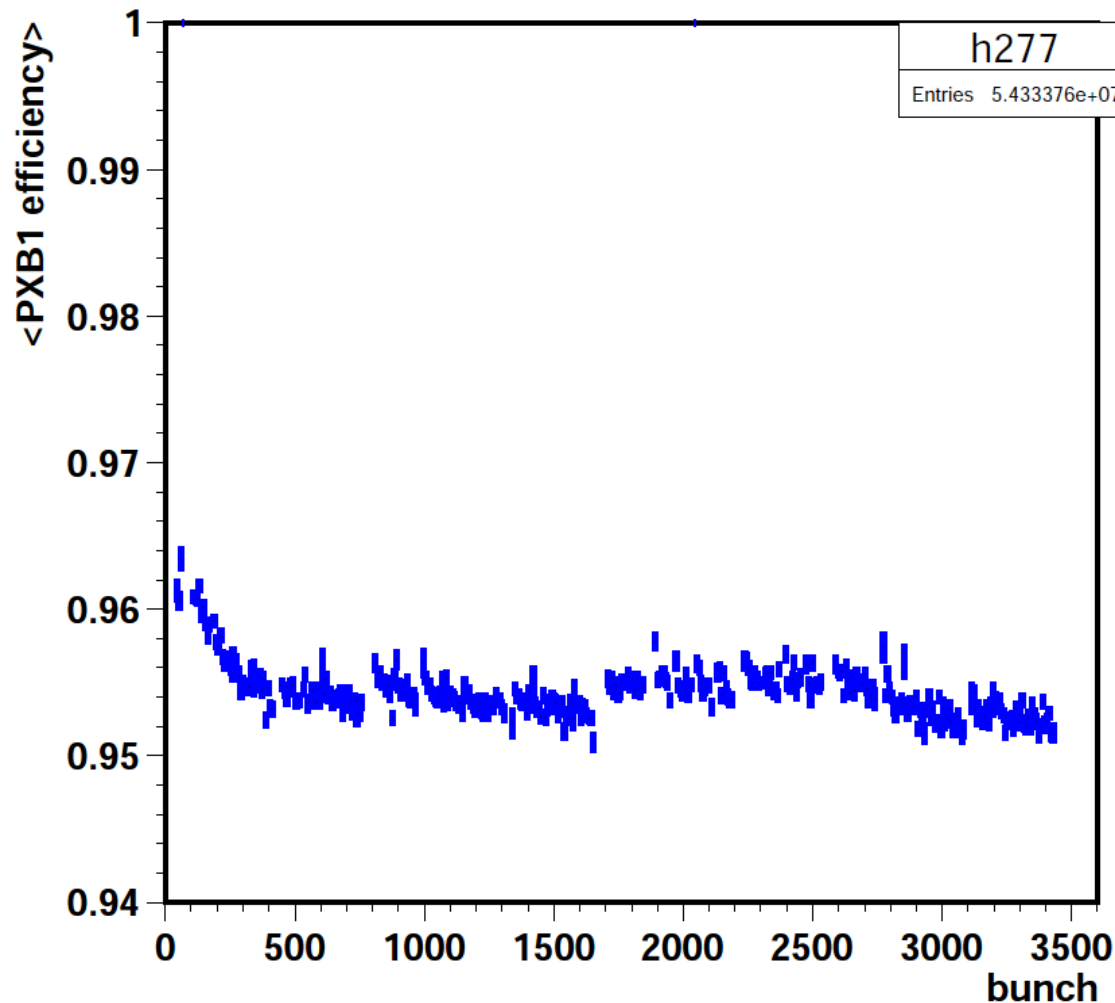


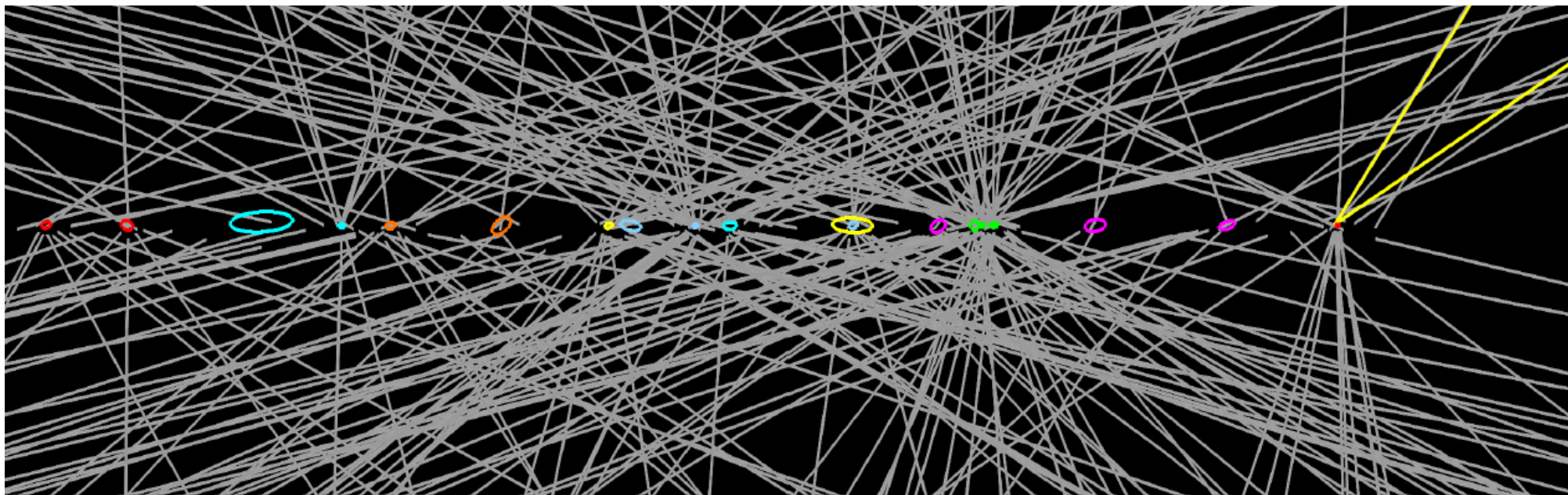
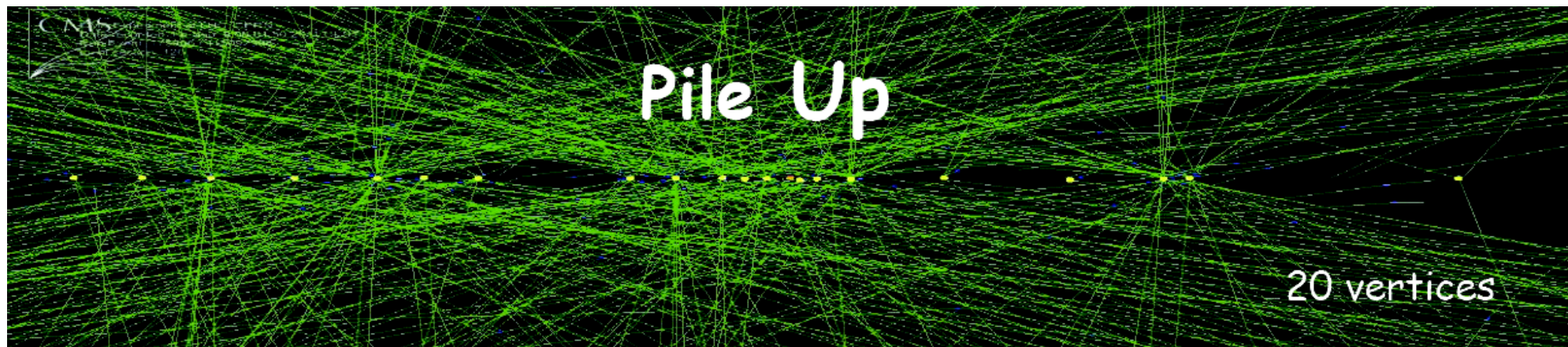
Barrel pixel dynamic inefficiency at PU 12

Daniel Pitzl, DESY
CMS Pixel DPG 22.9.2011



- Sep 2011 data
- Efficiency vs bunch

Pile up September 2011

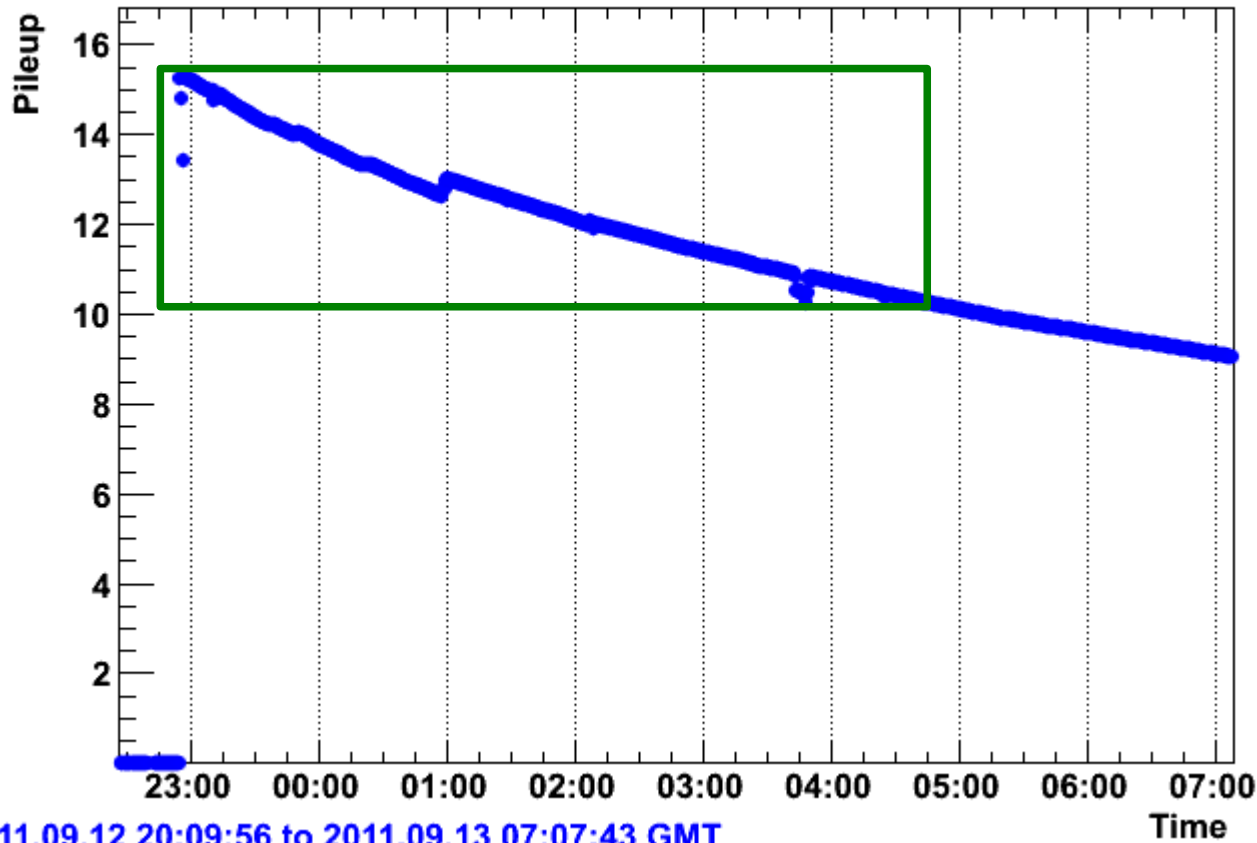


Data

- Sep 2011, early parts of fills 2092, 2093, 2094, 2101, 2103, 2104
 - 50 ns spacing, 1380 bunches, 1317 colliding
 - $\beta^* 1 \text{ m}$, $L_{\text{peak}} 3.2 \cdot 10^{33}$, starting pile up 15, $\langle \text{PU} \rangle 12$
- The pixel ROC efficiency may be affected by the history of the previous 156 or more bunch crossings (L1 latency or RO token):
 - data losses when Time Stamp or Data buffers are full,
 - data loss due to double column reset after a readout.
 - Study the pixel barrel efficiency as function of bunch number.
- Use hits on tracks (HitPattern) on AOD.
- SingleMu/AOD/PromptReco-v1

pile up

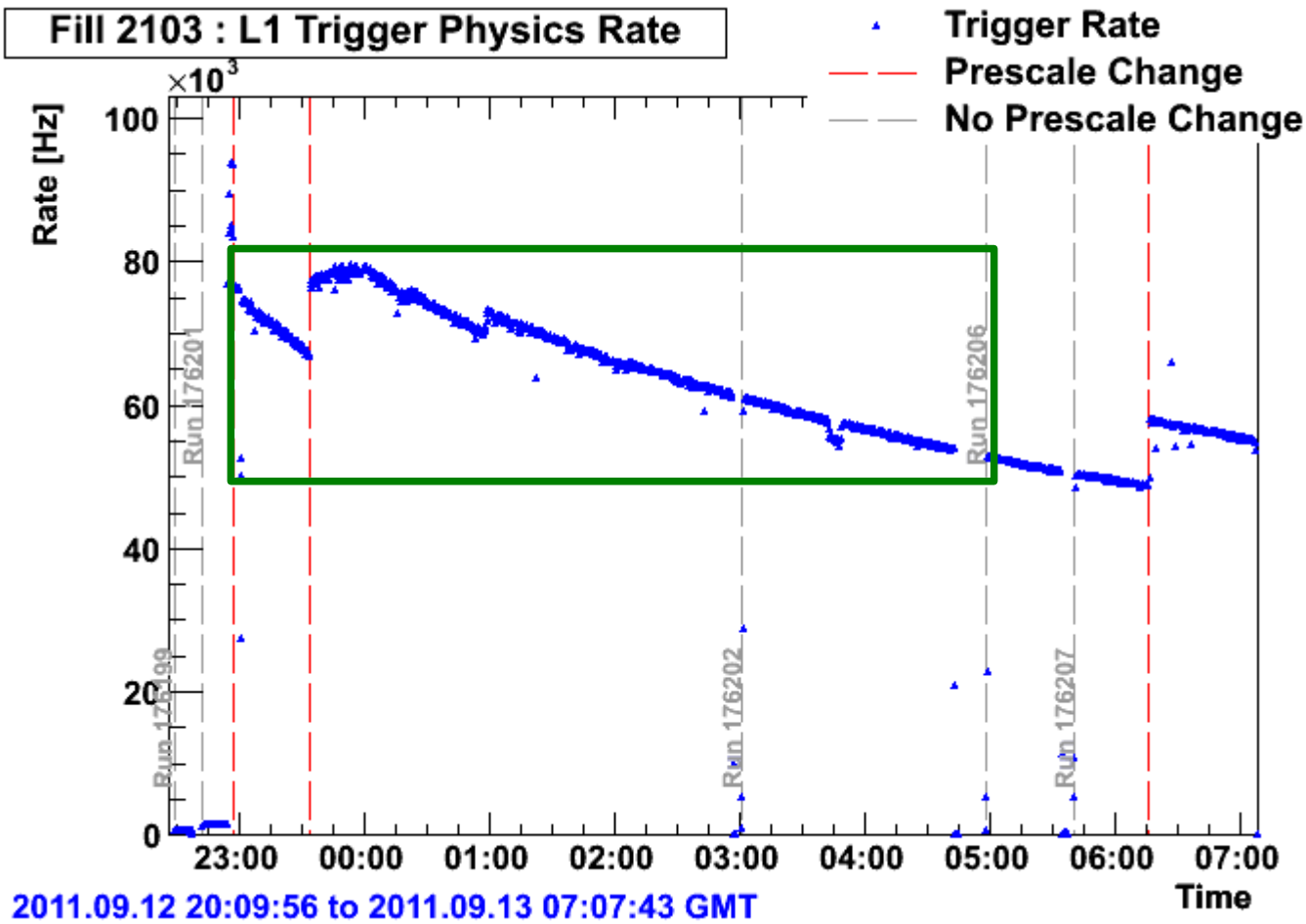
Fill 2103 : CMS Pileup Monitor



2011.09.12 20:09:56 to 2011.09.13 07:07:43 GMT

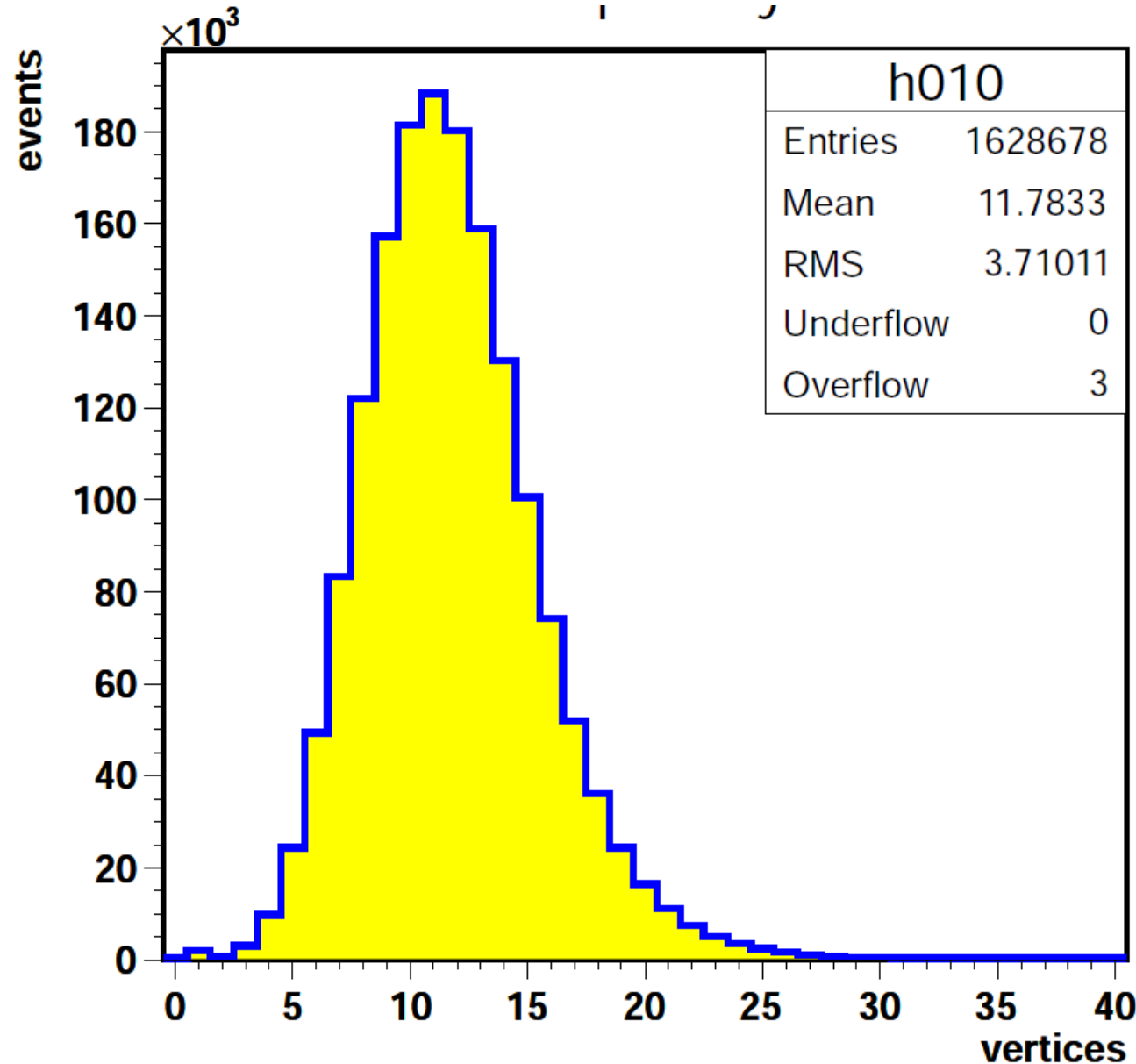
- Example fill 2103:
 - ▶ initial pile up 15.5
 - ▶ initial period down to pile up 10 used here.

CMS L1 trigger rate



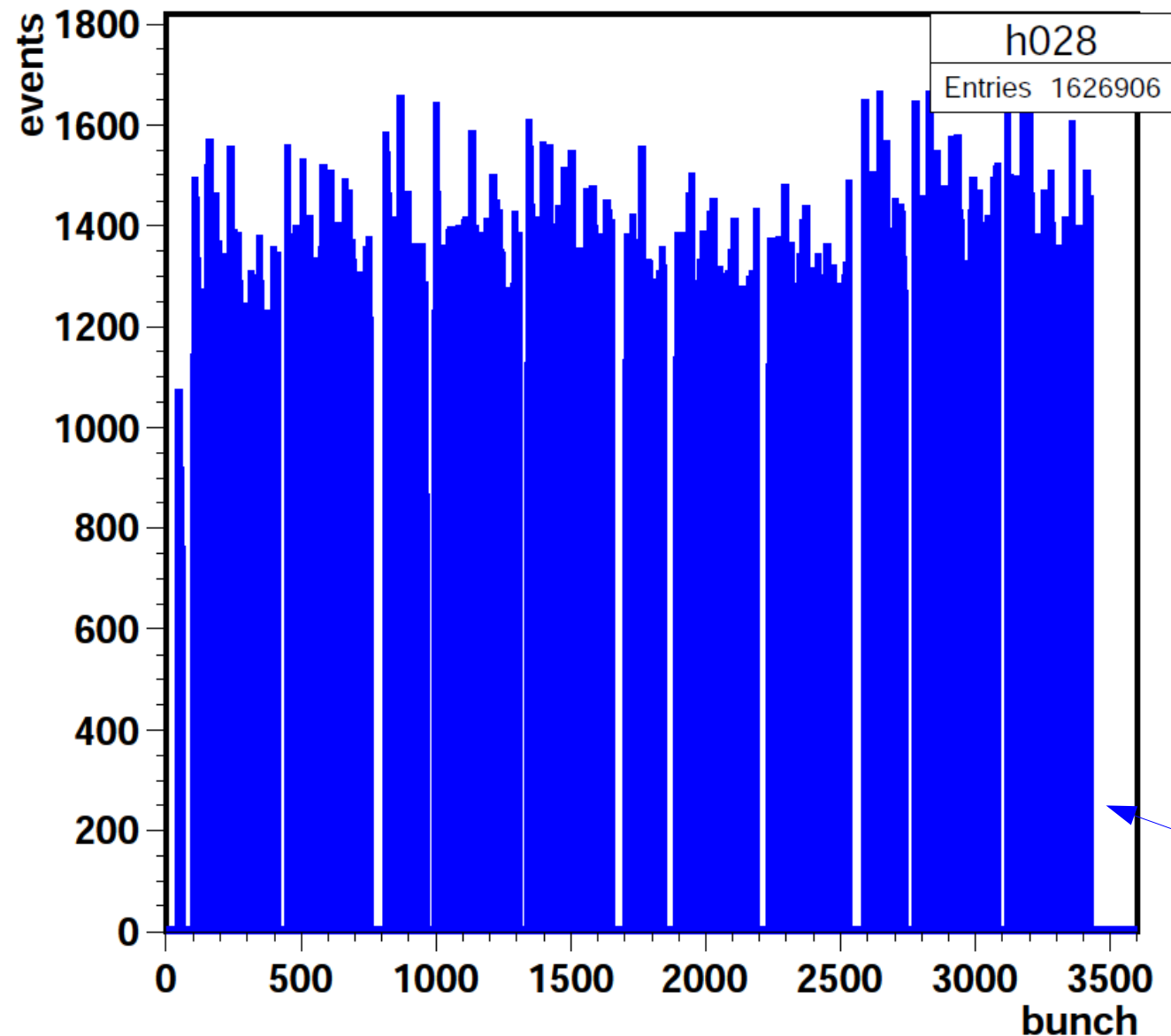
- Example fill 2103:
 - ▶ L1 trigger rate 80..50 kHz.
 - ▶ initial 2 runs in this fill used here.

pile up vertices



- Mean number of CMS reconstructed vertices in this sample is 11.8

Bunch pattern fill 1718

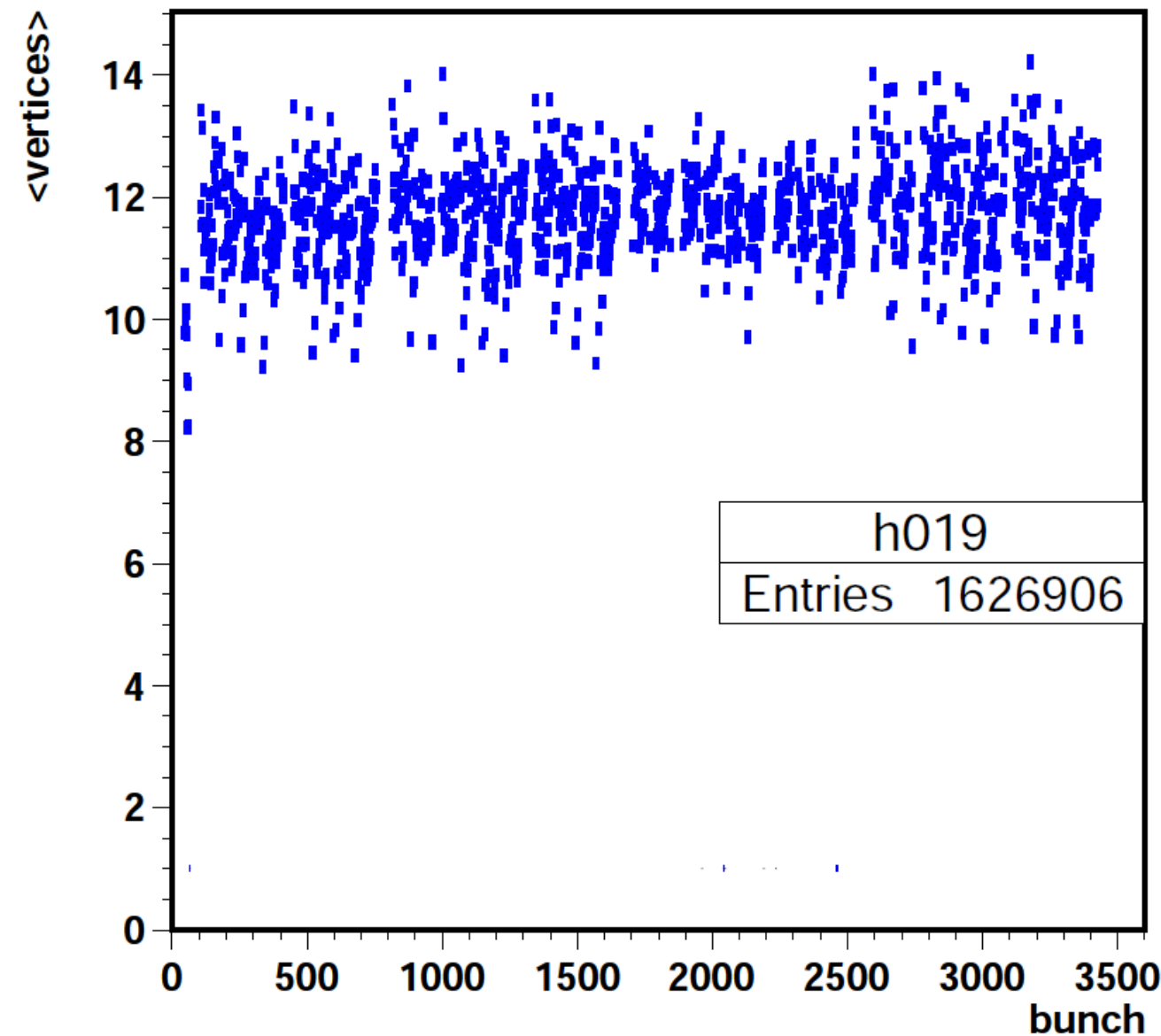


- LHC:
 - 26'659 m
 - 89 us / turn
 - space for 3564 bunches at 25 ns.
- Sep 2011:
 - kicker gap at end of fill pattern:
 - last filled bunch 3426
 - first filled bunch 45
 - **gap: 182 bunches = 4.5 μ s.**

50ns_1380b+1small_1318_39_1296_144bpi13inj.txt

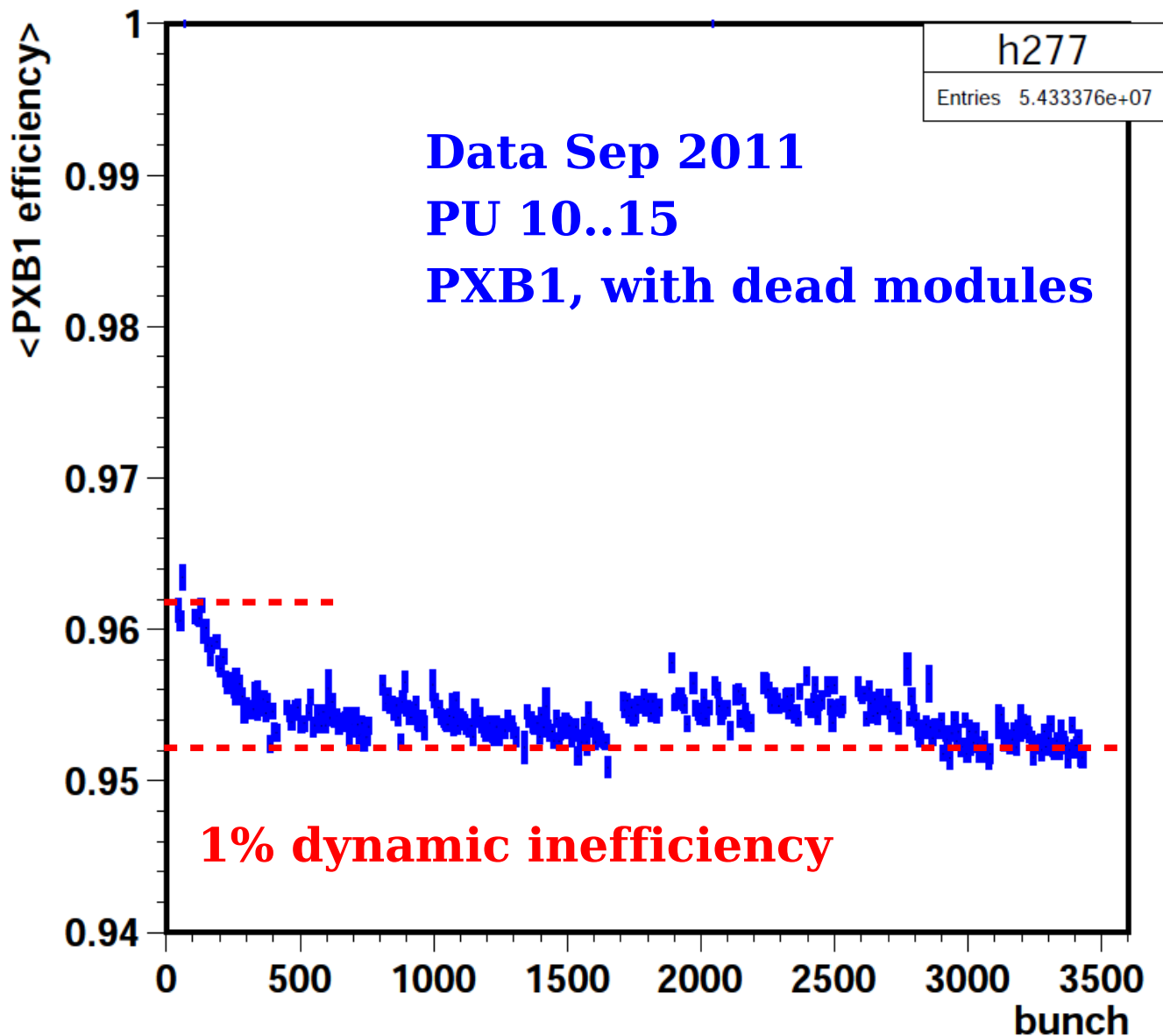
<http://lpc.web.cern.ch/lpc/fillingschemes.htm>

pile up per bunch



- mean number of primary vertices per bunch.
- early parts of Sep 2011 lumi fills.
- Variation from 9 to 14 on the mean pile up per bunch.

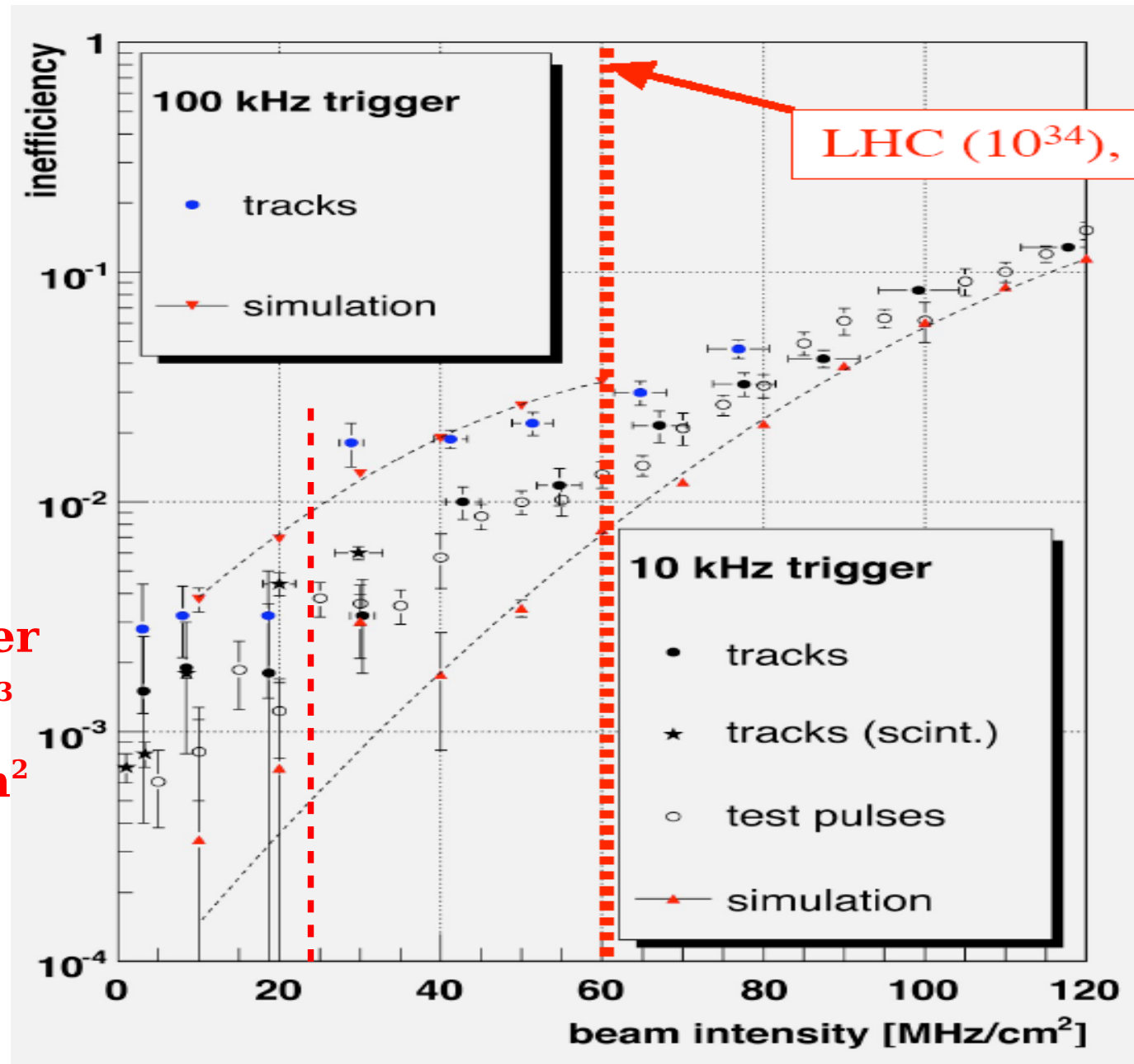
Pixel barrel layer 1 efficiency



- Efficiency = (tracks with hit in PXB1) / (tracks through PXB1 - z-gaps)
 - z-gaps taken out,
 - dead or bad modules **not taken out.**
- Mu sample, PromptReco, AOD.
- $p_t > 0.75$, primary.
- Peak efficiency 96.2%.
- Dynamic inefficiency -1%.

Pixel ROC inefficiency

Sep 2011
70 kHz trigger
 $L_{\text{avg}} = 2.5 \cdot 10^{33}$
 $\approx 25 \text{ MHz/cm}^2$
at 4.4 cm



PSI high rate test beam 2005

Data loss mechanisms

Present PSI46 readout chip simulated at LHC design luminosity

Pixel busy:

0.04% / 0.08% / 0.21%

pixel insensitive until hit
transferred to data buffer
(column drain mechanism)

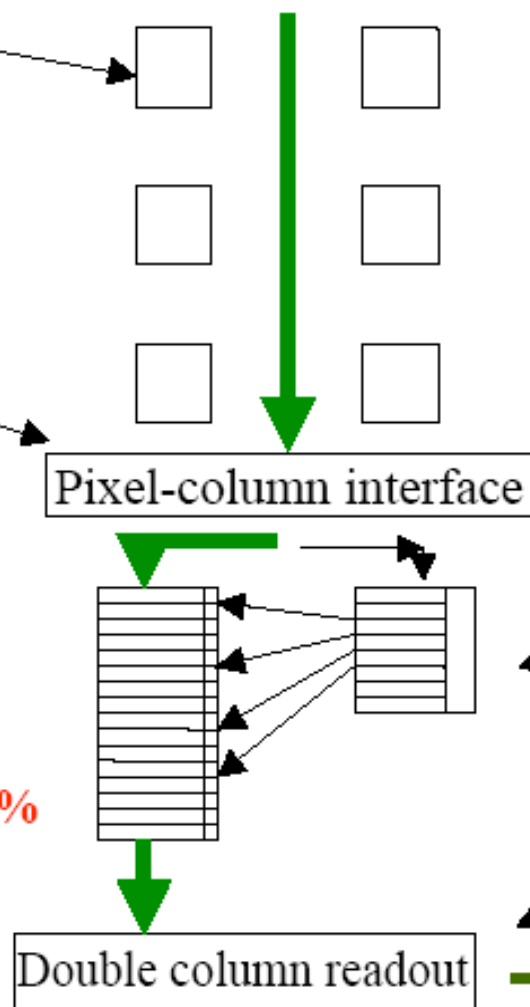
Double column busy:

0.004% / 0.02% / 0.25%

Column drain transfers hits
from pixel to data buffer.
Maximum 3 pending column
drains requests accepted

Data Buffer full:

0.07% / 0.08% / 0.17%



- 1xLHC: $10^{34} \text{cm}^{-2} \text{s}^{-1}$
- 11 cm / 7 cm / 4 cm layer
- total data loss @ 100kHz L1A:
 - 0.8%
 - 1.2%
 - 3.8%

Timestamp Buffer full:

0 / 0.001% / 0.17%

Readout and double column reset:

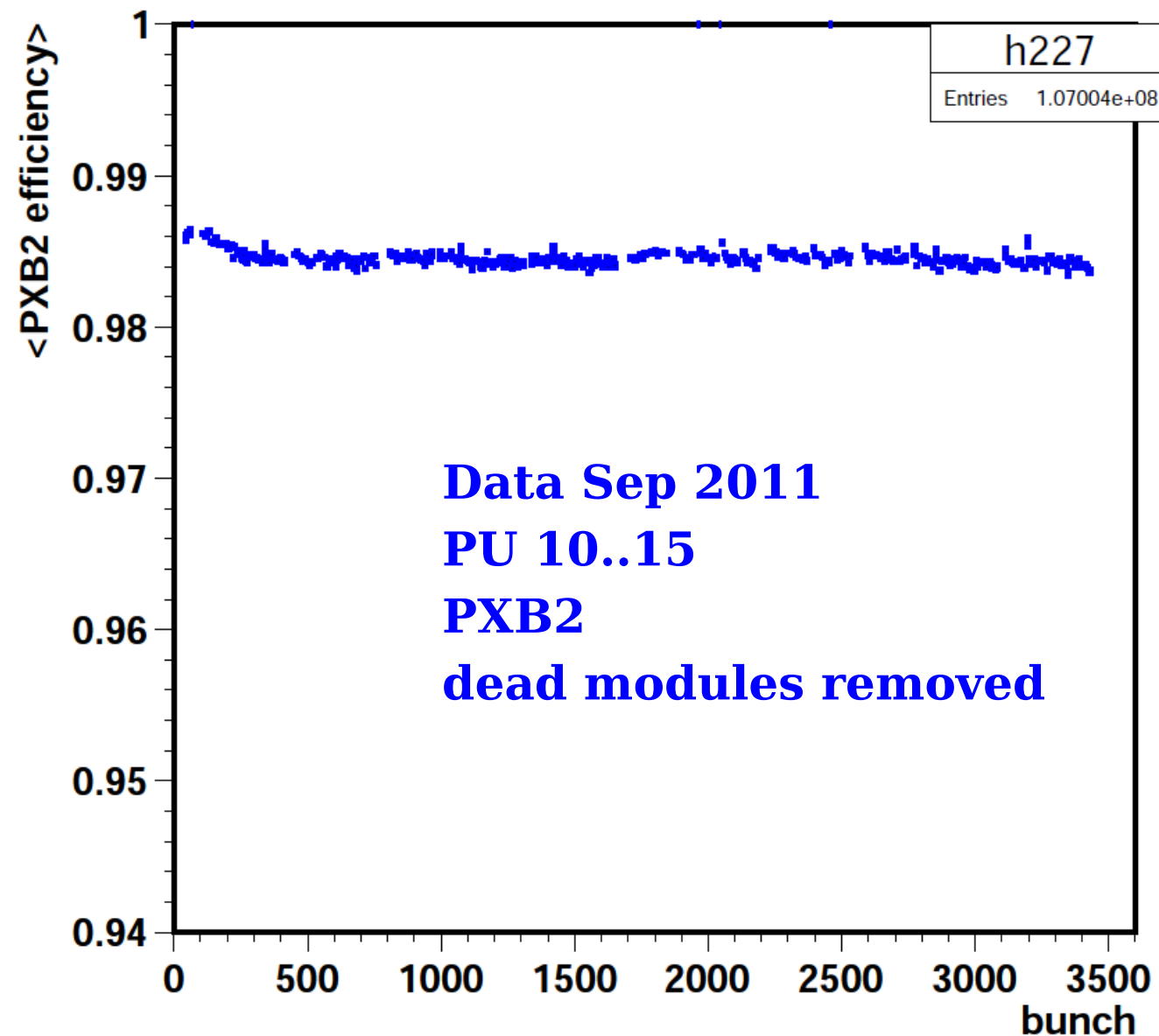
0.7% / 1% / 3.0%

for 100kHz L1 trigger rate

H.C. Kaestli, CMS Tracker upgrade workshop Feb 2007

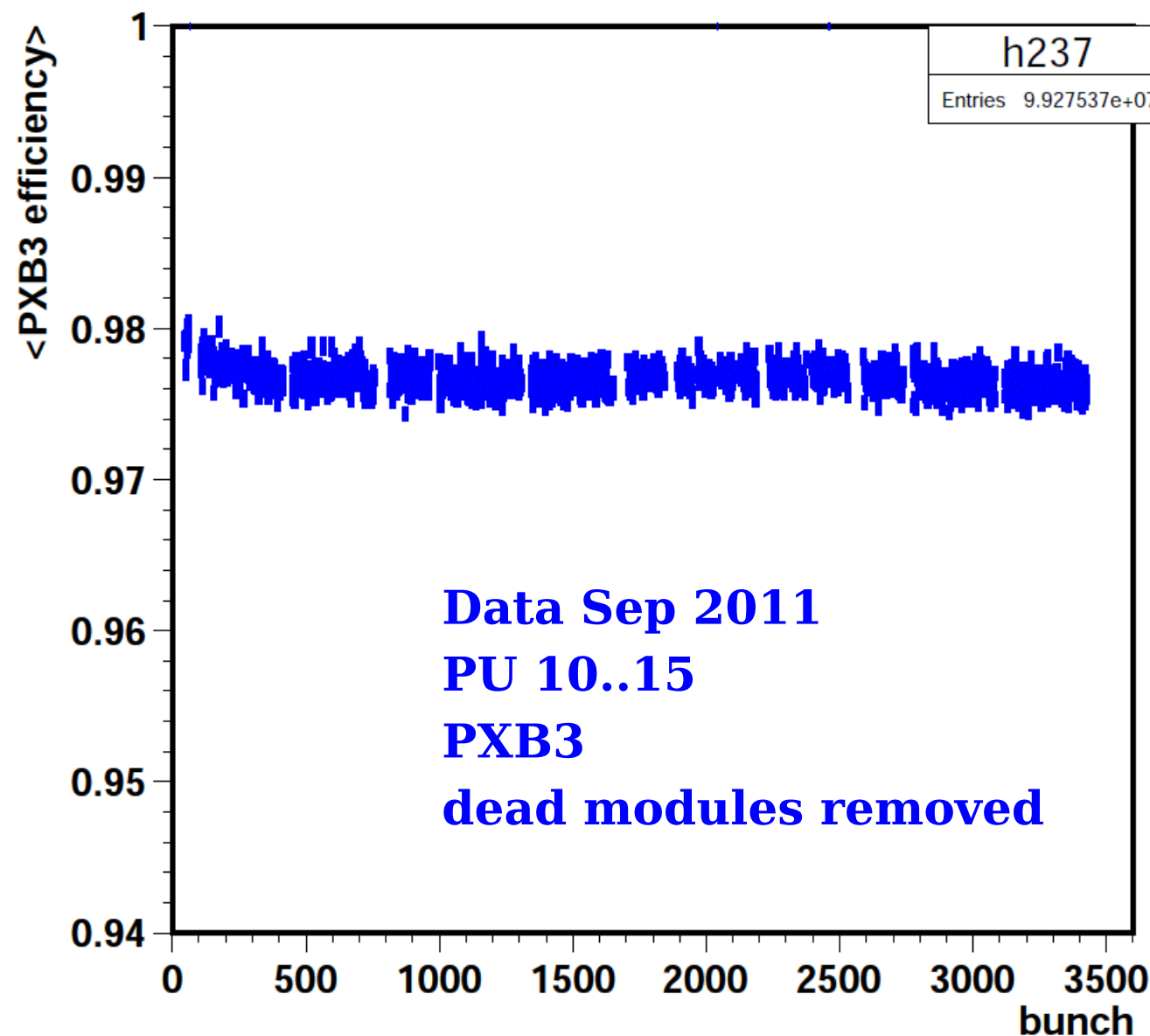
<http://indico.cern.ch/conferenceDisplay.py?confId=12094>

Pixel barrel layer 2 efficiency



- Efficiency = (tracks with hit in PXB2) / (tracks through PXB2 - z-gaps - dead modules)
 - z-gaps taken out,
 - dead or bad modules **are taken out.**
- Hit in PXB1 required.
- SingleMu sample, PromptReco, AOD.
- Top efficiency is 98.6%.
- Dynamic inefficiency: about -0.2%.

Pixel barrel layer 3 efficiency



- Efficiency as for layer 2
 - z -gaps taken out
 - **known** dead or bad modules **are taken out**.
- Hit in PXB1 or PXB2 required.
- Mean efficiency is 98.7%.
- Dynamic degradation: at most -0.1%.

Summary

- Dynamic inefficiency in PXB1 at $2.5 \cdot 10^{33}$ ($\langle \text{PU} \rangle 12$) is about -1%
- Similar studies on March 2011 data (with PU 5-6) gave -0.5%
- PXB2 dynamic inefficiency is about -0.2 at PU 12.
- Does it agree with simulation?