Pixel threshold trimming

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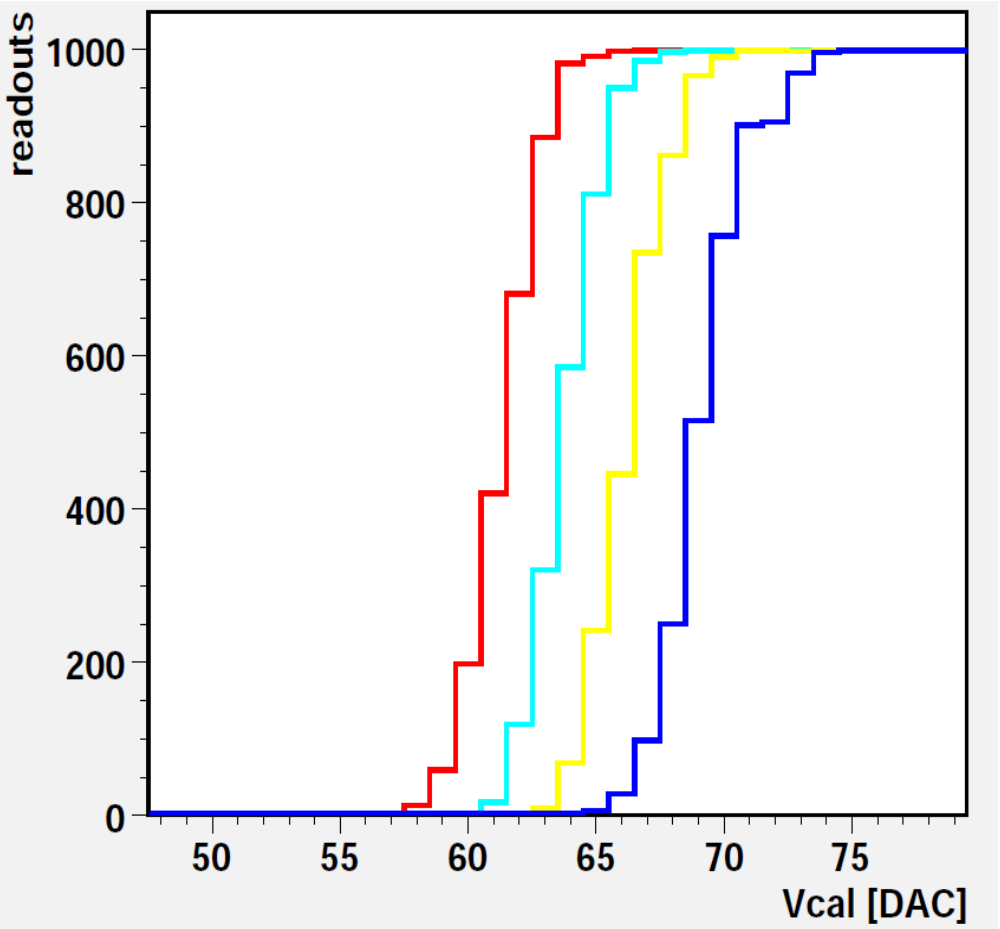
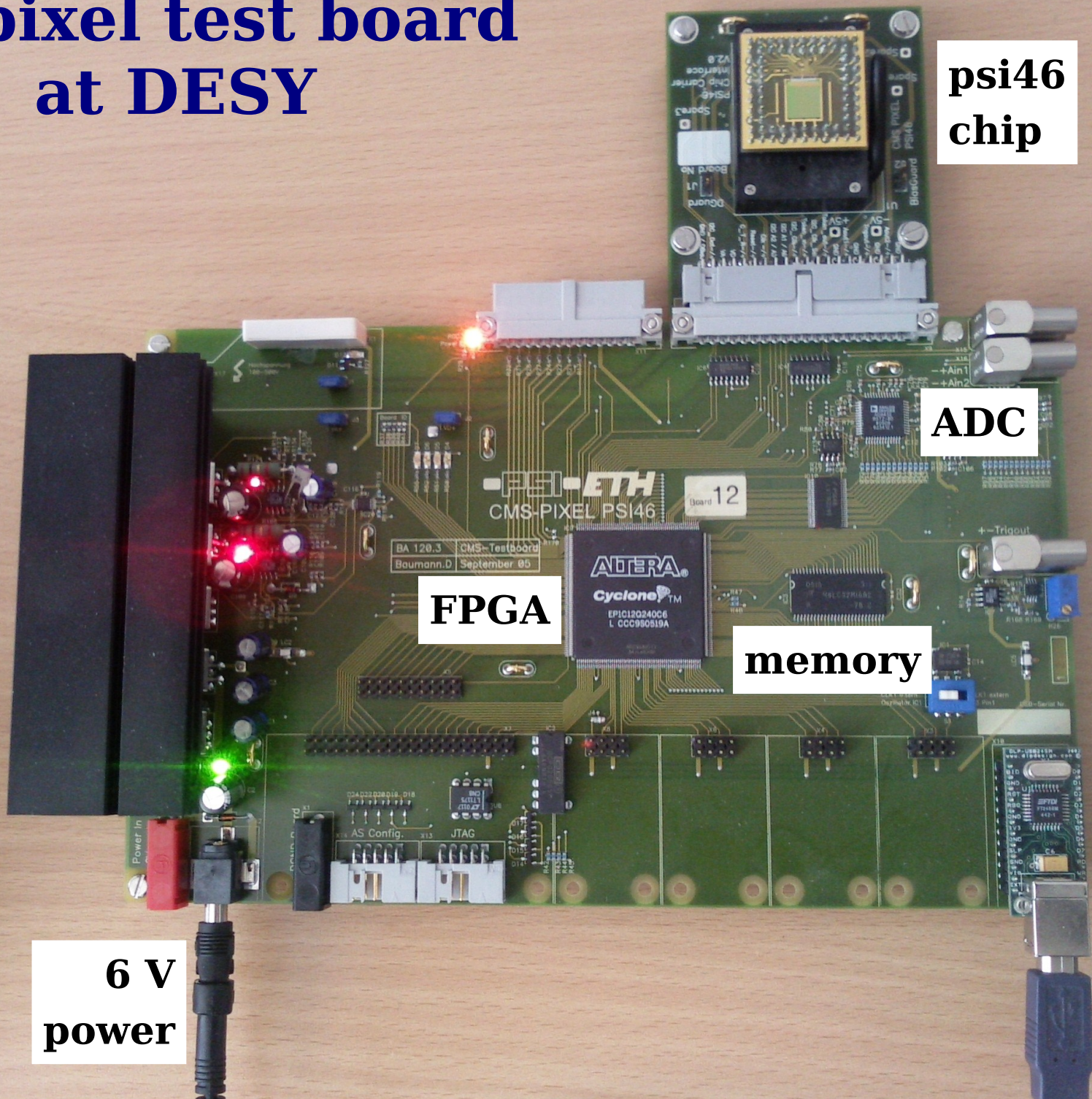
CMS Tracker Upgrade 23.9.2011

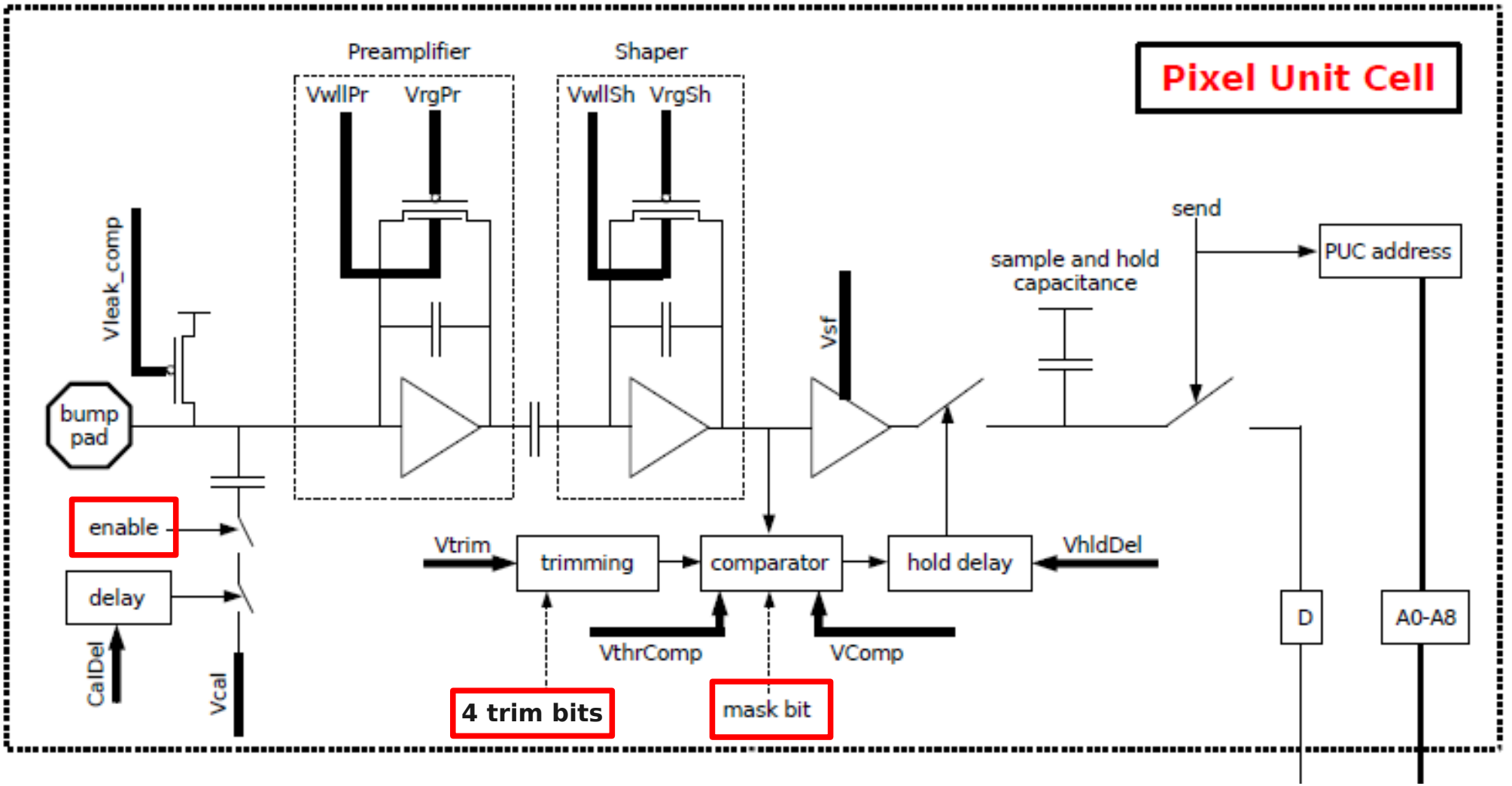


- trimming
- threshold
- noise
- gain results
- GUI

PSI pixel test board at DESY



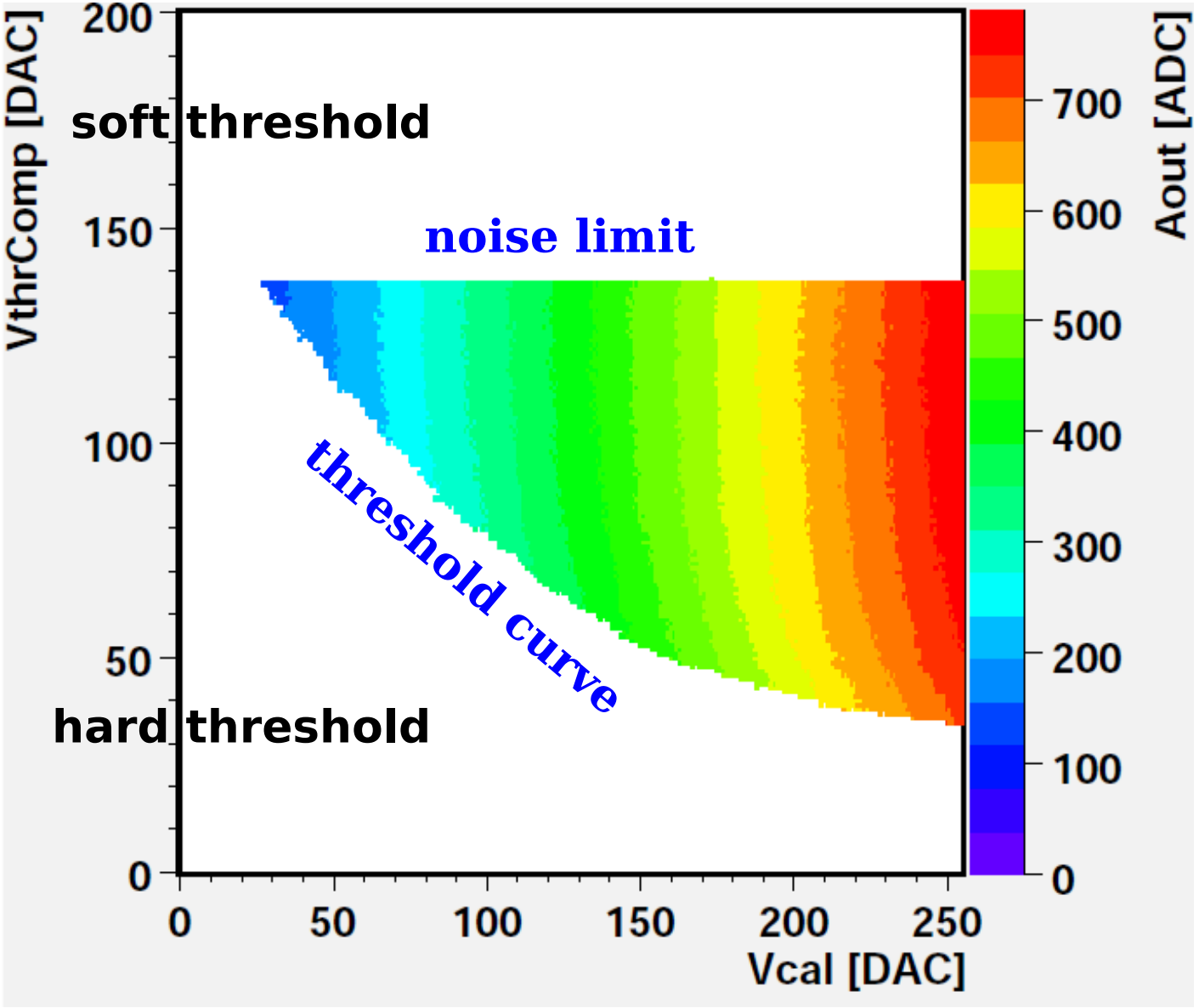
psi46 pixel readout chip



adjustable by programmable DAC, per ROC

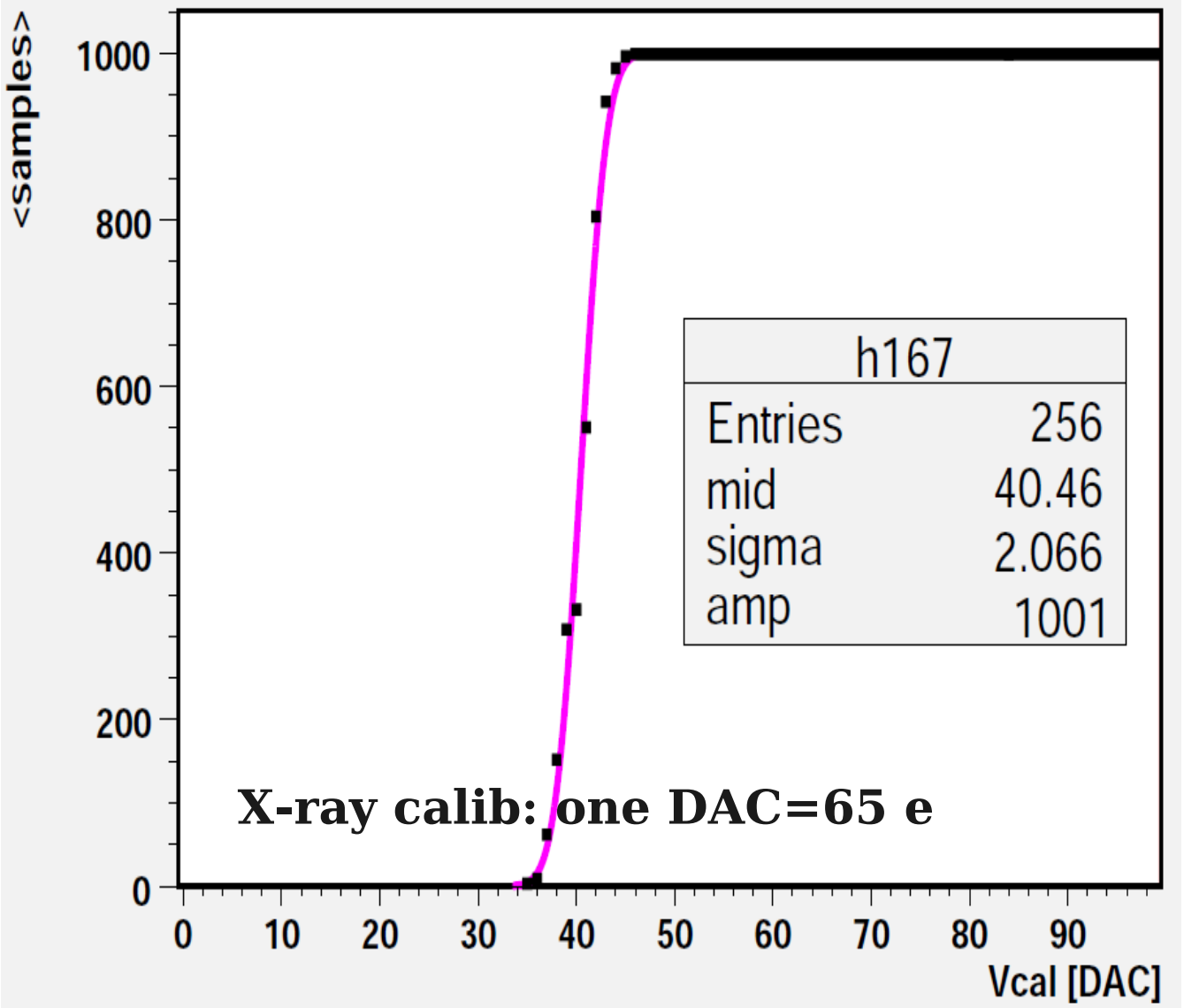
programmable register, per pixel

Comparator threshold



- One pixel
- Analog pulse height vs threshold and calibrate amplitude.
- White region:
  - no signal.
- Colored bands are not vertical:
  - time walk.

Threshold curve



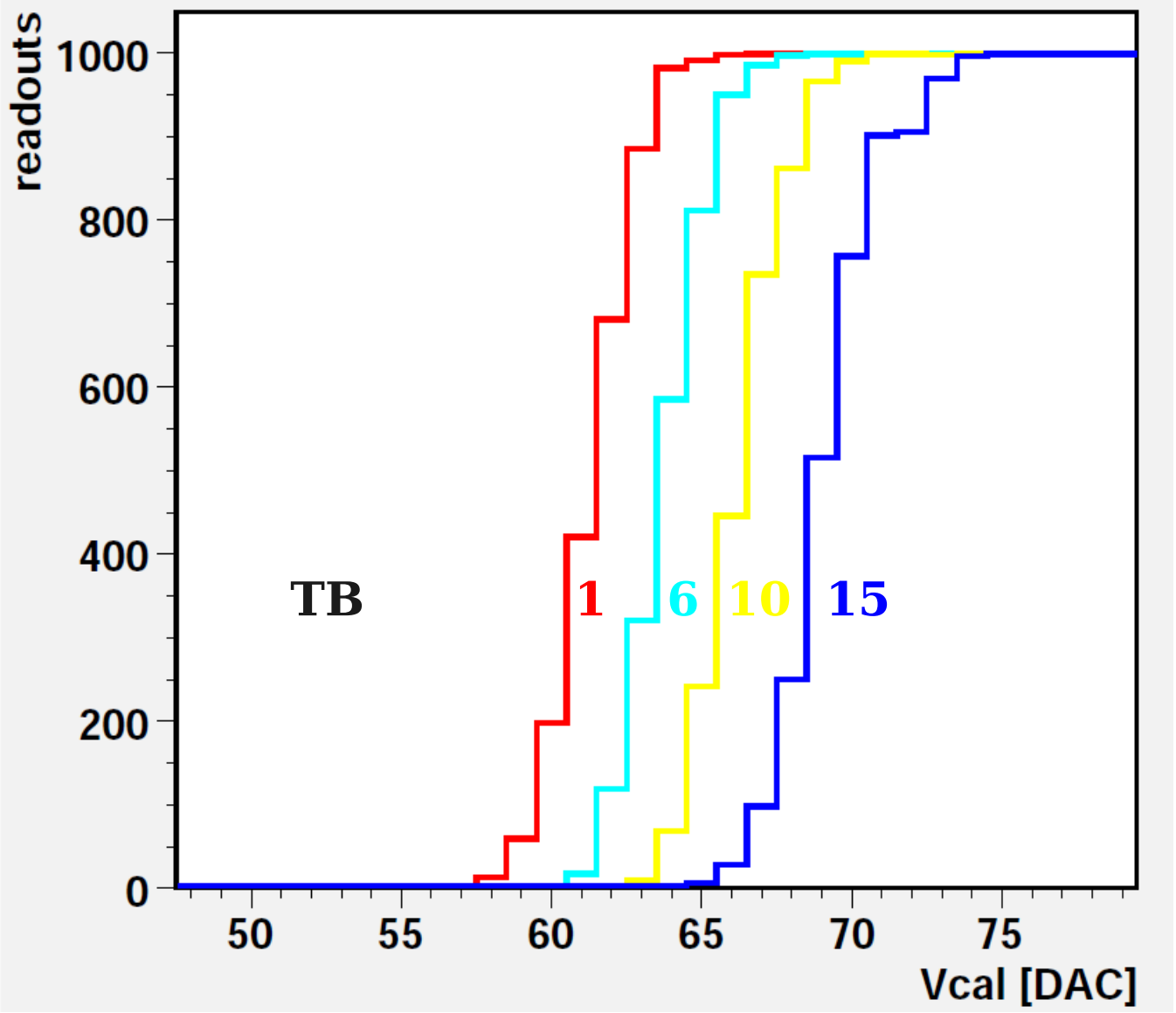
- One pixel.
- Fixed threshold
- Scan Vcal
  - 999 times
- count valid readouts
- threshold curve:
  - error function
  - width = noise
  - noise = 2.1 DAC
  - = 130 electrons.
  - (bare chip without sensor).

Threshold optimization algorithm

- If comparator thresholds are adjusted with global VthrComp only: spread of thresholds in ROC ~309 e^- (PSI value) due to transistor mismatches
- Unify pixel thresholds by 4 trim bits (values from 0 to 15) and scale with Vtrim DAC
- Each trim bit value is set such that Vcal -threshold of the pixel differs least from the selected target threshold in the procedure
- PSI threshold spread reduced to 87 e^- after the optimization (chip with sensor)

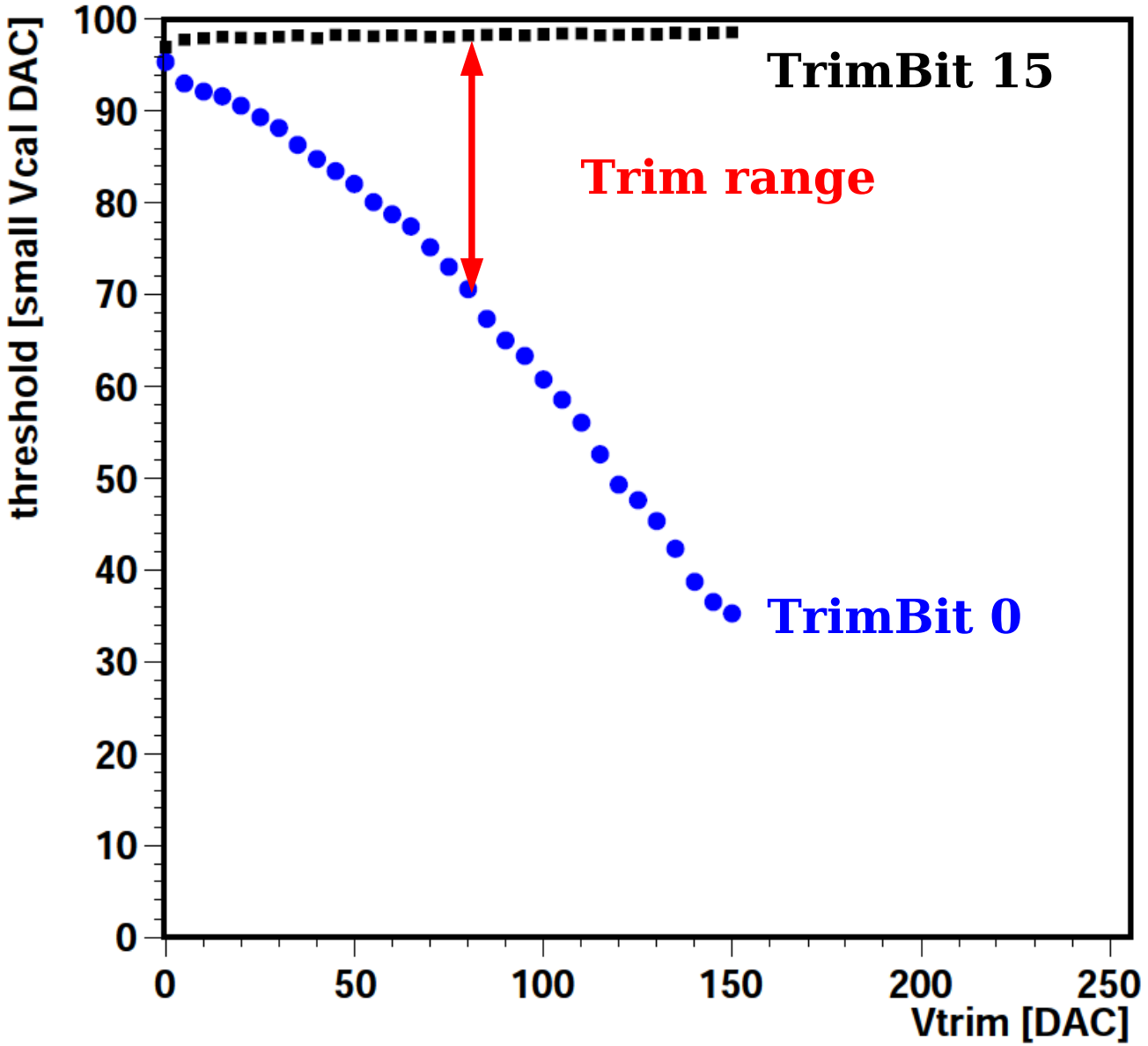
- Works only in Token Bit Manager emulator mode on FPGA

Threshold trimming

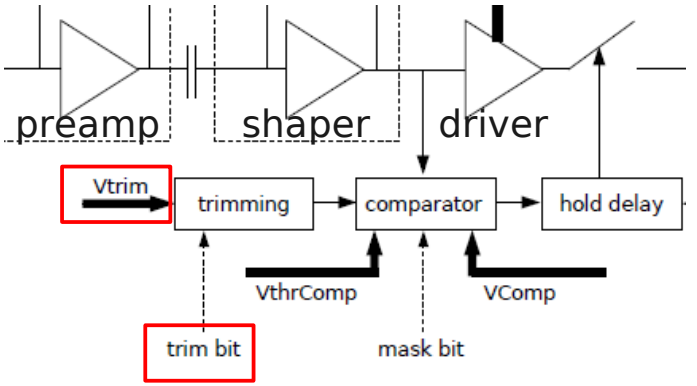


- One pixel.
- Vary trim bits:
  - threshold can be adjusted per pixel.
- Fast method of threshold curve acquisitions (transferring only the number of valid readouts from the FPGA) finally works for us:
  - use TBM emulator mode!

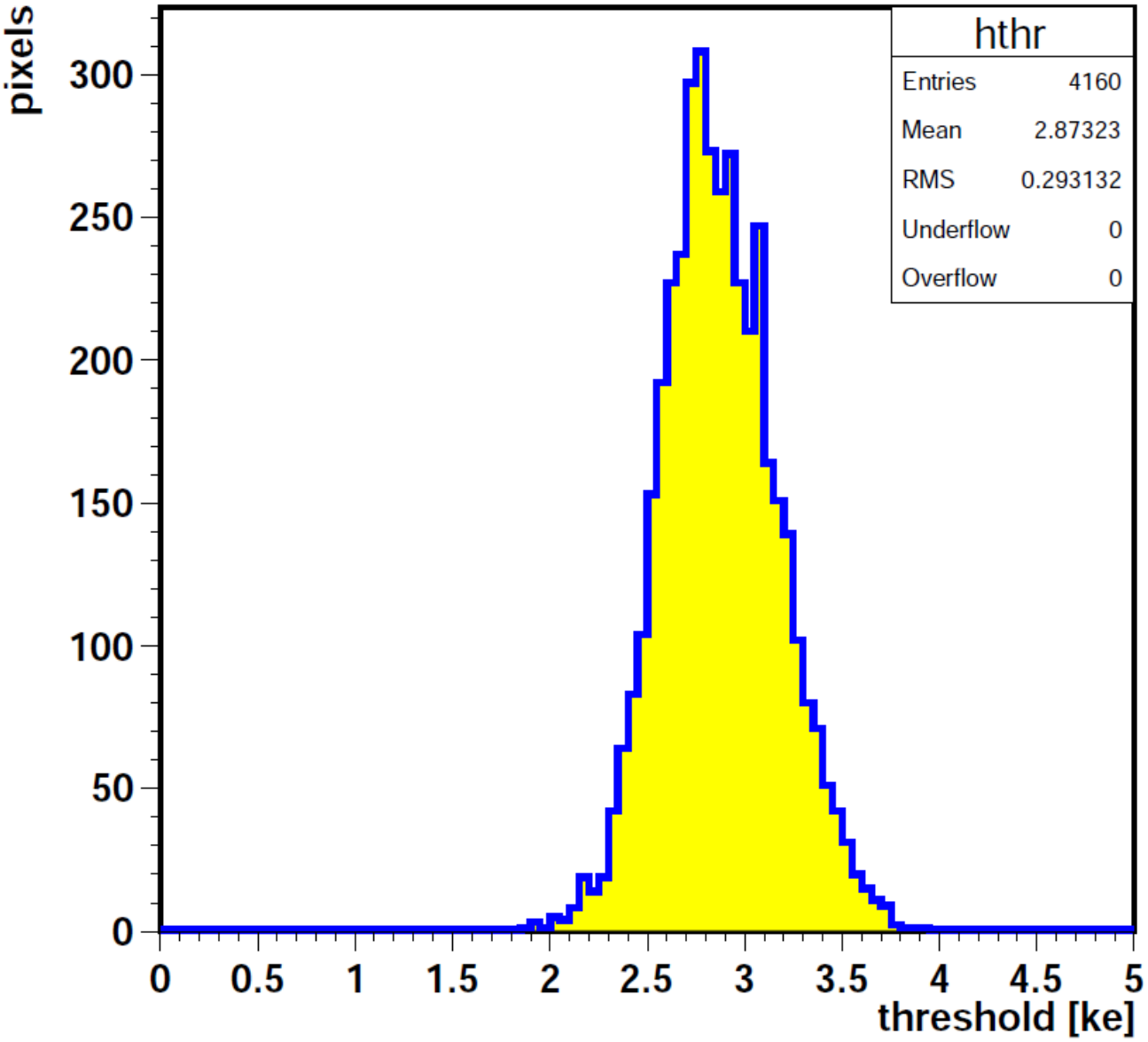
Trim range



- One pixel.
- Vary Vtrim
- TrimBit 15
- TrimBit 0
- 1 Vcal DAC = 65 e

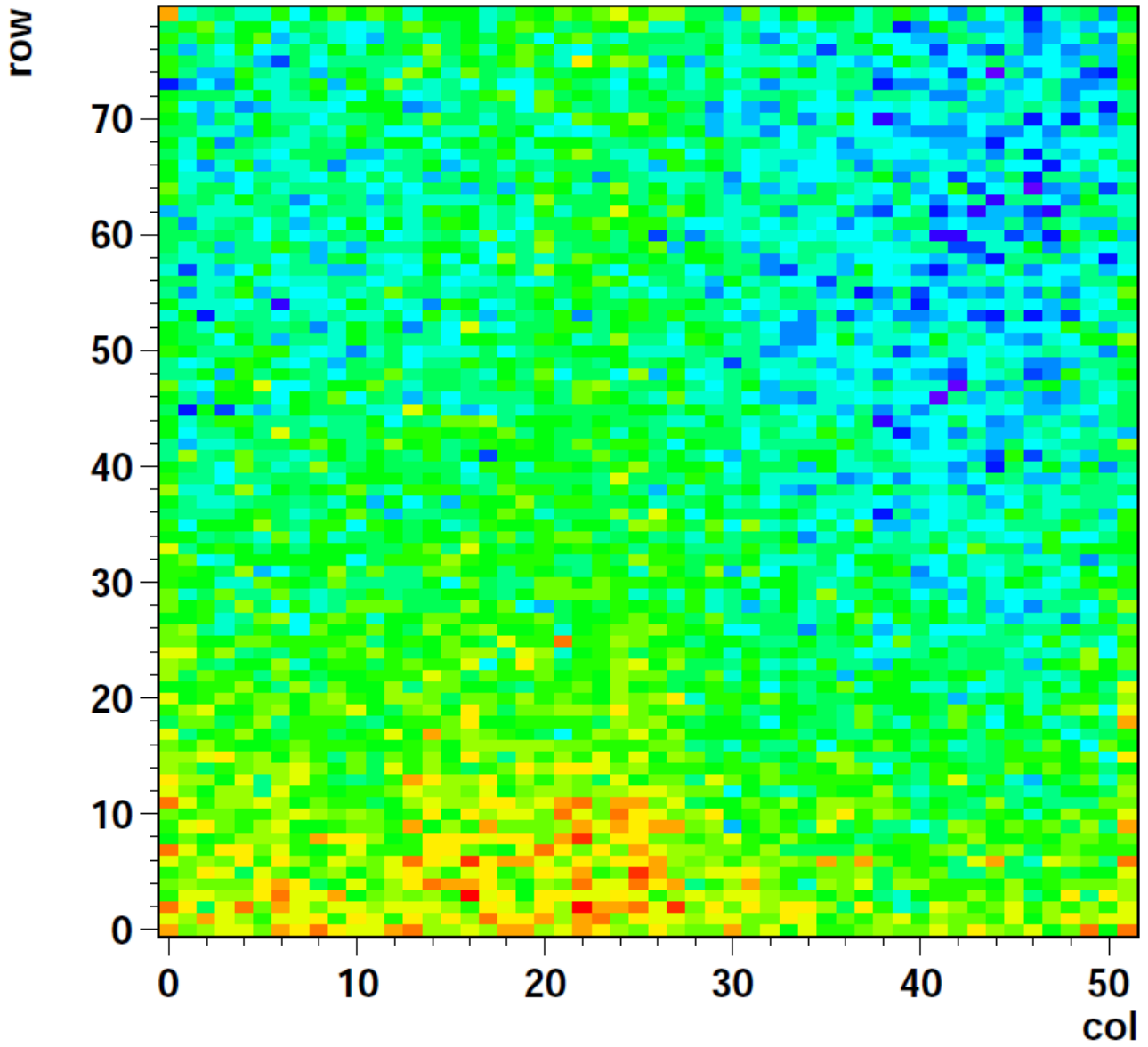


Threshold variation untrimmed



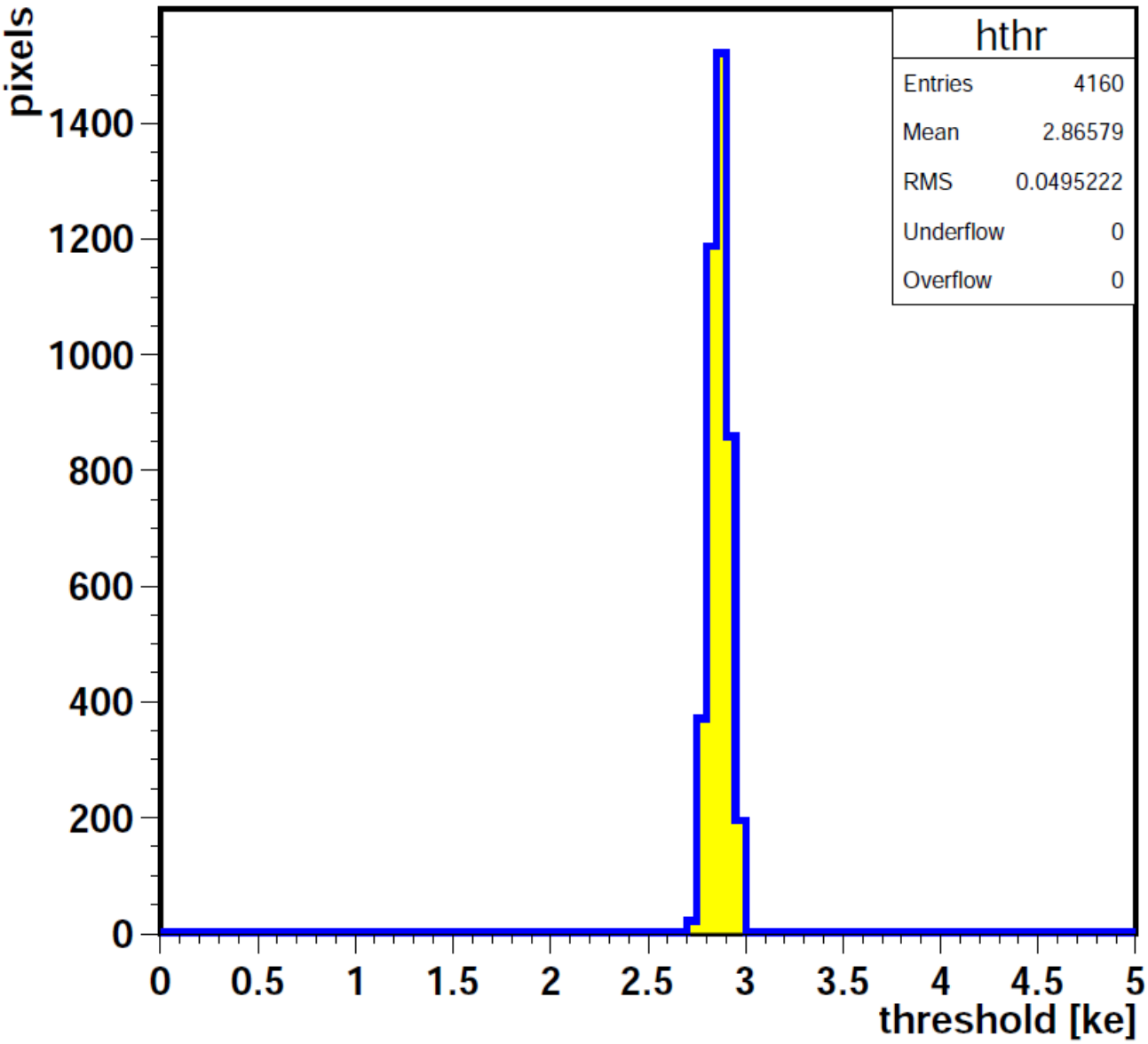
- Chip 0 (no sensor)
- VthrComp 124
-
- 10% spread
- 290 e threshold variation

Threshold variation untrimmed



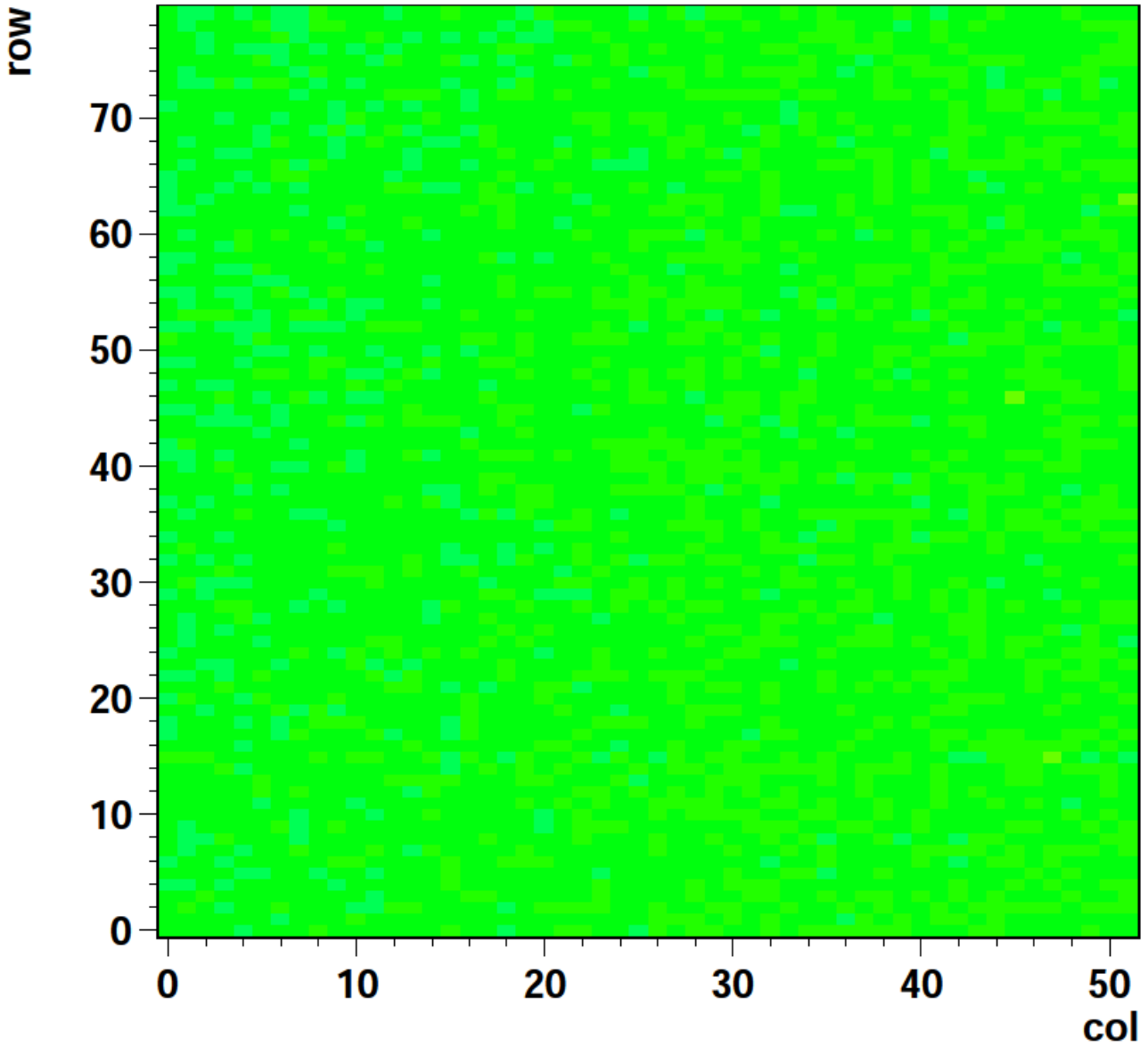
- Vertical scale – threshold in ke
- Chip 0 (no sensor)
- VthrComp 124
-
- 10% spread
-

Threshold variation trimmed



- Chip 0 (no sensor)
- VthrComp 112
- Vtrim 104
- 4160 TrimBits set.
- time: 3 min / chip
- 1.7% spread
- 50 e threshold variation!
-

Threshold variation trimmed



- Chip 0 (no sensor)
- VthrComp 112
- Vtrim 104
- 4160 TrimBits set.
- time: 3 min / chip
- 1.7% spread
- 50 e threshold variation!
-

Towards the minimum TrimVcal

Use as low as possible target Vcal: good charge sharing, good for radiated chip with low charges.

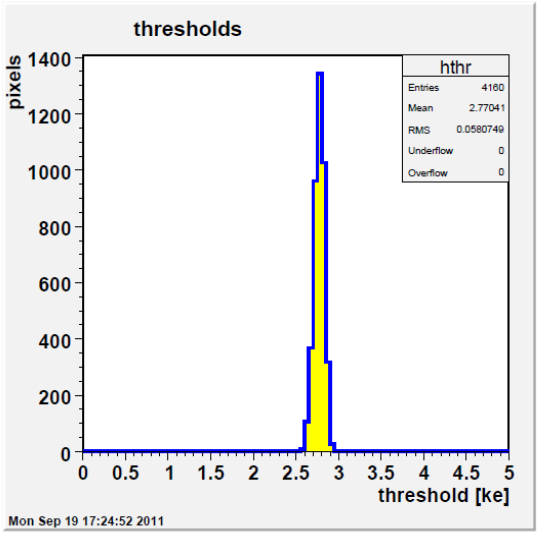
Observation at lowest Vcal: initially many pixels out of threshold range.

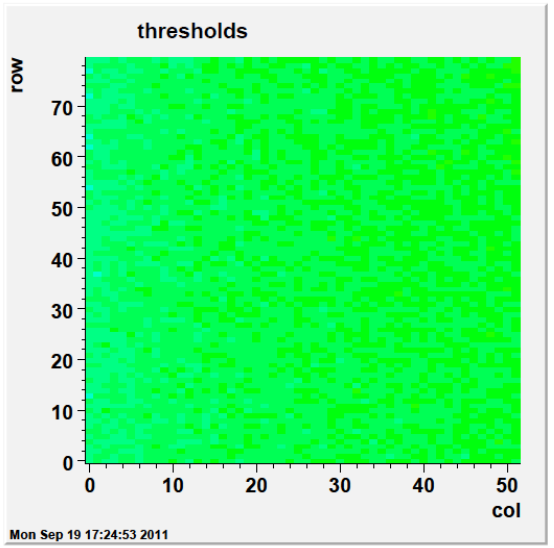
Chip2 (no sensor):

Vcal=40	Vcal=36	Vcal=32	Vcal=30	Vcal=28
1 pixel	55 pix.	489 pix.	1000 pix.	1500 pix.

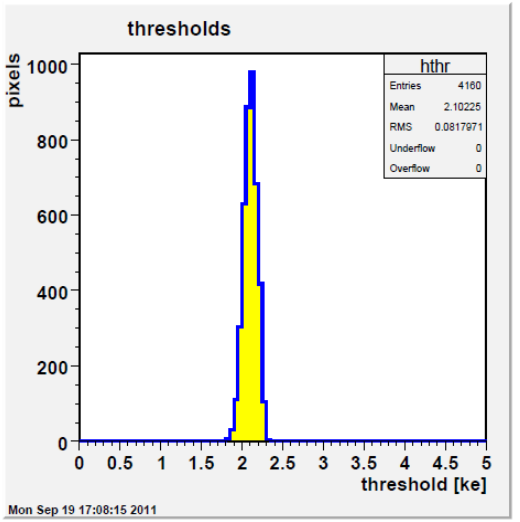
Towards the minimum TrimVcal

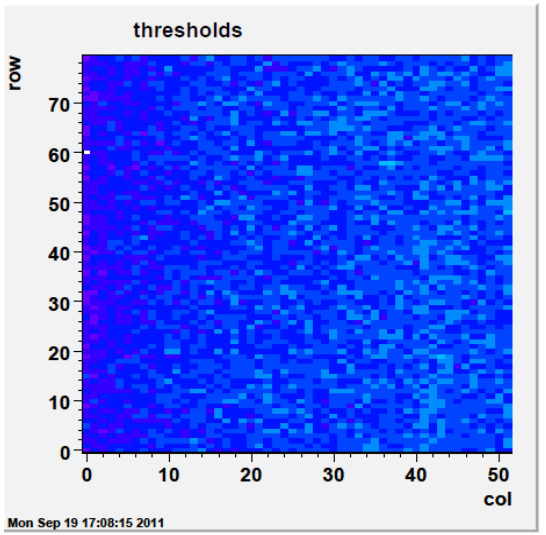
TrimVcal=40



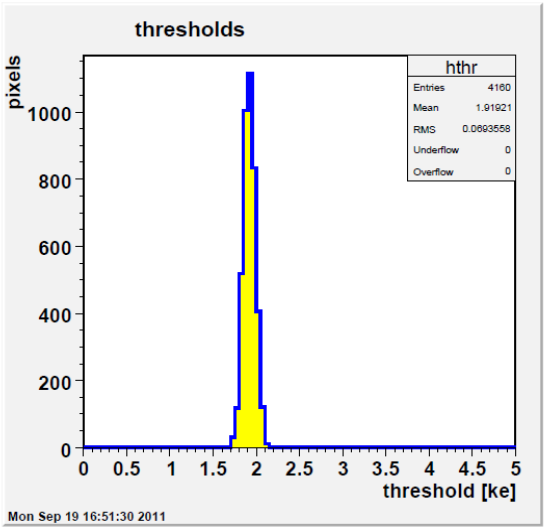


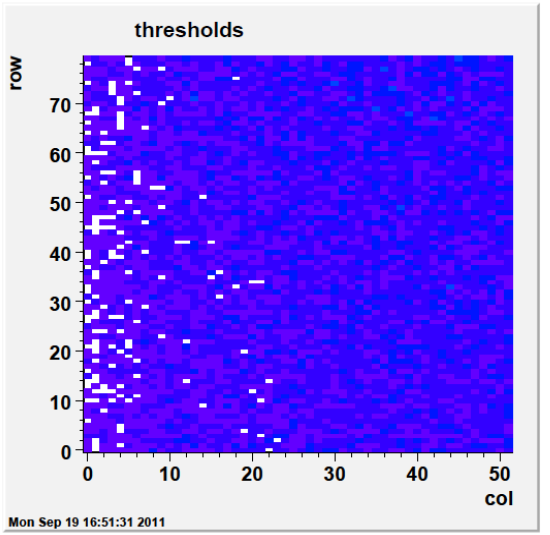
TrimVcal=32





TrimVcal=28

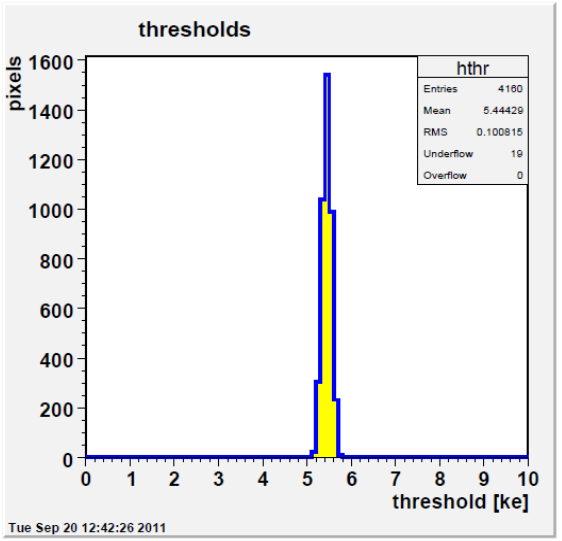


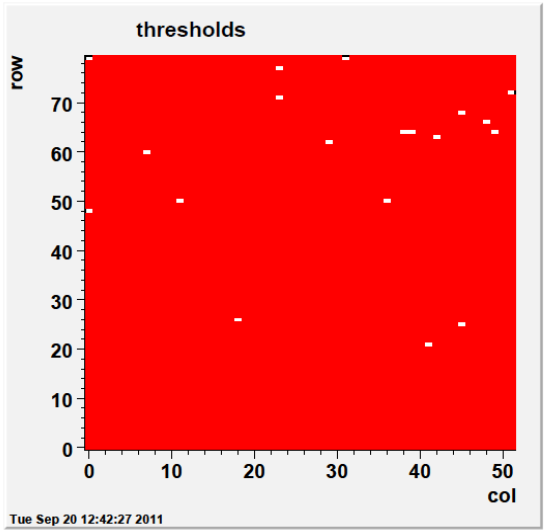


Chip2 (no sensor)

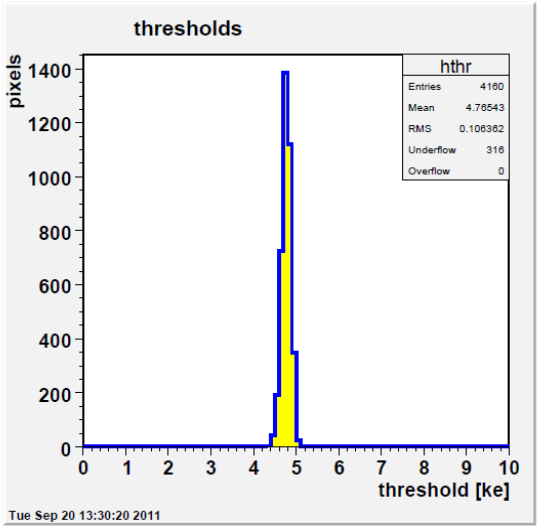
Tests with sensor

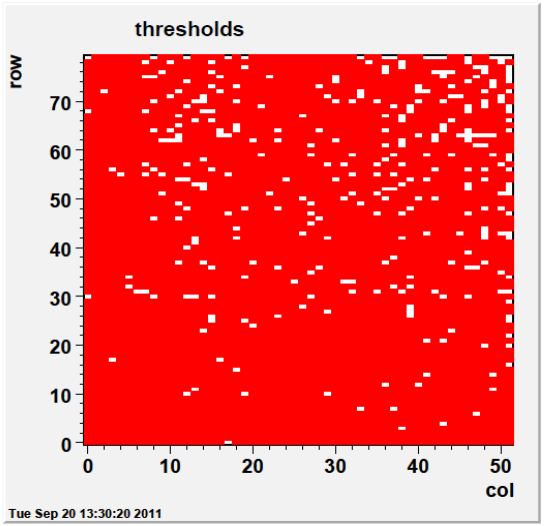
TrimVcal=80



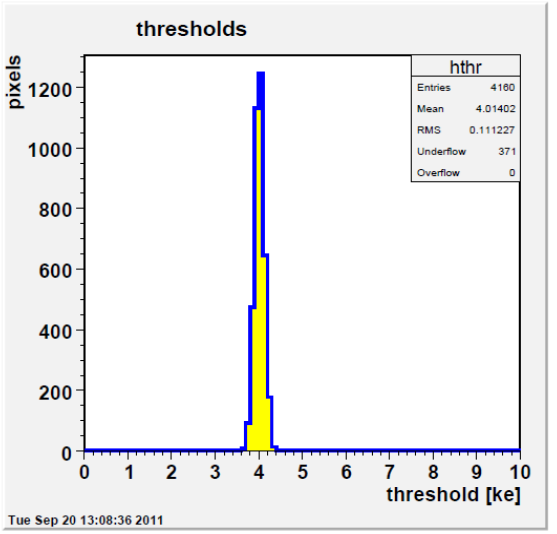


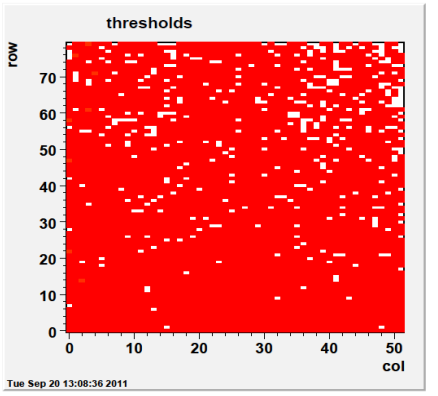
TrimVcal=70

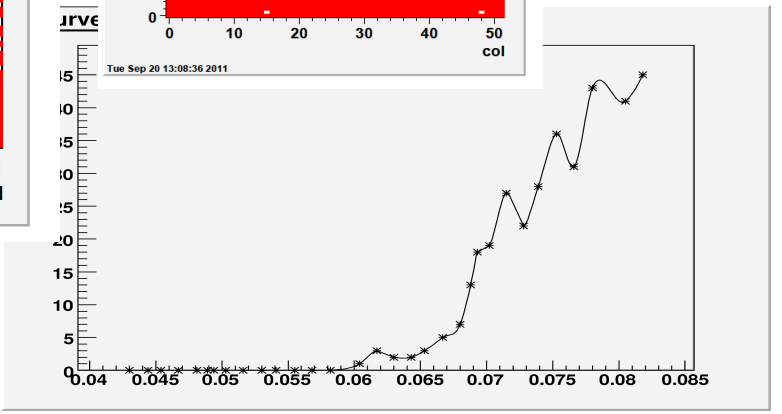




TrimVcal=60





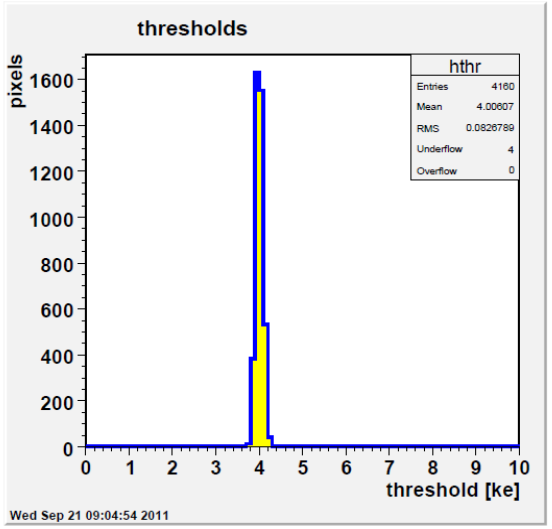


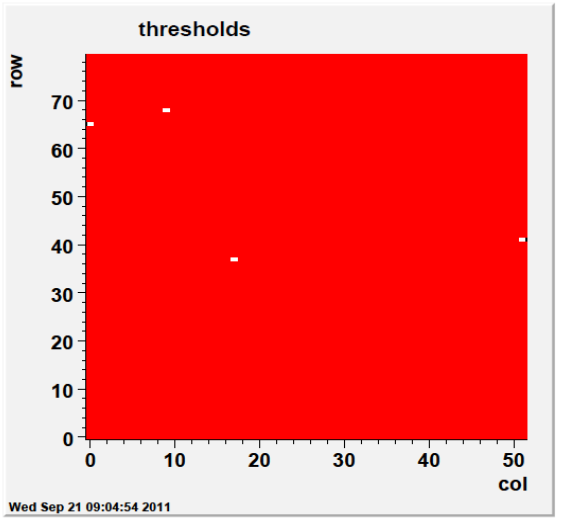
Underflows: bad fit of SCurves

<u>Chip6</u> (with sensor)

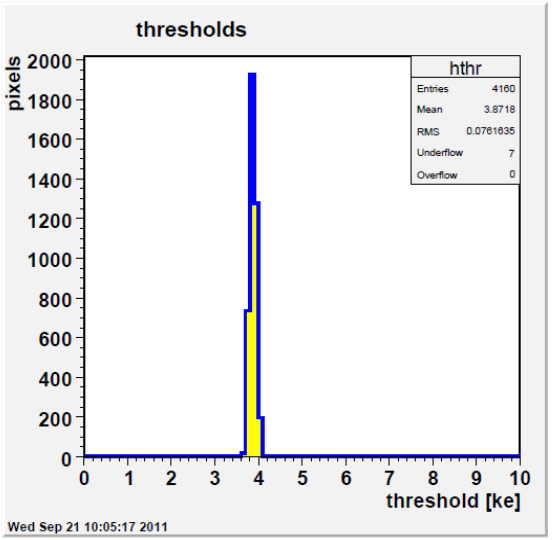
Tests with sensor

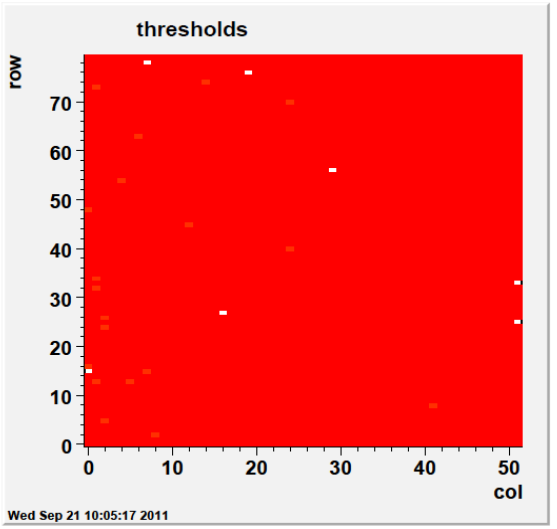
TrimVcal=60



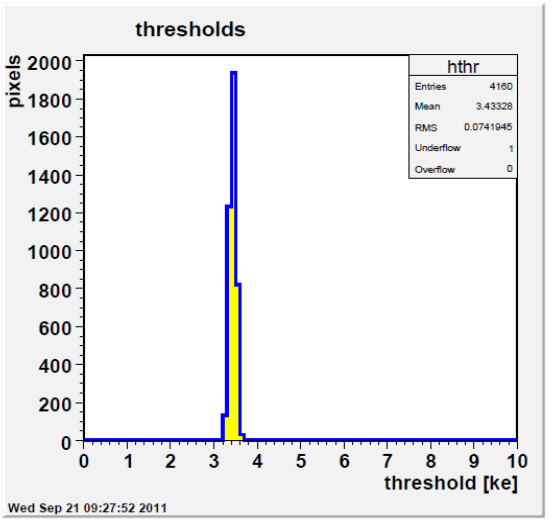


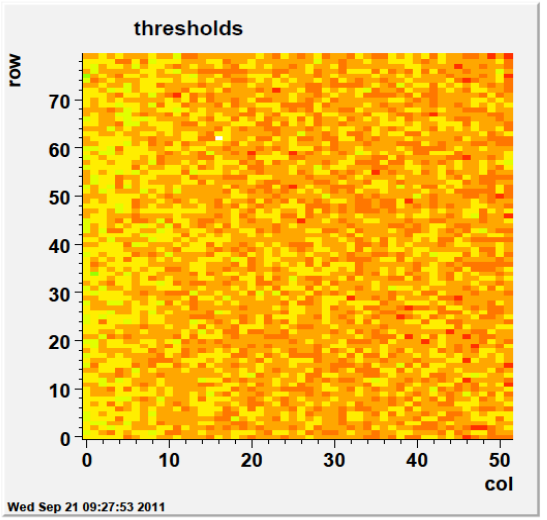
TrimVcal=55





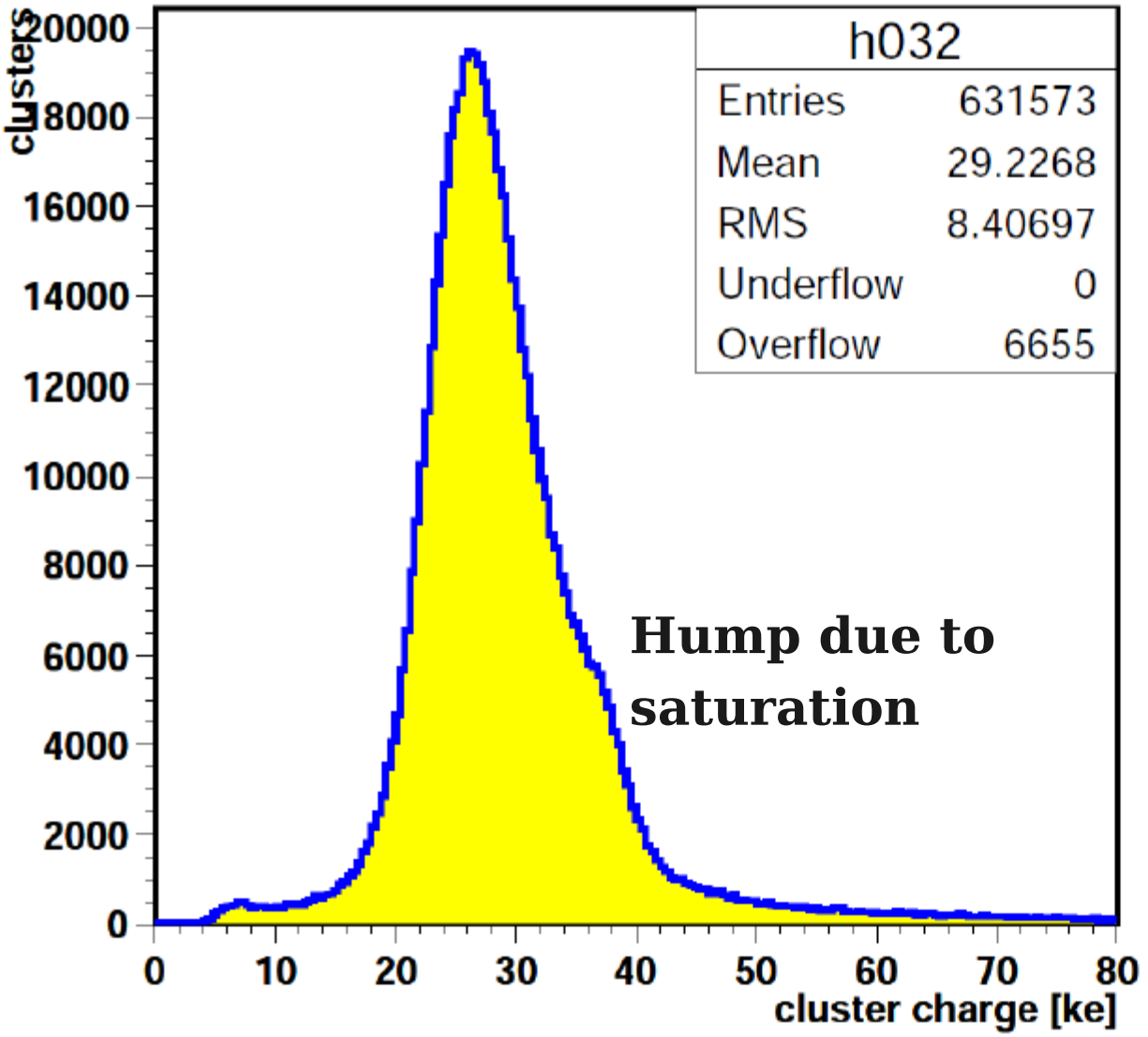
TrimVcal=50





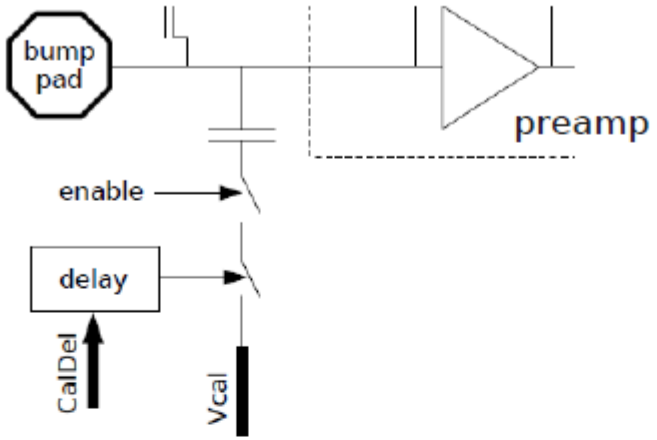
Chip8 (with sensor)

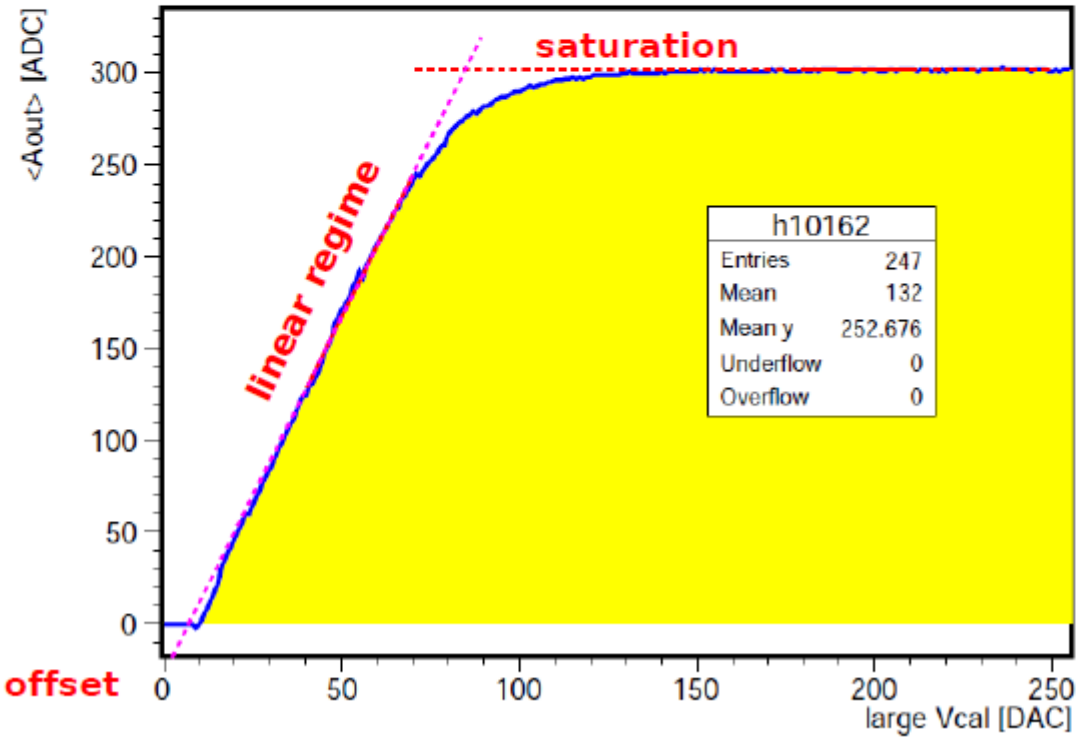
Cluster charge



- 2 GeV e+ test beam.
- Pixel detector at vertical incidence, fully depleted (-90V bias).
- No magnetic field.
- Test pulse gain calibration applied.
- Foot of small pulses:
  - wrong timing?
- Peak at 26 ke, OK for MIPs in 285 µm silicon.
- Hump: saturation.
- Tail: multi-pixel clusters.

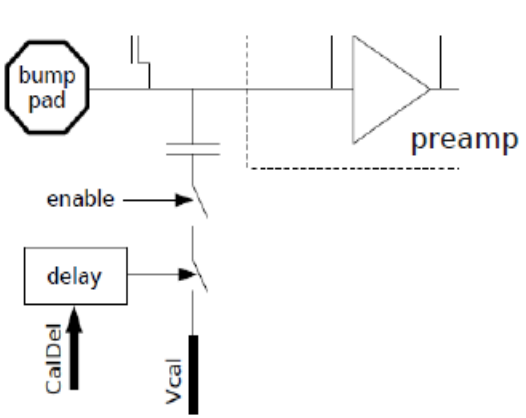
Internal gain calibration

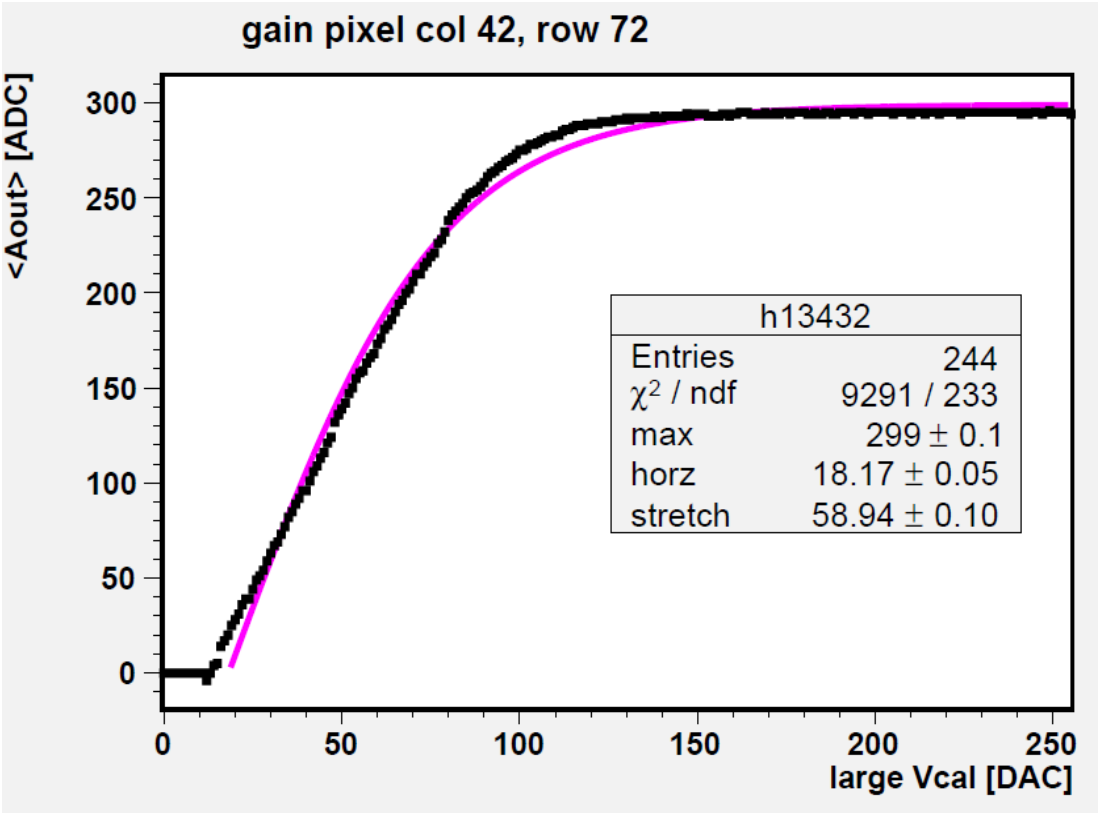




- Scan with internal calibrate pulse
- Linear regime above some threshold:
  - fit gain and offset
- Preamp saturation for large pulses
- Repeat for 4160 pixels

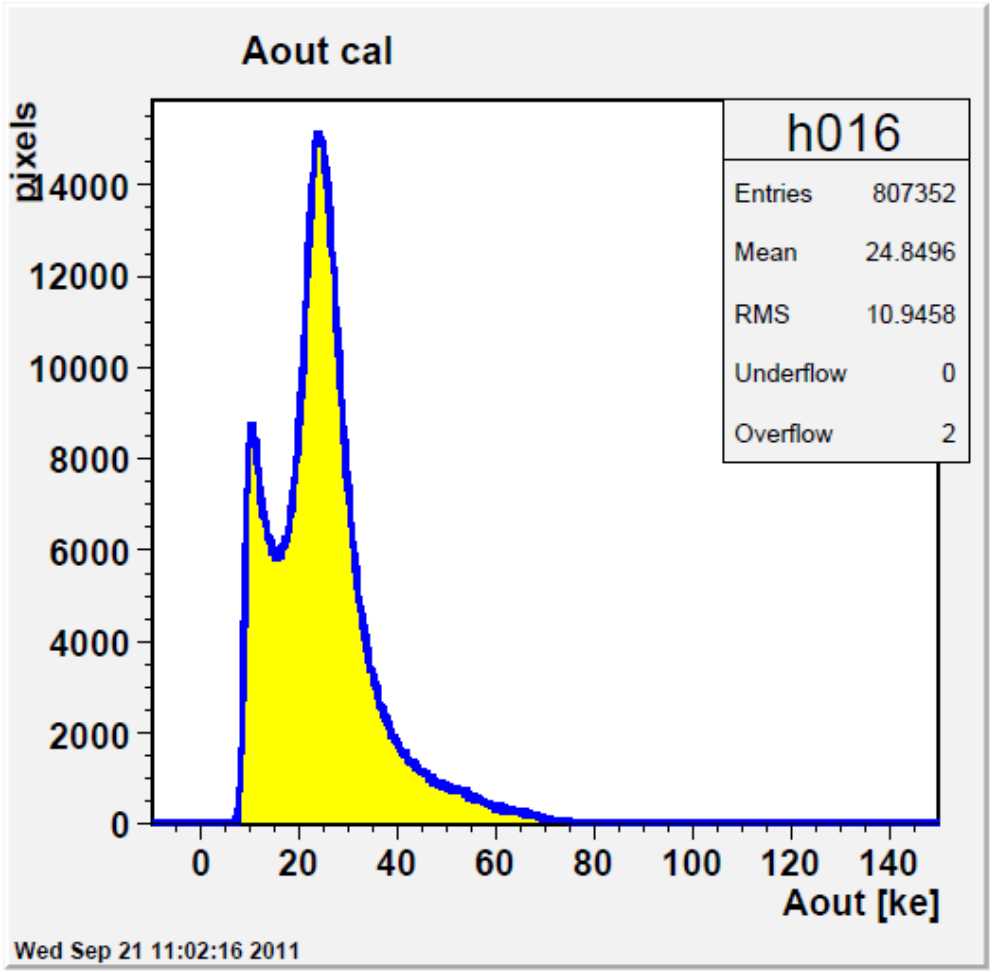
Internal gain calibration





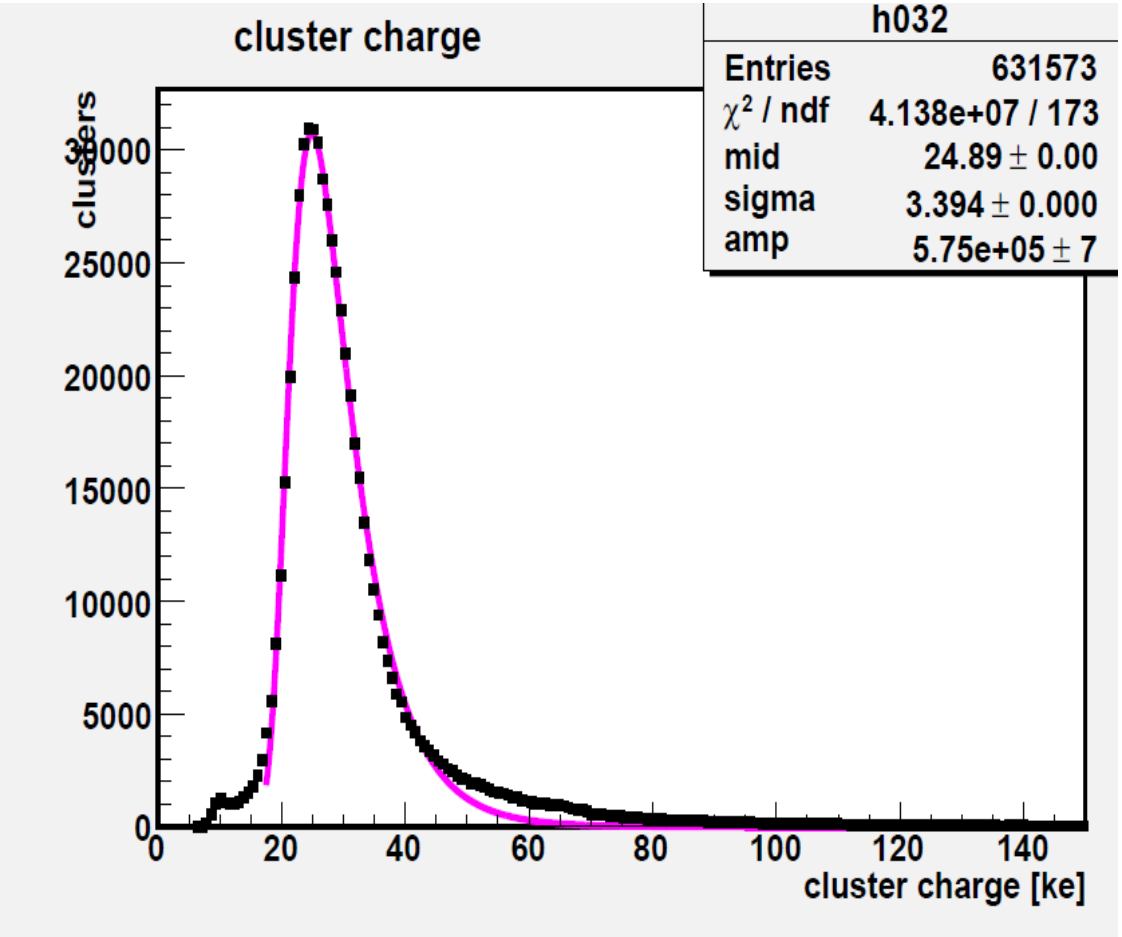
- Analog PH vs Vcal
- Scan with internal calibrate pulse
- Linear regime above some threshold
- Fit with a new hyperbolic tan function
- Preamp saturation for large pulses
- Repeat for 4160 pixels and extract calibration factors

Pixel charge

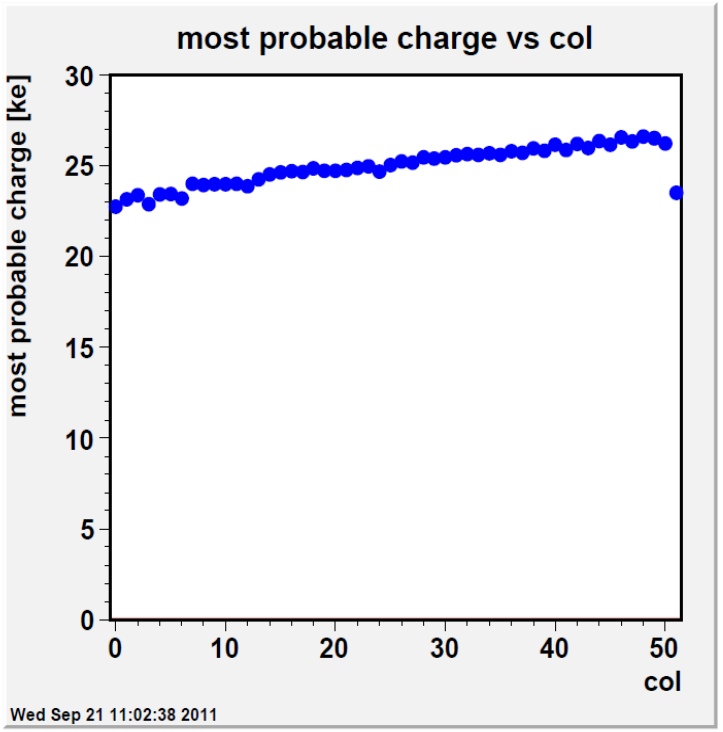


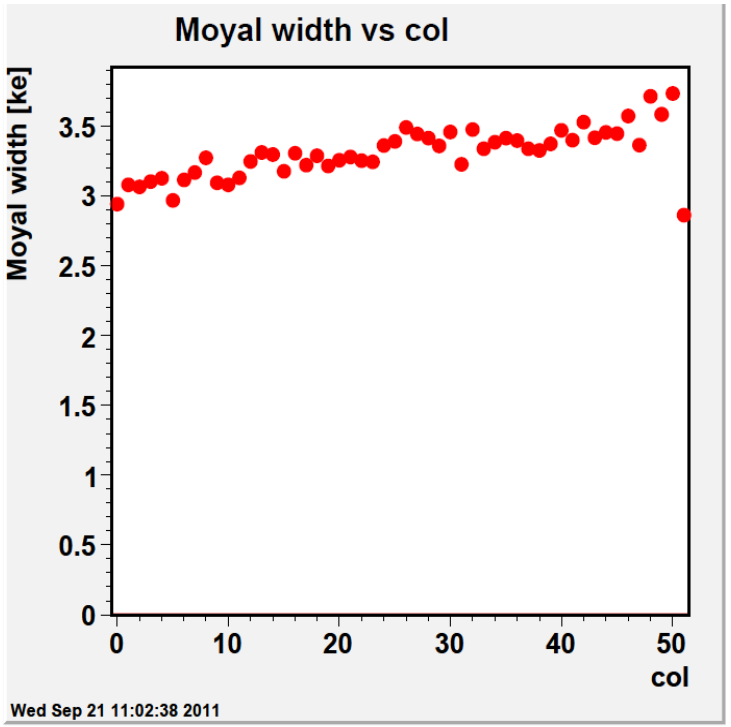
- 2 GeV e+ beam test
- No magnetic field
- New test pulse gain calibration applied
- Peak at 25 ke, Ok for MIP in 285 μm silicon
- No hump at 36 ke (as for linear fit, last presentation)

Cluster charge



- 2 GeV e+ beam test
- No magnetic field
- Test pulse gain calibration applied
- Chip 8, all pixels
- Fit by Moyal function: analytic approximation of Landau integral
- Left small peak due to wrong timing at test beam

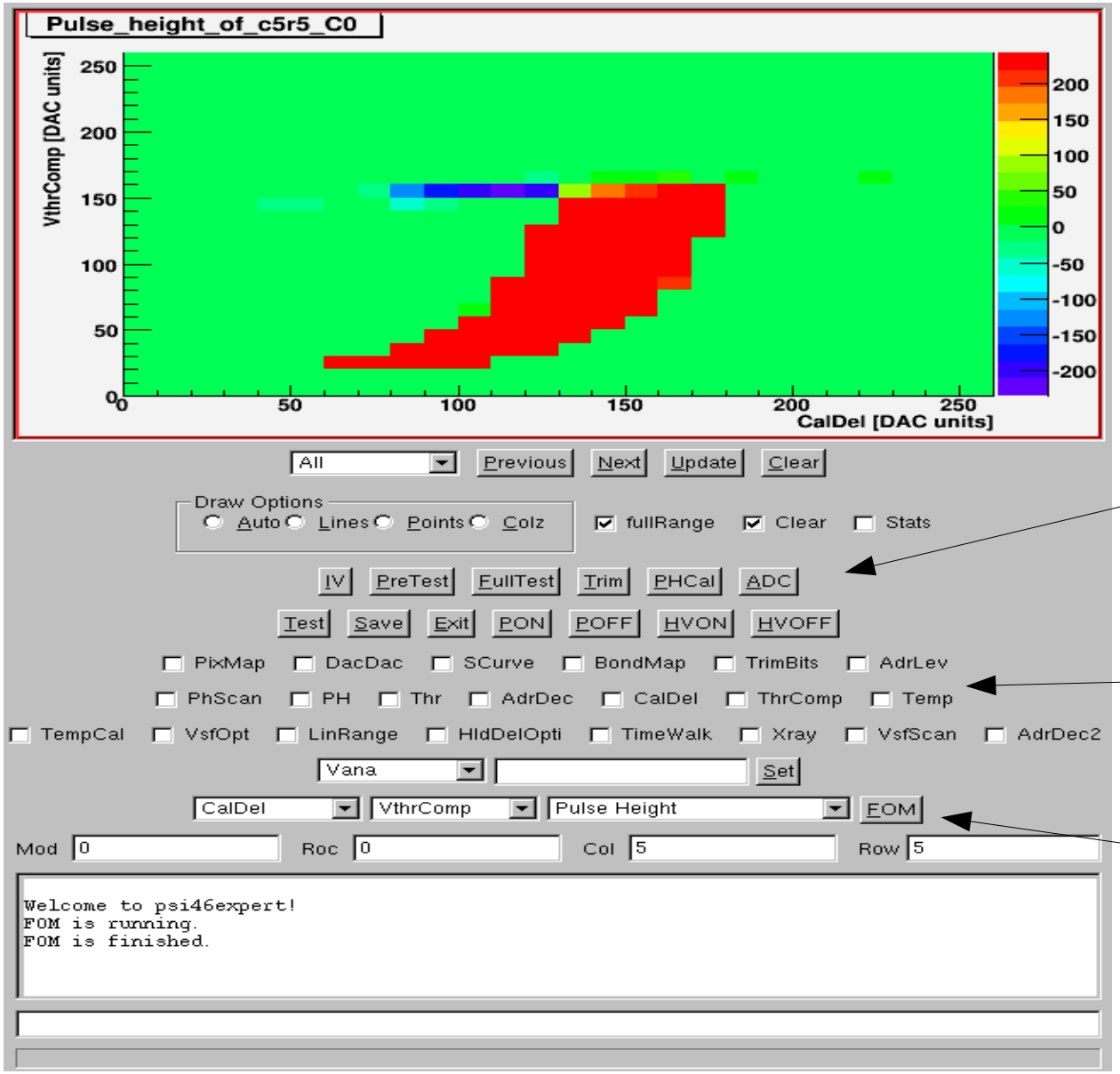




Cluster charge

- 2 GeV e+ beam test
- No magnetic field
- Test pulse gain calibration applied
- Chip 8, all pixels
- Moyal fit to each column
- Expect ~25 ke from 285 µm silicon
- Observe ~8% gain variation across chip8:
  - Test pulse (calibration) problem?
  - Check with X-ray source?

GUI



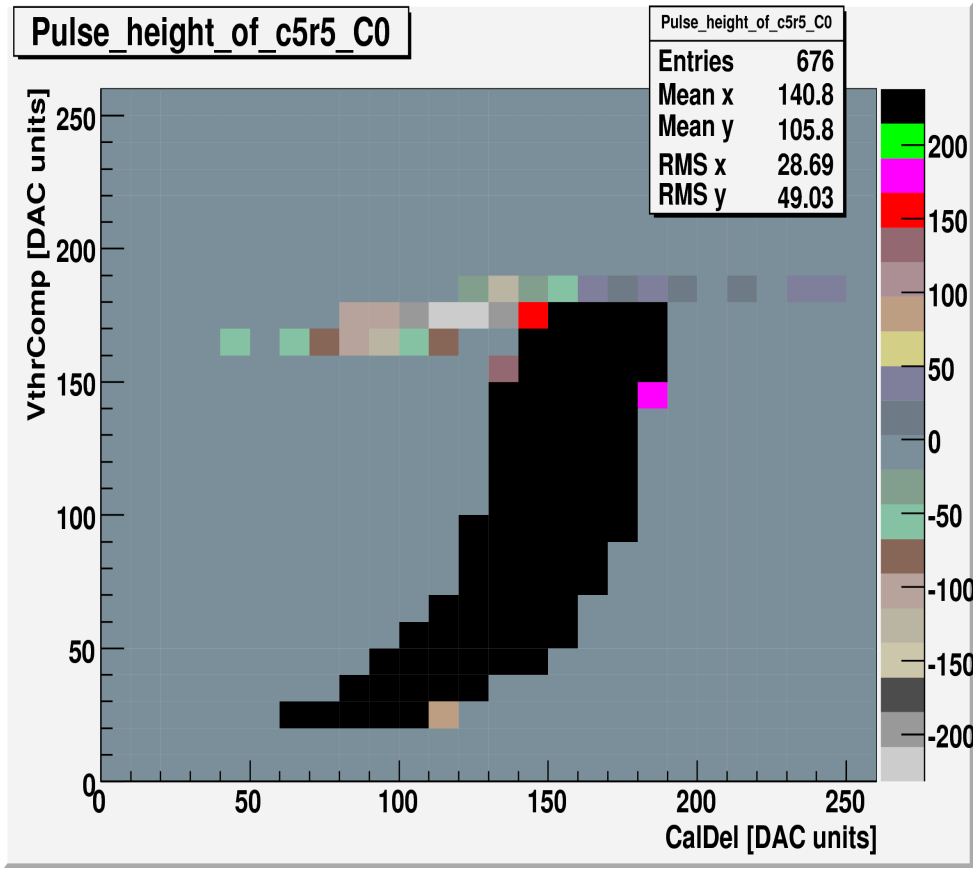
Calibration tests

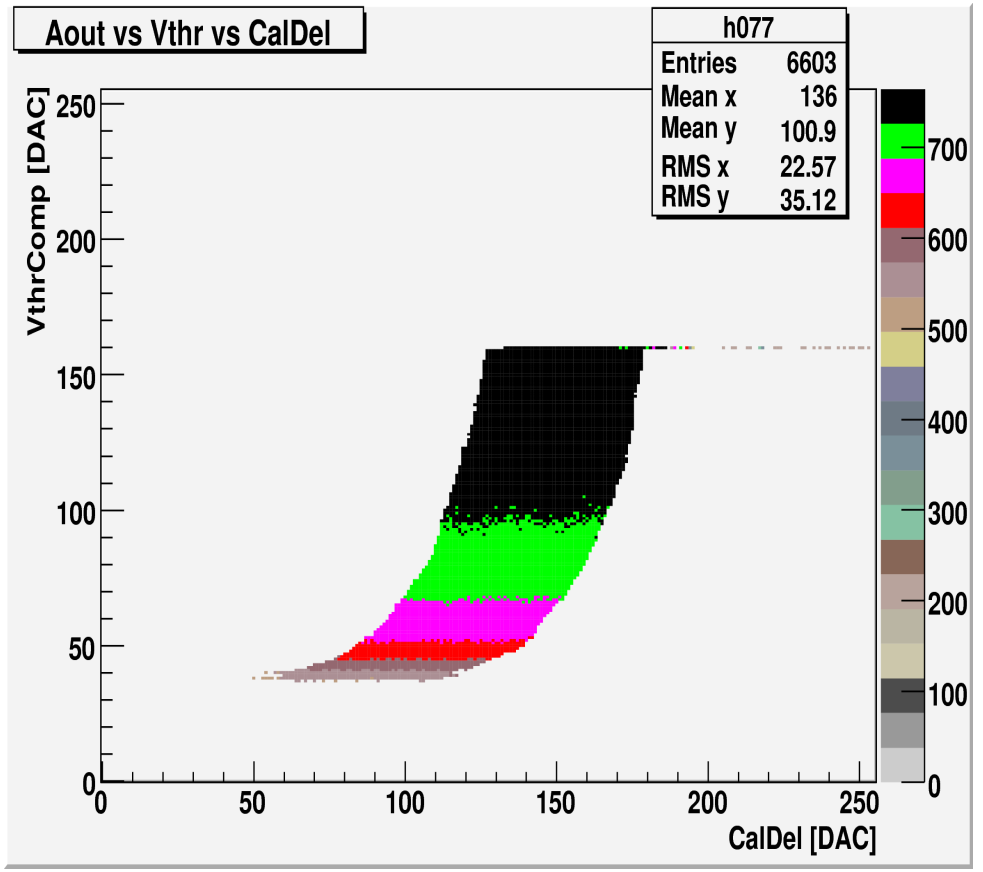
Individual tests

Parameter adjusting

VthrComp vs CalDel

Working space for Chip2 evaluated from GUI and “manually”

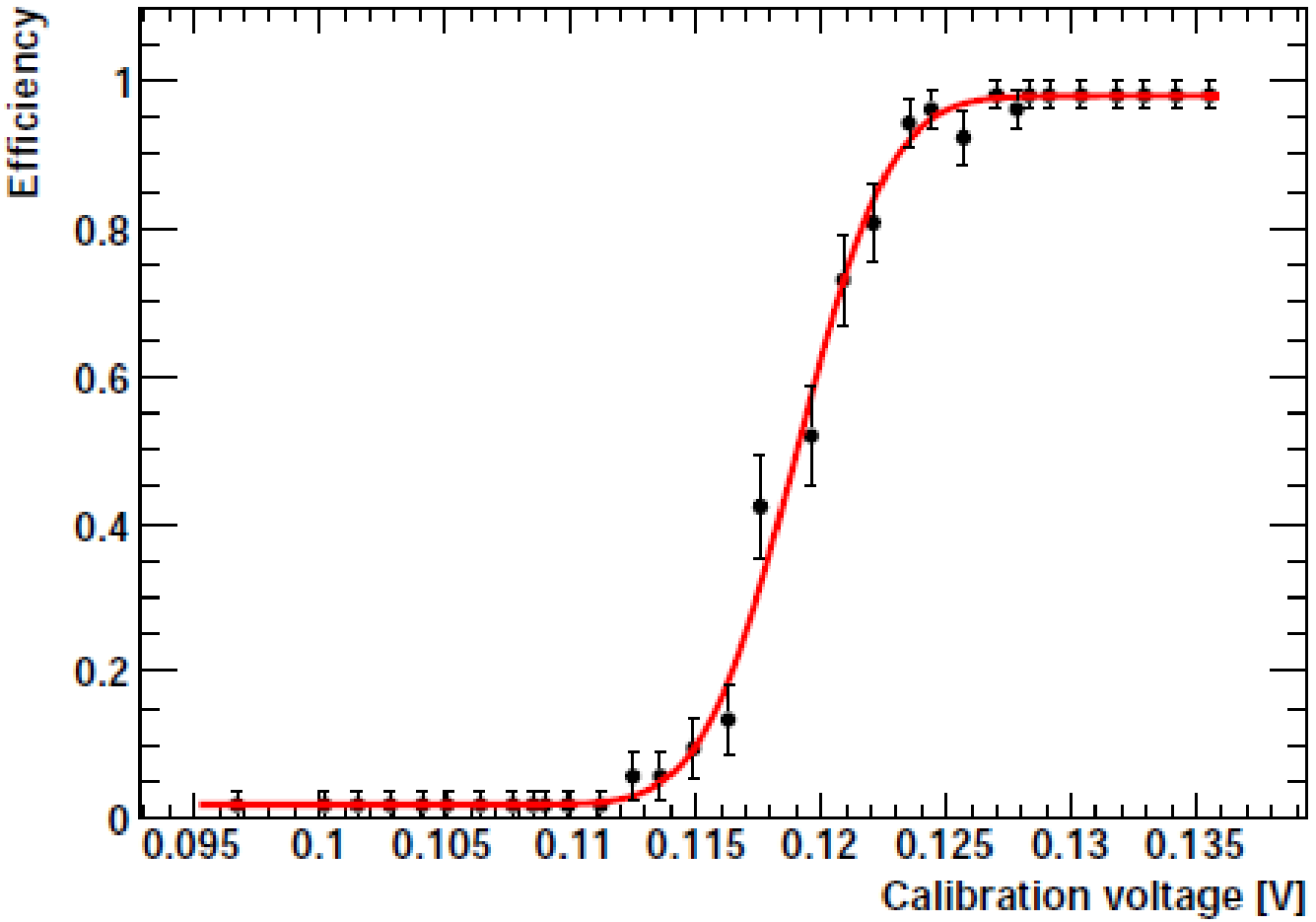




Summary

- S-curve code for fast pixel threshold determination put into operation:
  - works only in TBM emulator mode on the FPGA.
- Pixel threshold trimming algorithm put into operation:
  - several USB time delays had to be adjusted.
  - Acquire threshold maps, determine spread,
  - adjust trim range,
  - determine trim bits for each pixel.
- Results:
  - threshold variation reduced from 290 e to 50 e on chip without sensor and to 80 e with sensor.
- Calibration: gain variation across chip (~8%).
- Further:
  - apply settings in DESY test beam.

Threshold curve at PSI



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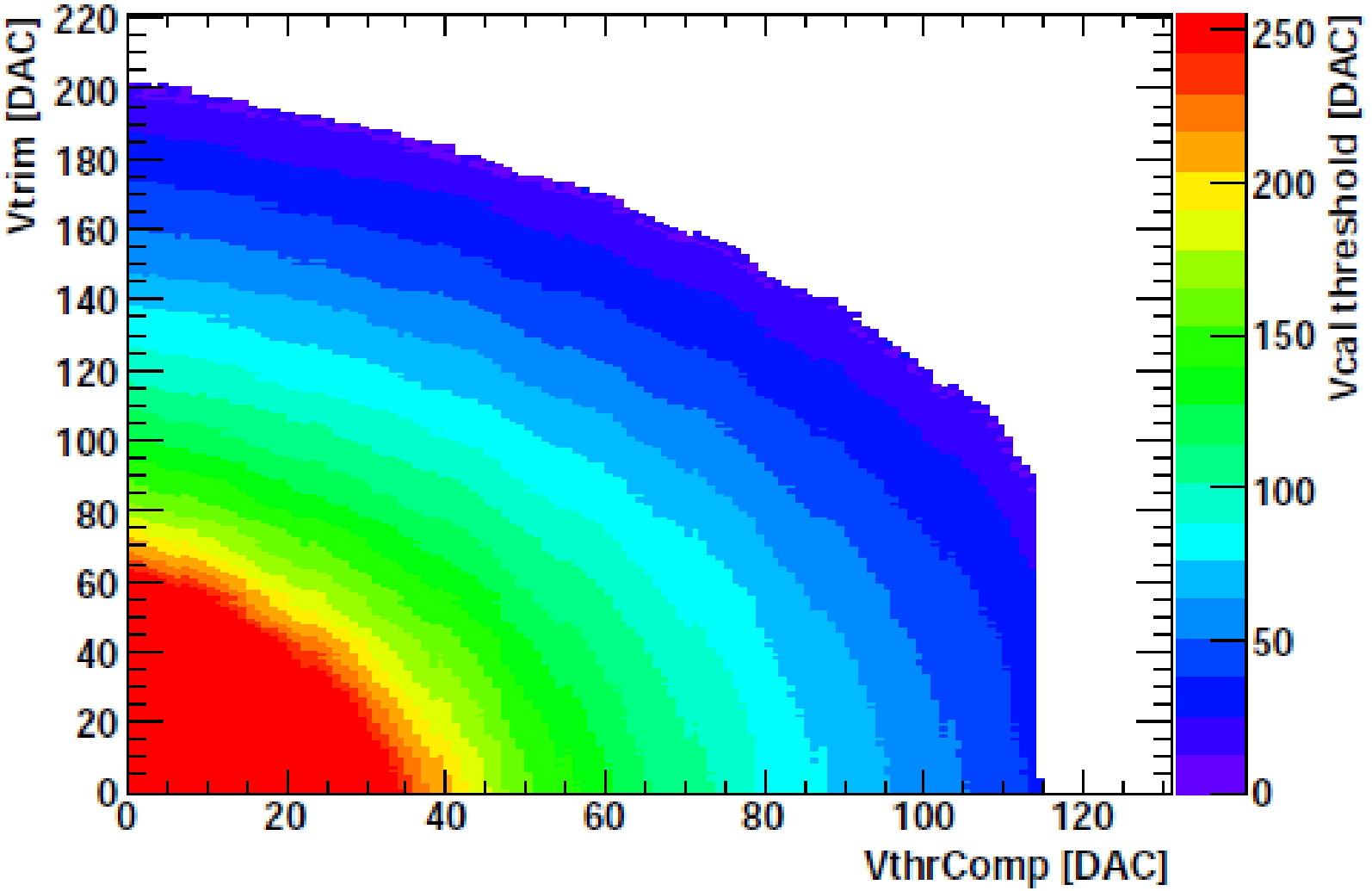
Threshold vs trim voltages



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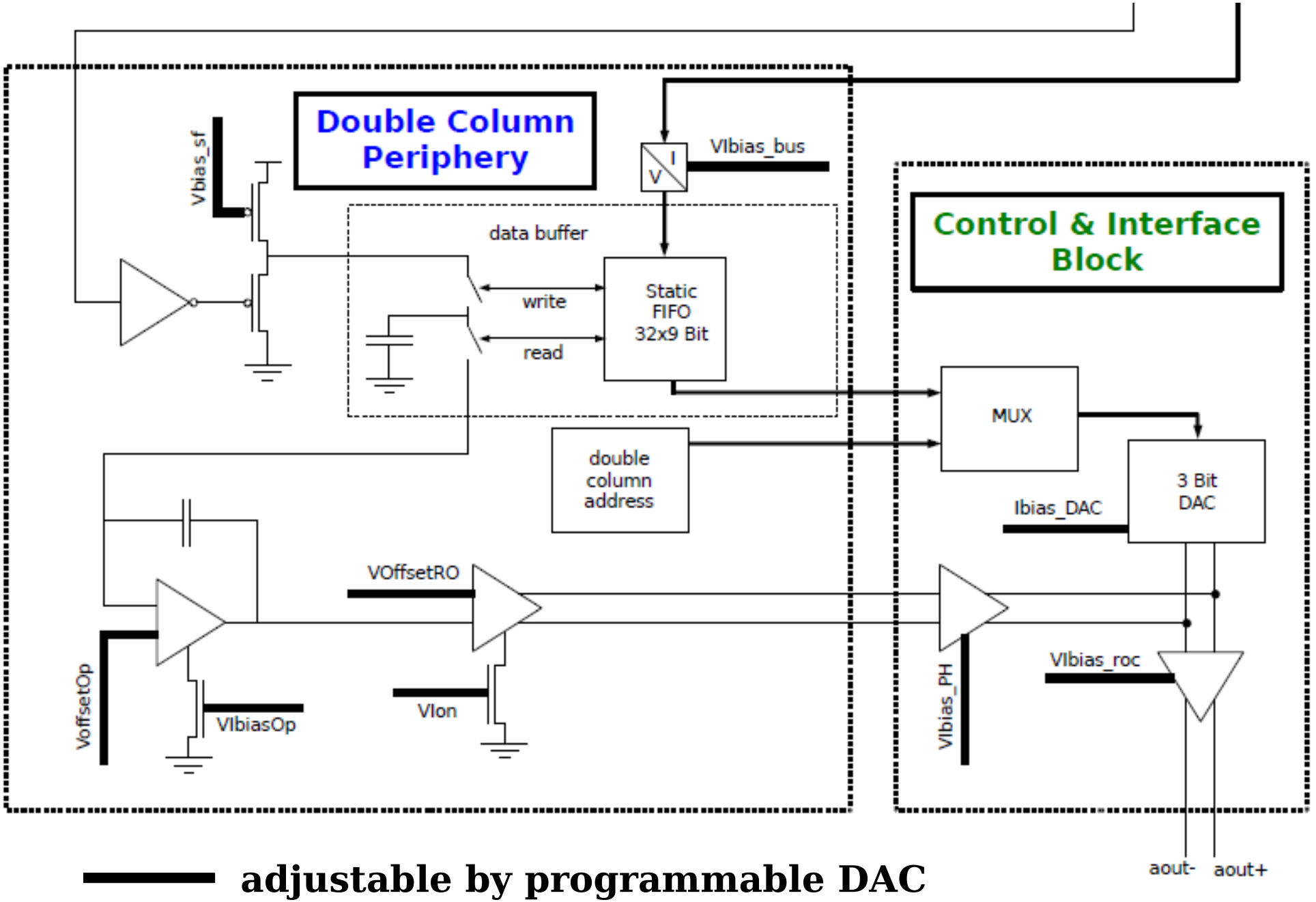
psi46 DACs

1	Vdig	6
2	Vana	150
3	Vsf	135
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	130
11	Vtrim	104
12	VthrComp	124
253	CtrlReg	0
254	WBC	98

13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	55
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VIColOr	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	125
27	RangeTemp	0

psi46 pixel readout chip



adjustable by programmable DAC