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FLAME-based ECAL-p readout status

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ECAL-p LUXE workshop, 27-31 January 2025, DESY Hamburg

Agenda

- Readout hardware status
- Amount of data generated during TB
- Schedule

FPGA & baseboard

Quick recap:

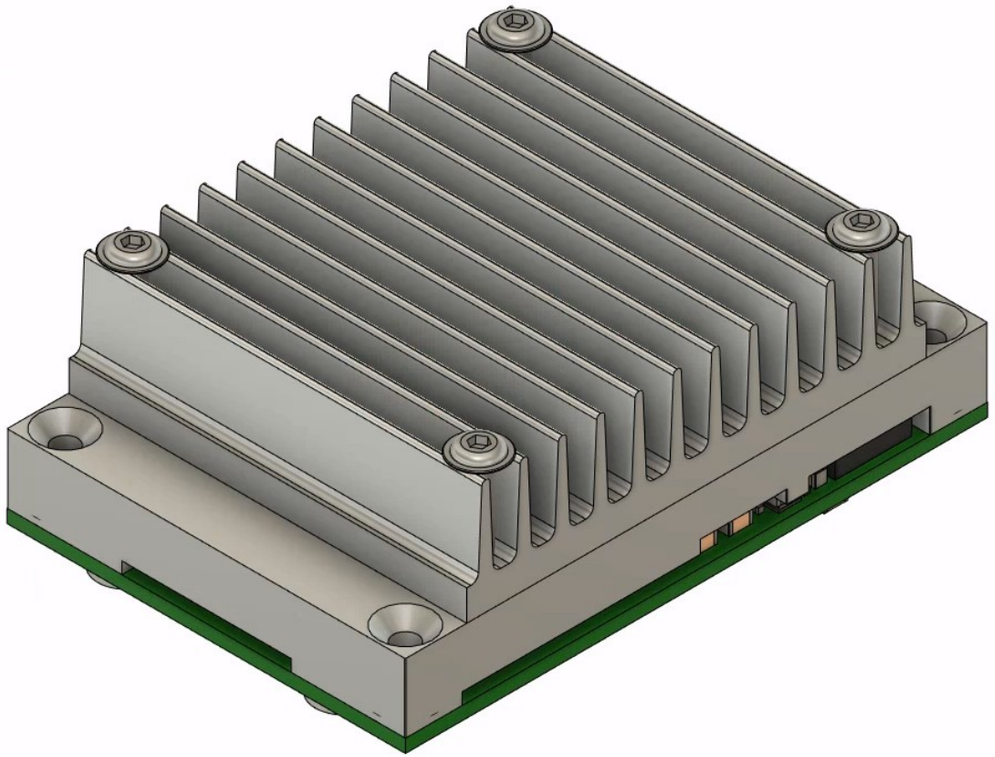
- FLAXE production failed → we cannot use FLAXE-based readout for next TB
- We decided to use FLAME-based readout from previous TBs

- Existing DAQ was based on Trenz TE0808 FPGA modules, hosted on TEBF0808 development baseboards
  - But we have only three baseboards (+ fourth in TAU)
  - There was no change to buy ~10 from Trenz before June 2025

FPGA & baseboard

Currently we have **13 (14)** FPGA modules:

- 9 fully assembled
- 2 bought by Veta
- 2 “naked” – dedicated heatsink to be fabricated by Warsaw
- (+1 in TAU)



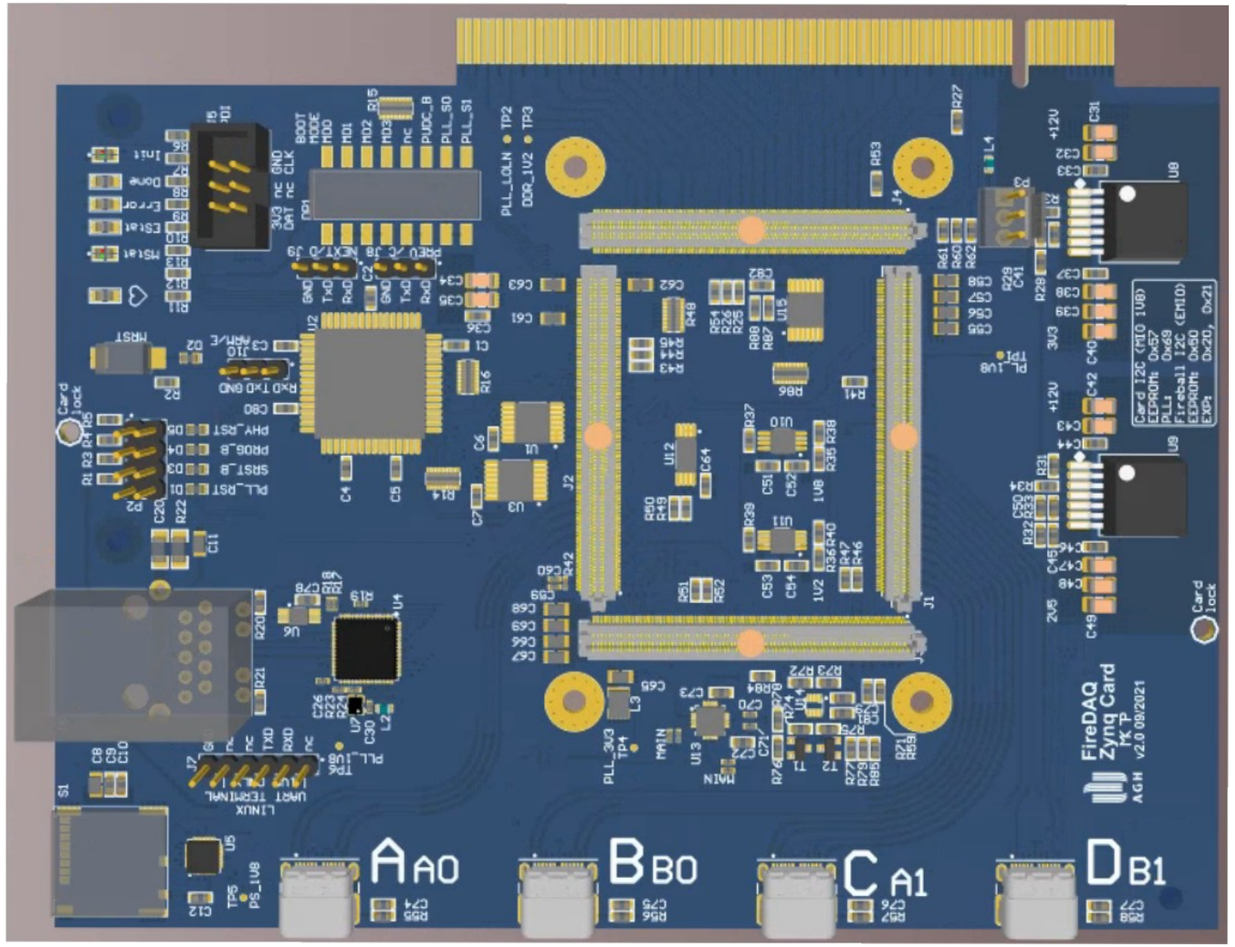
FPGA baseboard

We decided to use custom baseboard developed for FCAL
This board had few issues:

- **Most crucial parts** (LVDS fanouts for clock and trigger distribution) **obsolete and no longer available**
- Overly complicated power supply sequence control
- Overly complicated synchronization scheme
- Custom mechanics (never made)

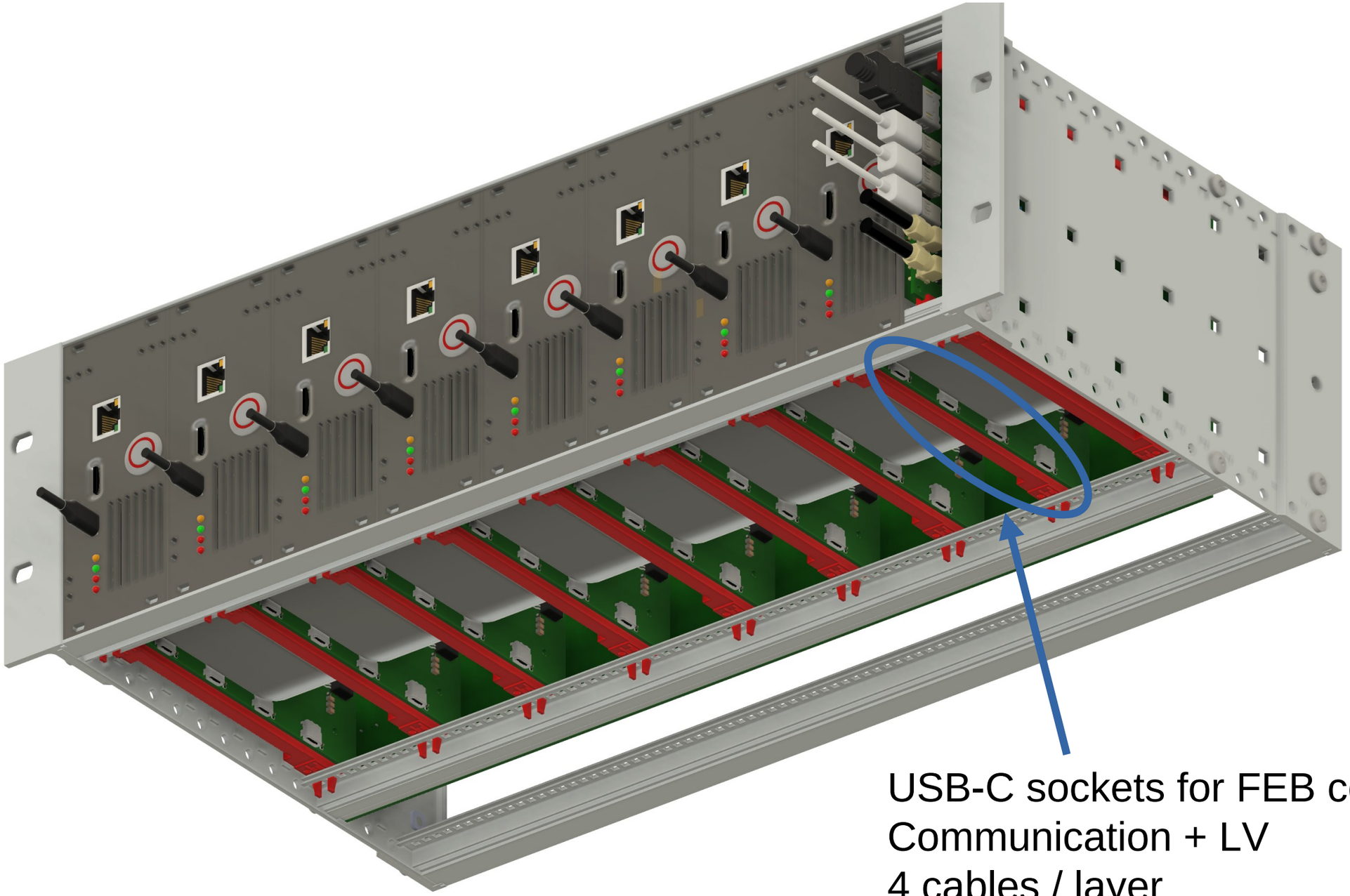
I decided to upgrade the FPGA board

- Simplified power control and synchronization
- Up-to-date parts
- Fit to the 19” rack case



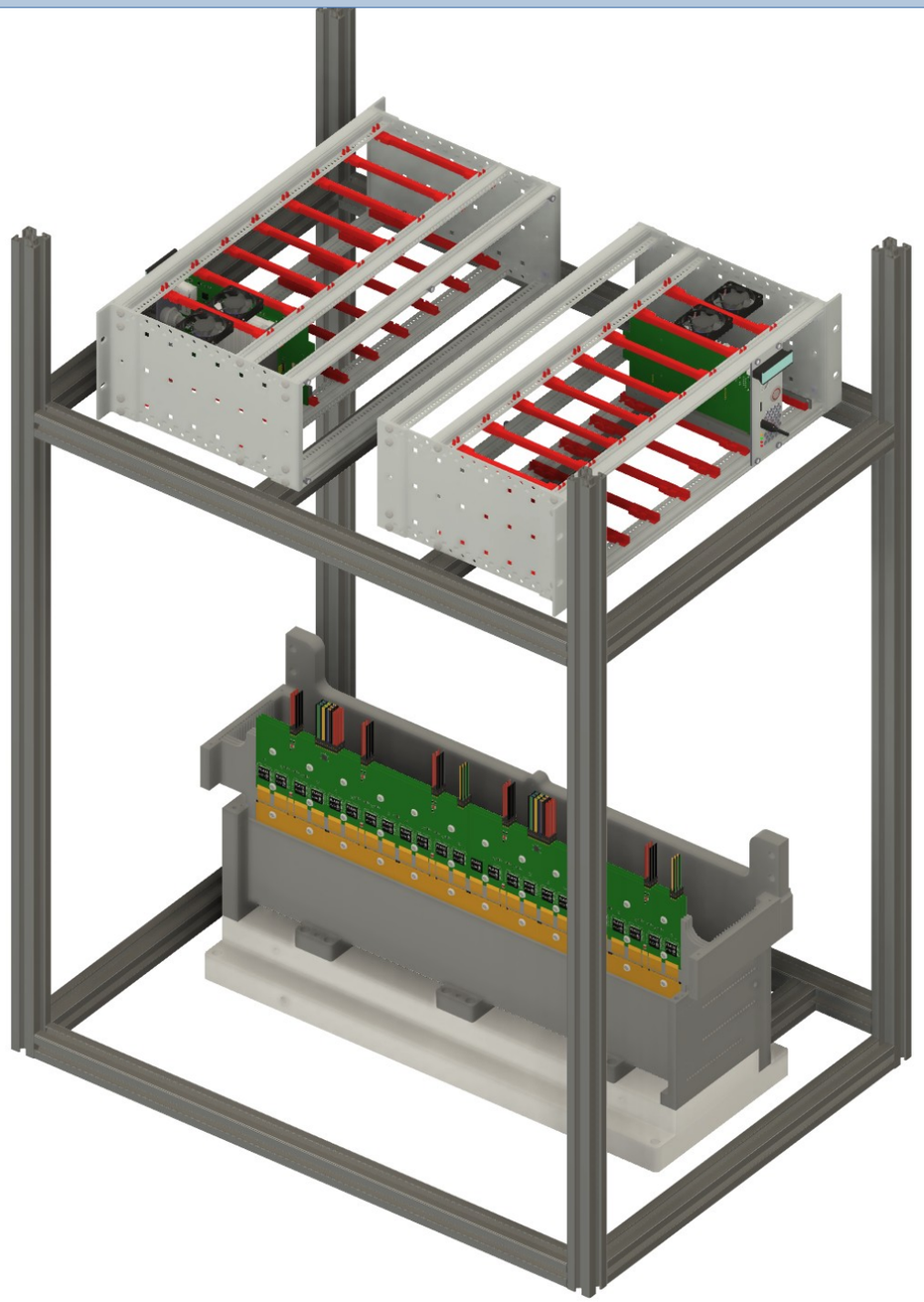
Readout rack

Readout rack – bottom view



USB-C sockets for FEB connection
Communication + LV
4 cables / layer

Scaffolding



Initial concept

Needs “real” design, awaits for a few decisions:

- Usage of old tungsten plates
- Design of the transportation plate

- Faraday cage (light shielding) design is directly related to the design of the scaffolding

Rack readout

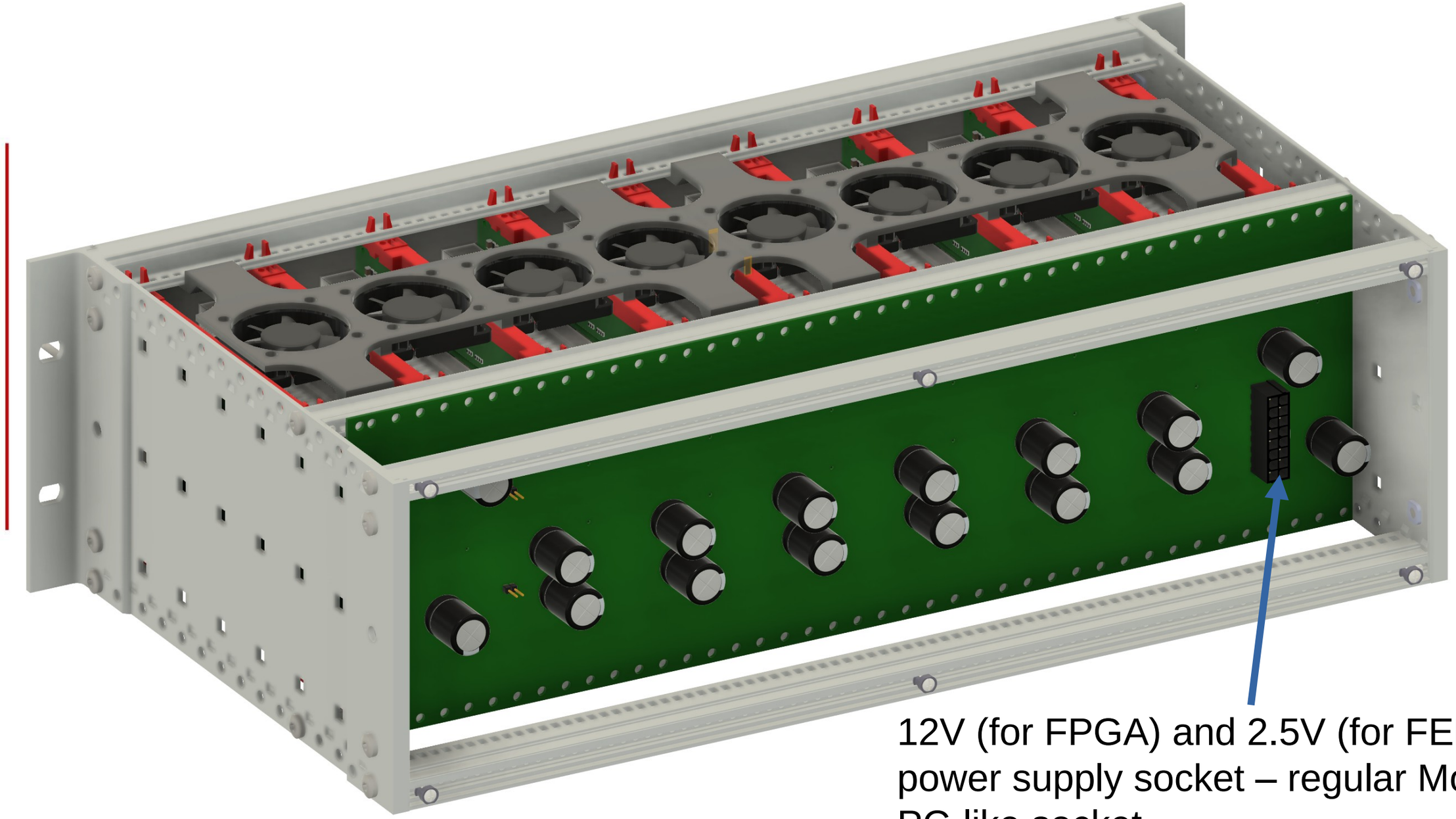
Each rack hosts **eight** FPGA cards – two racks needed for the TB

- Each rack can work in a standalone mode
- Both racks have exactly the same hardware and are fully interchangeable
- Racks will automatically configure itself to a master – slave scheme depending on how the cables are connected between them
- In case of failure cards can be easily swapped and will automatically take a new role – there is no special master FPGA synchronization card

FLAME-based readout can work in a self-trigger mode

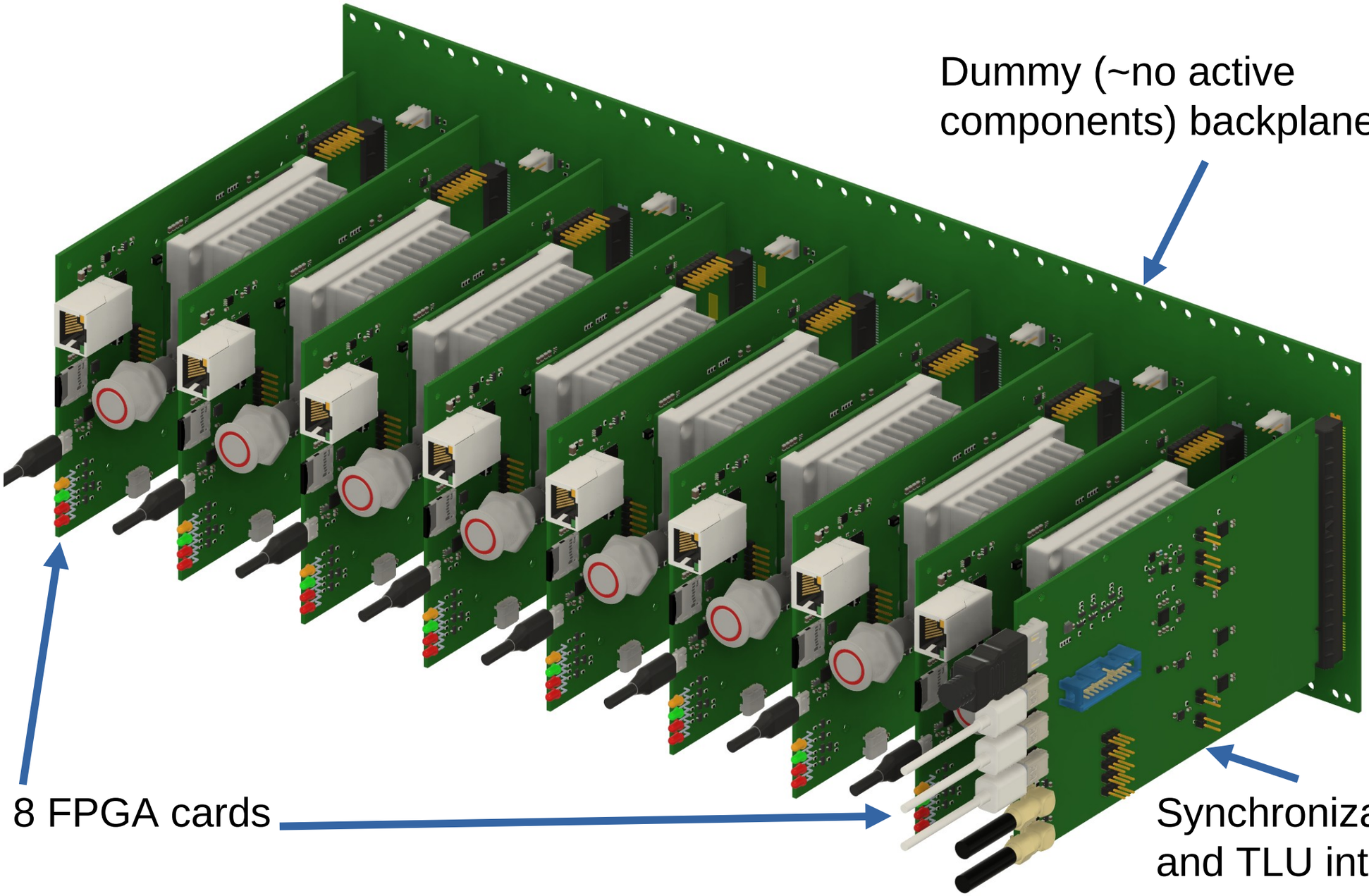
- Cosmic muons (without scintillators) or radioactive source measurements are available
- One rack can be send to Valencia (after TB) for sensor study and will not need any additional instrumentation, apart from LV power supply and a PC

Readout rack – rear view

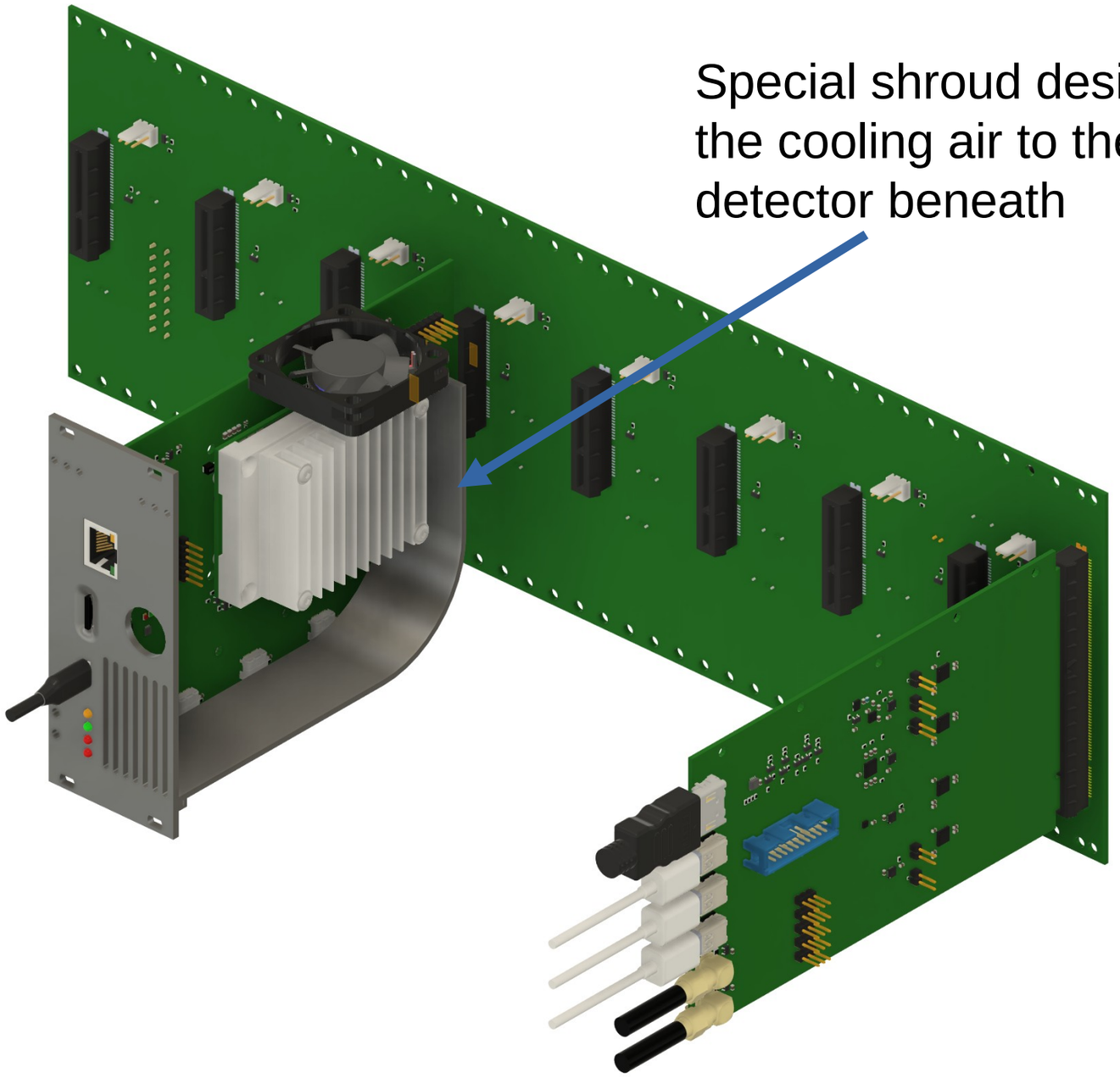


12V (for FPGA) and 2.5V (for FEBs) power supply socket – regular Molex PC-like socket

Readout rack “without rack” – backplane and cards



Readout rack “without rack” – backplane, cards and cooling



Special shroud designed to direct the flow of the cooling air to the front panel, away from the detector beneath

FPGA card, synchronization card and backplane PCBs submitted last week.

Estimated shipment date: this Friday

Rack PCBs – fabrication status

Order number	PCB name	Service	Order date	Planned shipment
E1668400	**FireDAQ_Card_Rack**	**DEFINED IMPEDANCE pool**	**24 Jan 2025**	**31 Jan 2025**

NUMBER	TYPE	PCB VISUALIZER®	ASSEMBLY VISUALIZER	REMARKS	STATUS	QUANTITY	FILES	USER NAME
E1668400	PCB	PCB Visualizer®	Analyse BOM & CPL		Panelise	15 (PCB)		jmoron@agh.edu.pl
E1668400-ST	Stencil	PCB Visualizer®			Stencil Incoming	1 (Panel)		jmoron@agh.edu.pl

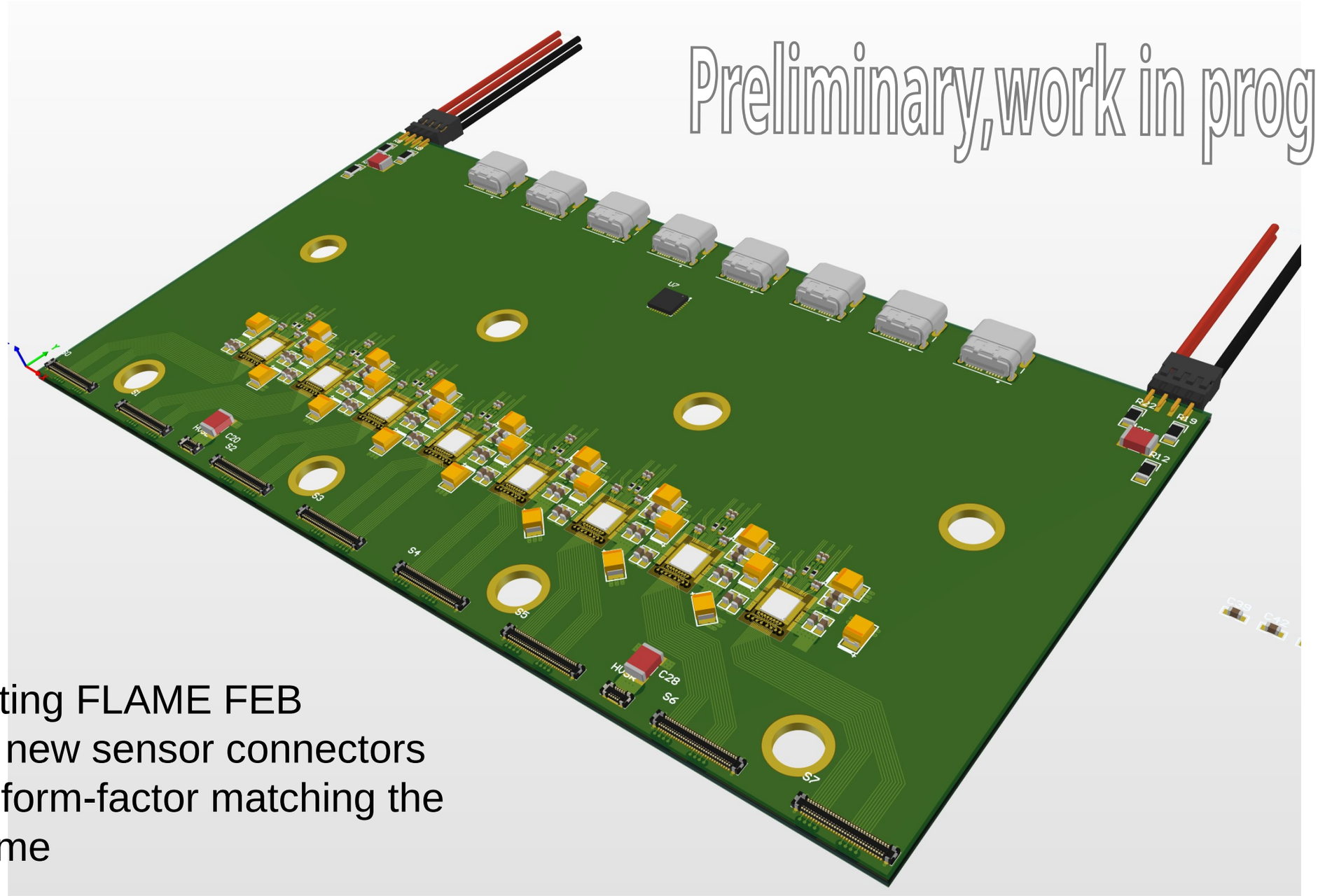
Order number	PCB name	Service	Order date	Planned shipment
E1668173	**FireDAQ_Sync_Rack**	**DEFINED IMPEDANCE pool**	**23 Jan 2025**	**30 Jan 2025**

NUMBER	TYPE	PCB VISUALIZER®	ASSEMBLY VISUALIZER	REMARKS	STATUS	QUANTITY	FILES	USER NAME
E1668173	PCB	PCB Visualizer®	Analyse BOM & CPL		In production	5 (PCB)		jmoron@agh.edu.pl
E1668173-ST	Stencil	PCB Visualizer®			Accepted after inspection	1 (Panel)		jmoron@agh.edu.pl

Order number	PCB name	Service	Order date	Planned shipment
E1668171	**FireDAQ_Backplane_Rack**	**DEFINED IMPEDANCE pool**	**23 Jan 2025**	**30 Jan 2025**

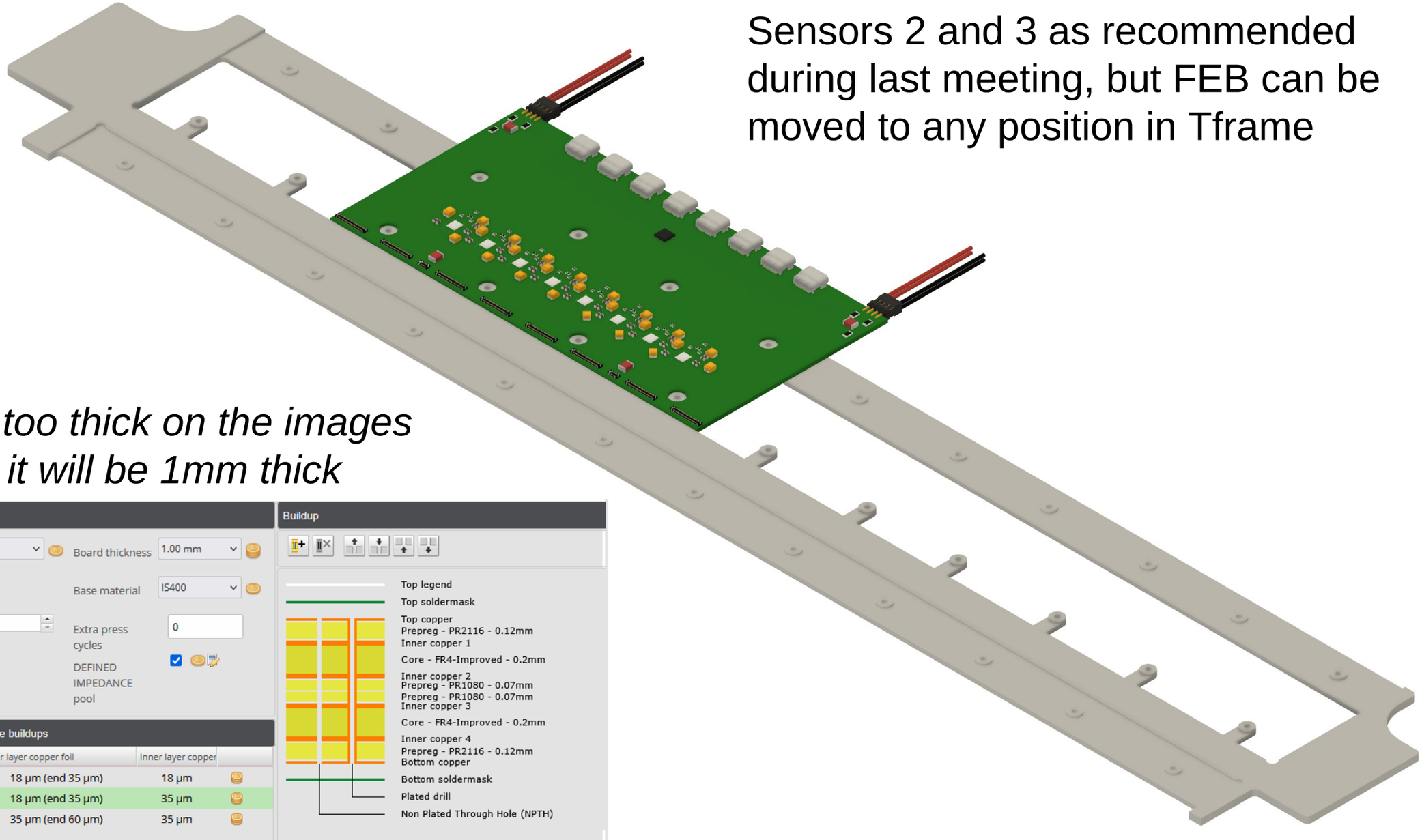
NUMBER	TYPE	PCB VISUALIZER®	ASSEMBLY VISUALIZER	REMARKS	STATUS	QUANTITY	FILES	USER NAME
E1668171	PCB	PCB Visualizer®	Analyse BOM & CPL		In production	5 (PCB)		jmoron@agh.edu.pl

FEB



Existing FLAME FEB
with new sensor connectors
and form-factor matching the
Tframe

FEB in Tframe



Sensors 2 and 3 as recommended during last meeting, but FEB can be moved to any position in Tframe

PCB is too thick on the images shown, it will be 1mm thick

Material

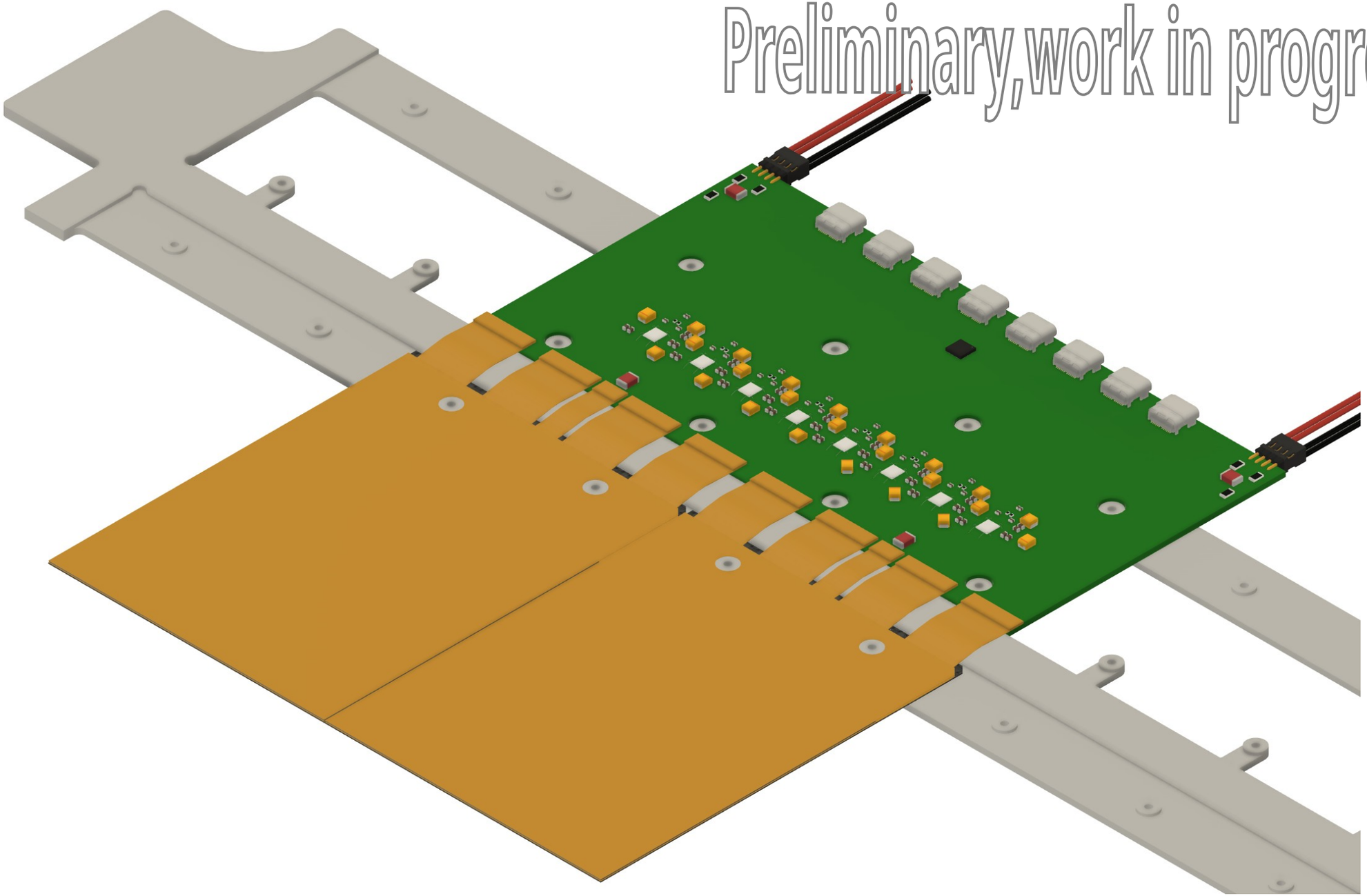
Number of layers	6	Board thickness	1.00 mm
Reversed buildup	☐	Base material	IS400
Blind/Buried via runs	0	Extra press cycles	0
Special buildup	☐	DEFINED IMPEDANCE pool	☑

Available defined impedance buildups

Core thickness	Outer layer copper foil	Inner layer copper
0.200 mm	18 µm (end 35 µm)	18 µm
0.200 mm	18 µm (end 35 µm)	35 µm
0.200 mm	35 µm (end 60 µm)	35 µm

Buildup

FEB with sensors in Tframe



Sensor pad to ASIC channel map

	A0	17	19	21	23	25	27	29	31	17	19	21	23	25	27	29	31	A4	
	A3	16	18	20	22	24	26	28	30	16	18	20	22	24	26	28	30	A7	
	A3	0	2	4	6	8	10	12	14	0	2	4	6	8	10	12	14	A7	
	A3	17	19	21	23	25	27	29	31	17	19	21	23	25	27	29	31	A7	
	A3	1	3	5	7	9	11	13	15	1	3	5	7	9	11	13	15	A7	
	A2	16	18	20	22	24	26	28	30	16	18	20	22	24	26	28	30	A6	
	A2	0	2	4	6	8	10	12	14	0	2	4	6	8	10	12	14	A6	
	A2	17	19	21	23	25	27	29	31	17	19	21	23	25	27	29	31	A6	
	A2	1	3	5	7	9	11	13	15	1	3	5	7	9	11	13	15	A6	
	A1	16	18	20	22	24	26	28	30	16	18	20	22	24	26	28	30	A5	
	A1	0	2	4	6	8	10	12	14	0	2	4	6	8	10	12	14	A5	
	A1	17	19	21	23	25	27	29	31	17	19	21	23	25	27	29	31	A5	
	A1	1	3	5	7	9	11	13	15	1	3	5	7	9	11	13	15	A5	
	A0	16	18	20	22	24	26	28	30	16	18	20	22	24	26	28	30	A4	
	A0	0	2	4	6	8	10	12	14	0	2	4	6	8	10	12	14	A4	
	A0	1	3	5	7	9	11	13	15	1	3	5	7	9	11	13	15	A4	

Proposed logical channel numbering in data file

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
15	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
14	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
13	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
12	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
11	176	177	178	179	180	181	182	183	184	185	186	[illegible]	188	189	190	191
10	160	161	162	163	164	165	166	167	168	169	[illegible]	171	172	173	174	175
9	144	145	146	147	148	149	150	151	[illegible]	[illegible]	[illegible]	155	156	157	158	159
8	128	129	130	131	132	133	134	[illegible]	[illegible]	[illegible]	138	139	140	141	142	143
7	112	113	114	115	116	[illegible]	[illegible]	[illegible]	[illegible]	121	122	123	124	125	126	127
6	96	97	98	99	100	[illegible]	[illegible]	[illegible]	104	105	106	107	108	109	110	111
5	80	81	82	[illegible]	84	85	86	87	88	89	90	91	92	93	94	95
4	64	65	66	[illegible]	[illegible]	69	70	71	72	73	74	75	76	77	78	79
3	48	49	50	[illegible]	52	53	54	55	56	57	58	59	60	61	62	63
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Preliminary

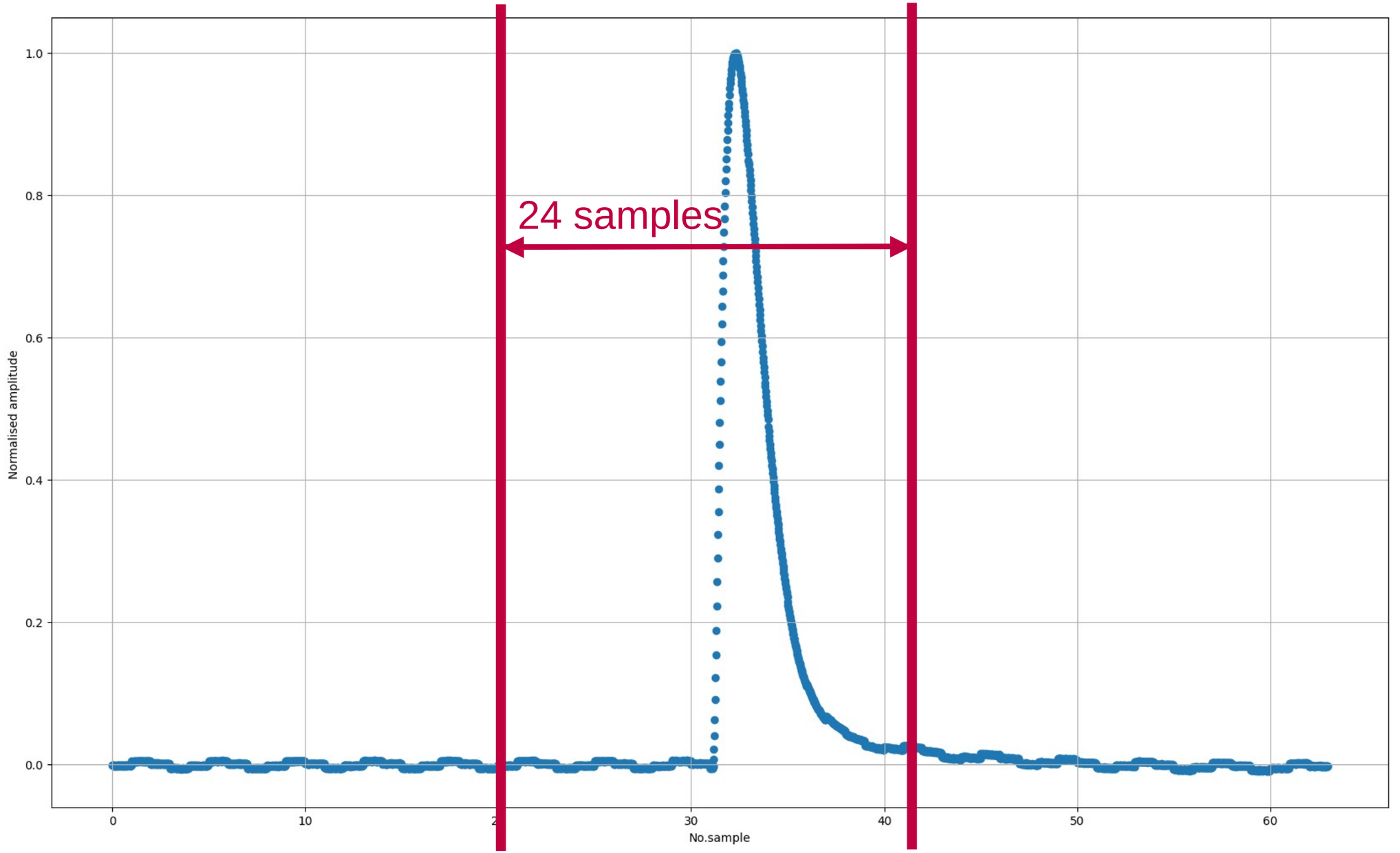
Bandwidth and data

Assumptions:
- “Smooth” testbeam – data collected from Monday, 18:00 till Sunday 12:00, 23h / day
- 11 layers, 256 channels each
- 1 kHz trigger rate (5 GeV electrons)

Without debug data (ZS data only at 12% occupancy): **~1 TB of data**

With debug data:
- Previous TB case: 63 debug data samples / channel / event: **~175 TB of data**
  Required DAQ bandwidth: **3.12 Gbps**

Amount of debug samples



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With debug data:
- Previous TB case: 63 debug data samples / channel / event: **~175 TB of data**
  Required DAQ bandwidth: **3.12 Gbps**

- With ~24 debug data samples / channel / event: **~65 TB**
  Required DAQ bandwidth: **1 Gbps**

Theoretical limit of system bandwidth:
- Quad UDP parallel links: **<3.8 Gbps**
- Quad WD Red Pro 4TB HDD in RAID0: **<11 Gbps**

New LUXE DAQ PC is equipped with 14 TB of HDD (four 4TB HDDs).
If we want to collect ~65 TB, a new four 16-18 TB HDDs are needed!

There is also compression option (*results preliminary!*)

Compression

ROOT files are compressed. For example:

- TB 2022, run 4636 – around 1 Mevents, 128 channels with 63 debug data samples
- Raw binary data: **16 GB**
- ROOT file size: **6.1 GB – 62%** compression ratio

We have tested multiple compression algorithms using file containing 25.000 events with 24 debug samples with original size of 325 MB. Such a file will be collected in 2.25 second for 11 layers

Algorithm	Compression time	Compression time to collection time ratio	Compression ratio
ROOT (*algorithm ?*)	?	?	62 %
bzip2	12.5 s	5.5	67 %
gzip / zip	16 s	7.1	53 %
7z	32.9 s	14.6	72 %
7z using bzip2 multicore *using all cores of the PC*	1.9 s	0.85	67 %
zstd *highest compression*	1m 57.7 s	141.6	65 %

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zstd *highest compression*	1m 57.7 s	141.6	65 %
zstd	**1.2 s**	**0.53**	**56 %**

Preliminary

HDDs

Capacity	WD Red Plus	WD Red Pro	Quad HDD capacity	EUR / TB
8 TB	231	268	32 TB	28.9 / 34
10 TB	296	320	40 TB	29.6 / 32
12 TB	313	380	48 TB	26 / 32
14 TB		420	56 TB	30
16 TB		424	64 TB	26.5
18 TB		522	72 TB	29
20 TB		575	80 TB	29
22 TB		640	88 TB	29
24 TB		699	96 TB	29

Currently we have four 4 TB WD Red Pro.
Motherboard supports only four drives

https://www.westerndigital.com/de-de/products/internal-drives/wd-red-pro-sata-hdd?sku=WD161KFGX

TB plan and remarks

Assuming “smooth” testbeam:
- data collected from Monday, 18:00 till Sunday 12:00, 23h / day

we are going to collect ~475 M events

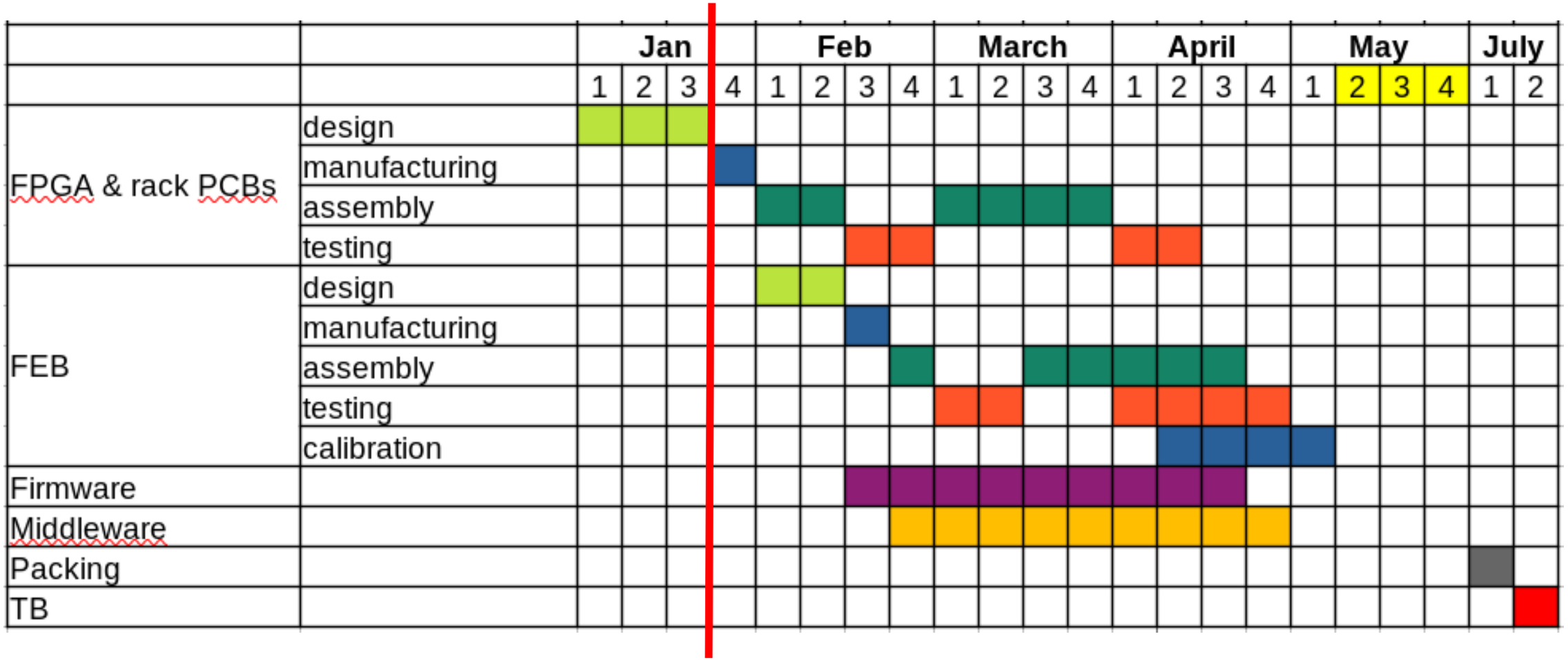
We need detailed physics plan for the TB
- What we want to measure – configurations, X-Y scans, rotations
  - How many steps, how many events / configuration

We need to estimate time needed for “manual labour” inside area – e.g. X-Y scan can be made using green stage, rotation needs entering the area but is quite fast, but changing the stack can be quite time consuming task.

Detailed plan will allow to estimate the amount of collected data more precisely.
In addition, the more detailed study on ZSTD compression will give us quite exact HDD space requirements.

We need to think about post-TB logistics:
- How long it will take to disassemble the detector
- Do we want to do it on Sunday or find some space to work on Monday and use the beam time up to the limit?
- We agreed that everything goes back to Krakow, right?

Schedule



Not included here:

- Software – see Dawid talk
- Mechanical integration – tbd.