AGH University of Science and Technology

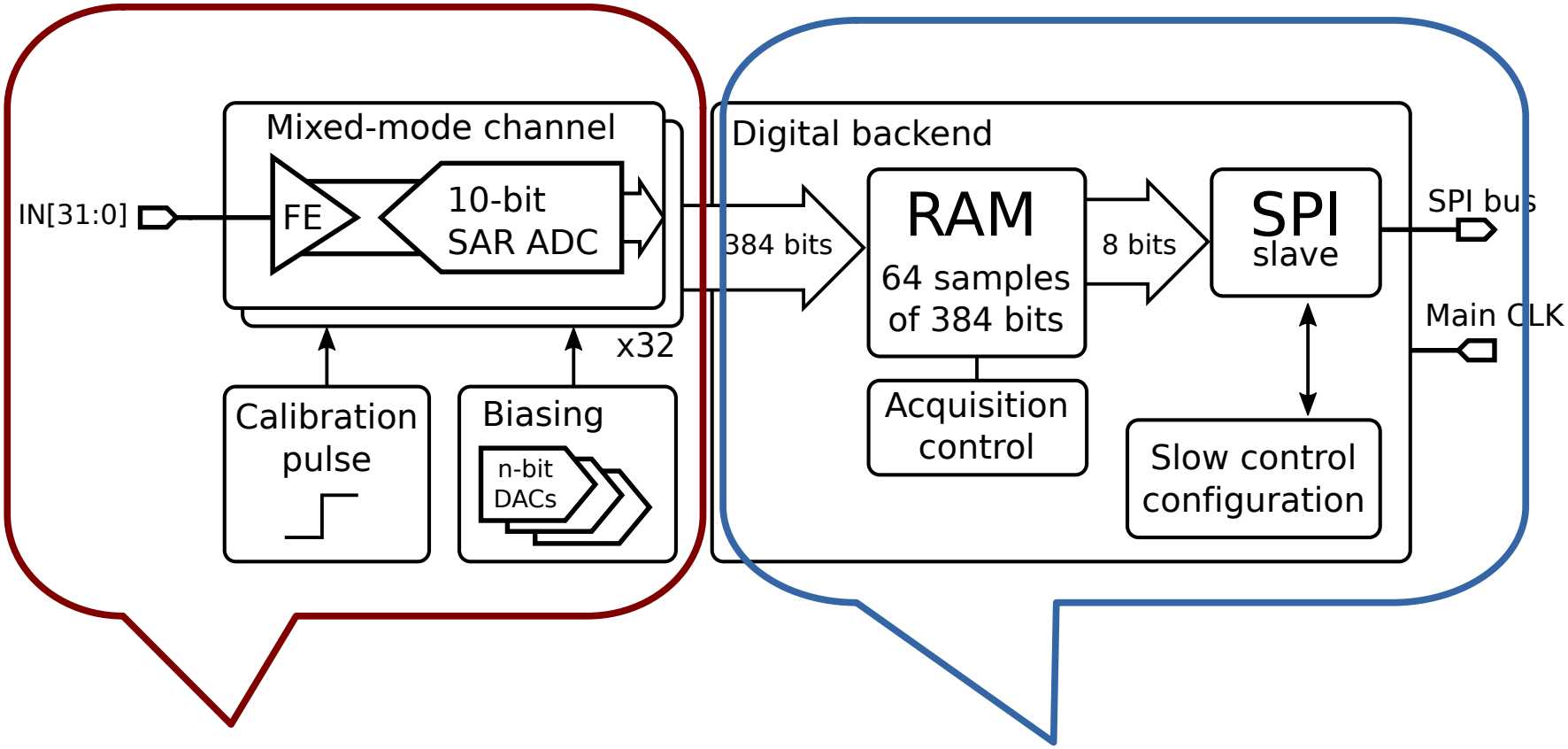
FLAXE status

Marek Idzik

Faculty of Physics and Applied Computer Science
AGH University of Krakow

27-31 January 2025, DESY

FLAXE architecture

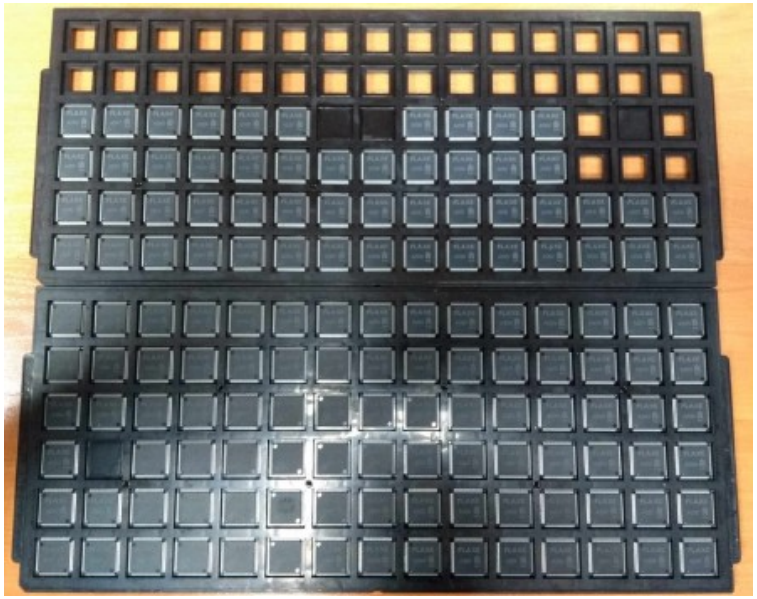


Copied from FLAME

New “simple” slow readout with memory

FLAXE – Qualification tests

Out of ~1000 fabricated chips, 142 were packaged and tested

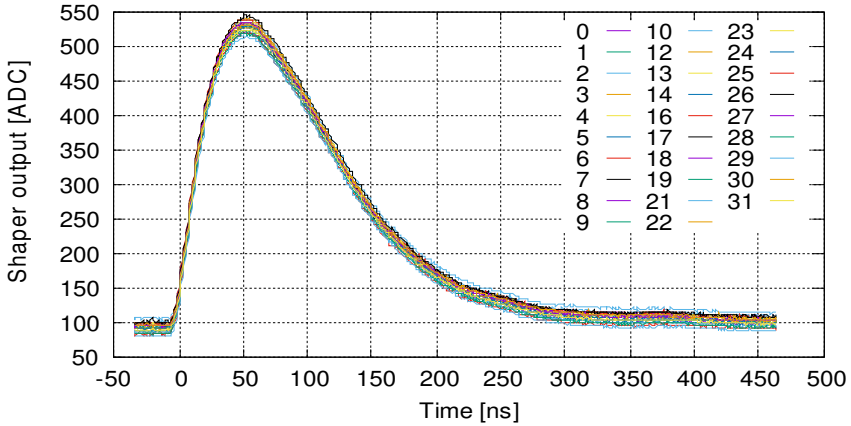


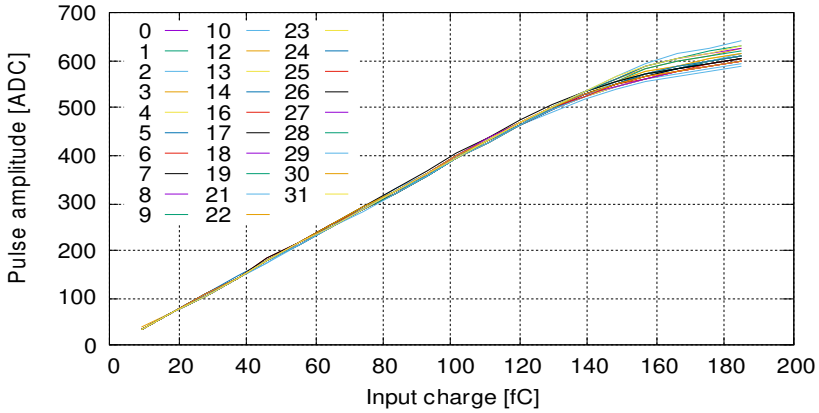
Test	Good	Acceptable	Bad	Failed
Overall ASIC yield	0 [0%]	6 [4.2%]	5 [3.5%]	131 [92.3%]
Supply shorts	92 [64.8%]	0 [0%]	0 [0%]	50 [35.2%]
Power consumption in sleep mode	7 [7.6%]	9 [9.8%]	30 [32.6%]	46 [50%]
Power consumption in always on	6 [12.8%]	9 [19.1%]	25 [53.2%]	7 [14.9%]
SPI SC register default read	33 [35.9%]	10 [10.9%]	46 [50%]	3 [3.3%]
SPI SC register write	10 [10.9%]	16 [17.4%]	21 [22.8%]	45 [48.9%]
Datapath RAM error map	0 [0%]	18 [38.3%]	3 [6.4%]	26 [55.3%]
Datapath RAM input sample	41 [87.2%]	3 [6.4%]	2 [4.3%]	1 [2.1%]
Biasing DAC's	17 [36.2%]	15 [31.9%]	1 [2.1%]	14 [29.8%]
Channel data readability	5 [10.6%]	12 [25.5%]	4 [8.5%]	26 [55.3%]
Channel trimDAC	0 [0%]	19 [90.5%]	1 [4.8%]	1 [4.8%]
FE response and pulse shape	0 [0%]	7 [33.3%]	4 [19%]	10 [47.6%]
FE gain	0 [0%]	7 [33.3%]	4 [19%]	10 [47.6%]

Our conclusion is that there was a production failure

FLAXE – Tests
6 chips got “acceptable” status

Chip Number	No. of working channels	No. of correct trimDAC’s	No. of correct shapes	No. of correct gains
25	19	20	11	16
32	26	25	25	26
76	22	23	19	20
84	27	28	16	27
136	30	30	28	29
139	27	27	25	26





Performance of working channels in very good agreement with simulations

JINST

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: October 31, 2024
ACCEPTED: December 18, 2024
PUBLISHED: January 22, 2025

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS
UNIVERSITY OF GLASGOW, SCOTLAND, U.K.
30 SEPTEMBER–4 OCTOBER 2024

FLAXE, a SoC readout ASIC for electromagnetic calorimeter at LUXE experiment

Jakub Moroń,* Mirosław Firlej, Tomasz Fiutowski, Marek Idzik and Krzysztof Świentek

Faculty of Physics and Applied Computer Science, AGH University of Krakow, Al. Mickiewicza 30, 30-059 Kraków, Poland

E-mail: jmoron@agh.edu.pl

ABSTRACT: The design and qualification results of a System on Chip (SoC) Application-Specific Integrated Circuit (ASIC), called FLAXE, fabricated in 130 nm CMOS technology are presented. FLAXE is a readout ASIC designed for ECAL-p, a compact electromagnetic calorimeter being a part of a detector system for Laser Und XFEL Experiment (LUXE) proposed at DESY, Hamburg, as an extension to the European X-ray Free Electron Laser (XFEL) facility. ECAL-p is a sampling calorimeter with a very compact design targeting small Molière radius, comprising 16 (up to 20) layers composed of 3.5 mm (1 X_0) thick tungsten absorber plates interspersed with silicon sensors. Sensor signal is read and shaped by the analogue readout channel, comprising a Charge Sensitive Amplifier (CSA) and a fully differential CR-RC shaper with 50 ns peaking time, which output is digitized in each channel by a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). Data from ADC are collected into the ASIC internal memory and read out by the Data Acquisition (DAQ) system between Bunch Crossings (BXs). Around 1000 ASICs have been fabricated and a first batch of 142 ASICs has been packaged and tested. The results of the qualification procedure, as well as measurement result of a single ASIC are presented and discussed.

2025 JINST 20 C01026

Summary and Plans

- Since FLAXE is not yet available, next test-beam will use FLAME
  - Unfortunately, it means much more work – FLAME-based setup (PCB production etc…) now and FLAXE setup in the FUTURE
- New FLAXE production is needed
  - we are preparing a slightly modified FLAXE version
  - we hope for production in February-March...
  - I hope to have enough money for production...
- and … be optimistic :)

Thank you for attention