



AKADEMIA GÓRNICZO-HUTNICZA
IM. STANISŁAWA STASZICA W KRAKOWIE
AGH UNIVERSITY OF KRAKOW

FLAME-based ECAL-p readout **update / follow up**

This research was funded by the National Science Centre, Poland, under the grant
no. 2021/43/B/ST2/01107

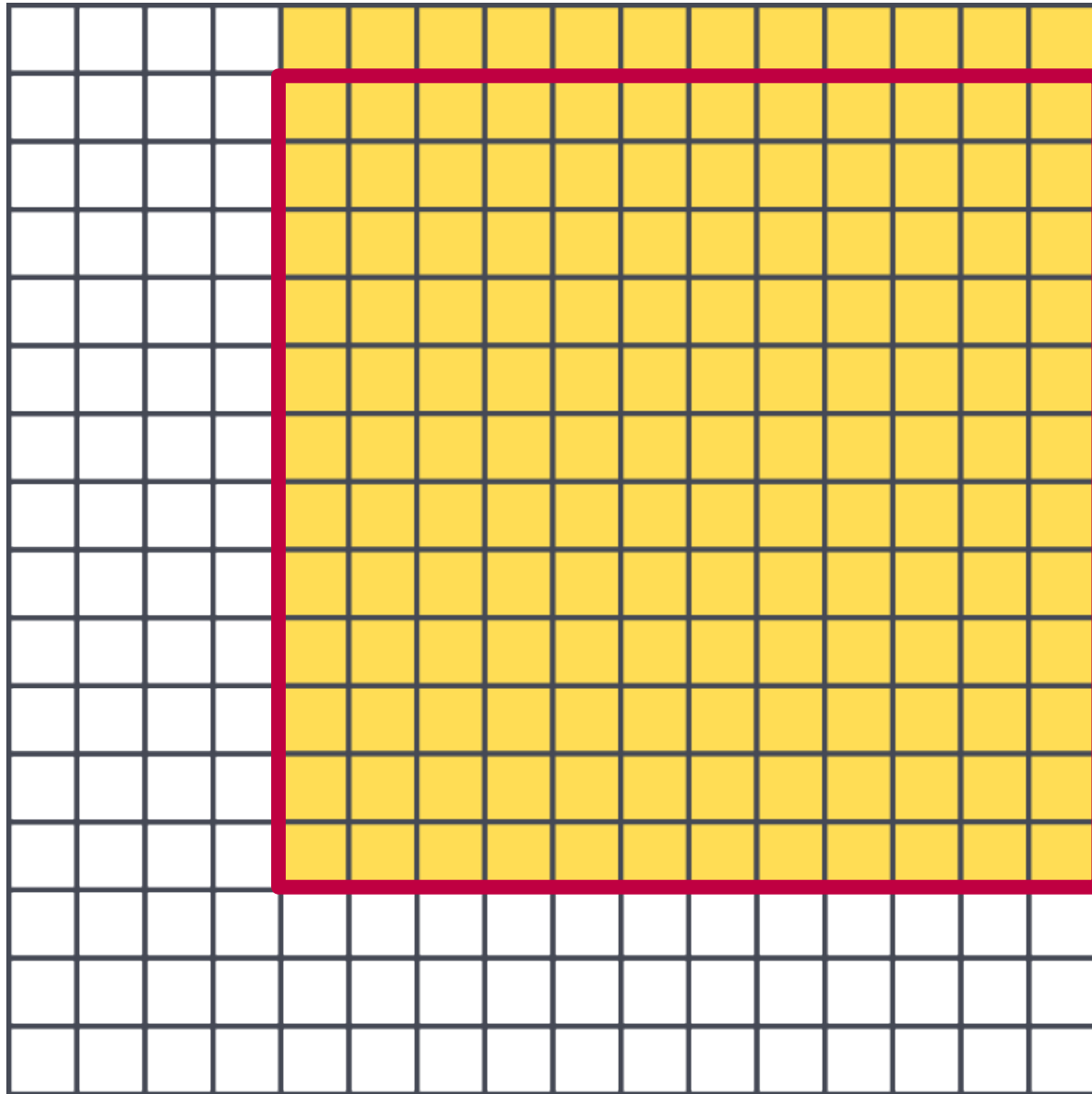
ECAL-p LUXE workshop, 27-31 January 2025, DESY Hamburg

Sensor pad to ASIC channel map

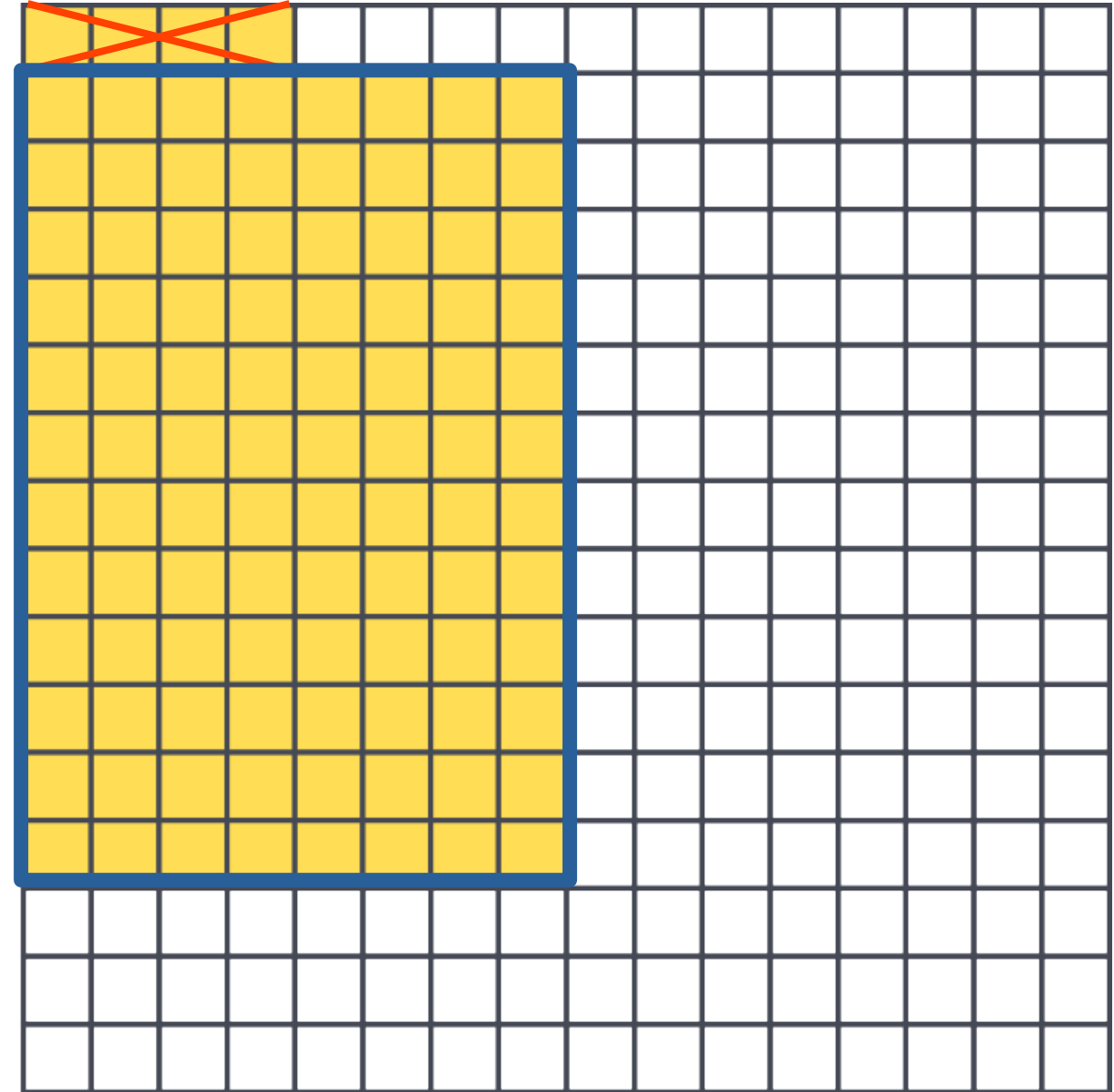
	A0	17	19	21	23	25	27	29	31	17	19	21	23	25	27	29	31	A4	
	A3	16	18	20	22	24	26	28	30	16	18	20	22	24	26	28	30	A7	
	A3	0	2	4	6	8	10	12	14	0	2	4	6	8	10	12	14	A7	
	A3	17	19	21	23	25	27	29	31	17	19	21	23	25	27	29	31	A7	
	A3	1	3	5	7	9	11	13	15	1	3	5	7	9	11	13	15	A7	
	A2	16	18	20	22	24	26	28	30	16	18	20	22	24	26	28	30	A6	
	A2	0	2	4	6	8	10	12	14	0	2	4	6	8	10	12	14	A6	
	A2	17	19	21	23	25	27	29	31	17	19	21	23	25	27	29	31	A6	
	A2	1	3	5	7	9	11	13	15	1	3	5	7	9	11	13	15	A6	
	A1	16	18	20	22	24	26	28	30	16	18	20	22	24	26	28	30	A5	
	A1	0	2	4	6	8	10	12	14	0	2	4	6	8	10	12	14	A5	
	A1	17	19	21	23	25	27	29	31	17	19	21	23	25	27	29	31	A5	
	A1	1	3	5	7	9	11	13	15	1	3	5	7	9	11	13	15	A5	
	A0	16	18	20	22	24	26	28	30	16	18	20	22	24	26	28	30	A4	
	A0	0	2	4	6	8	10	12	14	0	2	4	6	8	10	12	14	A4	
	A0	1	3	5	7	9	11	13	15	1	3	5	7	9	11	13	15	A4	

Outdated

Sensor instrumentation



12 columns x 13 rows
row on top edge to test leackage



8 columns x 12 rows + 4 pads on top
4 pads on top row may have large noise

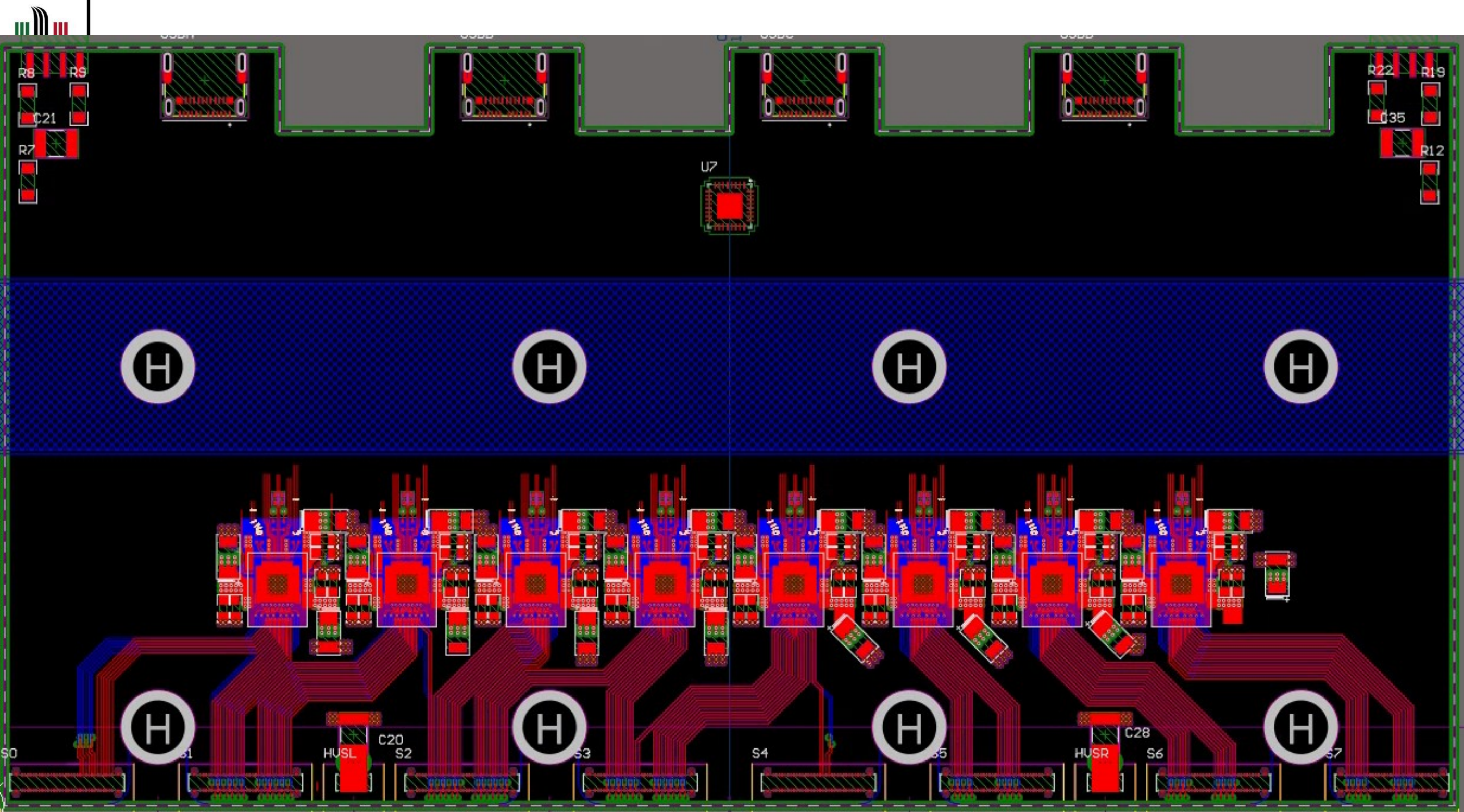
Sensor instrumentation

Last chance to change it is now!

***If anyone has any objections speak
now or forever hold your peace***

12 columns x 13 rows
row on top edge to test leackage

8 columns x 12 rows + 4 pads on top
4 pads on top row may have large noise



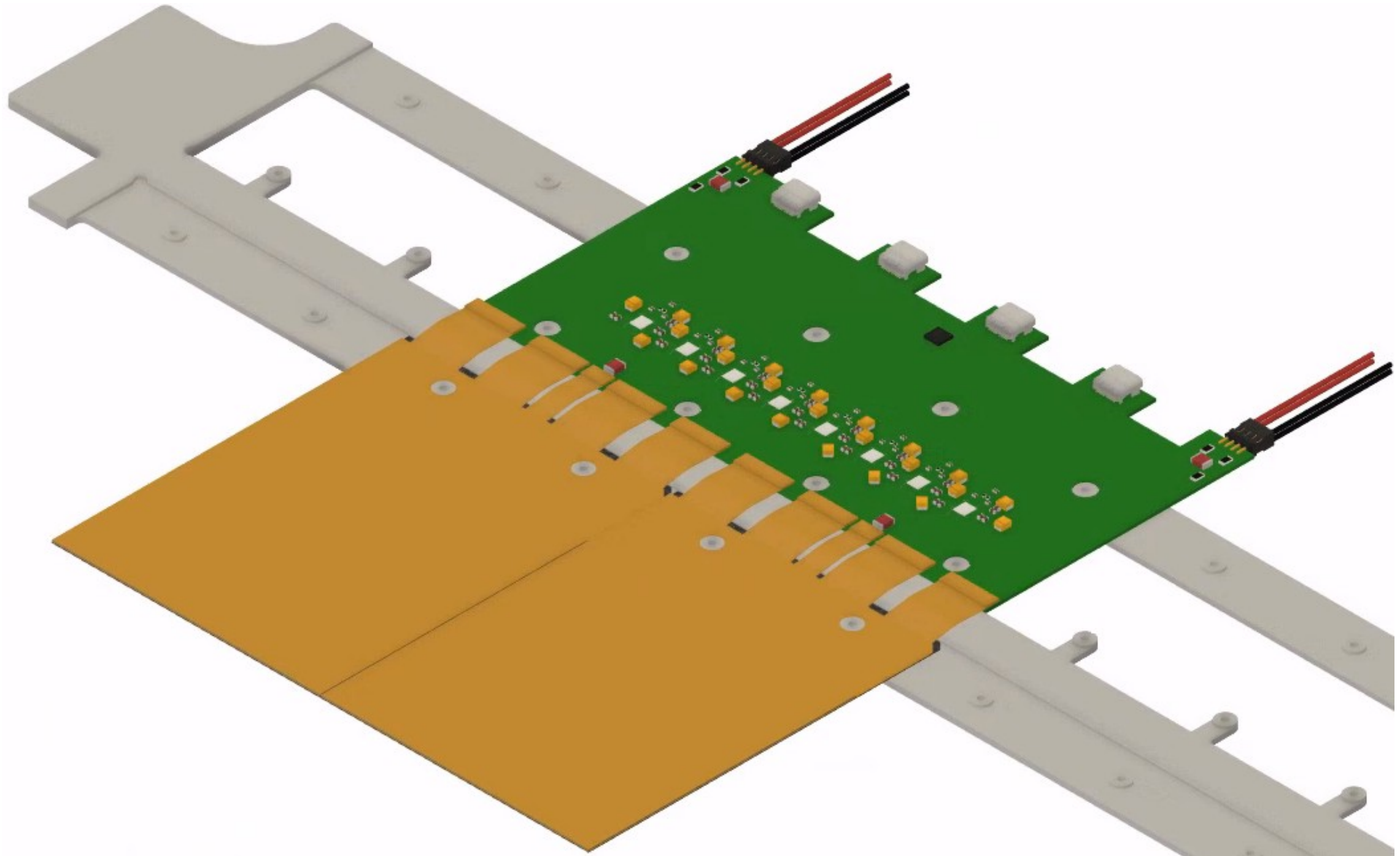
Updated channel map

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	...
15				A0	0	2	4	6	8	10	1	3	5	7	9	11	29	31	28	30					A4		
14				A4	4	6	8	10	12	14	16	18	20	22	24	26	16	18	20	22	24	26	28	30	A7		
13			A3	A4	12	14	16	18	20	22	24	26	28	30	0	2	0	2	4	6	8	10	12	14	A7		
12				A4	5	7	9	11	13	15	17	19	21	23	25	27	17	19	21	23	25	27	29	31	A7		
11			A3	A4	13	15	17	19	21	23	25	27	29	31	1	3	1	3	5	7	9	11	13	15	A7		
10			A2	A3	20	22	24	26	28	30	0	2	4	6	8	10	16	18	20	22	24	26	28	30	A6		
9			A1	A2	28	30	0	2	4	6	8	10	12	14	16	18	0	2	4	6	8	10	12	14	A6		
8			A2	A3	21	23	25	27	29	31	1	3	5	7	9	11	17	19	21	23	25	27	29	31	A6		
7			A1	A2	29	31	1	3	5	7	9	11	13	15	17	19	1	3	5	7	9	11	13	15	A6		
6				A1	4	6	8	10	12	14	16	18	20	22	24	26	16	18	20	22	24	26	28	30	A5		
5			A0	A1	12	14	16	18	20	22	24	26	28	30	0	2	0	2	4	6	8	10	12	14	A5		
4				A1	5	7	9	11	13	15	17	19	21	23	25	27	17	19	21	23	25	27	29	31	A5		
3			A0	A1	13	15	17	19	21	23	25	27	29	31	1	3	1	3	5	7	9	11	13	15	A5		
2																											
1																											
0																											

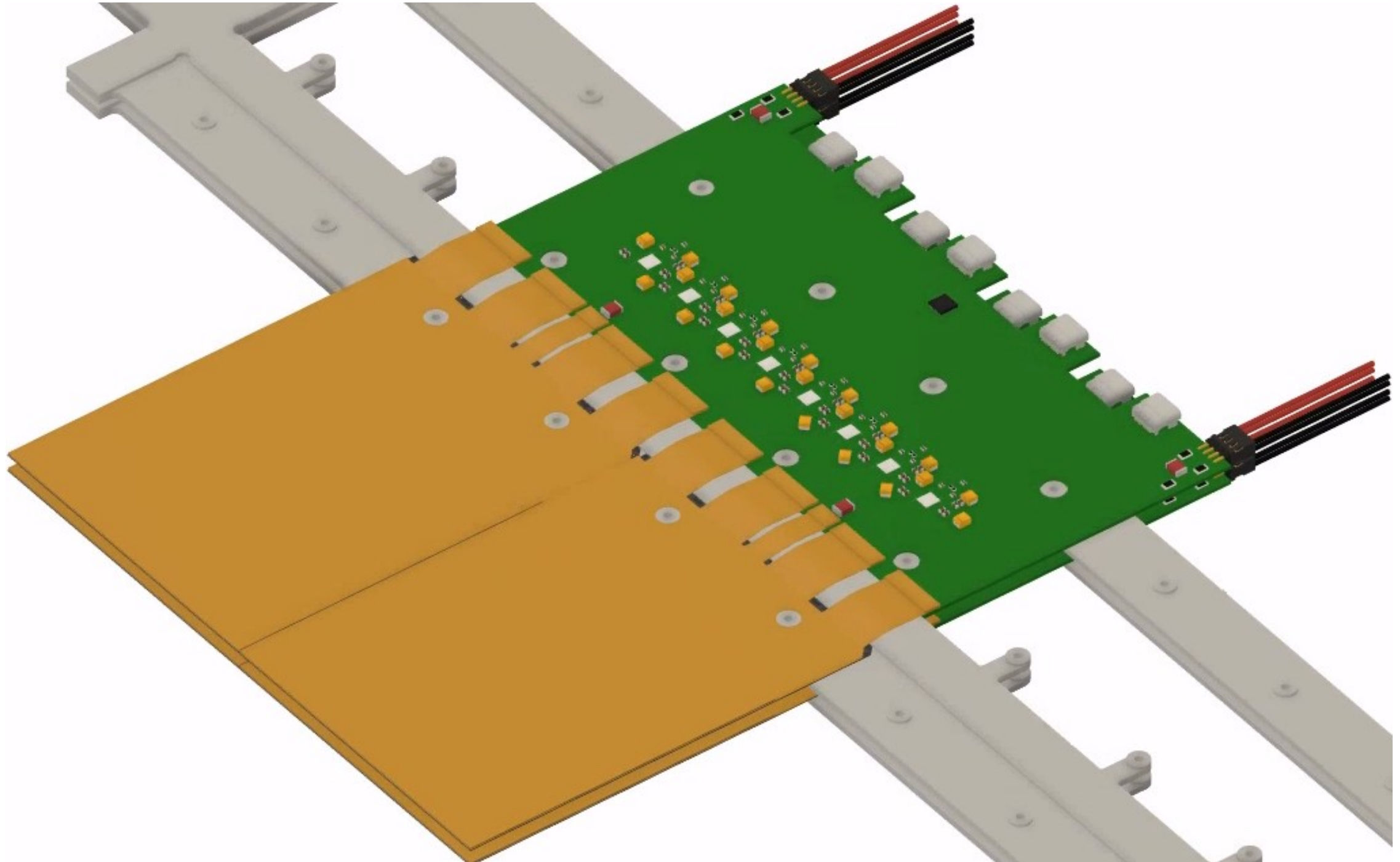
Proposed logical channel numbering in data file

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
15	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
14	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
13	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
12	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
11	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
10	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

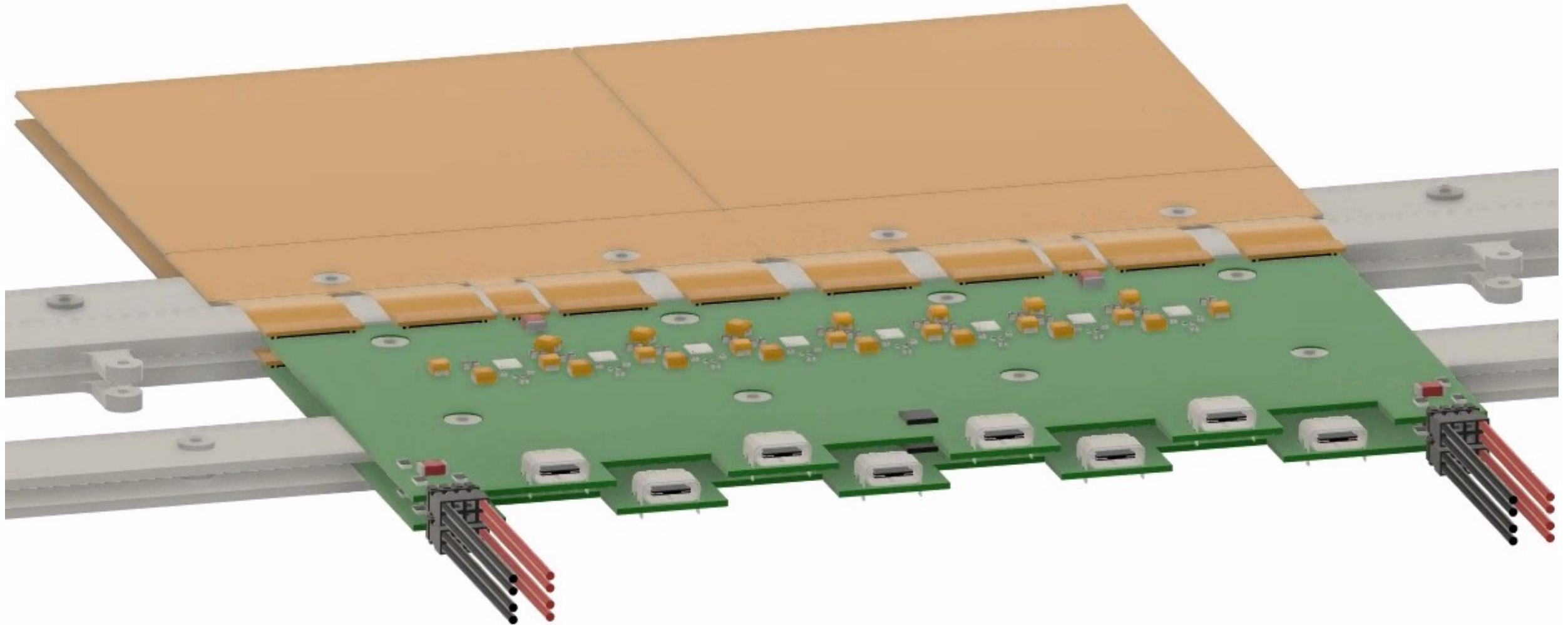
More realistic FEB



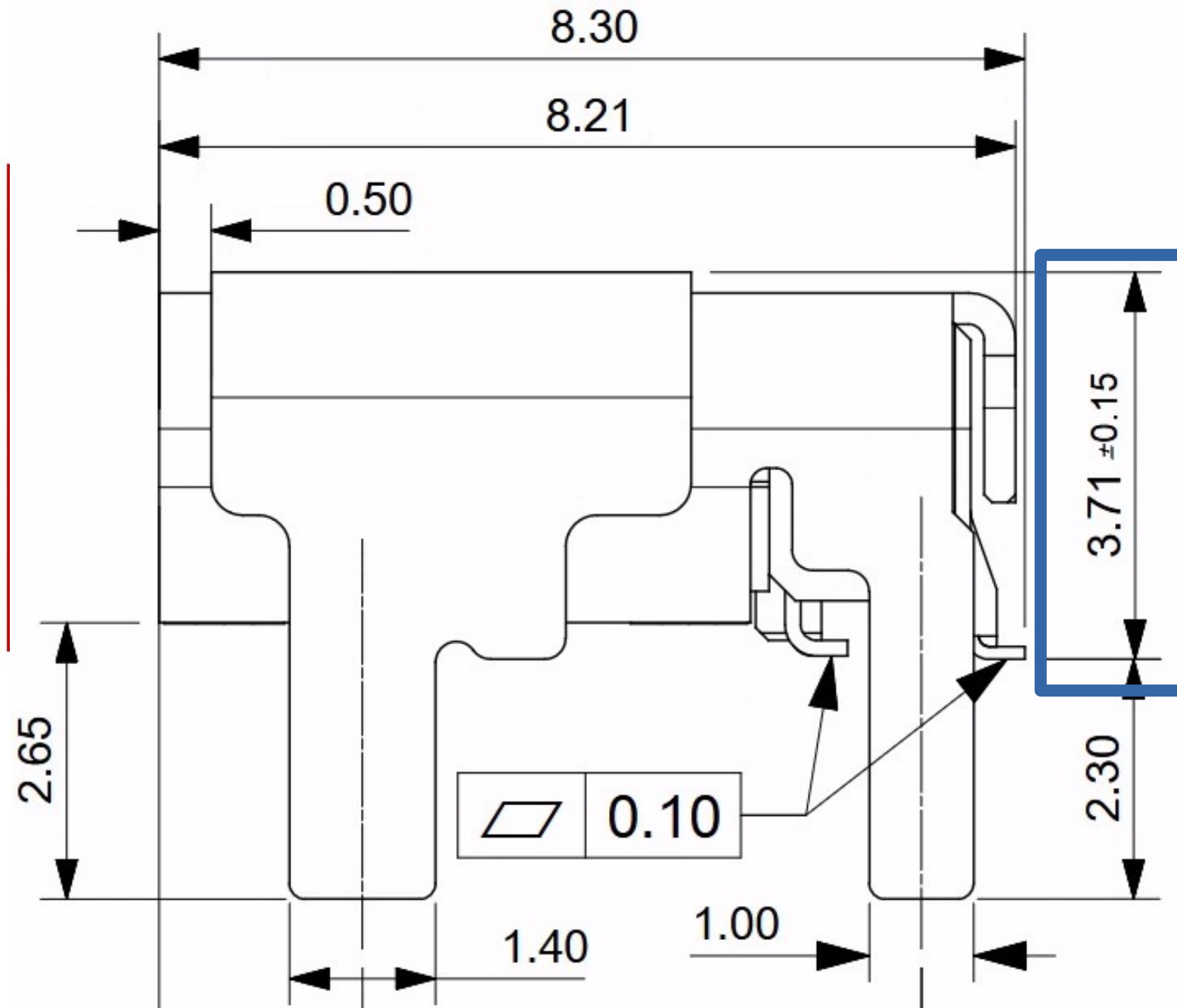
More realistic FEB - two layers



More realistic FEB - two layers



FEB USB socket thickness



PCB thickness:

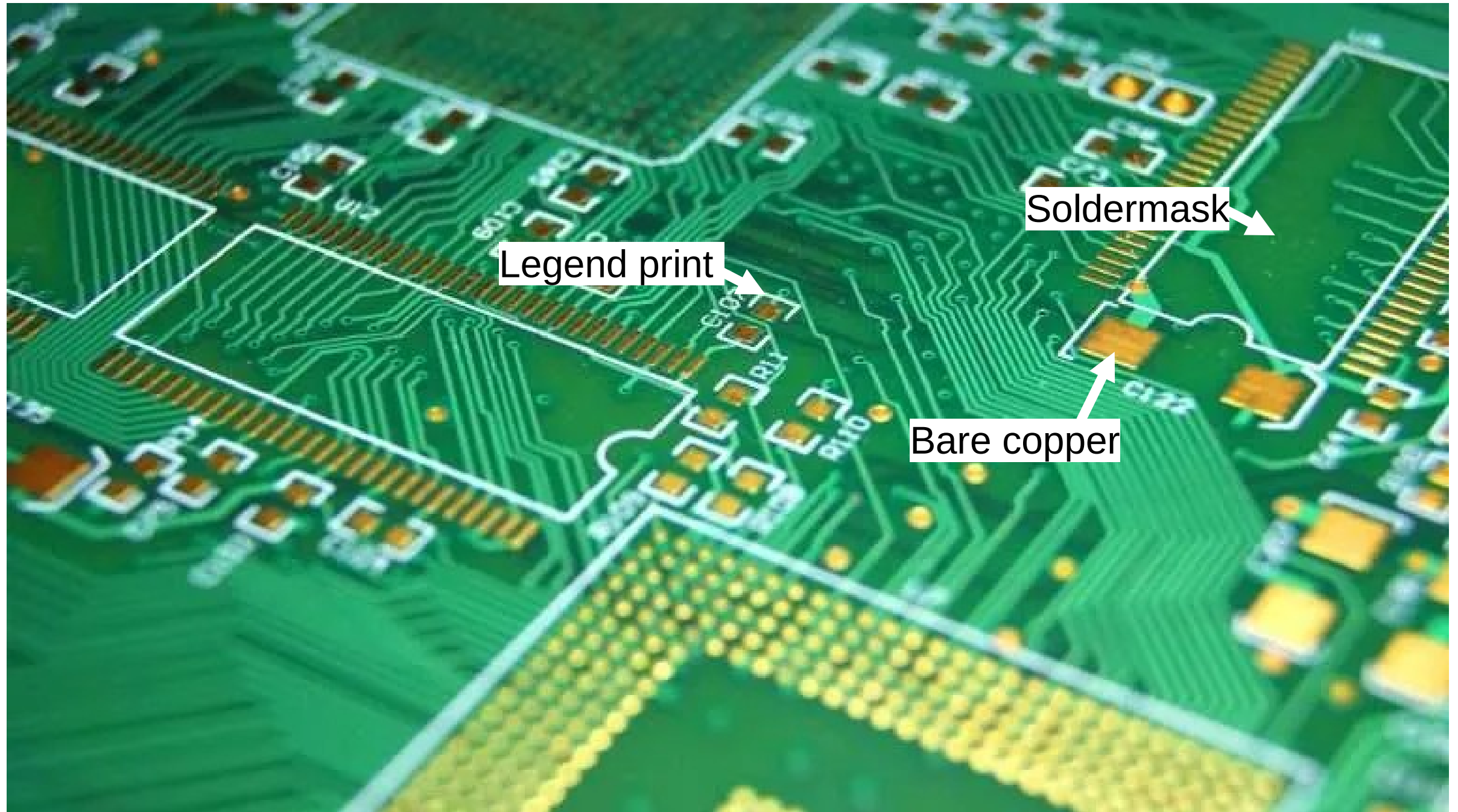
- Top surface to bottom surface:
910 μm $\pm$ 5%
- Copper: **+35 μm** on each side
- Soldermask:
+25 μm on each side
- Legend print:
+25 μm (top side only)

Worst case for USB height:

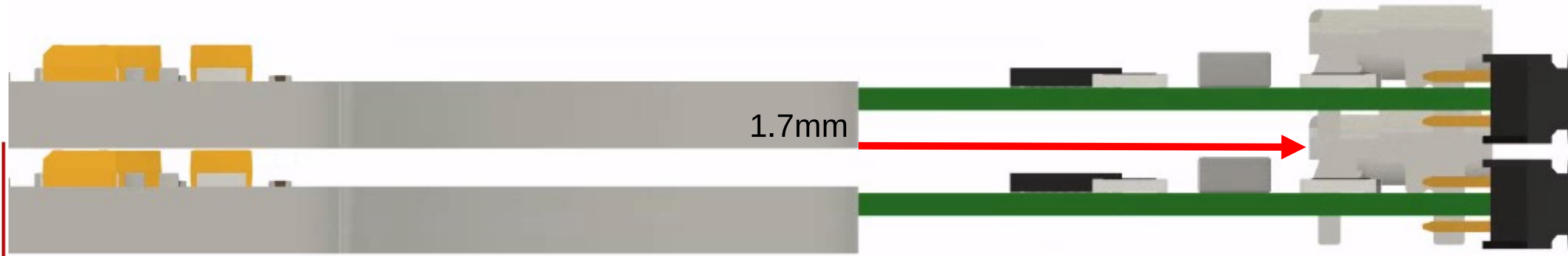
Bottom soldermask + PCB (+5%) + top copper + USB socket height:
4.875 mm > 4.7 mm

Best case: 4.485 mm, but we cannot count on this...

FEB USB socket thickness



Collision of Tframe with USB socket



We have interference of the Tframe with the USB sockets during assembly process:

- Tframe of the first (previous) layer hits socket on the second (next) layer during assembly or removal
- There is no interference if the second (last) layer is removed first

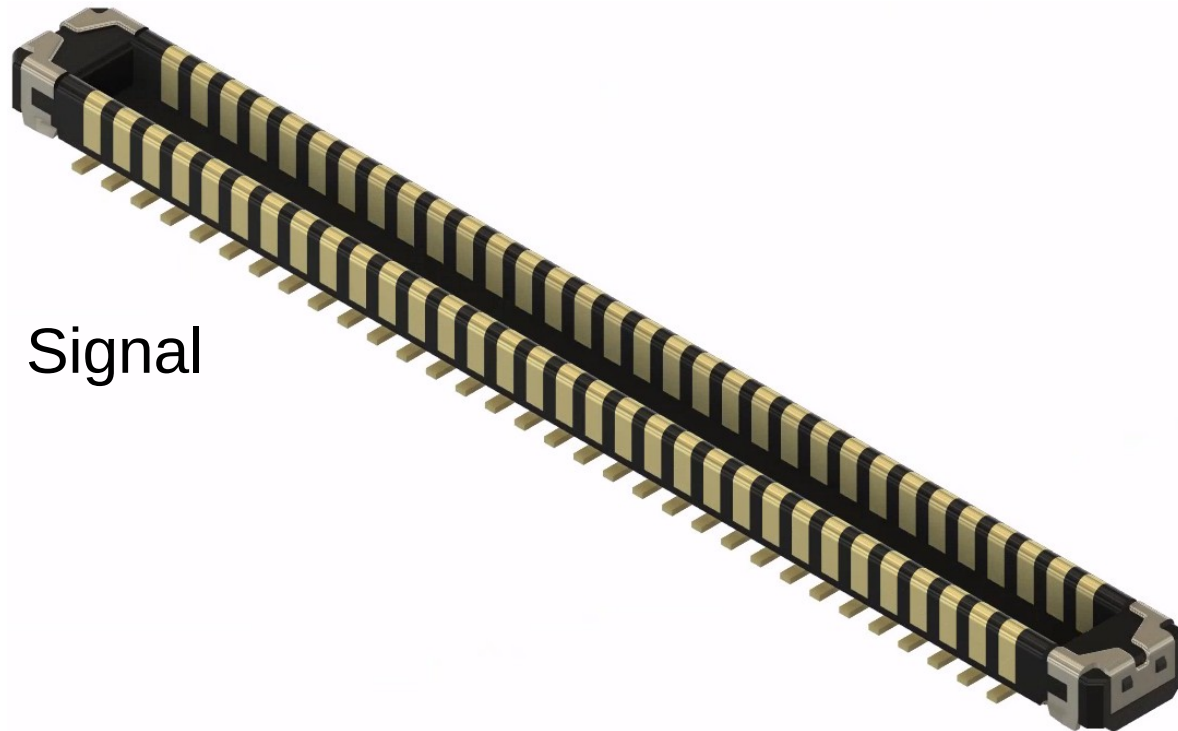
Consequences:

- Calorimeter have to be assembled from front to back (and disassembled from back to front)
- There is no way to remove arbitrary selected layer – only back-to-front order
- This disables the possibility of removal the first layer before adding the FCAL tungsten in front – *we already have some solutions*

Parts purchase

BM23PF0.8-64DP-0.35V

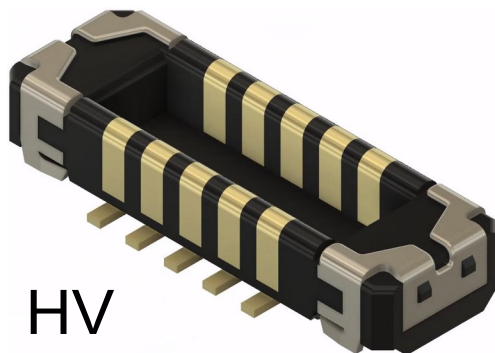
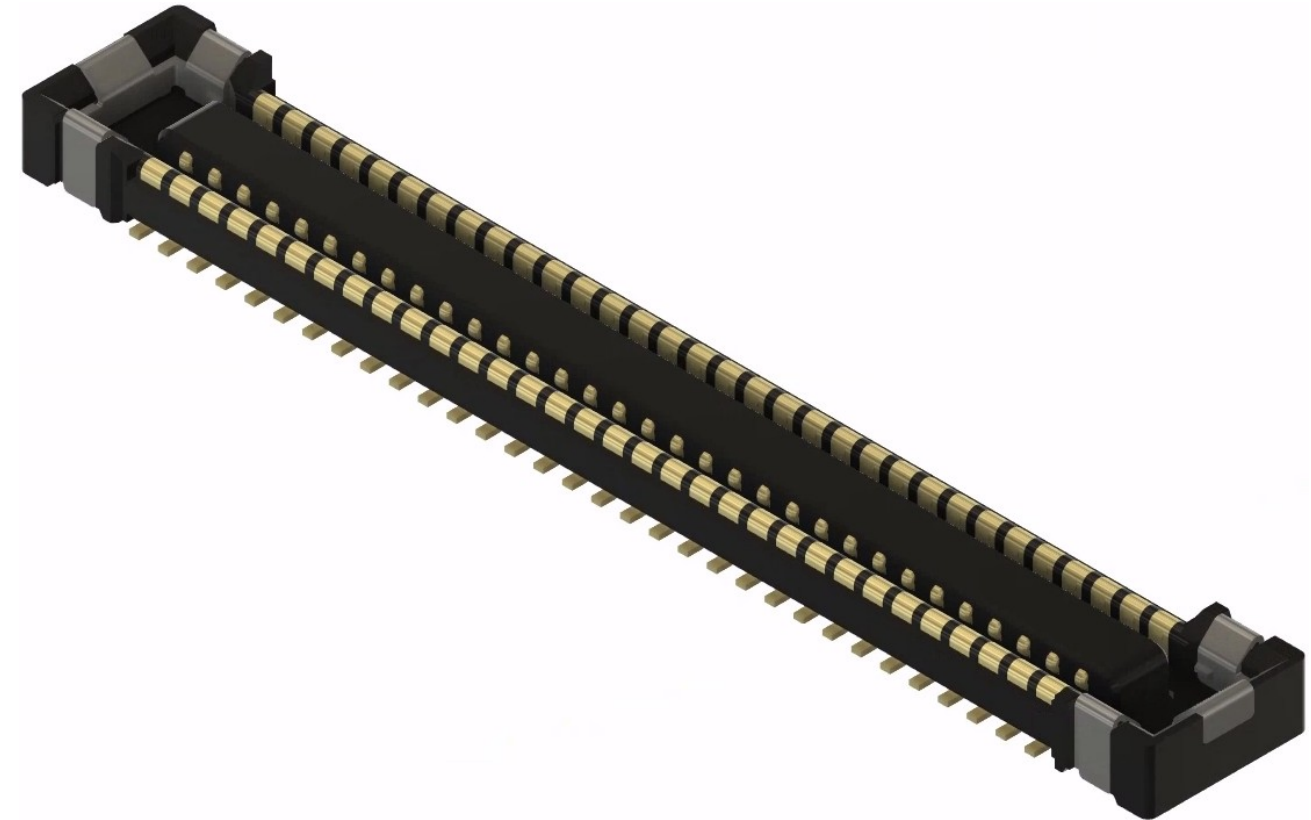
Plug – flex



Signal

BM23PF0.8-64DS-0.35V

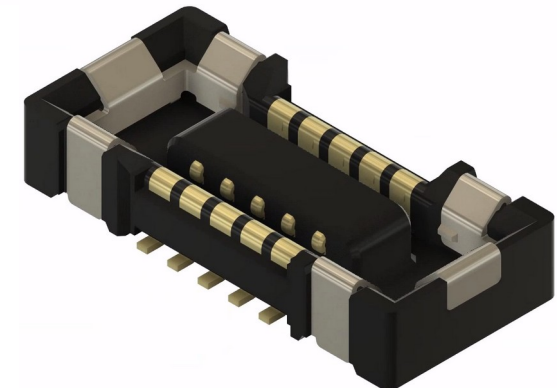
Socket – FEB



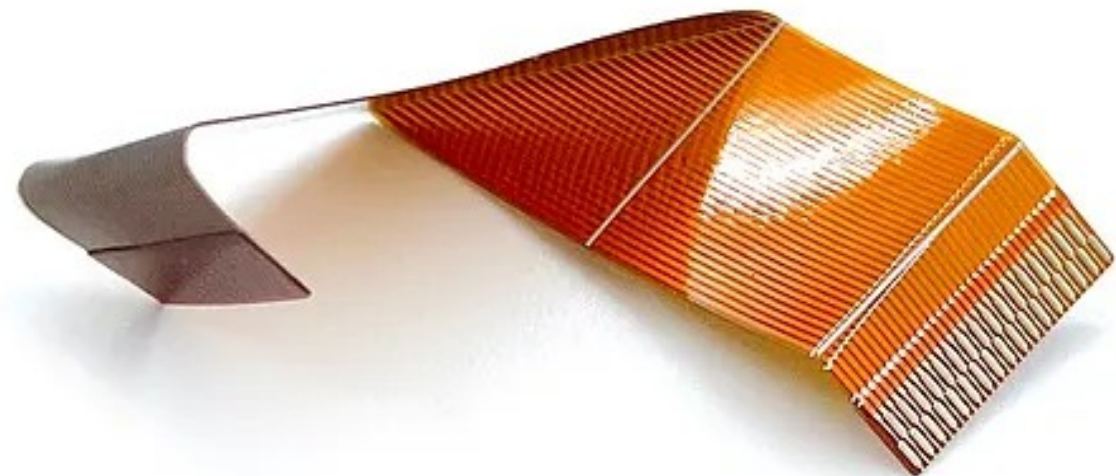
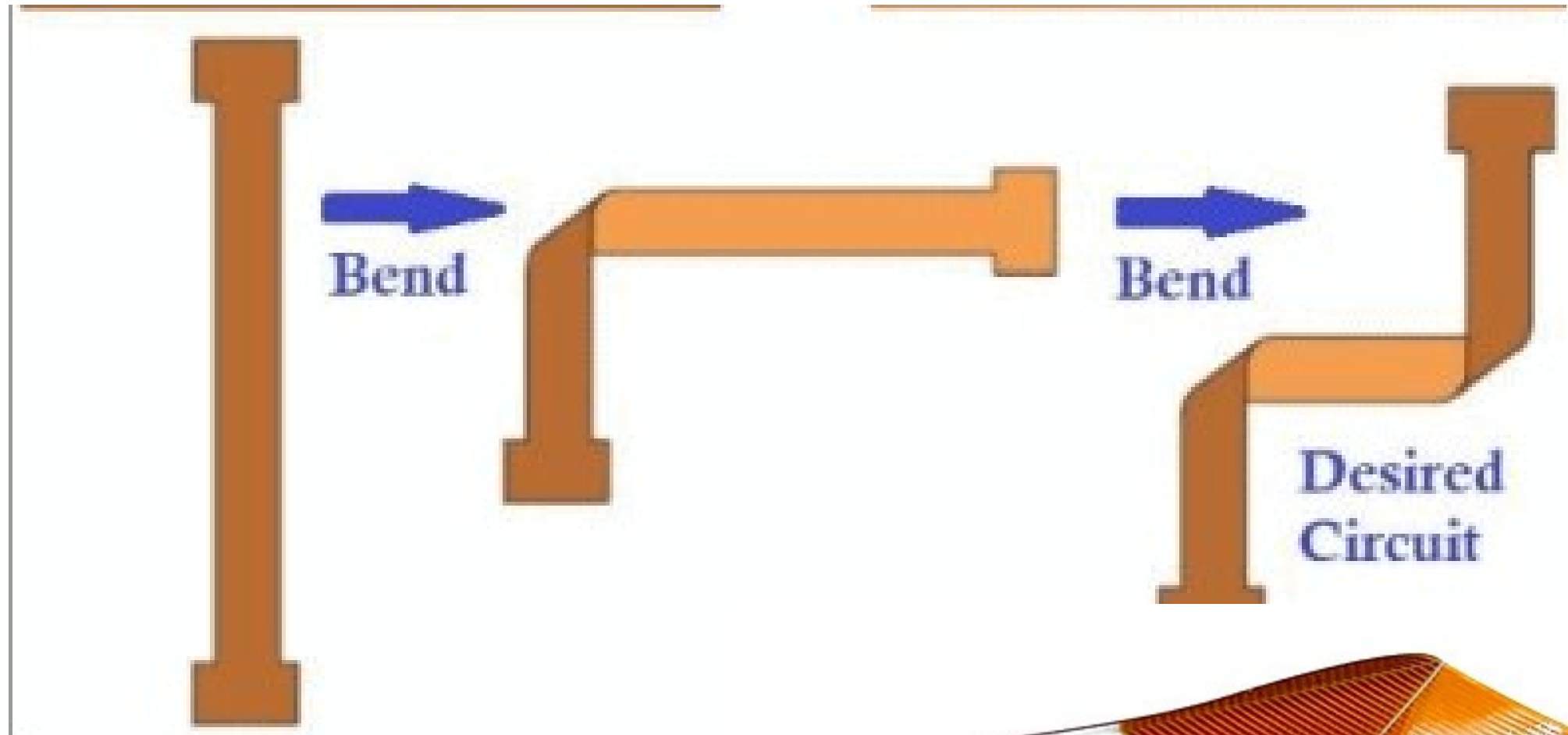
HV

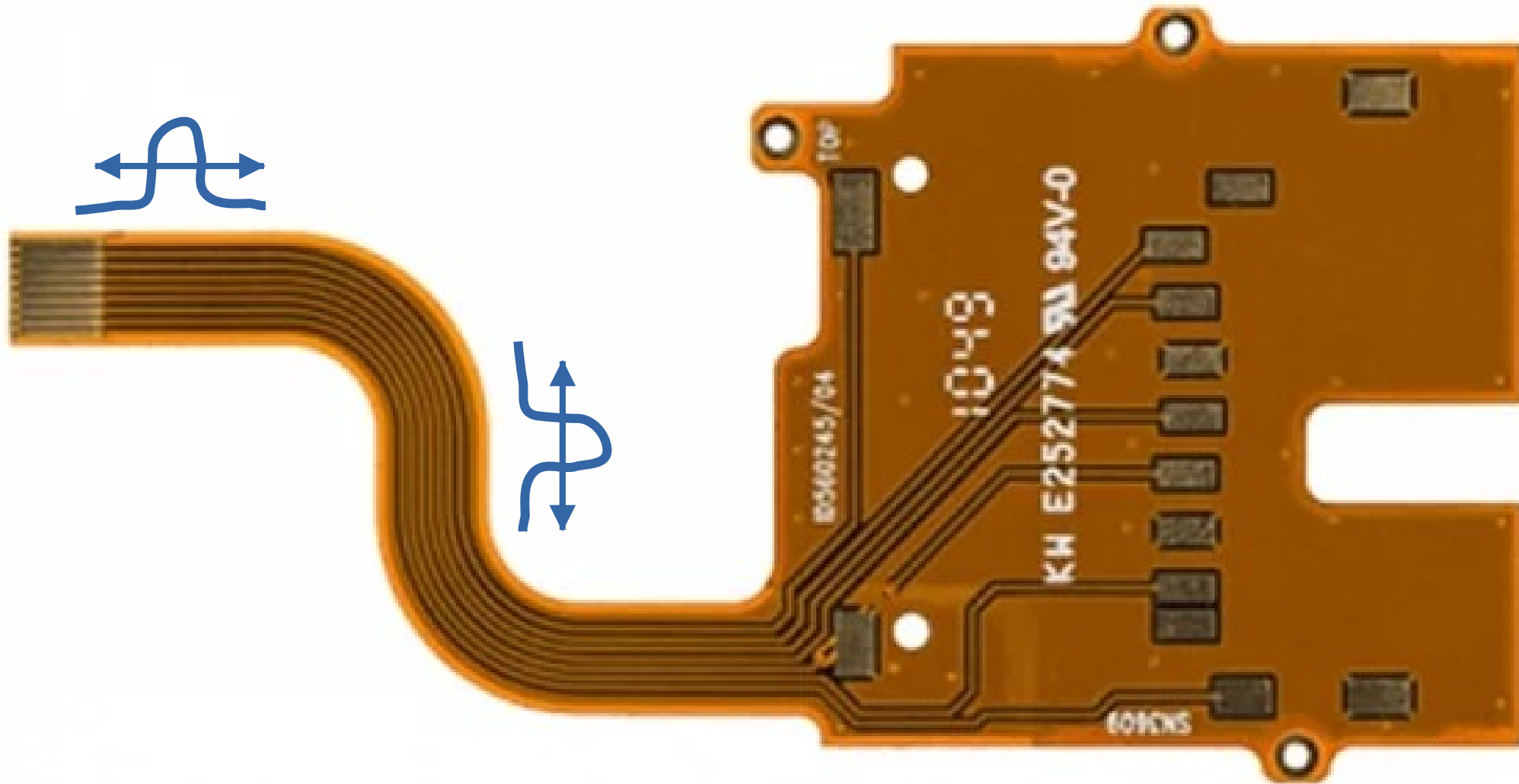
Who buy what?

- Yan – plugs for flex
- Me – sockets for FEB



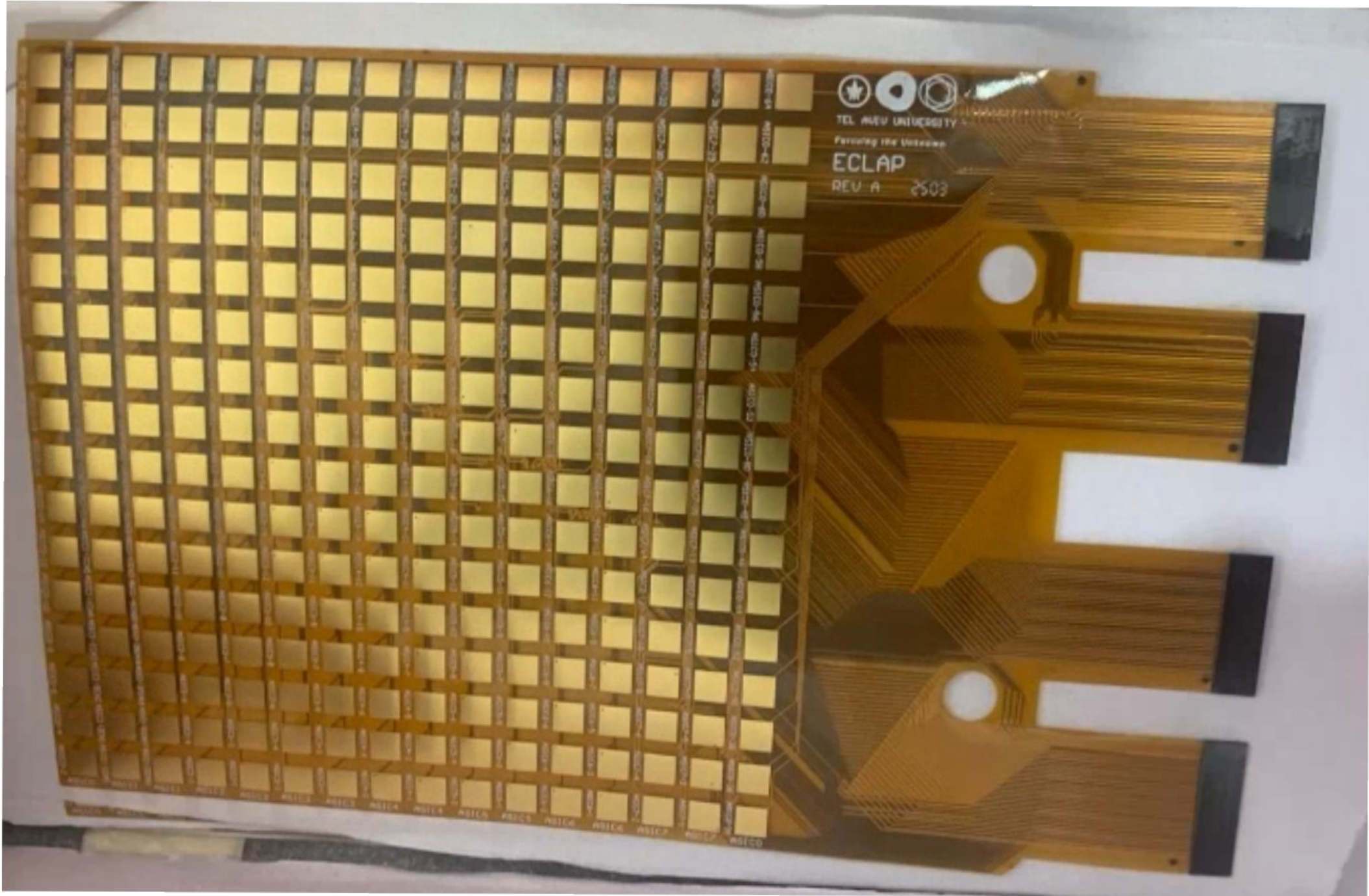
Possible solution for fanout flex



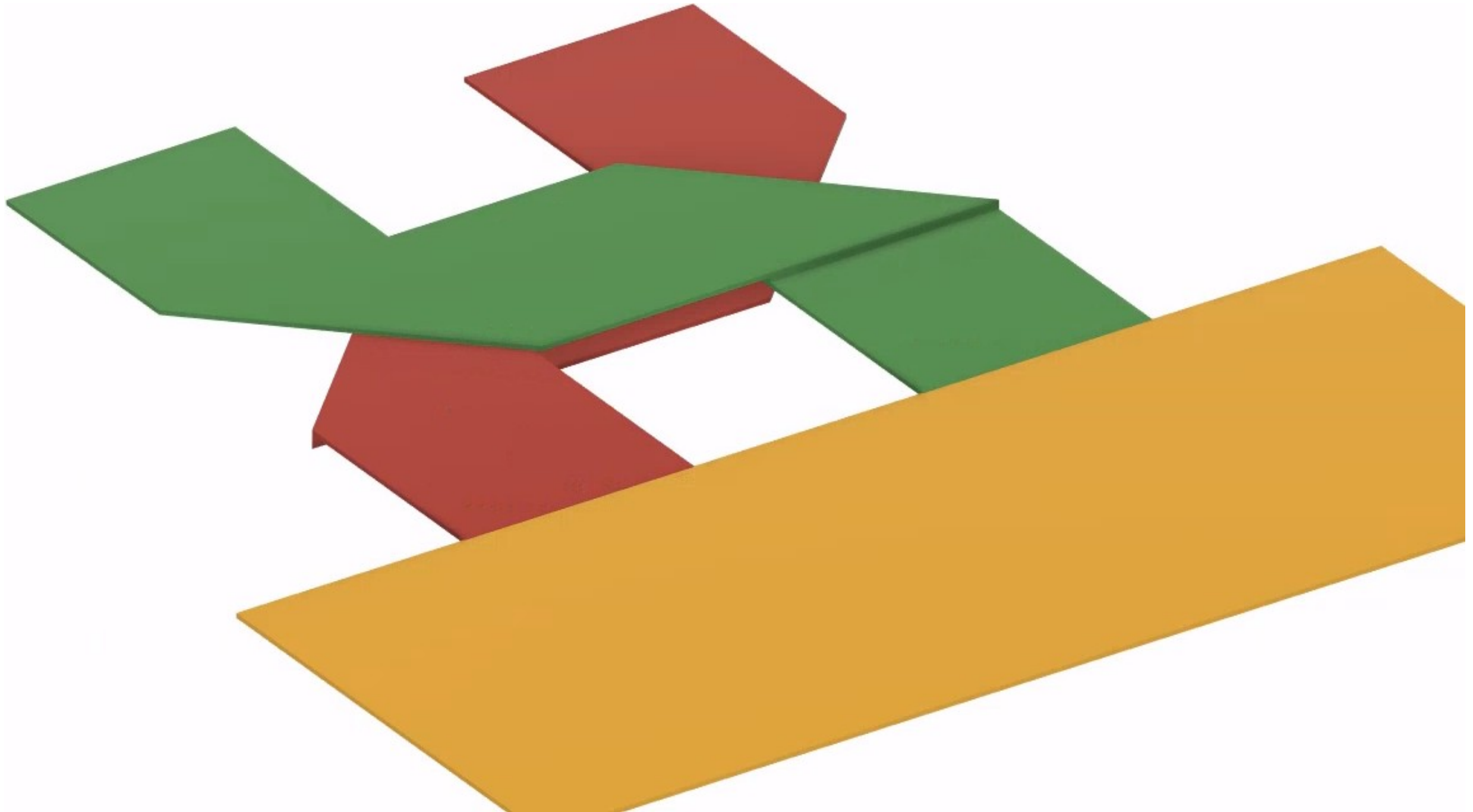


Two degrees of freedom in connector position – fanout to FEB connector alignment can be extremely relaxed!

Possible solution for fanout flex



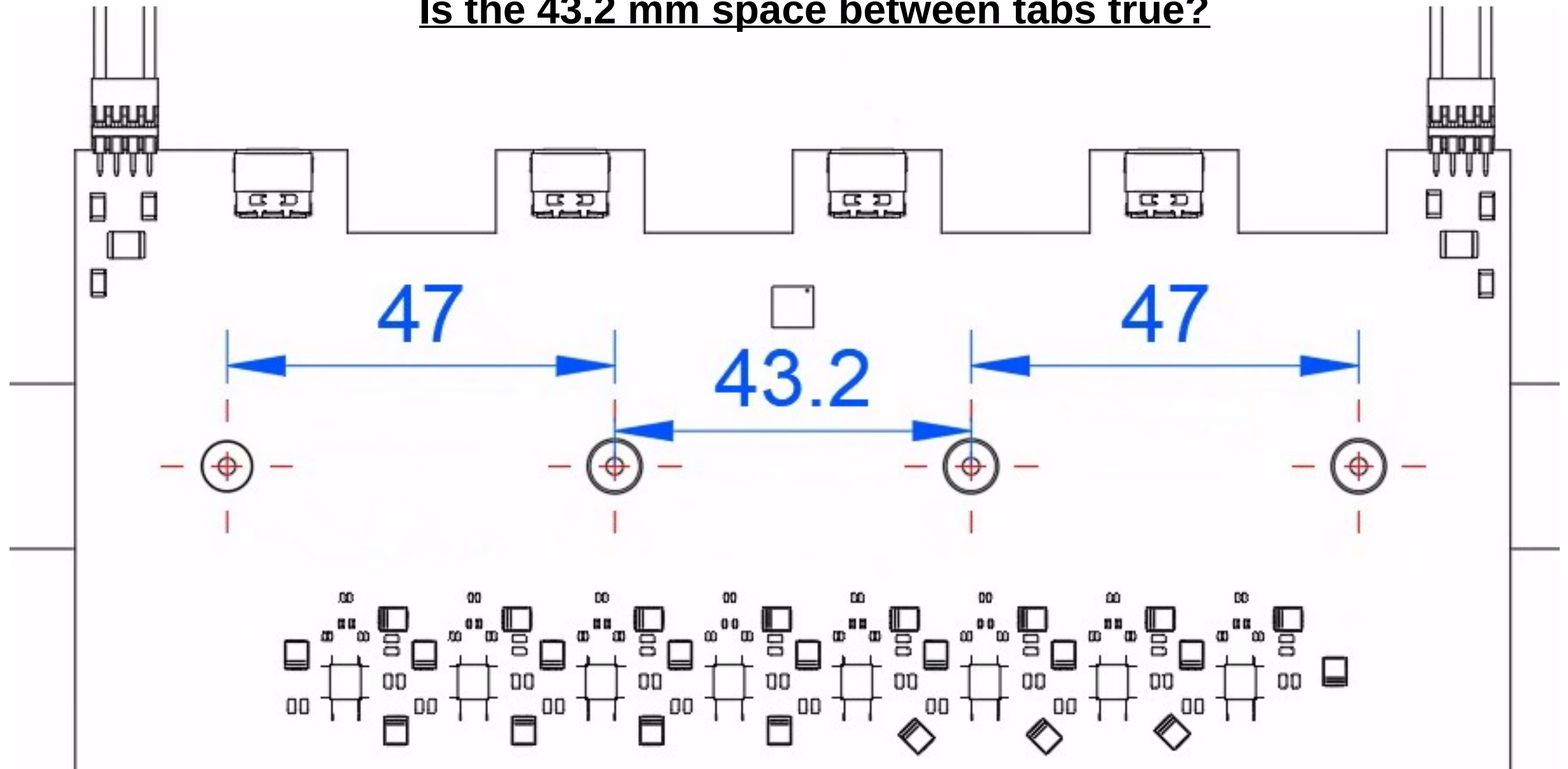
Possible solution for fanout flex



Request to Warsaw crew: Please keep the design in the GitLab repository up to date!

- There are no 1.2mm combs available
- Name the parts in English please
- The 0.3mm gap between the sensors is still true?

Is the 43.2 mm space between tabs true?



Additional tungsten

