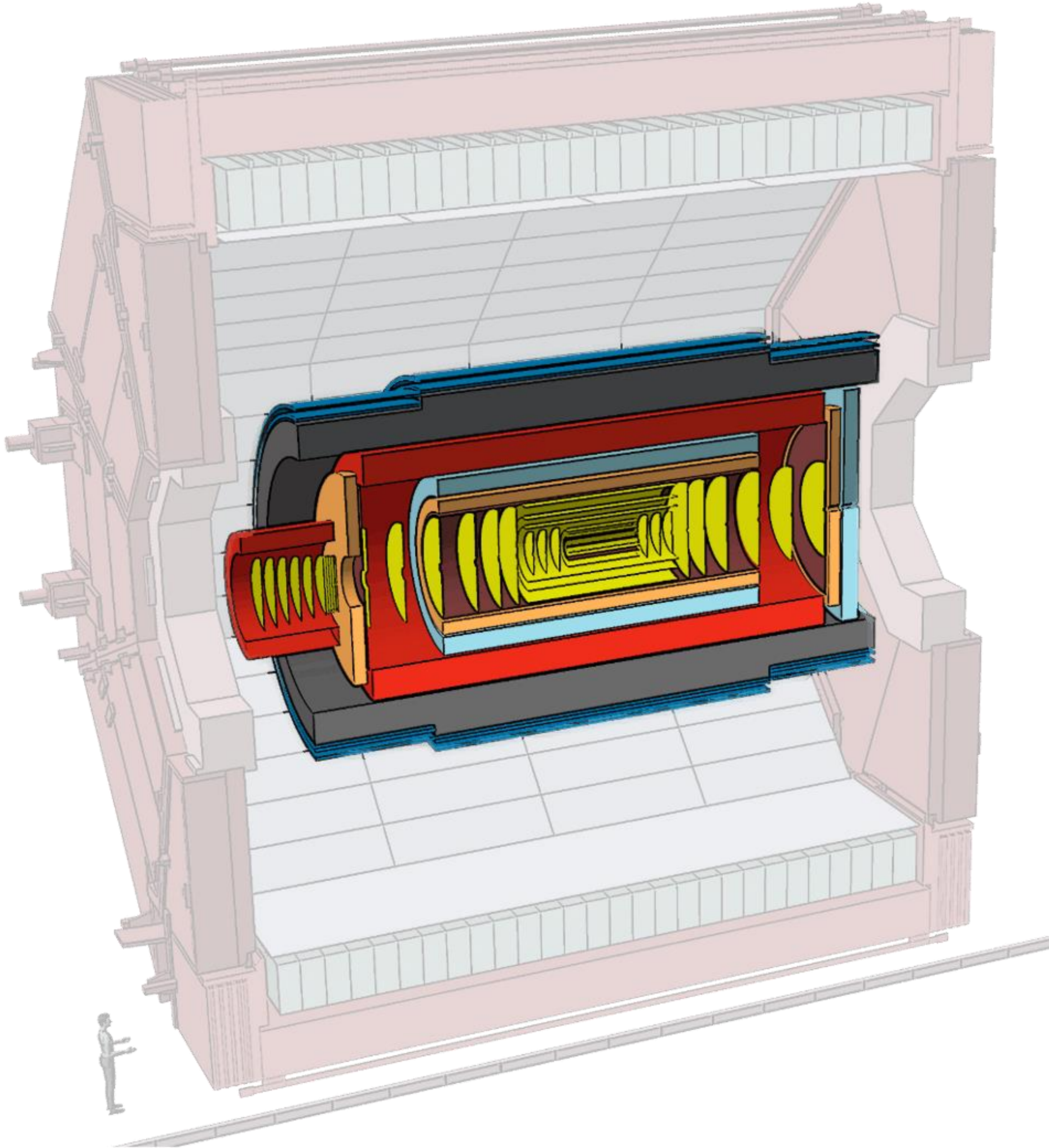
Tracking systems of ALICE 3

A new heavy-ion detector at the LHC

17th Terascale Detector Workshop 2025
20.03.2025

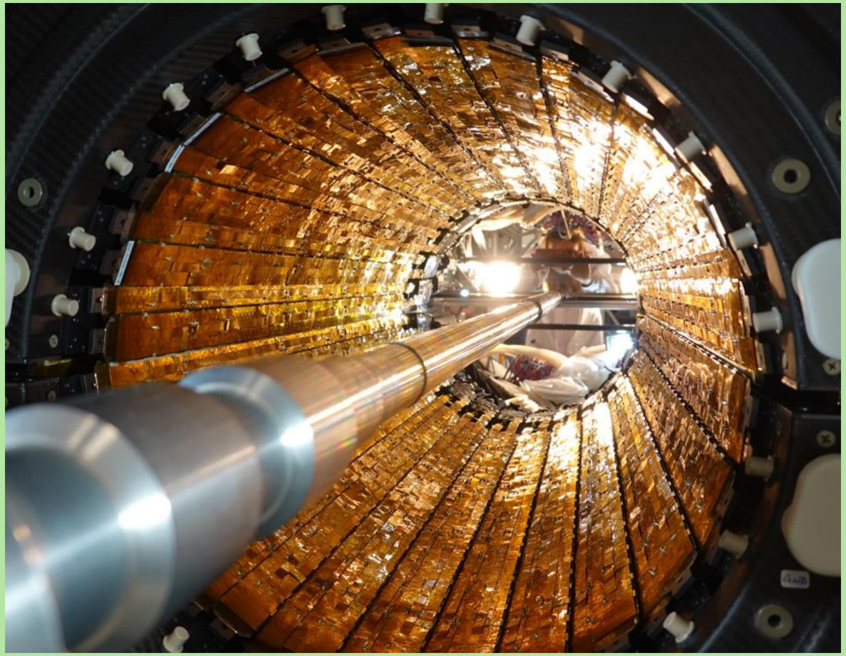
Berkin Ulukutlu (TUM) on behalf of
ALICE Collaboration

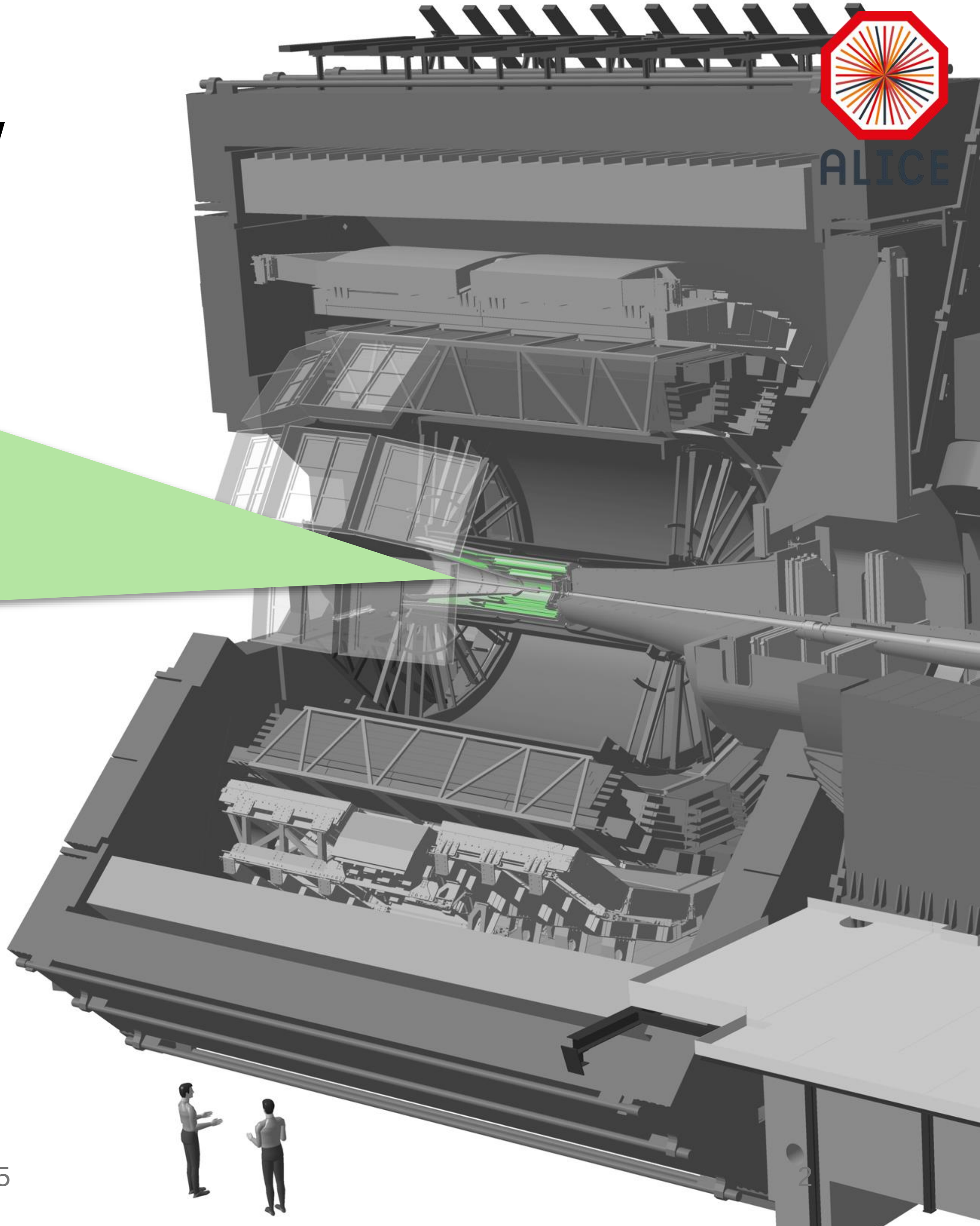


Tracking in ALICE: Now

ALICE ITS2 based on ALPIDE MAPS

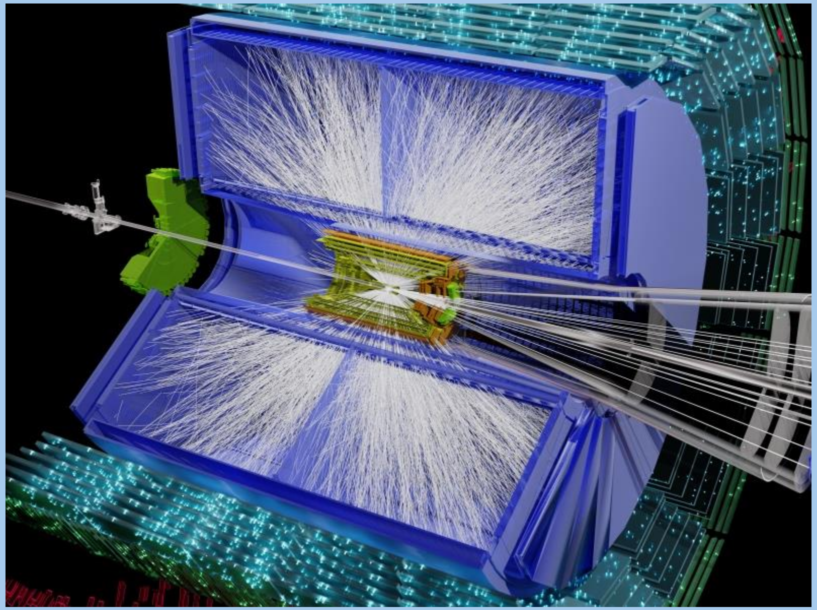
- 10 m^2 area
- 12.5 billion pixels with size of ~29x27 μm
- [F. Reidt et al. NIM A (2022) 166632]



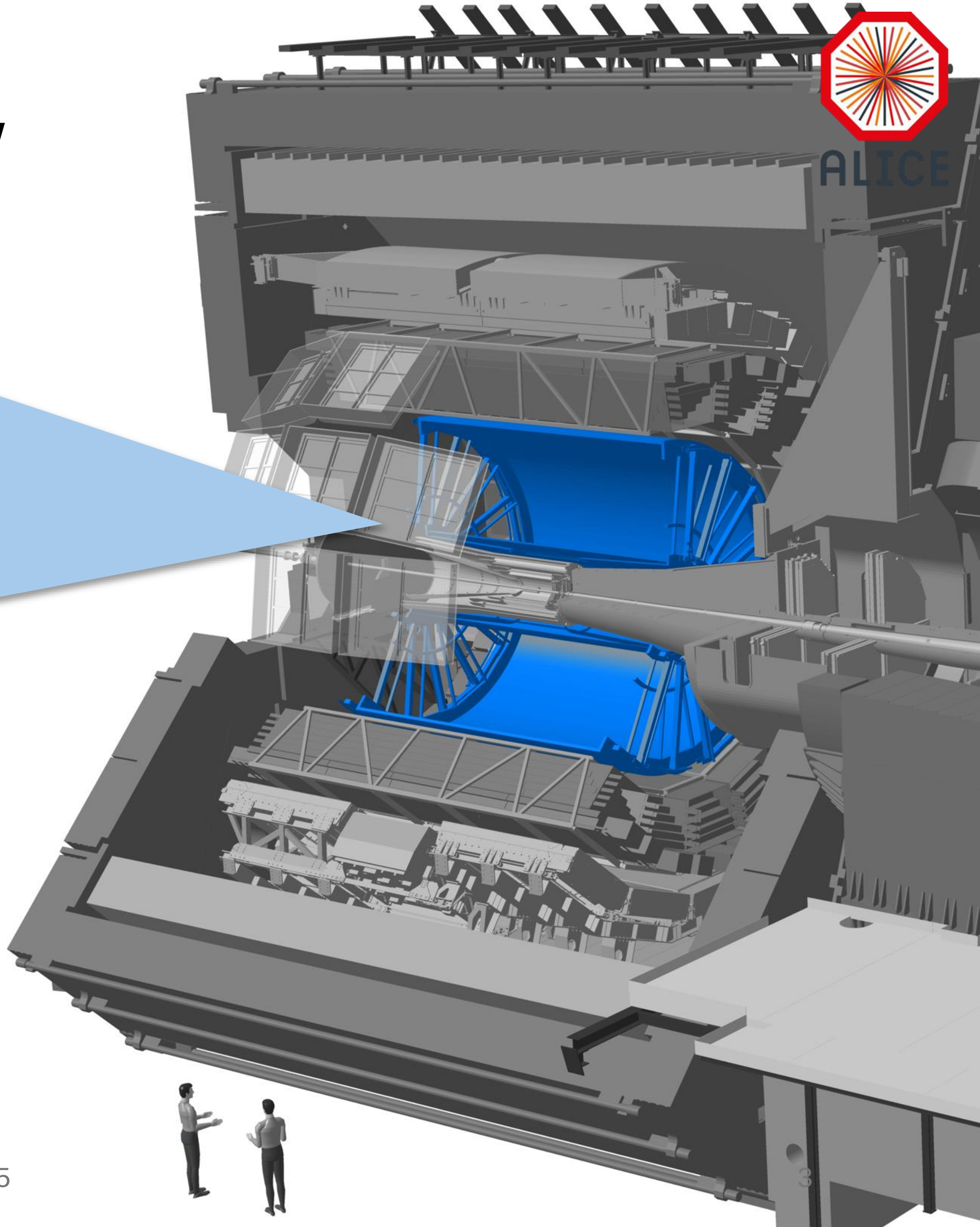


Tracking in ALICE: Now

ALICE TPC based on GEMs
- Continuous readout
- PID via d*E*/dx measurement
- [ALICE TPC coll. 2021 JINST 16 P03022]

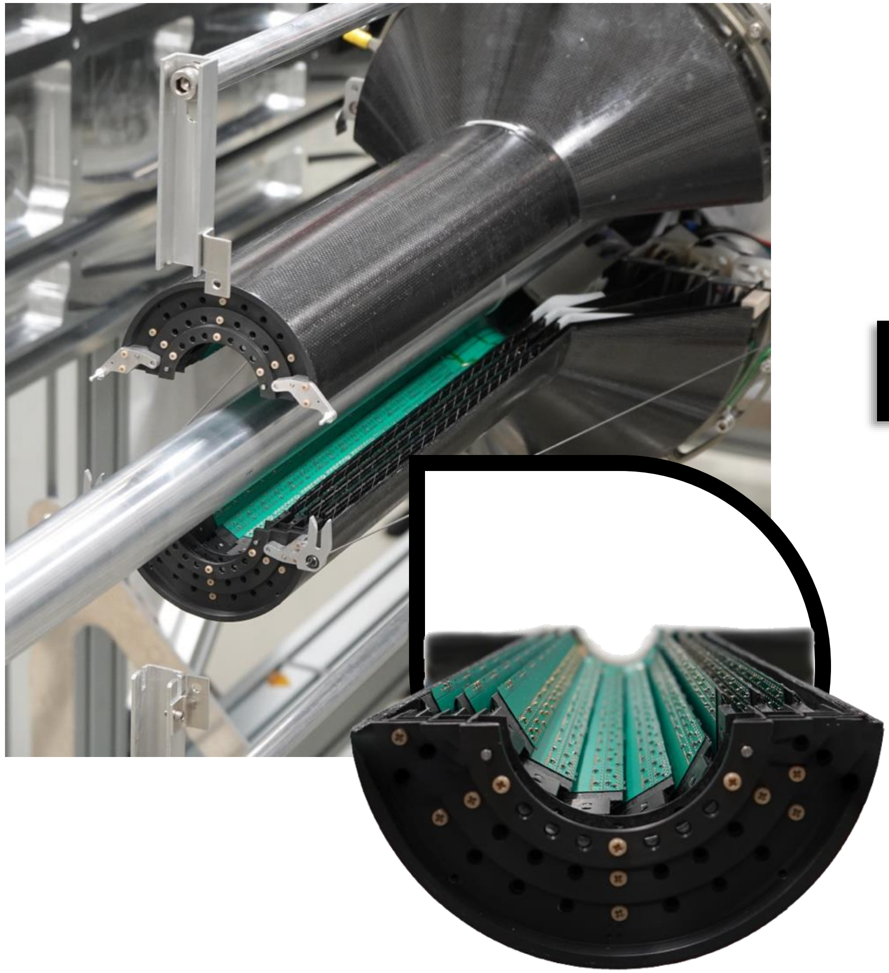


- **Precedent in Bonn:** FOPI TPC was the first ungated GEM TPC [NIM A 869 (2017) FOPI TPC]

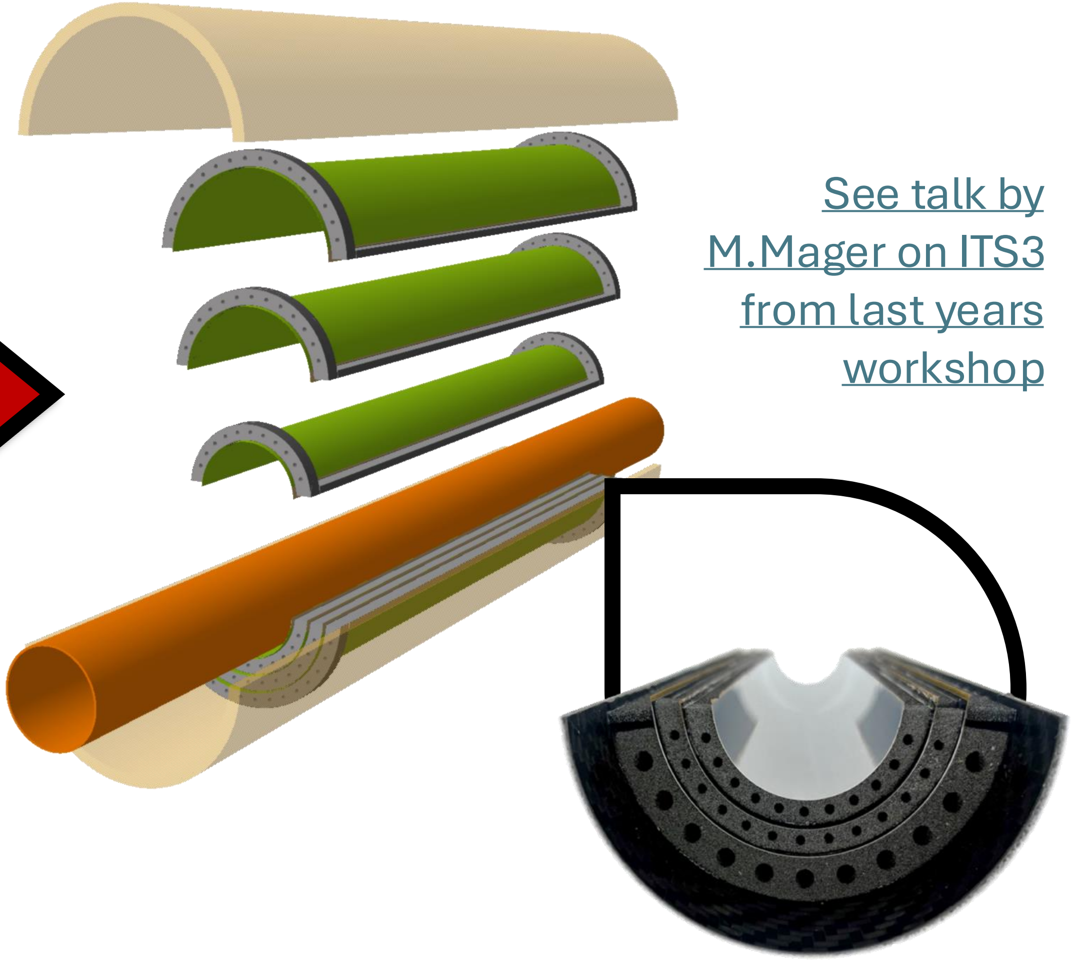


Tracking in ALICE: Next step ITS3

ALICE ITS2 Inner Barrel



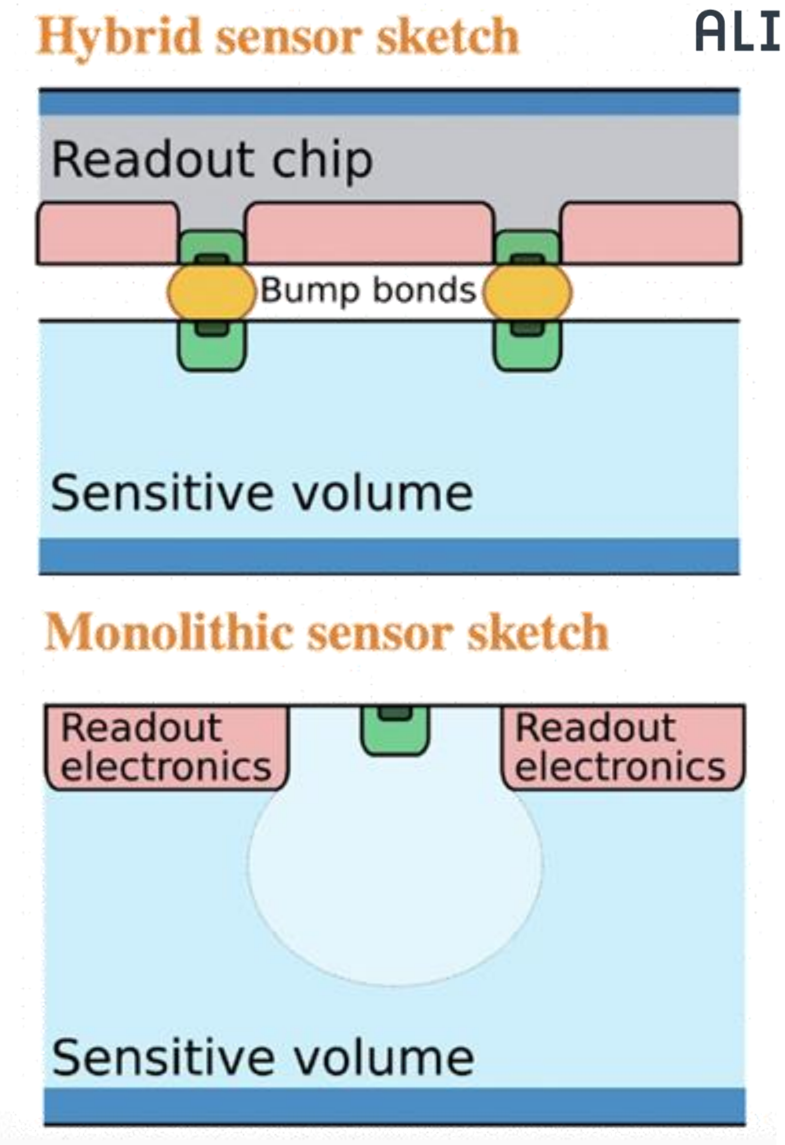
ALICE ITS3



[See talk by M.Mager on ITS3 from last years workshop]()

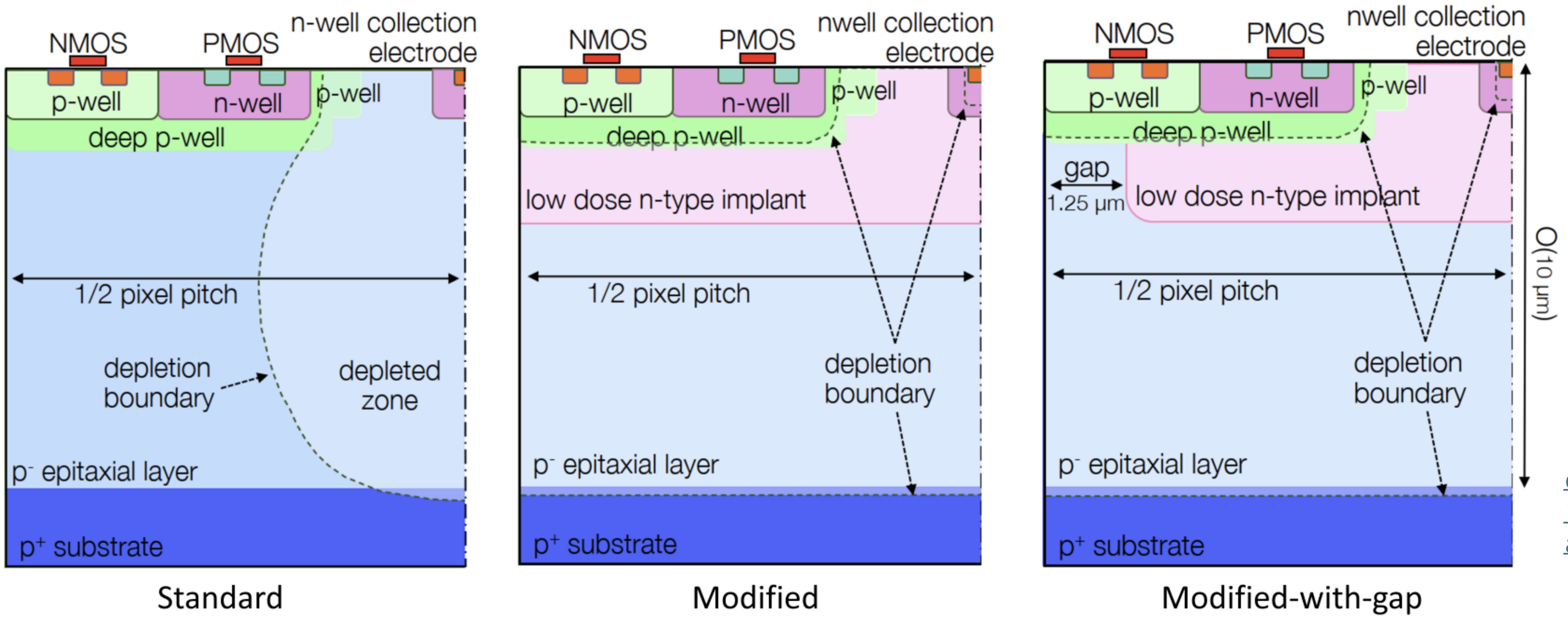
Monolithic active pixel sensors

- Single silicon chip contains both the detection volume and the readout electronics
- Advantages:
  - Low capacitances = low power (10-100 mW/cm^2)
  - Thin: < 50 µm (0.05% X_0 per MAPS)
  - Highly integrated (around 100 transistors in-pixel)
  - Commercially available process
- See detector seminar on MAPS at CERN by W. Snoeys



CMOS MAPS with 65 nm technology

- For 65 nm CMOS process the epitaxial layer thickness is 10 µm (vs ~25 µm for ALPIDEs in 180 nm) due to planarity requirements
- Modified doping profile for improved charge collection is needed



doi.org/10.48550/arXiv.2309.14814

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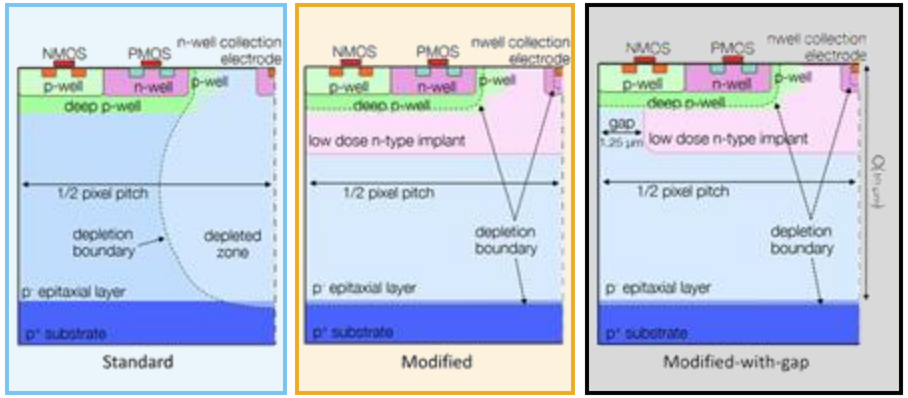
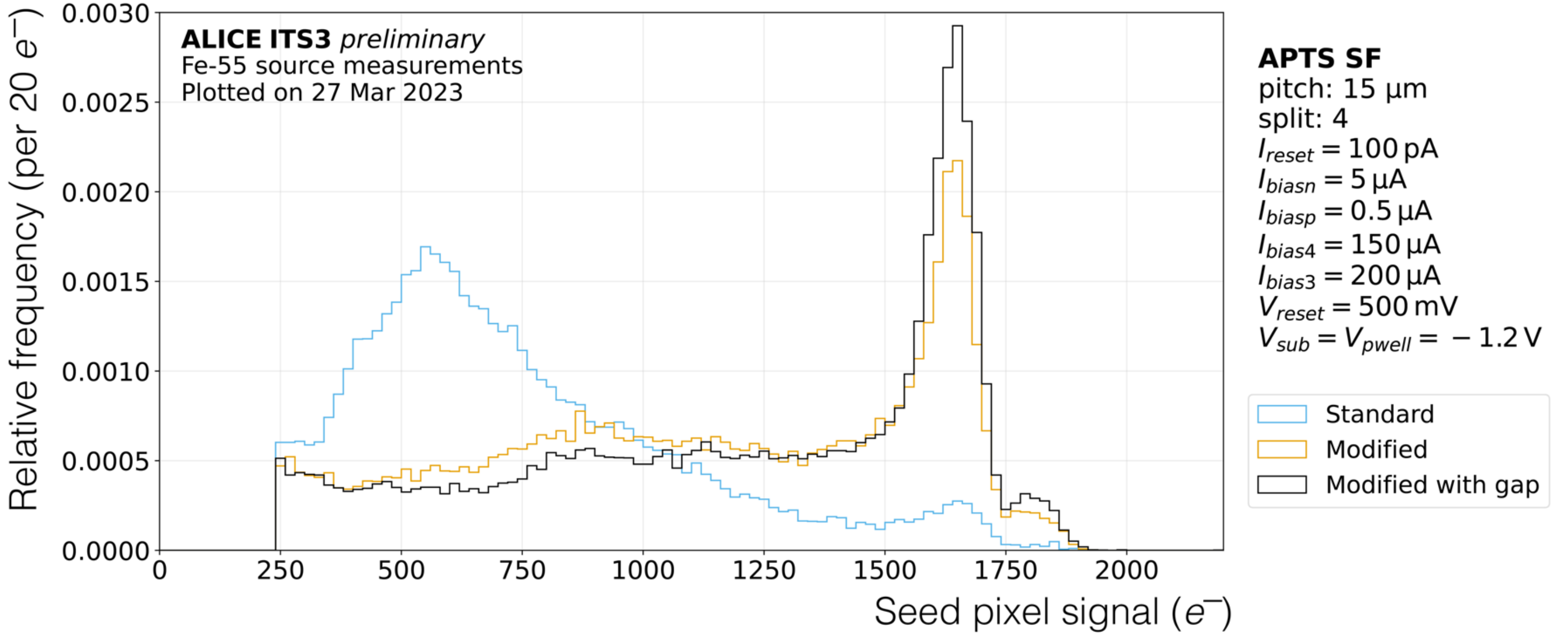
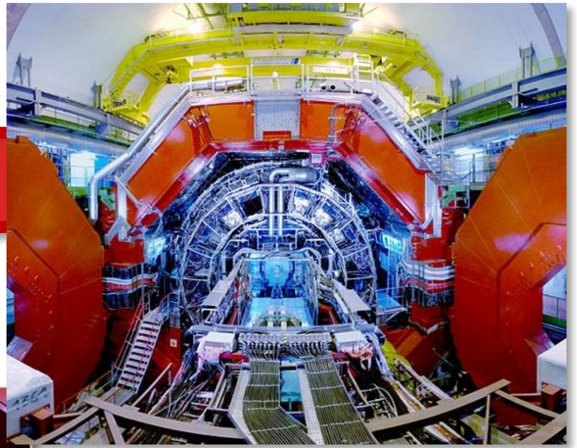


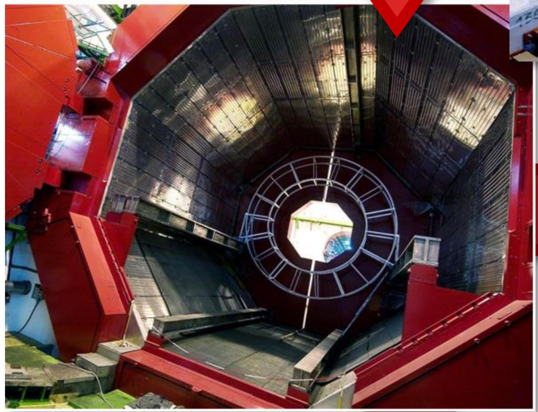
[F.Carnesecchi et al. NIM A (2024) 169896]

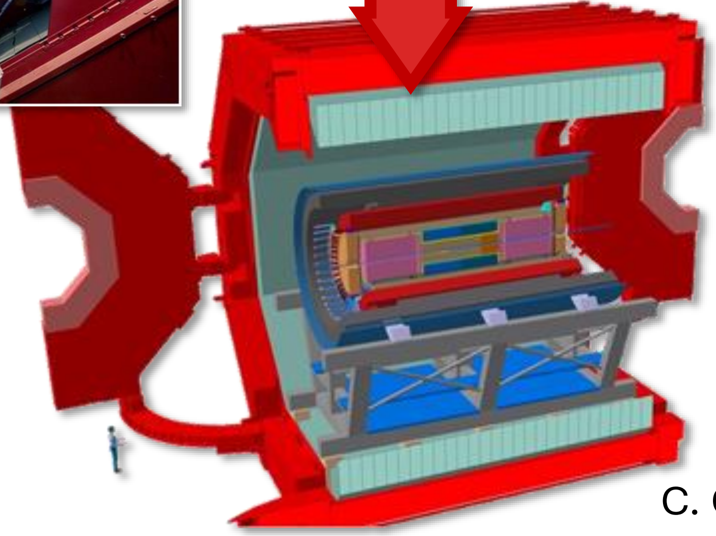


ALICE 3: A new detector at the LHC

- Upgrading almost all components of current ALICE experiment
  - New barrel detectors with discs
  - New super conducting magnet (2T)
  - The current L3 magnet will remain but not used
- Detector concept:
  - compact low-mass all-silicon tracker
  - excellent vertex reconstruction
  - wide acceptance $|\eta| < 4$
  - PID in wide p_T range
  - high readout rate in A-A and pp







Credits
C. Gargiulo

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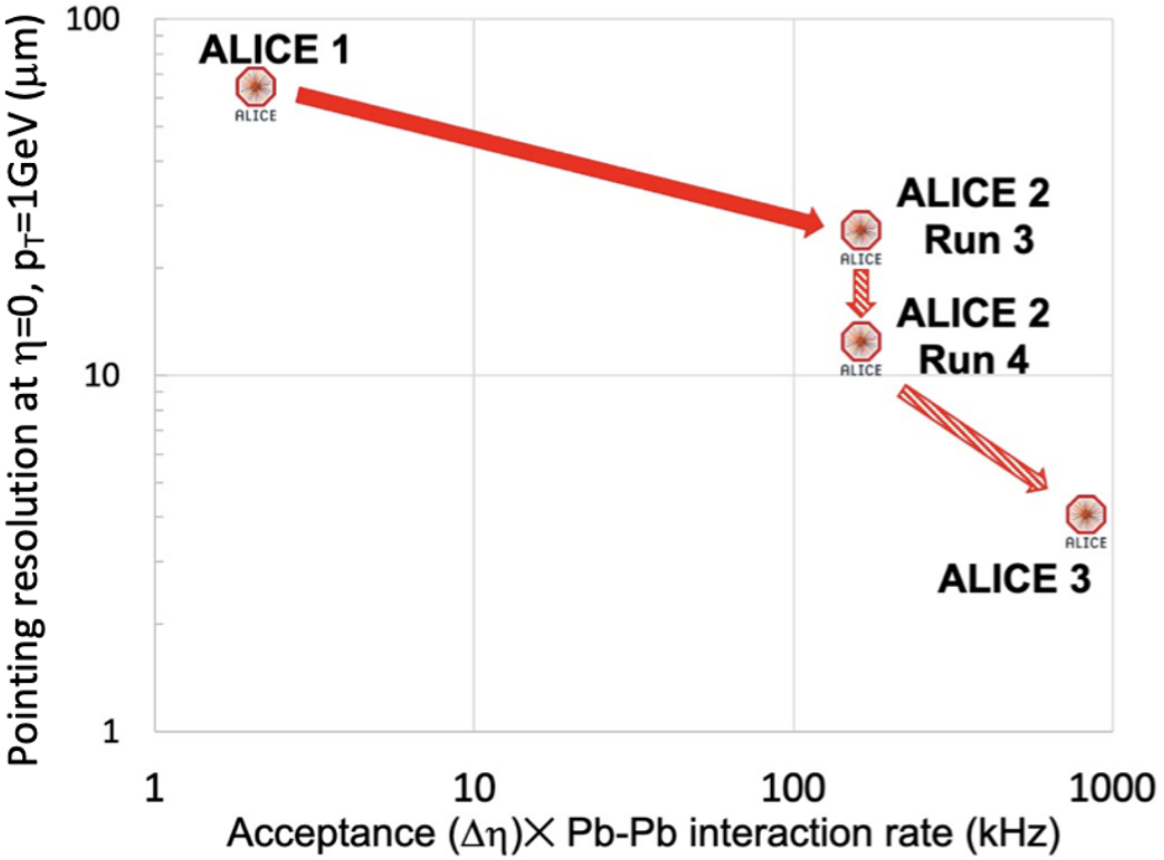
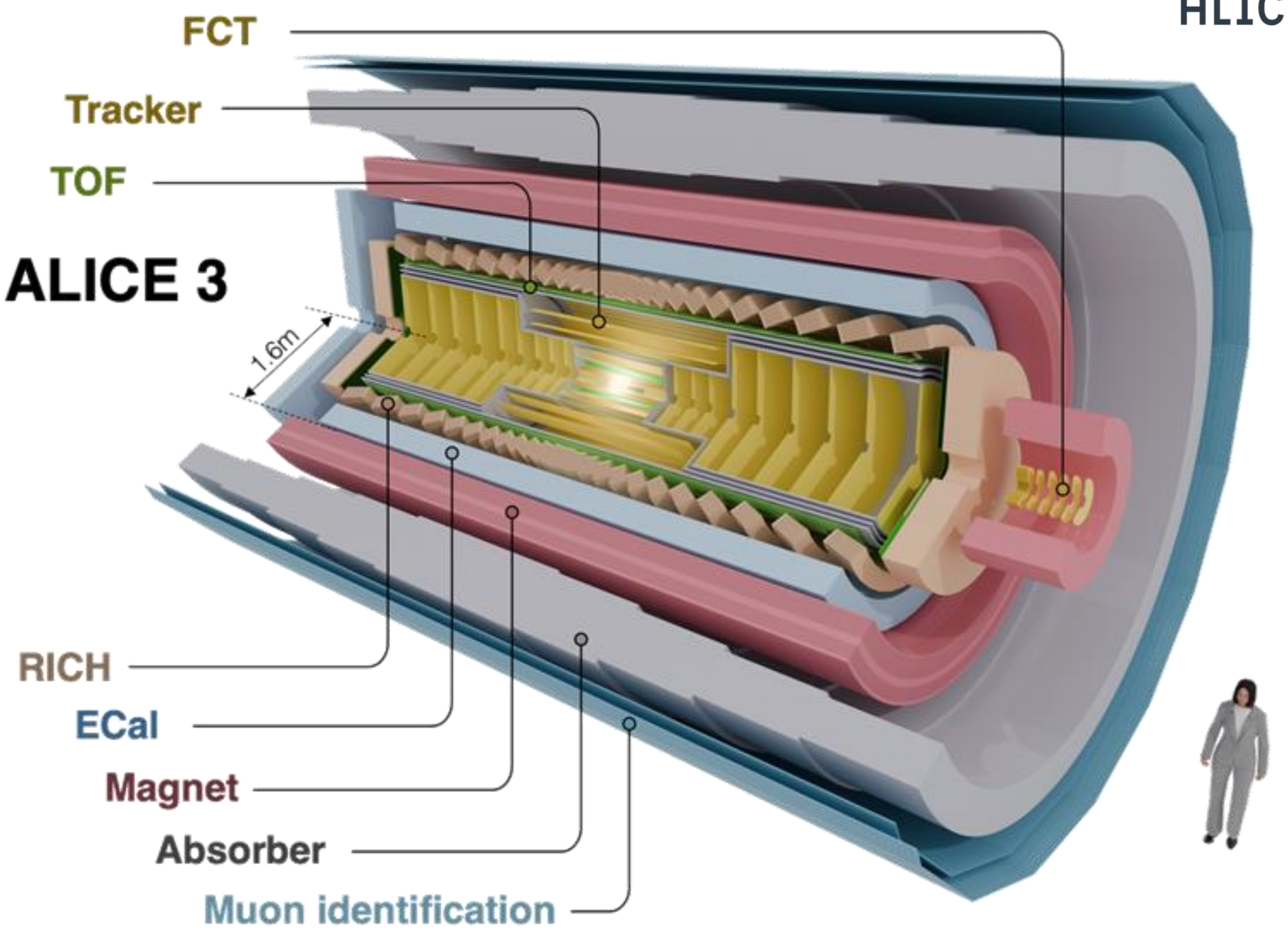
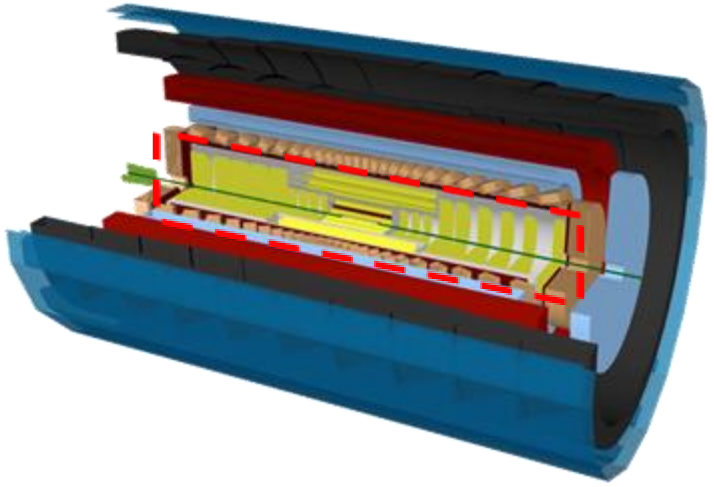


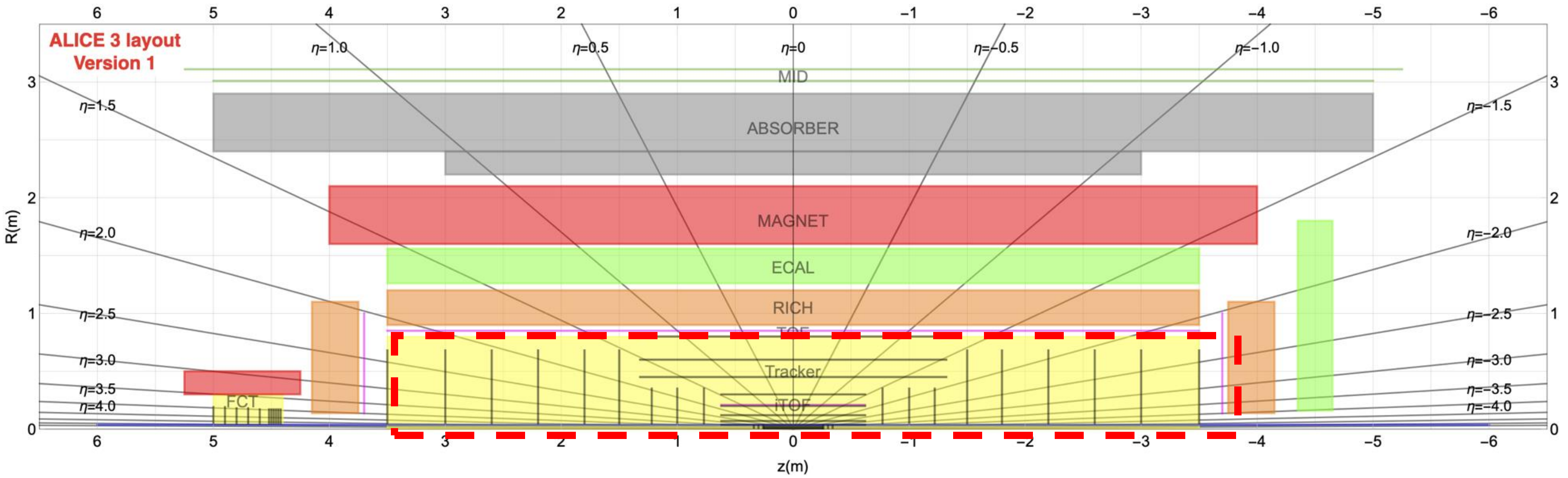
ALICE 3 layout

- Tracking done by 11 layers of silicon pixel MAPS trackers
- PID with TOF, RICH and Muon ID
  - **Next talk by Manuel on TOF & PID!**



ALICE 3 trackers



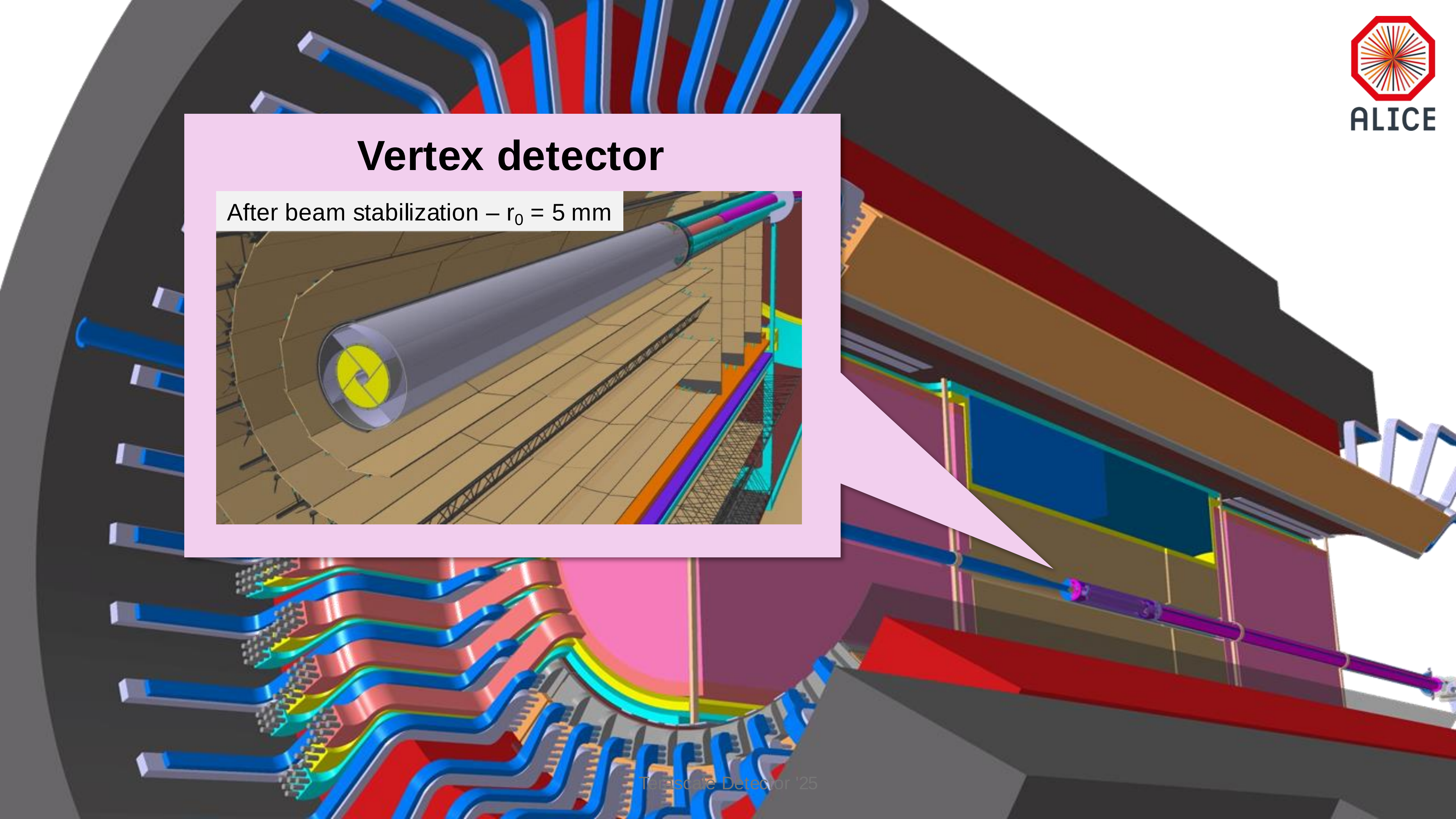


Dimensions of the inner tracker

	Layer	Material thickness (% X_0)	Intrinsic resolution (µm)	Barrel layers: Length Δz (cm)	Barrel layers: Radius (r) (cm)	Forward disks: Position ($\|z\|$) (cm)	Forward disks: R_{in} (cm)	Forward disks: R_{out} (cm)
Vertex Detector	0	0.1	2.5	50	0.50	26	0.50	2.5
	1	0.1	2.5	50	1.20	30	0.50	2.5
	2	0.1	2.5	50	2.50	34	0.50	2.5
Middle Layers	3	1	10	124	3.75	77	5	35
	4	1	10	124	7	100	5	35
	5	1	10	124	12	122	5	35
	6	1	10	124	20			

Dimensions of the outer tracker

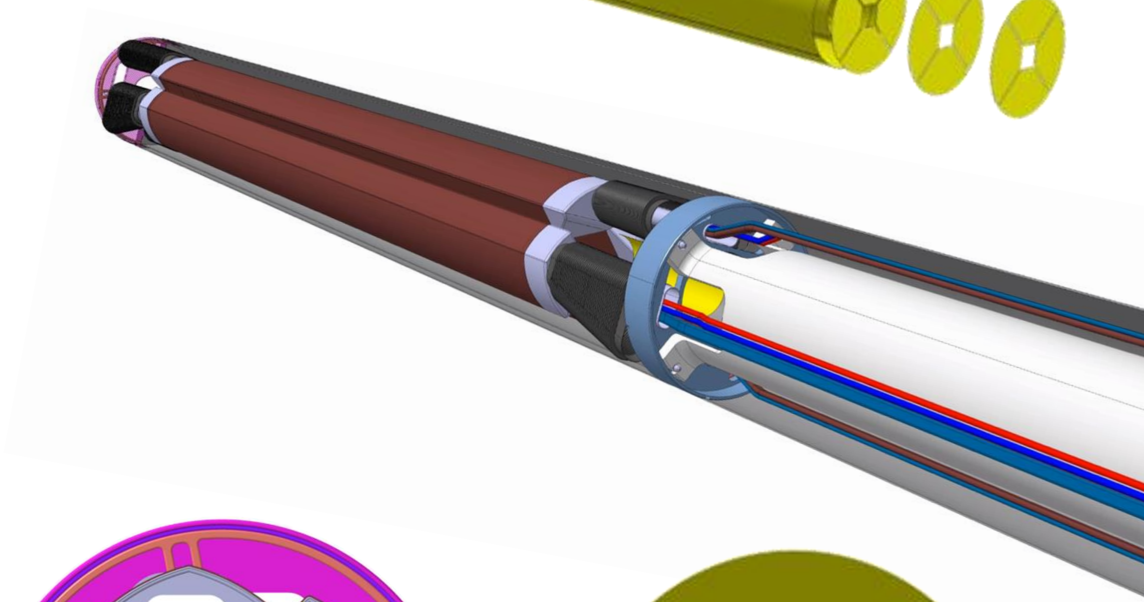
Layer	Det.	Material thickness (% X_0)	Intrinsic resolution (µm)	Barrel layers: Full length (Δz) (cm)	Barrel layers: Radius (r) (cm)	Forward disks: Position ($\|z\|$) (cm)	Forward disks: R_{in}–R_{out} (cm)
6	IT/OT	1	10	1×124	20	150	5–68
7	OT	1	10	1×129	30	180	5–68
8	OT	1	10	2×129	45	220	5–68
9	OT	1	10	2×129	60	260	5–68
10	OT	1	10	2×129	80	300	5–68
11	OT	1	10			350	5–68

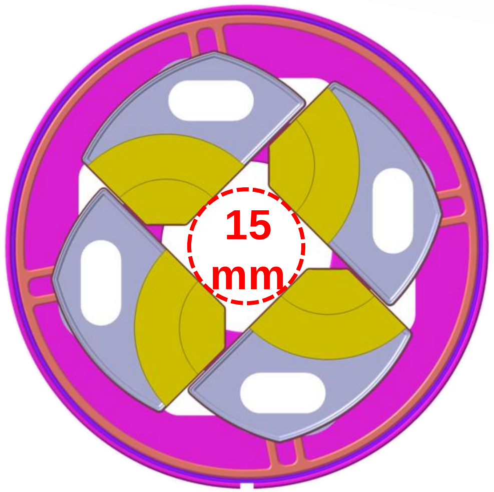


Vertex detector

Vertex detector

- Stitched and bent MAPS sensors placed in a secondary vacuum in the LHC beampipe
  - Consists of four retractable petals (IRIS)
  - 3 detection layers (barrel + disks)
  - Material budget: 0.1% X_0 / layer
  - In closed position inner radius of down to 5 mm
  - In opened position inner radius of 15 mm
- Open position needed during LHC filling prior to beam focusing





Credits Corrado Gargiulo

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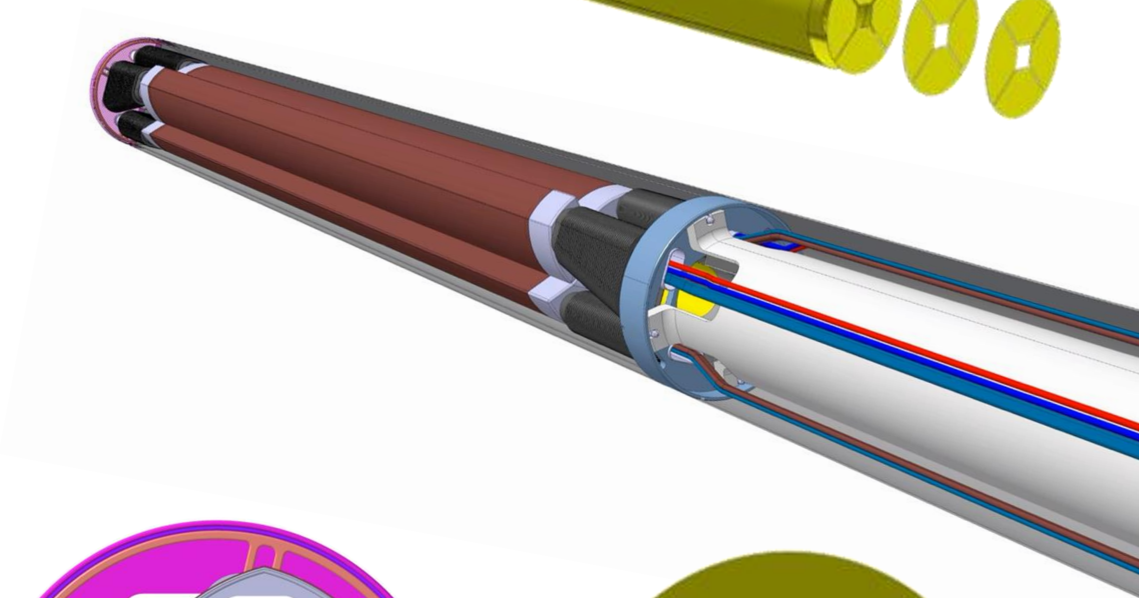
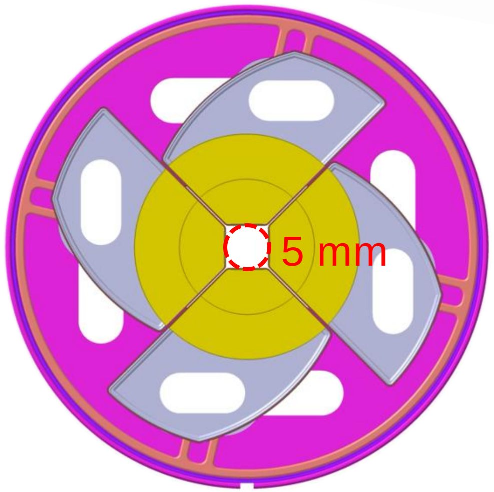
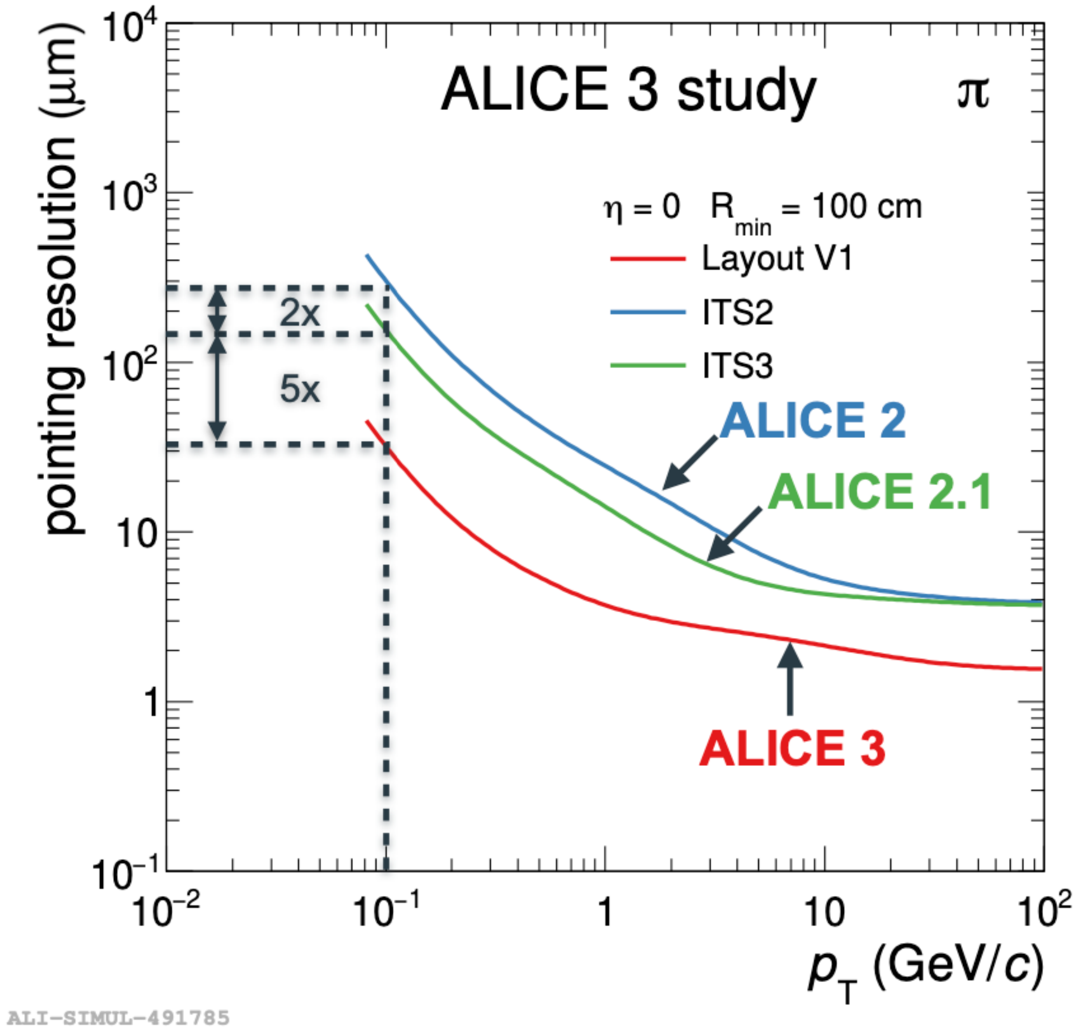




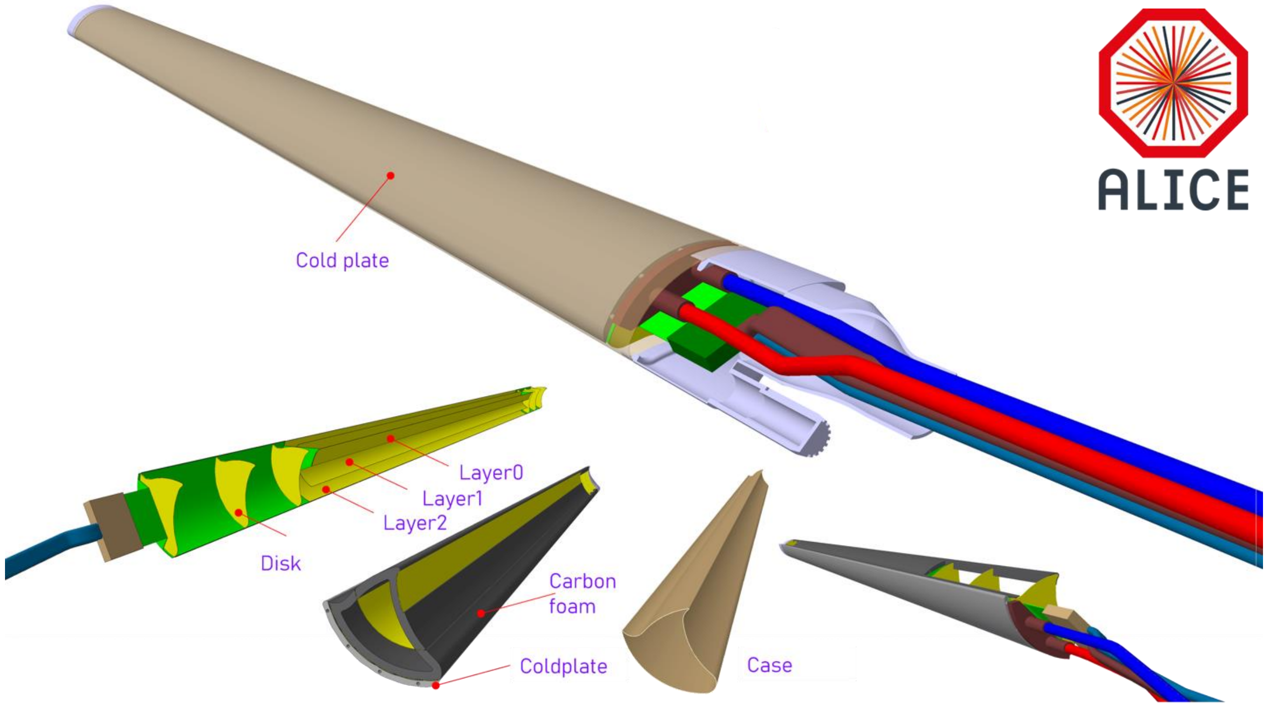
Resolution impact

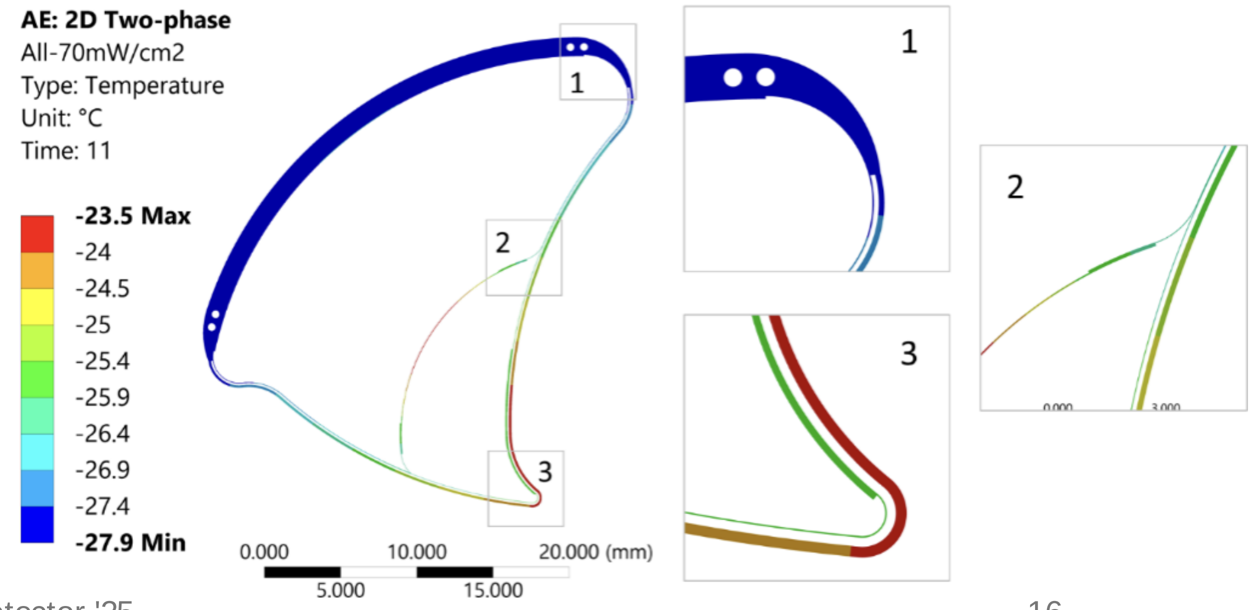
- Pointing resolution $\propto r_0 \cdot \sqrt{x/X_0}$
  - driven by radius and material of first layer
  - minimal radius given by required aperture
- Up to factor 5 improvement achievable with the planned 5 mm of inner radius



Vertex detector cooling

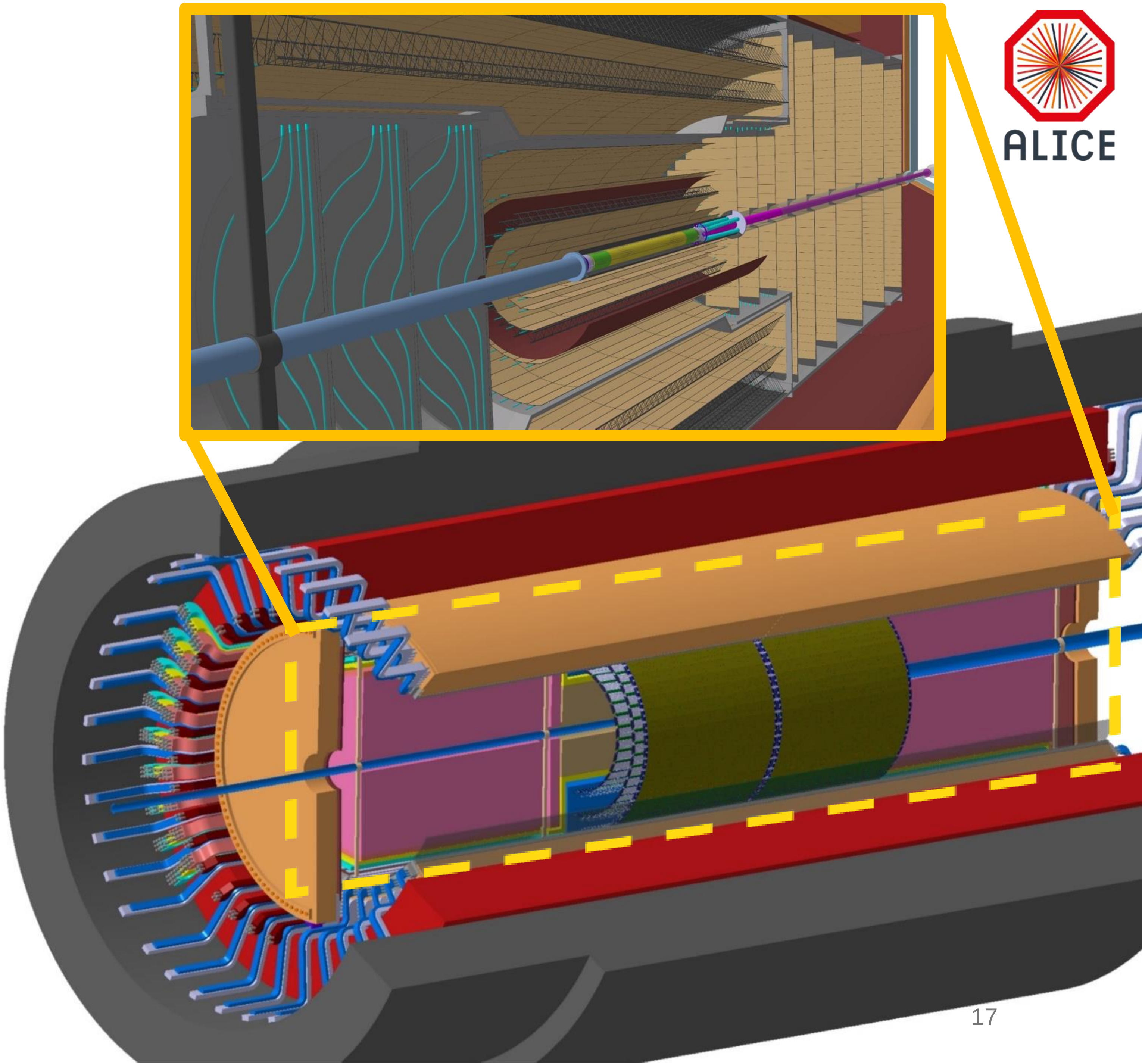
- Cooling is a major challenge since the sensors will be inside a secondary vacuum
- Investigated cooling approach: CO_2 cooling down to -35°C of petal cases
- Heat dissipation of sensors (70 mW/cm^2) with thin carbon paper and radiative cooling





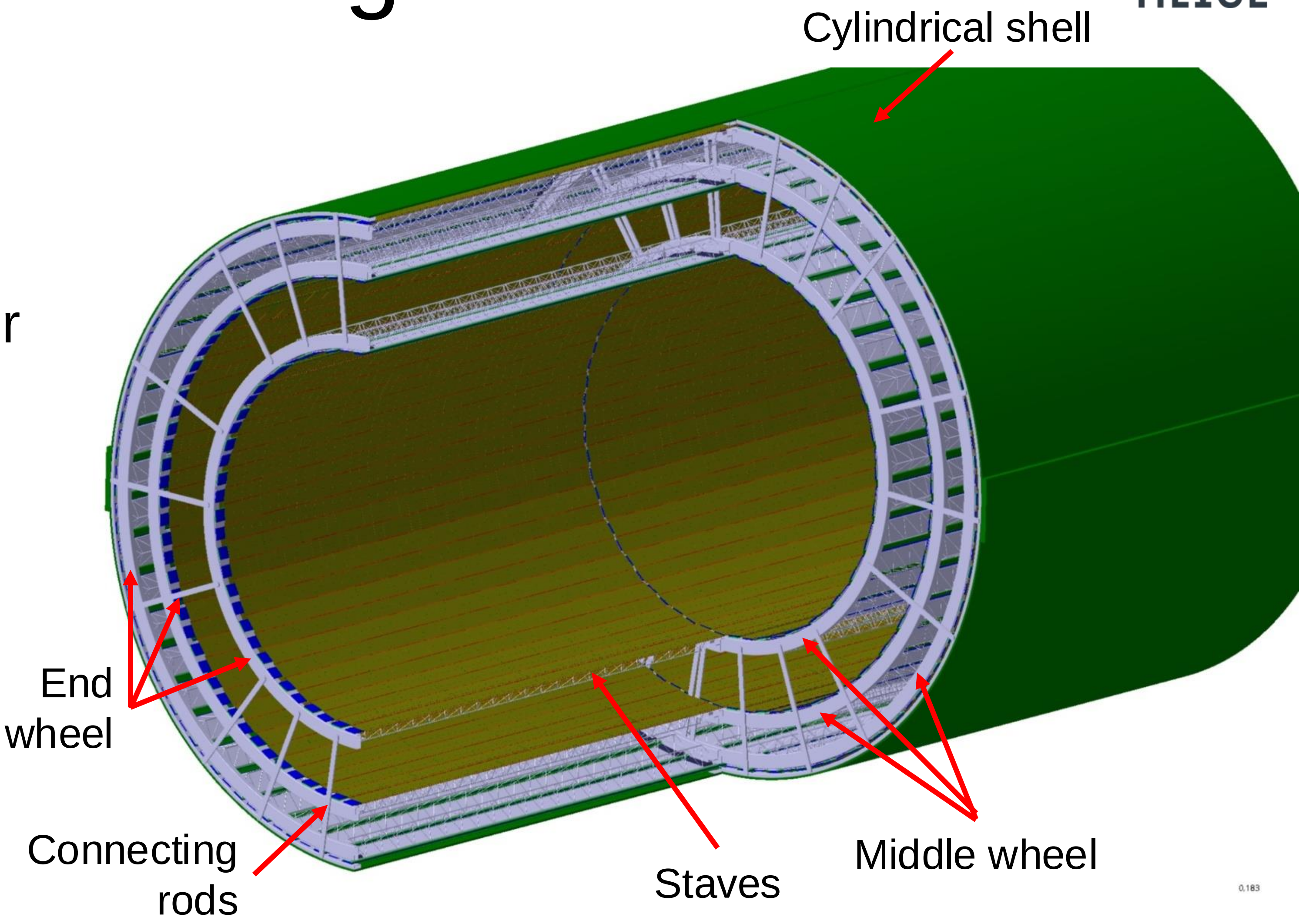
Middle layers & outer tracker

- 60 m^2 of MAPS!
- Industrial production of sensors (~2000 wafers) and modules (~10,000) required due to the detector scale
- Aiming for mass manufacturable and modular design

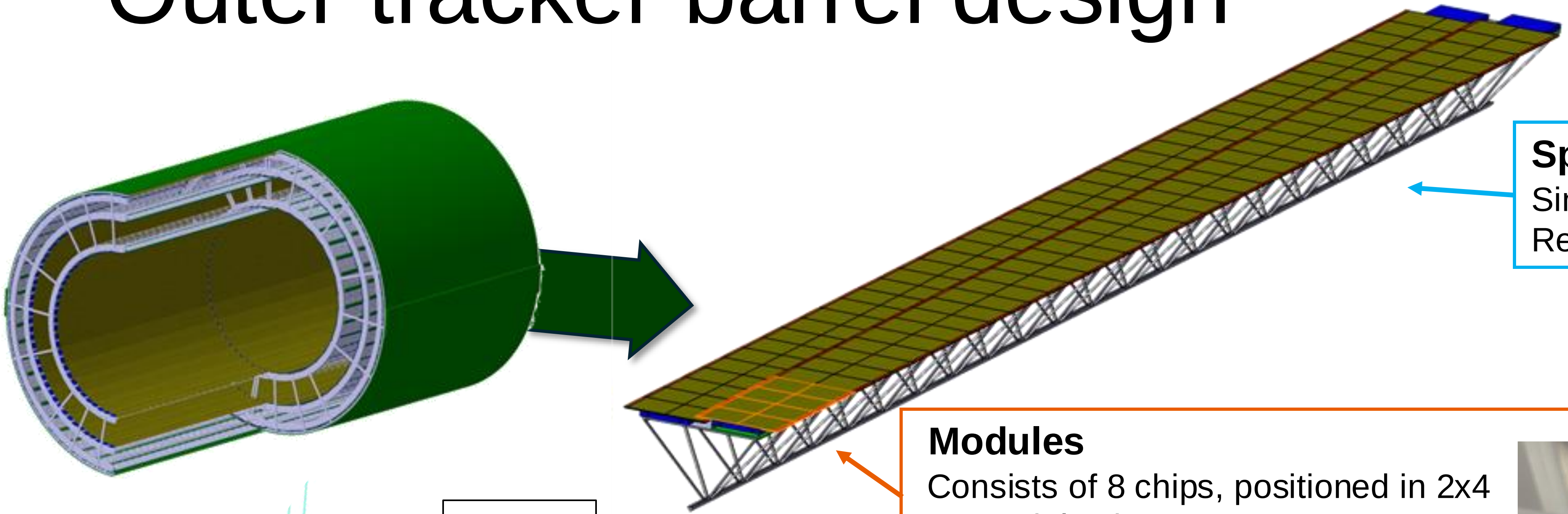


Outer tracker barrel design

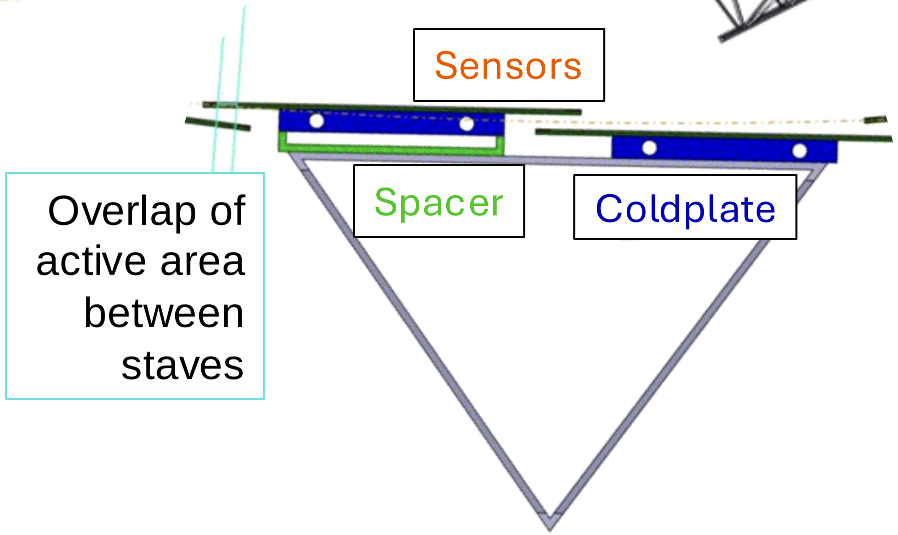
- 4 barrel layers (35 cm < R < 80 cm)
- Material budget: 1% X_0 / layer
- Low power consumption: $O(20\ \mathrm{mW/cm^2})$
- Spatial resolution 10 μm (pixel pitch = 50 μm)
- O(100 ns) time resolution



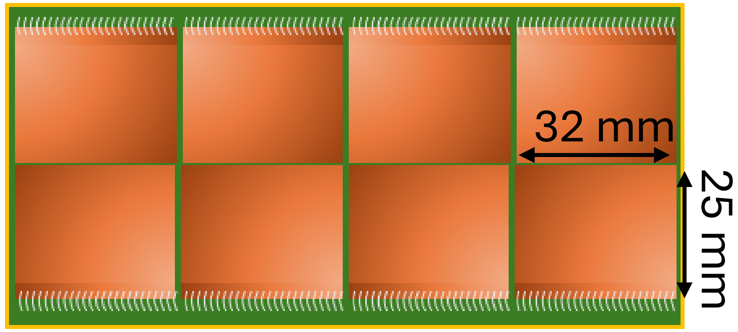
Outer tracker barrel design

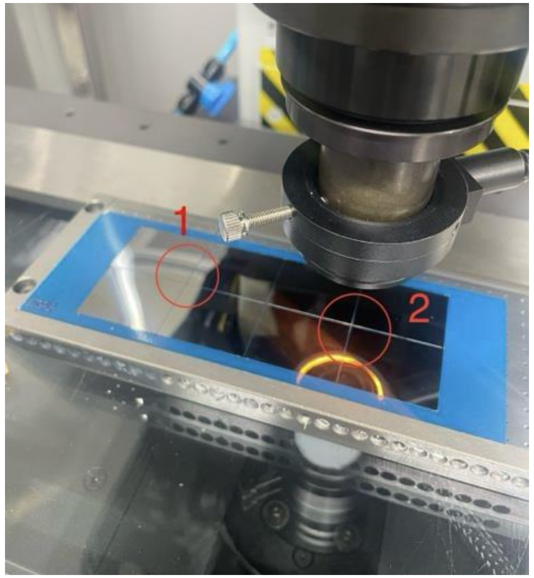


Spaceframe
Similar geometry as ITS2
Ready for industrialization



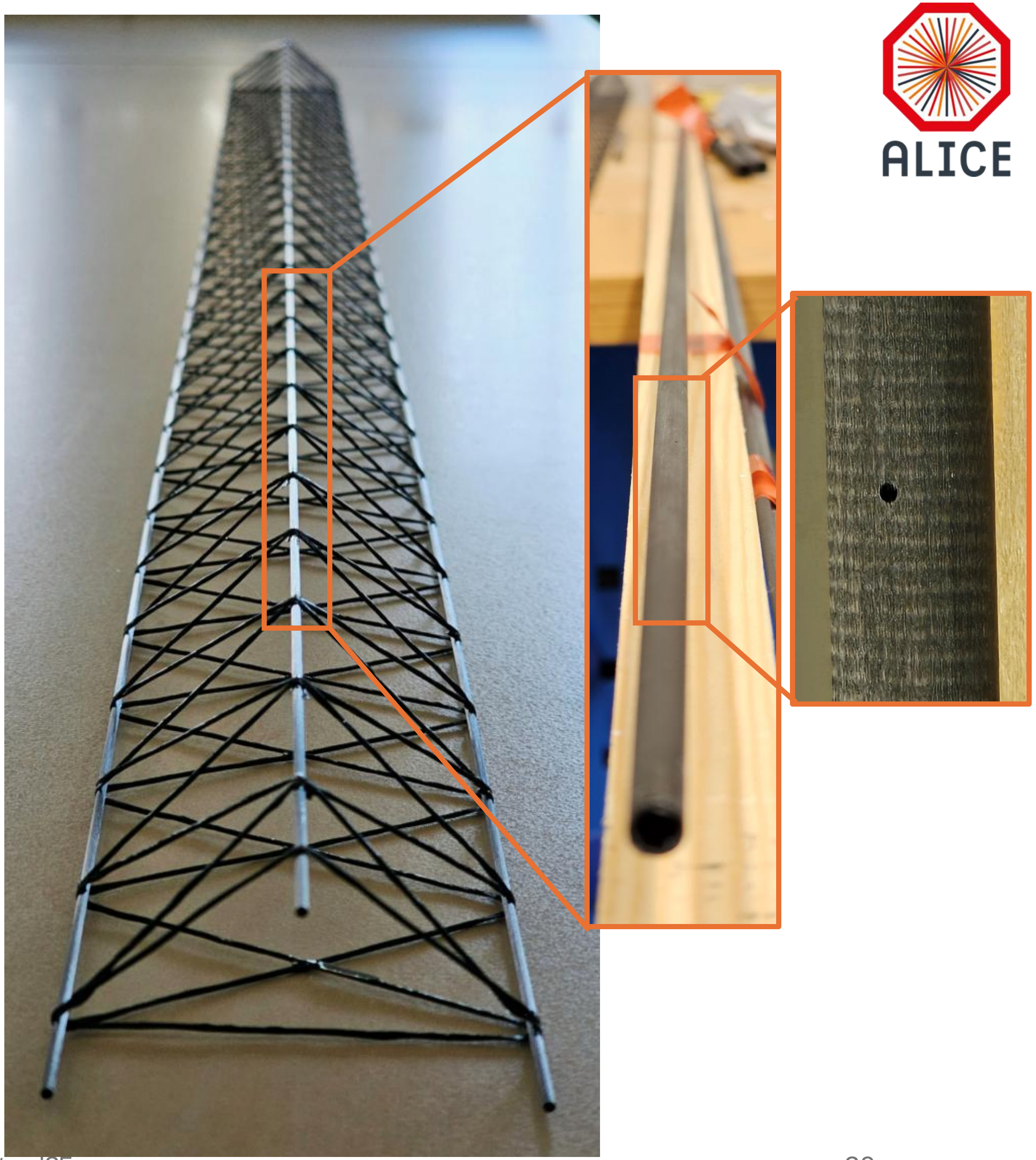
Modules
Consists of 8 chips, positioned in 2x4
10 modules in one row
20 modules on single spaceframe
Industrial assembly tests ongoing





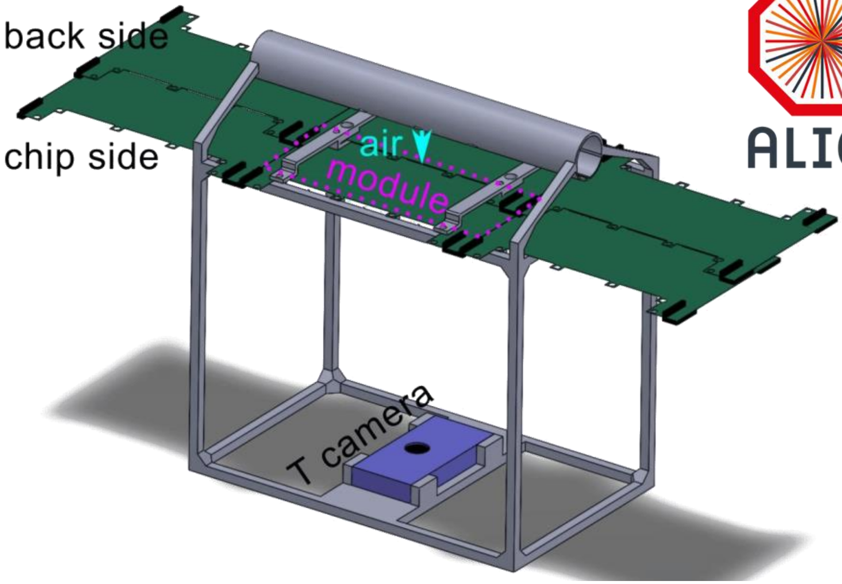
Outer tracker cooling

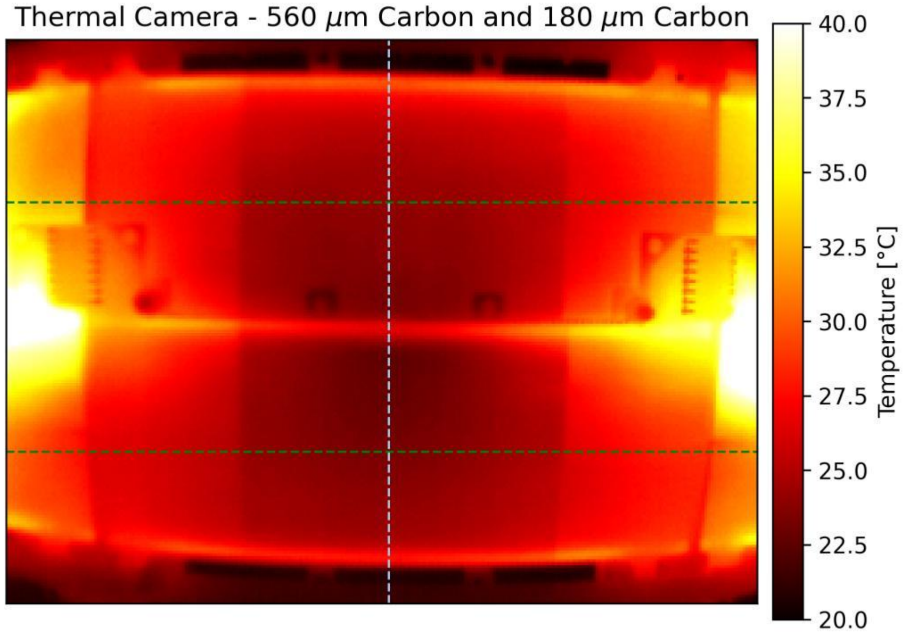
- The baseline cooling method is water cooling with a cold plate underneath the modules
  - Challenging for modularity (replacing not functional modules after stave assembly)
- Air cooling as a low material alternative
  - Using carbon tubes integrated into the spaceframe as air pipes
  - Local cooling via exhaust holes on the air pipe shooting cold air onto module surface
    - Similar approach was recently demonstrated for the CBM STS at FAIR/GSI

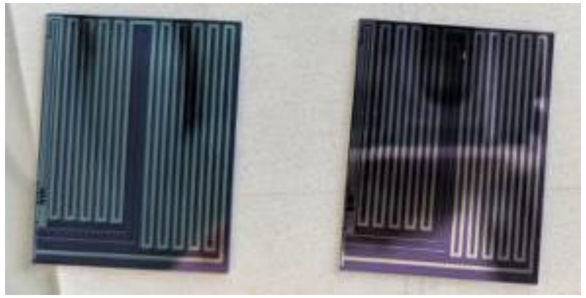


Cooling and vibration studies

- Demonstrator wind tunnel for air cooling tests
  - Emulating the heat production of sensors (20 mW/cm^2) in the flex printed circuit
  - Testing different air vent hole sizes, air velocity/pressure
- Measured cooling performance and vibrations
  - Cooling for single modules demonstrated
  - Vibrations can be significantly reduced with an additional light carbon layer
  - Full scale demonstrator under construction with staves fully populated with dummy sensors



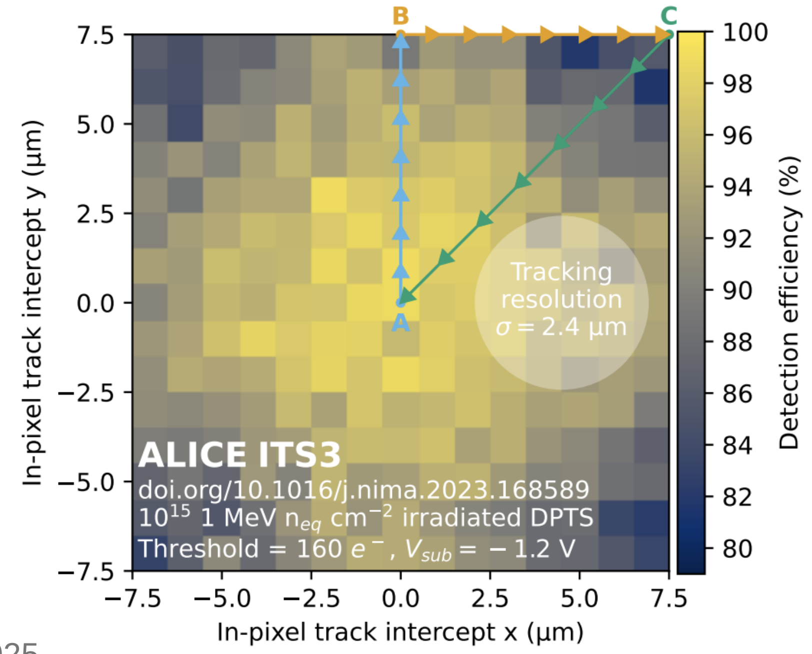


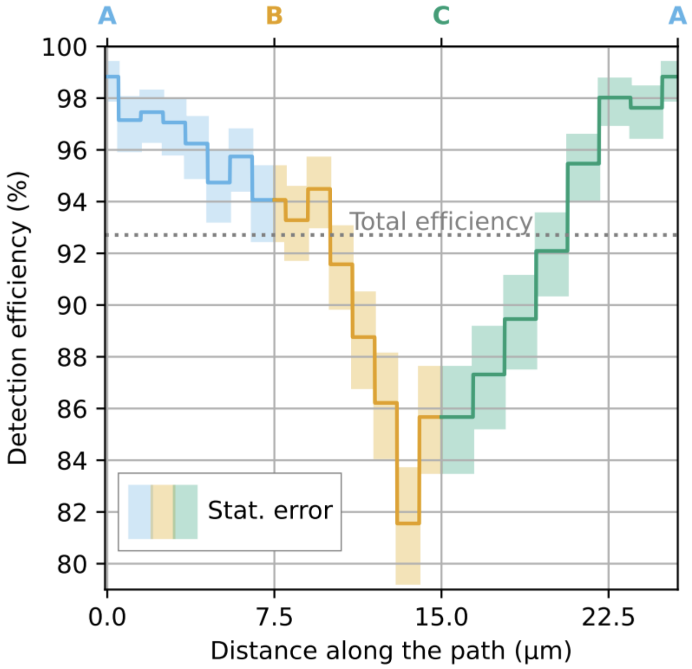


MADHAT thermal dummy OT chips produced at Bonn

MAPS with large pixel pitches

- Increasing pixel pitch up to 50 µm is possible to reduce power
- Efficiency loss is observed in the pixel corners after irradiation
  - For larger pixel pitches a larger degradation is expected
  - Has to be studied with large pixel pitch test structures

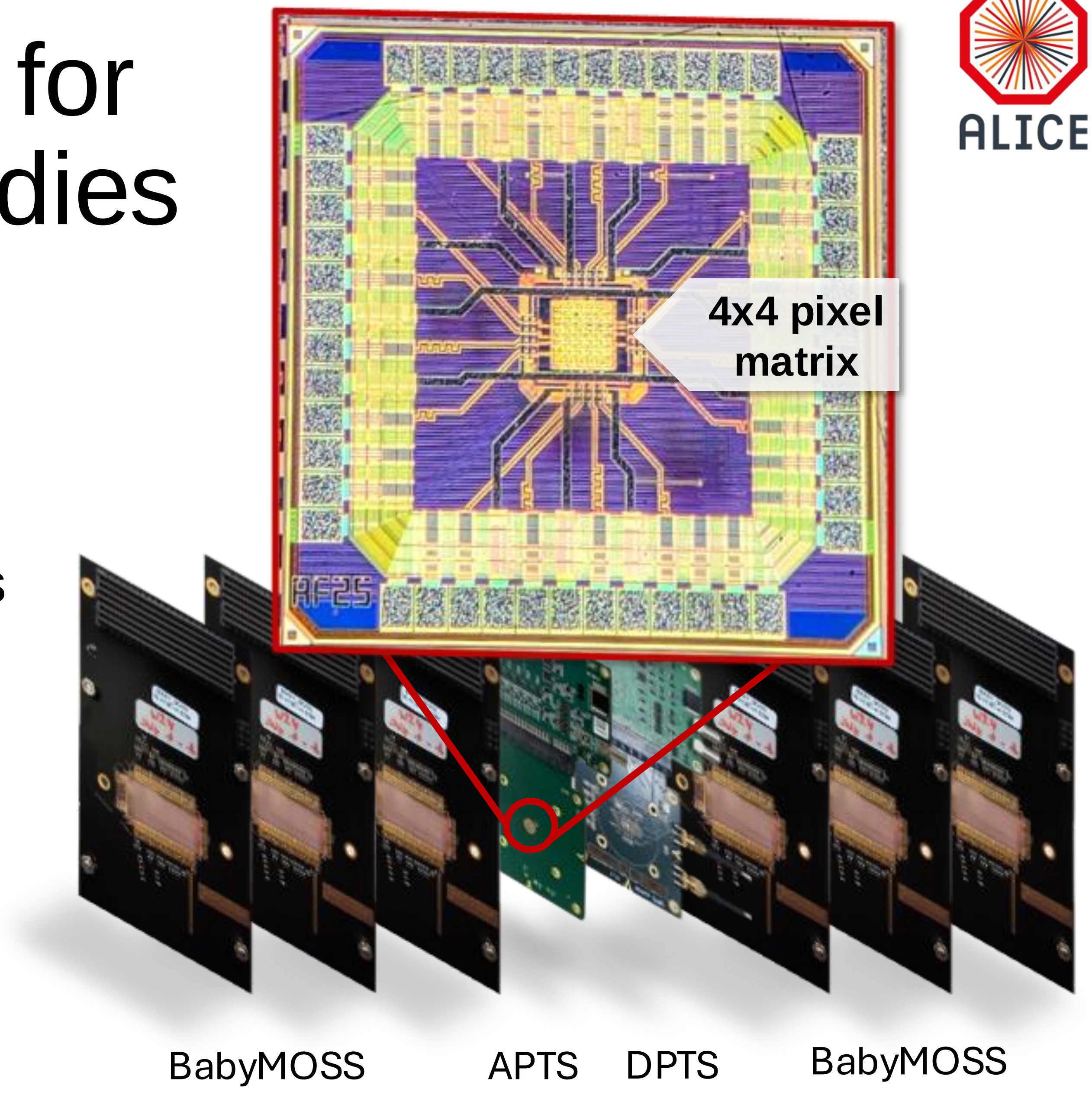




15 µm pitch DPTS in-pixel detection efficiency for 10^{15} 1 MeV n_{eq} cm^{-2} [G. Rinella et al. NIM A (2023) 168589]

Telescope validation for large pitch APTS studies

- In the upcoming months large pitch (30, 40 & 50 μm) variants of the Analog Pixel Test Structures (APTS) will be produced
- The performance of these structures will dictate the sensor design for ALICE Outer Tracker
- Telescope featuring BabyMOSS reference layers and DPTS for triggering with high beam rates demonstrated (up to 100kHz)



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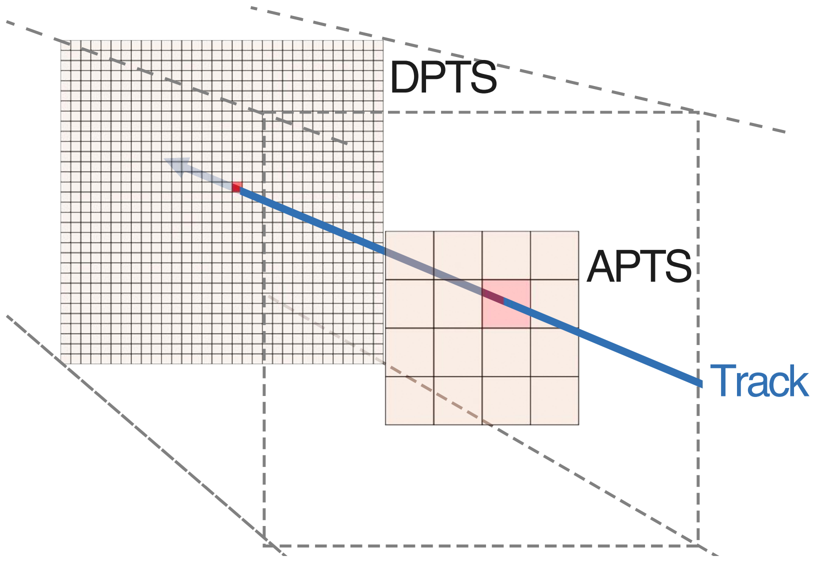
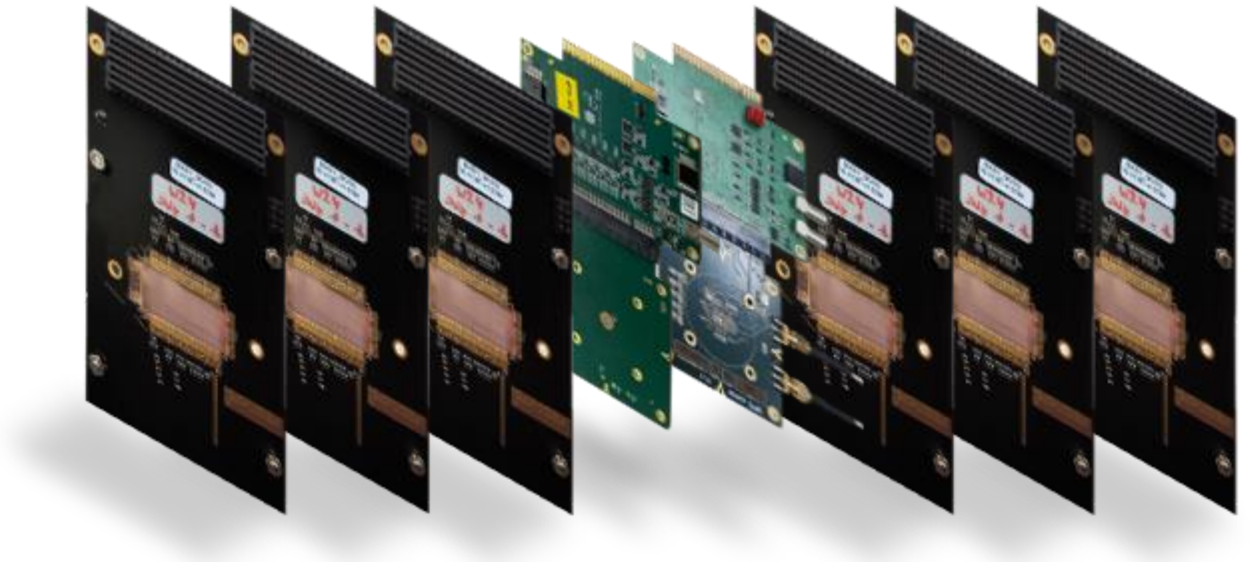
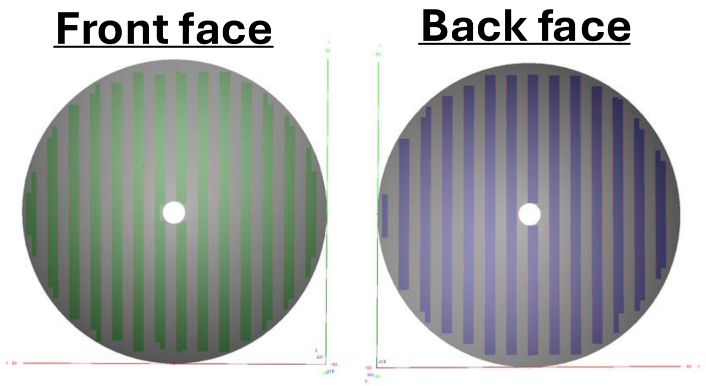


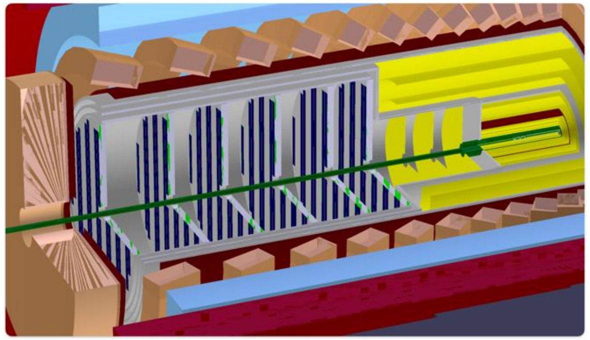


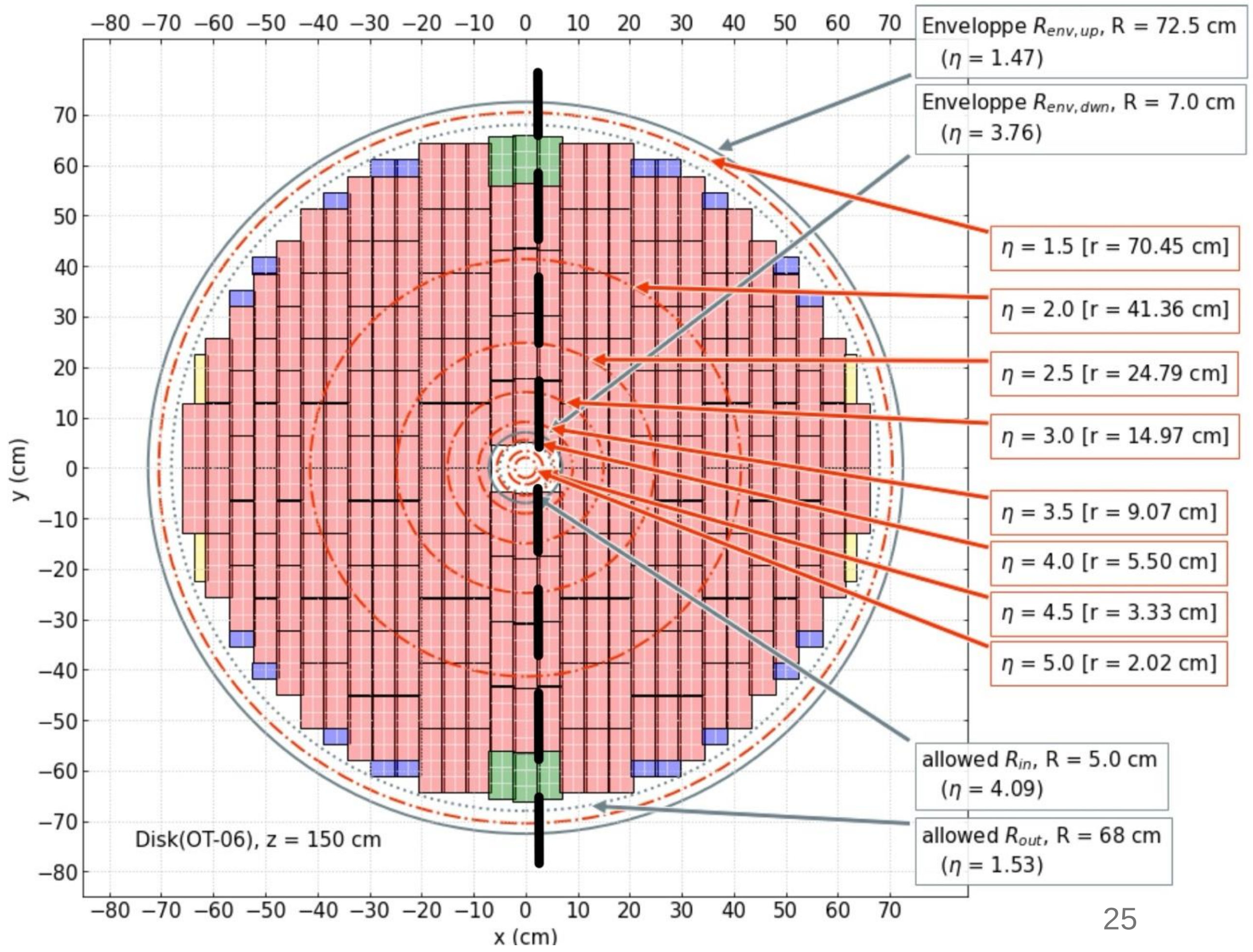
BabyMOSS APTS DPTS BabyMOSS

Outer tracker discs

- The discs will mostly share the same module design as the barrel layers
  - Some smaller modules needed to fill the edges
- Modules mounted alternatingly on either face of a carbon disc plate
  - Overlapping the sensor periphery dead-zones
- Layout optimization studies ongoing

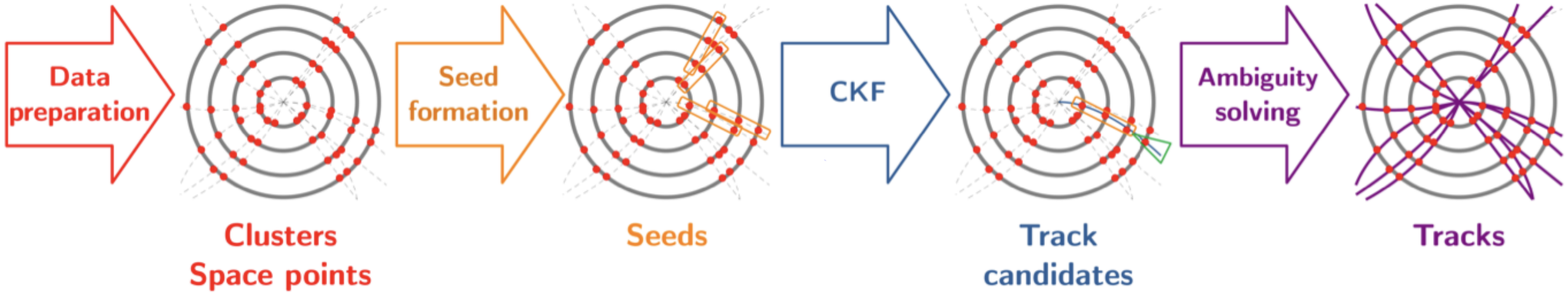




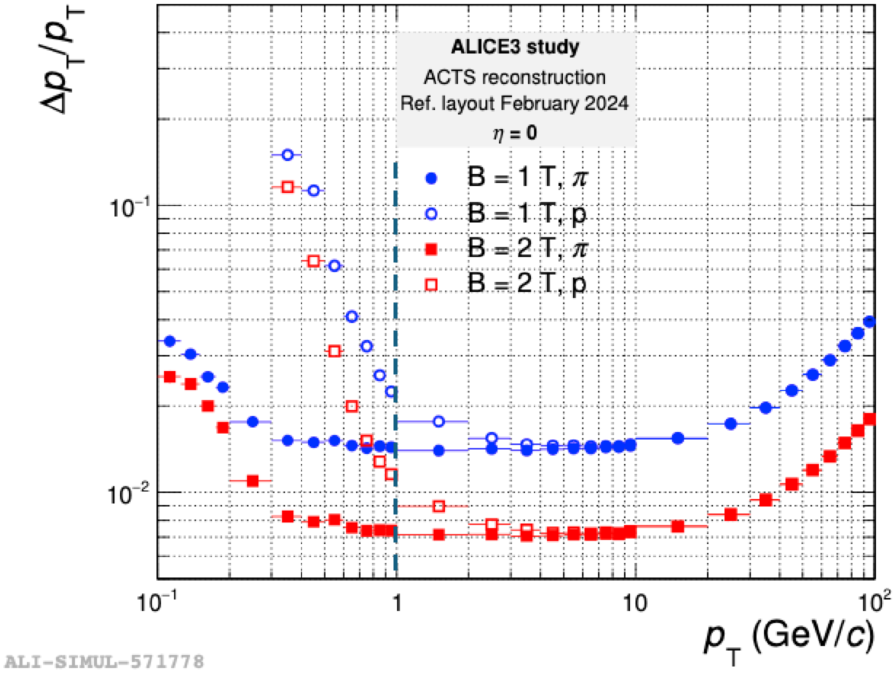


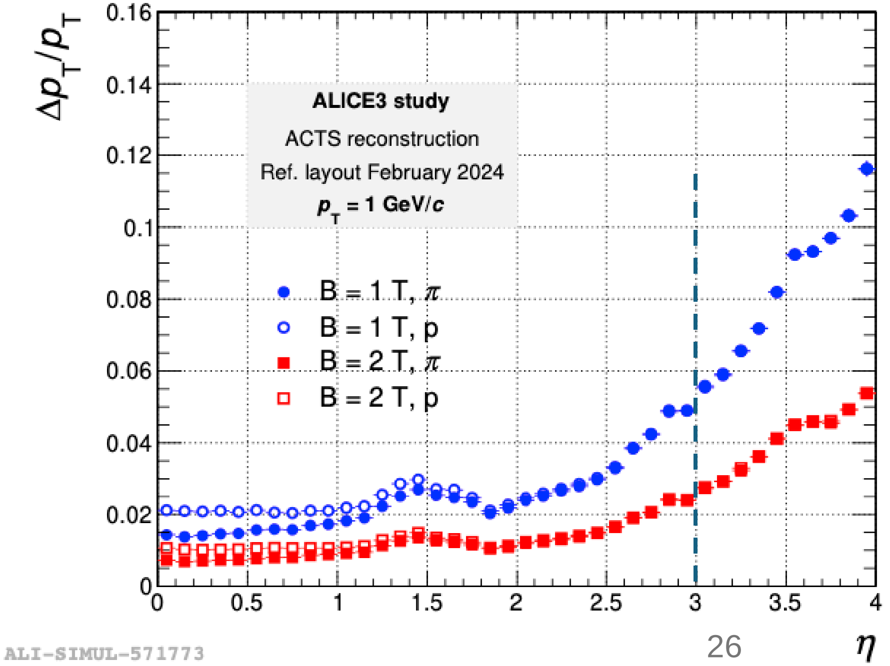
Simulated performance

- Using ACTS [A. Salzburger et. al., Comput. Software Big Sci 6, 8 (2022)] for seeding & tracking performance studies
  - ACTS workflow:



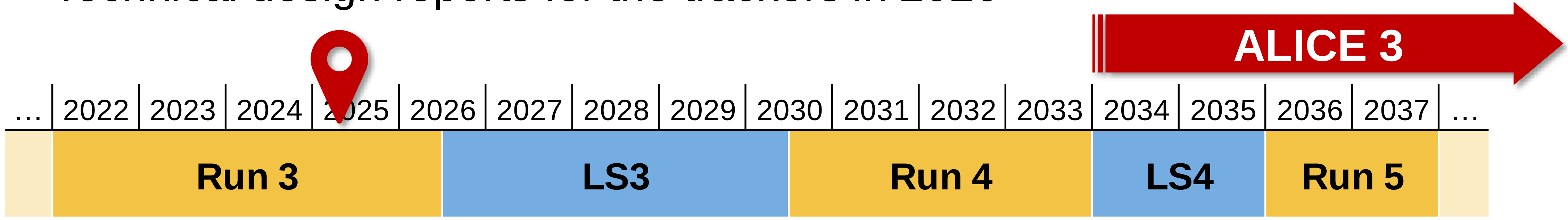
- p_T resolution for pions (using 2T solenoid magnetic field)
  - ≈ 0.7% at p_T ~ 1 GeV/c
  - < 2% up to $|\eta|$ ≈ 3





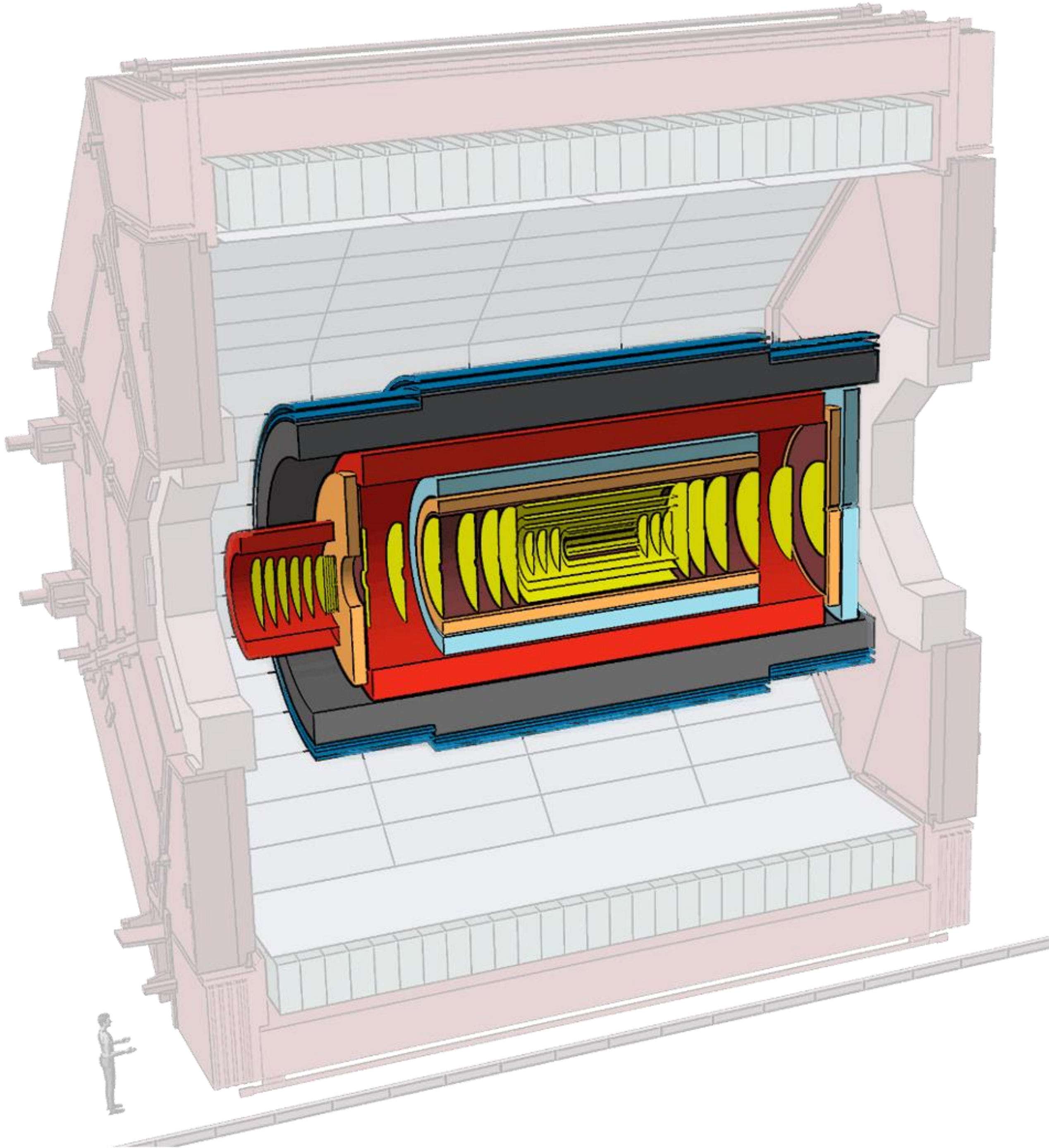
Summary and outlook

- ALICE 3 will exploit the HL-LHC as a heavy-ion collider till end of Run 5
  - Innovative (and challenging) silicon-based detector concept: ultra-light wide-acceptance tracker, continuous readout
  - Pioneering several R&D directions with broad impact on future HEP experiments (e.g. FCC-ee)
- Intense R&D ongoing on all aspects of detector design
  - Sensor architecture strongly inherits from the MAPS experience from ITS2 & ITS3 upgrades
- Technical design reports for the trackers in 2026



Thank you for the attention!

Any questions?



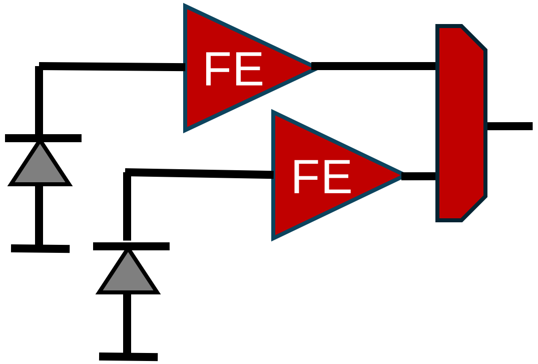
Sensor requirements for future ALICE trackers

		ALICE 3	
	ALICE ITS3	Vertex Detector	Tracker (ML/OT)
Position resolution **(μm)**	5	2.5	10
Pixel size **(μm²)**	0(20 x 20)	0(10 x 10)	0(50 x 50)
Time resolution (ns RMS)	0(1000)	100	100
In-pixel hit rate (Hz)	54	120	54 (barrel)
Fake-hit rate (1 pixel / event)	$< 10^{-7}$		
Power consumption (**mW / cm²)**	35	70	20
Particle hit density (MHz / cm²**)**	8.5	120	0.8
Non-Ionising Energy Loss (1 MeV **neq / cm²)**	3×10^{12}	1×10^{16}	6×10^{13}
Total Ionising Dose (**Mrad)**	0.3	300	3 (barrel)
X/X_0 **/ layer**	0.09% (average), 0.07% (most of active region)	0.10%	1.00%

Pixel grouping - alternative to large pitch pixels

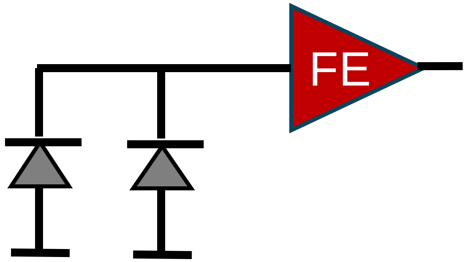
Digital grouping:

- Reduced data rate
- No advantage on power consumption density from larger effective pitch



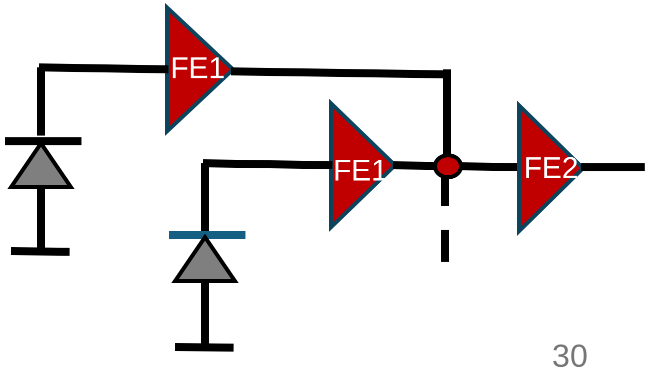
Analog direct grouping:

- S/N degradation, input capacitance increase (limited number of nodes ~2), power density reduced by number of connected nodes (1/n ~ 1/2)

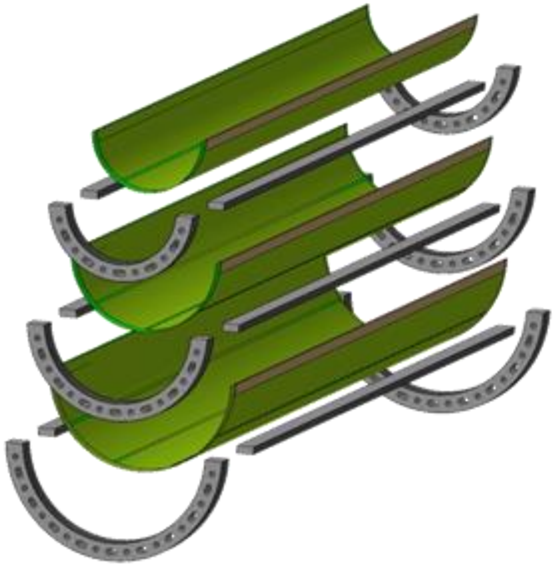


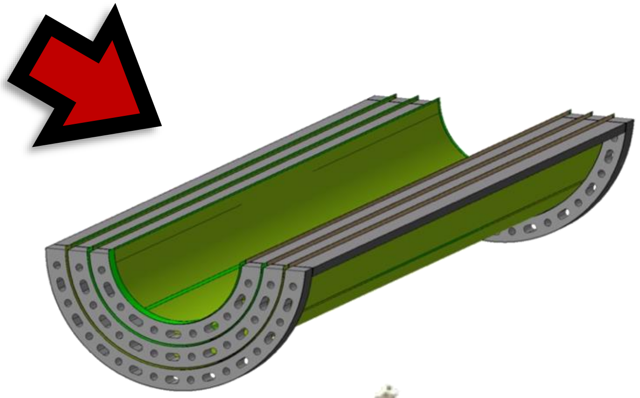
Analog staged grouping:

- Pre-amplify signals with FE1 and sum up potentially more nodes without loosing S/N
- Gain in power consumption not guaranteed

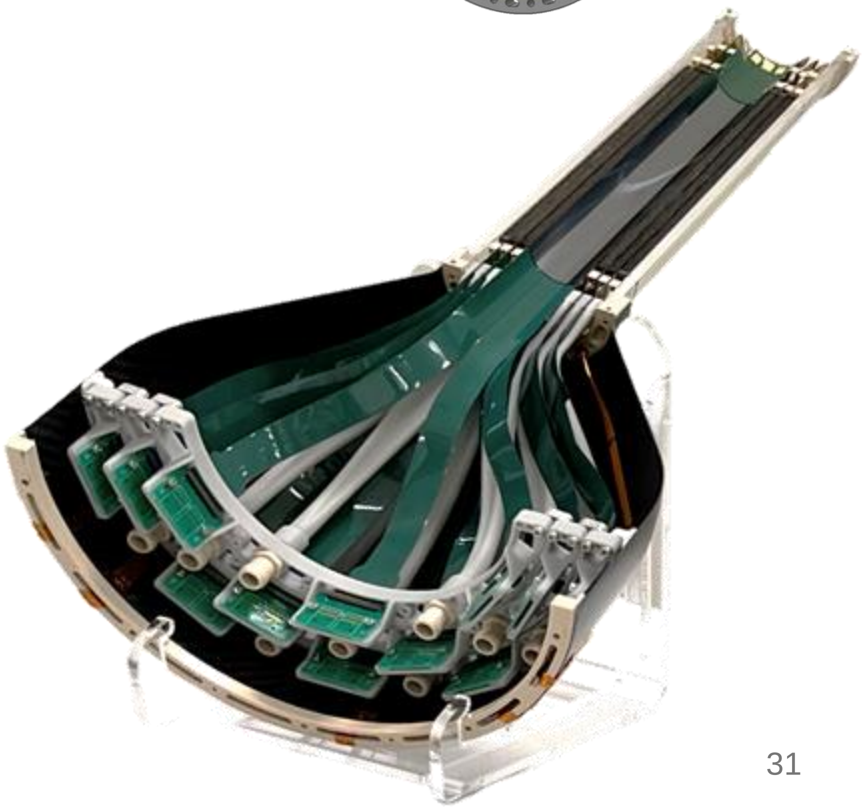


ITS3





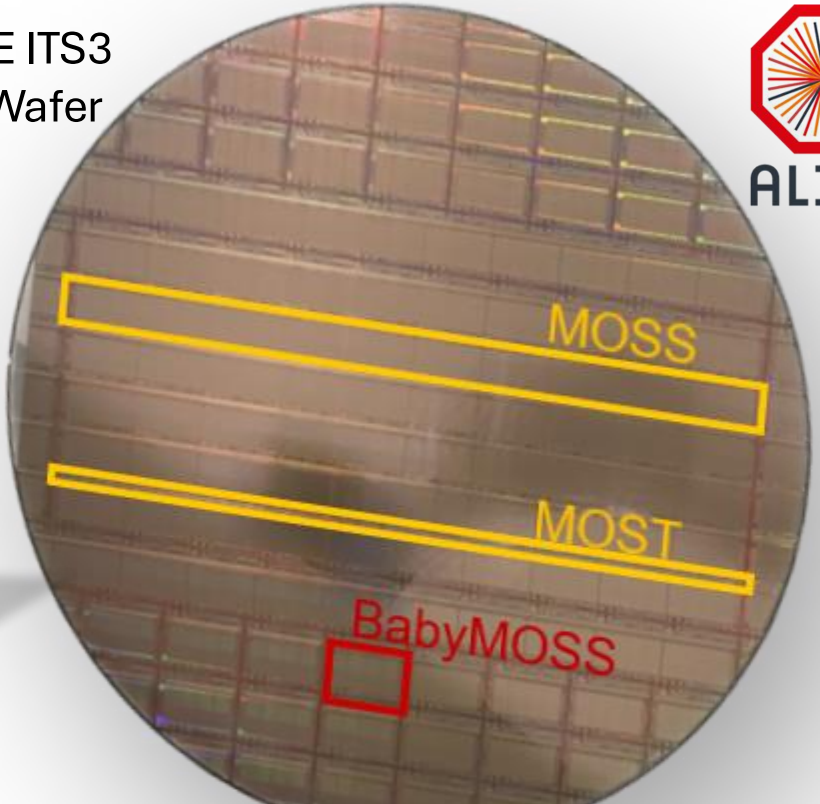
- Replacement of the Inner Barrel of the ITS2 with 3 layers of curved, 50 µm thick, wafer-scale MAPS in 65 nm CMOS process
- Air cooling and ultra-light mechanical supports (carbon foam)
- Reduction of L_0 radius: from 24 mm to 19 mm
- Reduction of material budget per layer: → from 0.36% X/X_0 to 0.09% X/X_0



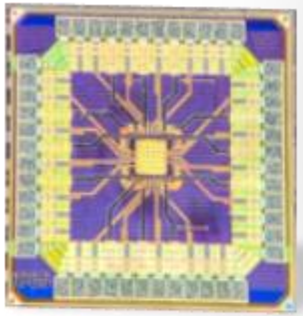
ITS3 sensor glossary

- MOSS (MOnolithic Stitched Sensor)
  - Wafer scale stitched MAPS prototype
  - Pixel matrix divided to eight regions with different pixel density and front-end implementations
- BabyMOSS
  - Fully functional chip with a single MOSS repeated sensor unit (RSU)
- APTS (Analog Pixel Test Structure)
  - 4x4 pixels
  - Direct connection to the signal from the analog frontend of each pixel
- DPTS (Digital Pixel Test Structure)
  - 32x32 pixels
  - Time encoded pixel positions and ToT (time-over-threshold) output after the discriminator stage from pixel

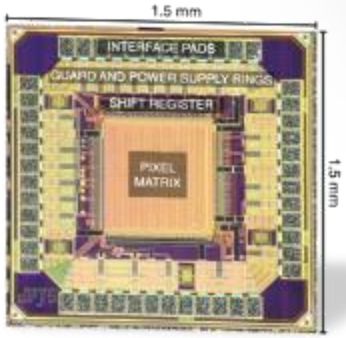
ALICE ITS3
ER1 Wafer



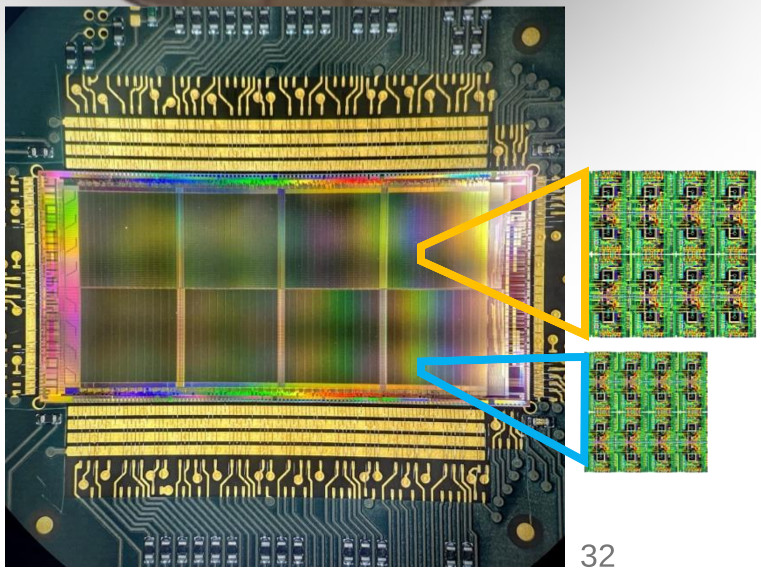
APTS



DPTS

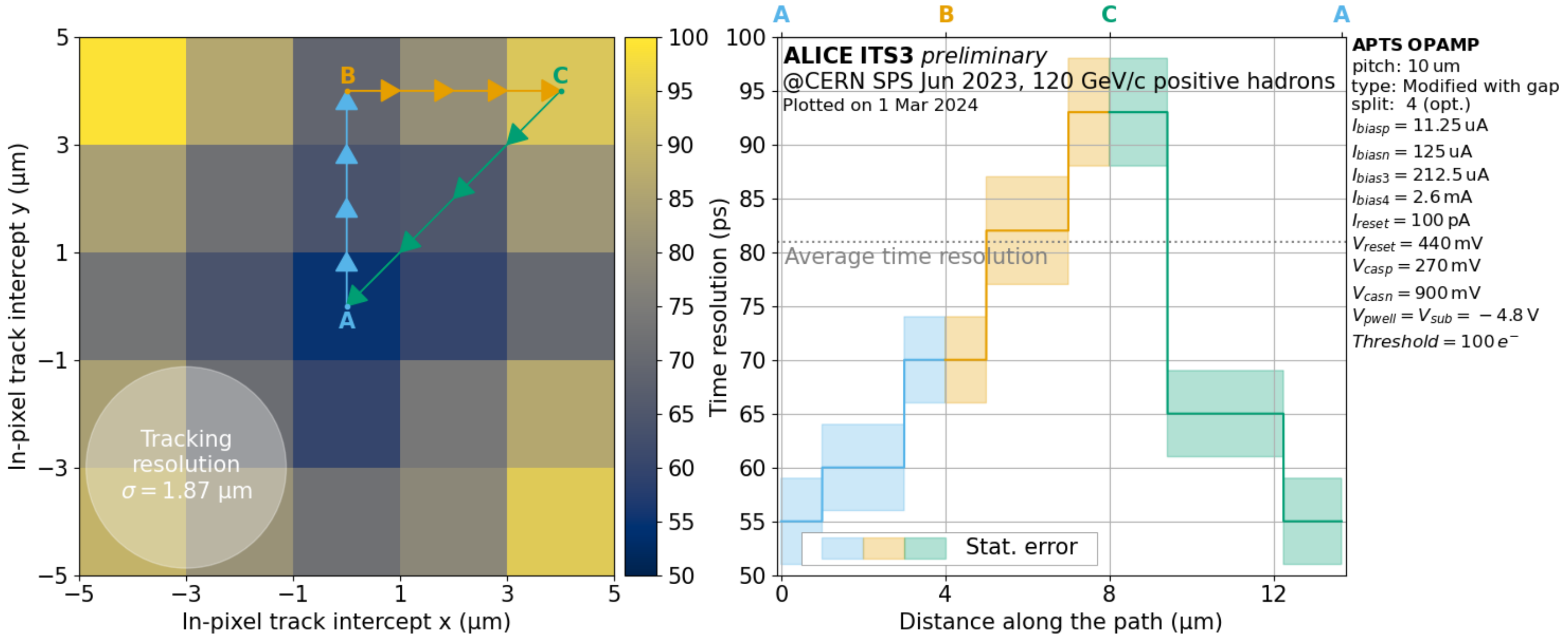


BabyMOSS
mounted on
carrier PCB



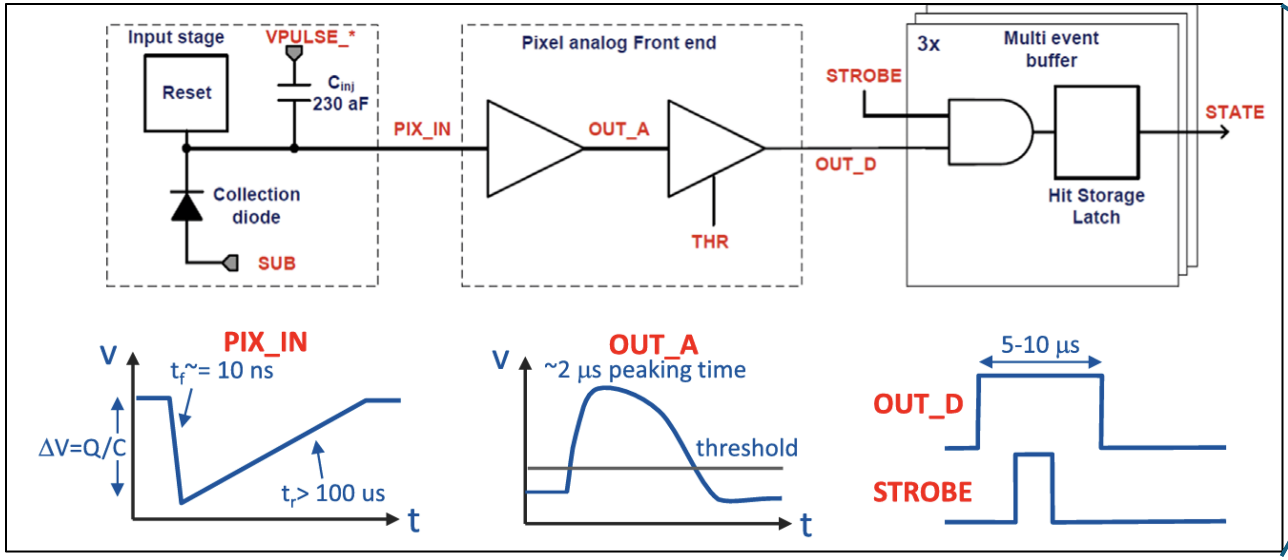
Timing - Intrinsic pixel timing resolution

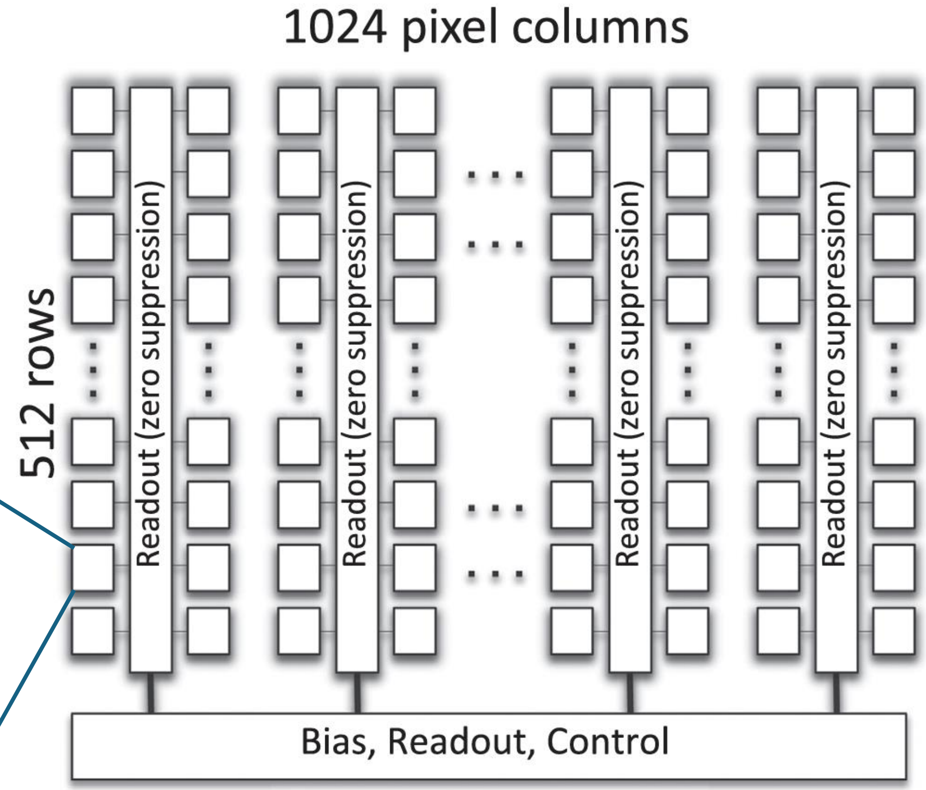
- Intrinsic pixel timing performance is not the problem for the tracker layers!
- With increased power consumption in the pixel front-end a timing resolution below 100 ps demonstrated with APTS-OpAMP
- With moderated settings in DPTS σ_t = 6.3 ns ± 0.1 ns



Timing - Readout with priority encoder

- Synchronous readout with priority encoder
- Pixels with hit write to local event buffer when strobed
- Double pixel column readout sequentially

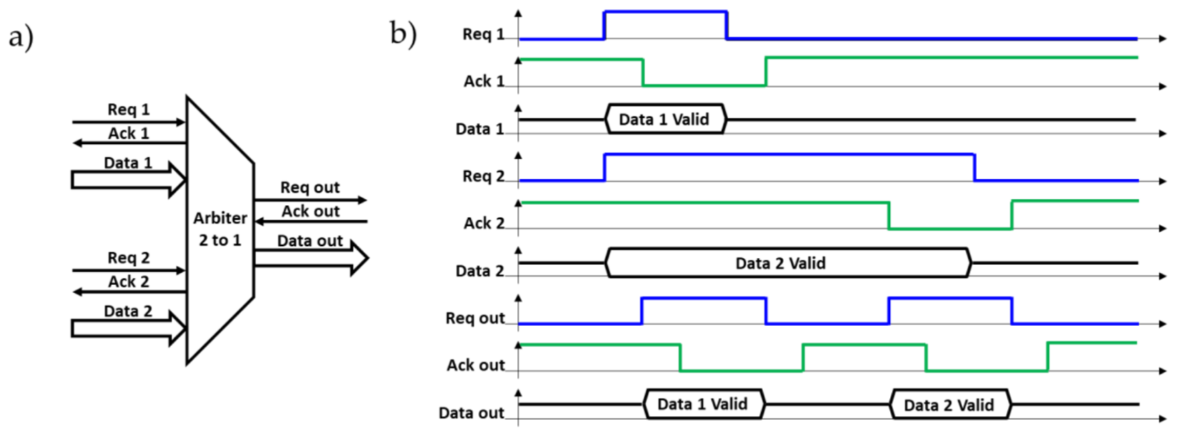


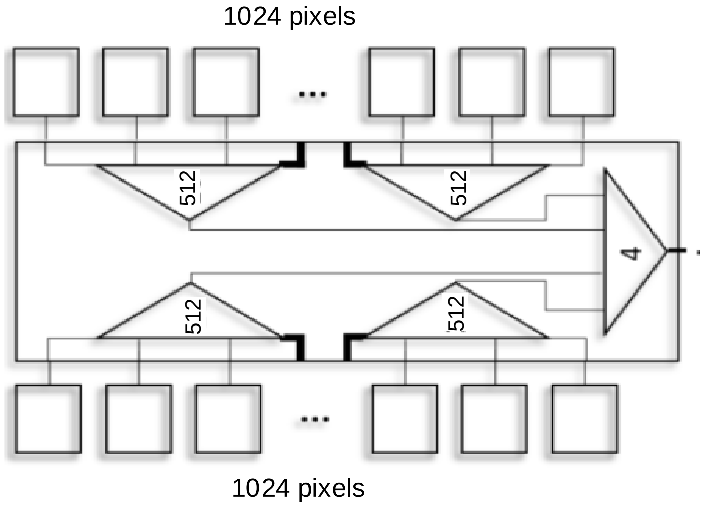


Timing - Readout asynchronously

- Approach described in https://doi.org/10.1016/j.nima.2024.169663
- Based on Asynchronous Fixed Priority Tree Arbiter
  - Asynchronous = no clock distribution
  - Fixed = Hardware-coded priority order in the arbiter
- Upcoming test structure: SPARC (IPHC+IRFU)
  - Chiplet planed for 65nm process in ITS3 ER2
  - Re-use with DPTS pixel FE (provided by CERN)
  - 4 controller sizes tested: 2:1, 4:1, 16:1, 64:1
  - Pixel size: 24.1x16.0 μm^2

Functioning principle

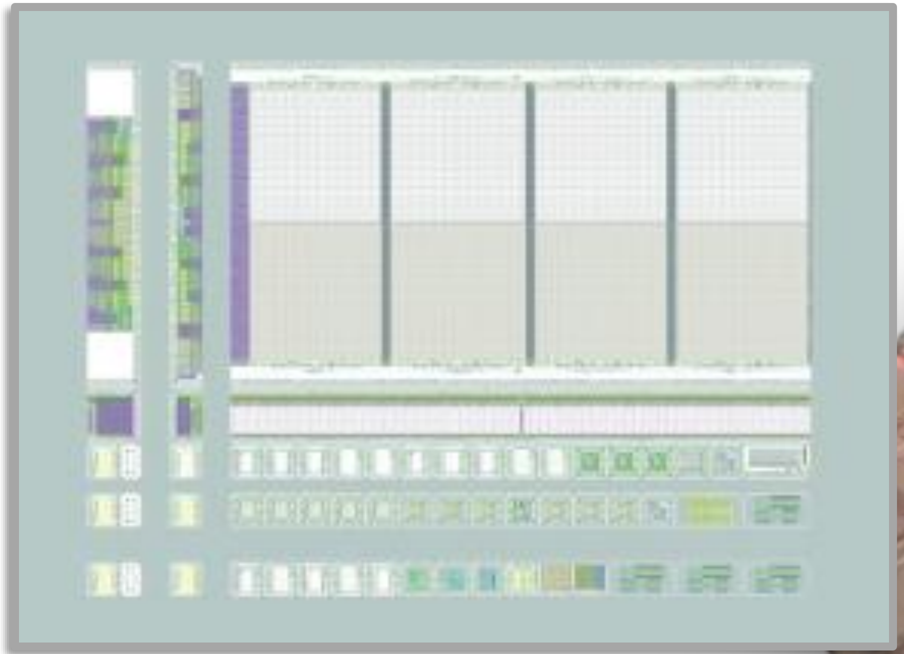




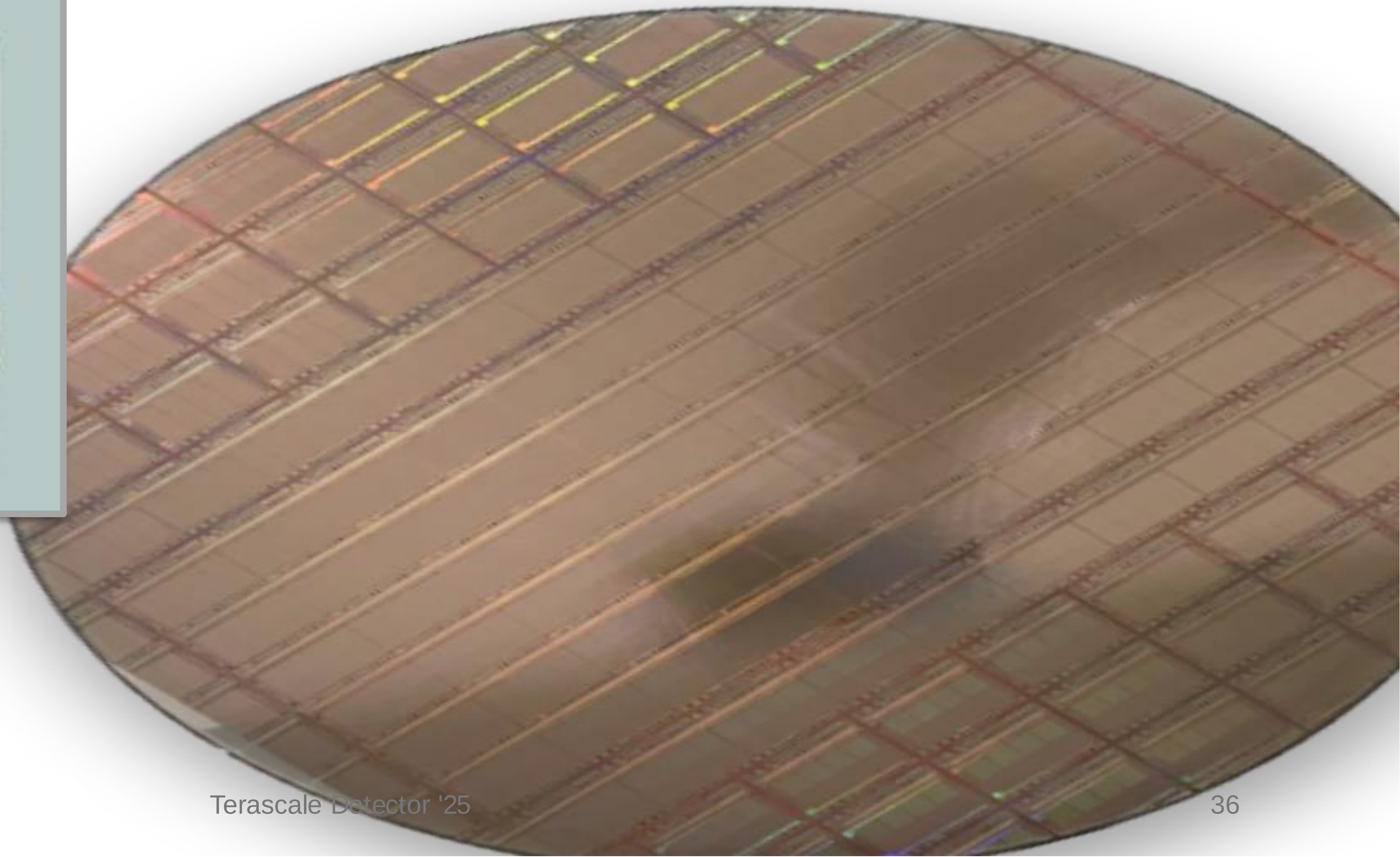
Possible implementation for trackers

MOSS Stitching

ALICE ITS3 Engineering Run 1 Wafer

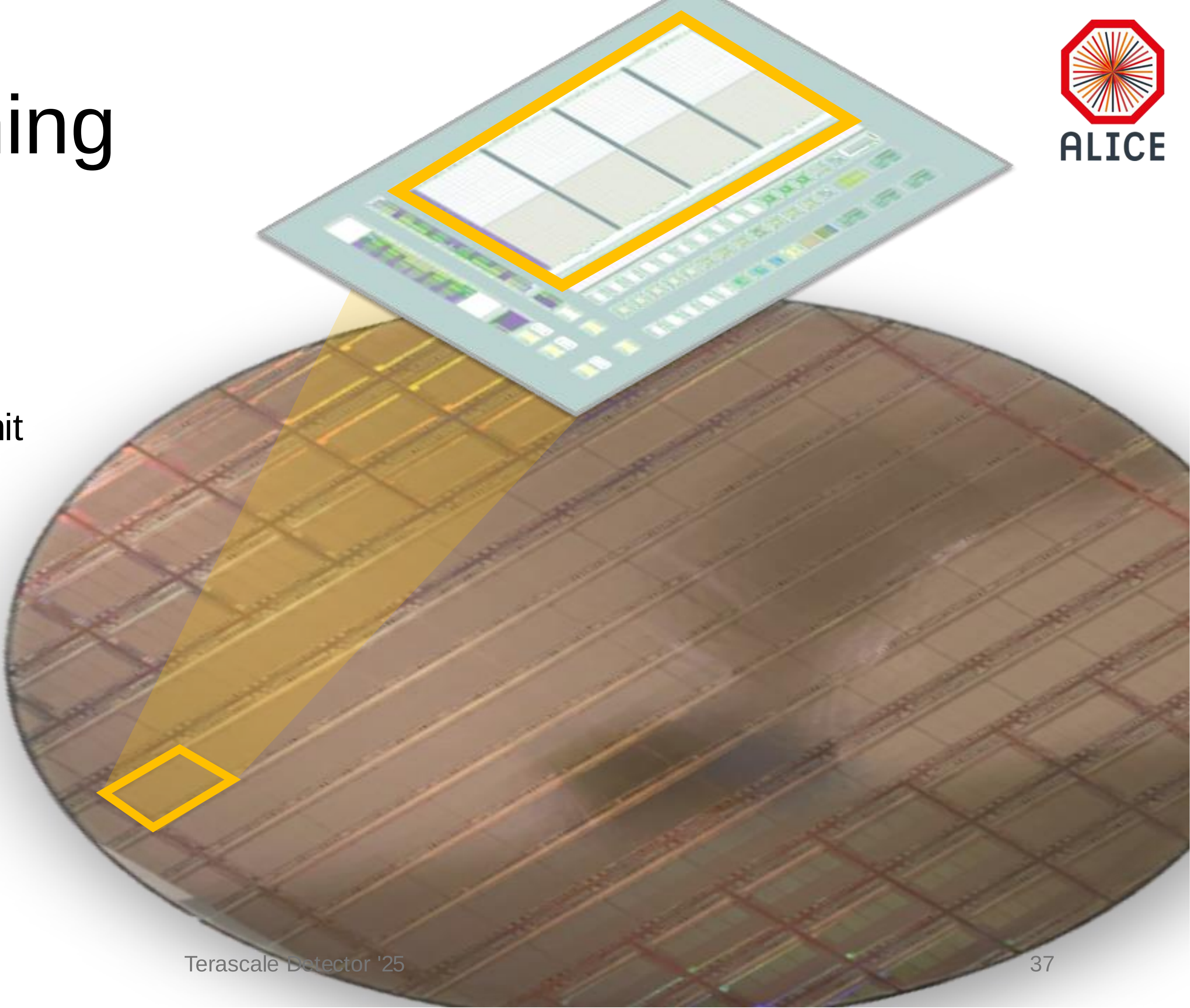


Design reticle

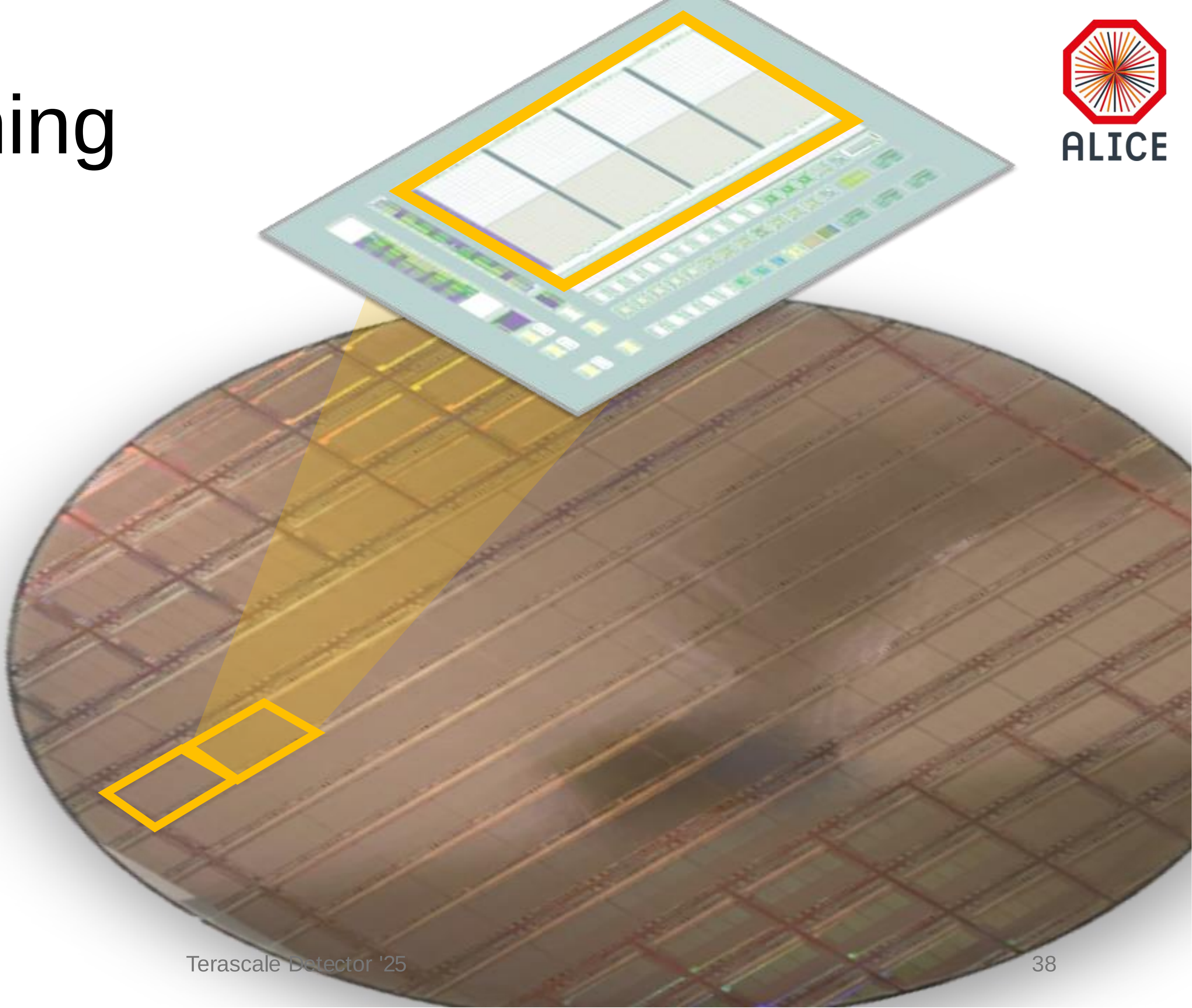


MOSS Stitching

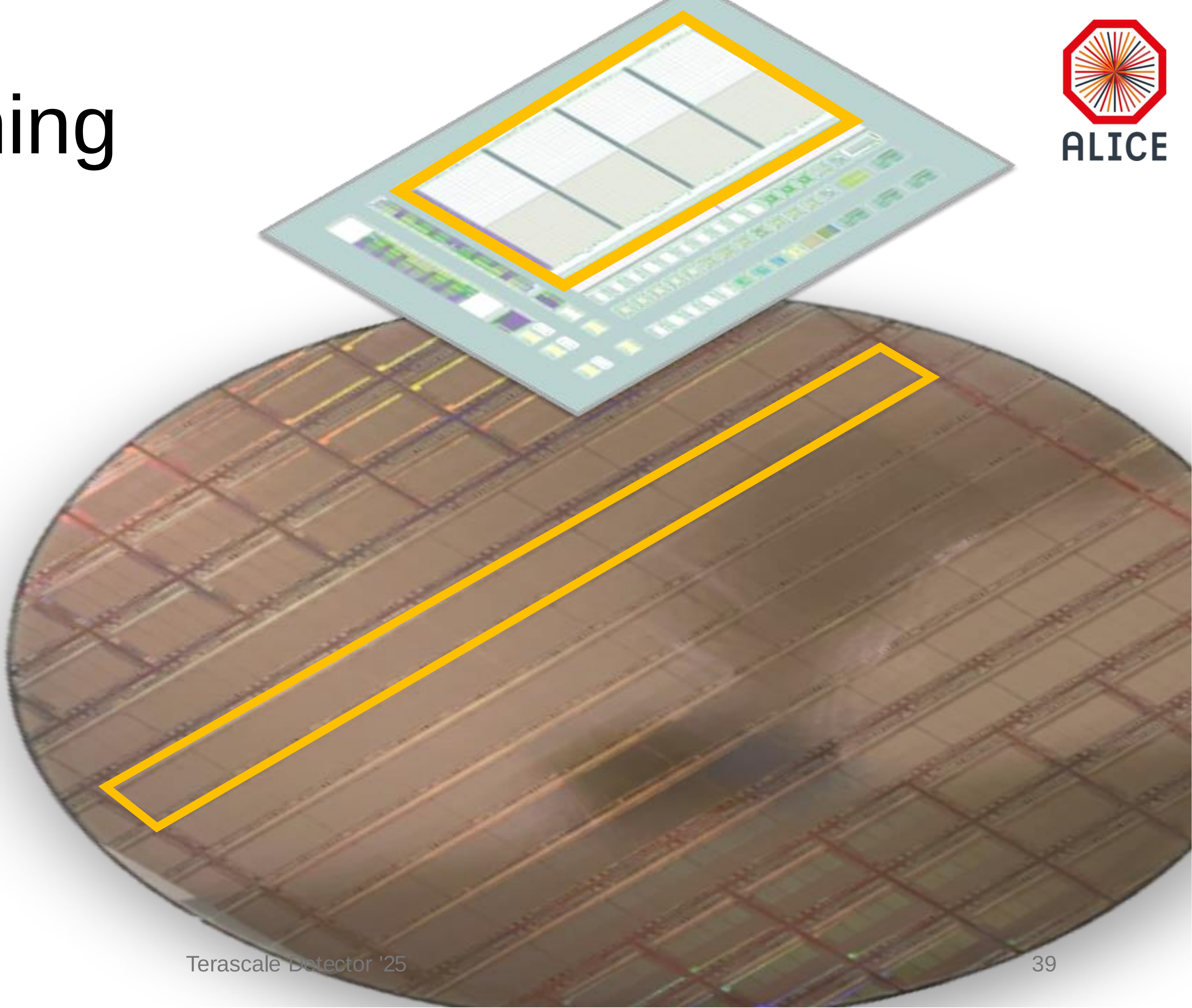
Expose Repeating Sensor Unit



MOSS Stitching



MOSS Stitching



MOSS Stitching

Expose End Caps