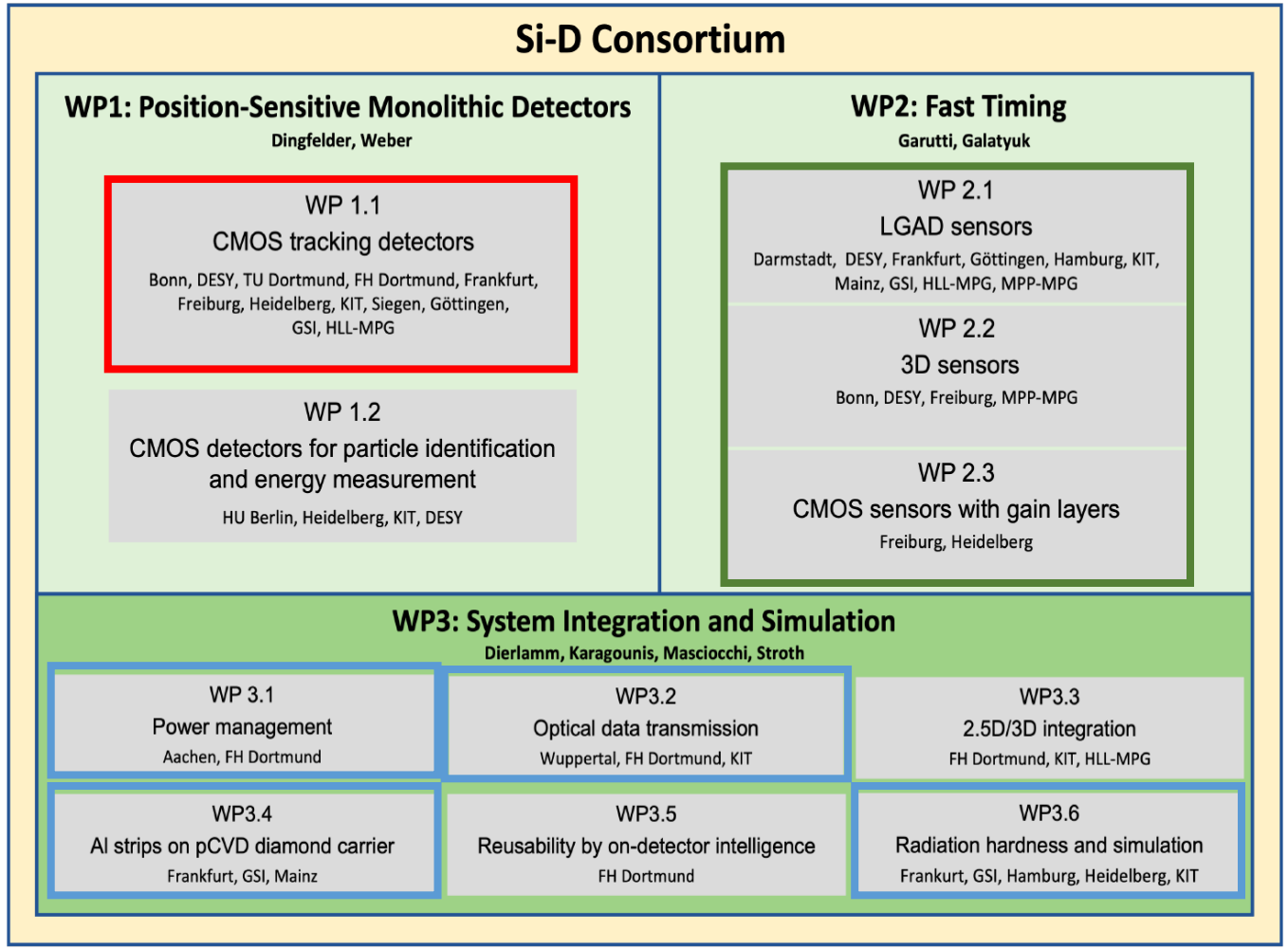
Si-D Consortium

Silicon detector activities in Germany

Jochen Dingfelder (U. Bonn)

17th Terascale Detector Workshop 2025, Bonn

Si-D consortium: Funded projects



WP1.1.1 Low-cost, large-area CMOS sensors with short strips
(**Freiburg**, FH & TU Dortmund, Bonn, DESY)

WP 1.1.2 Monolithic sensors for vertex layers
(**Heidelberg**, **KIT**)

WP 1.1.3 All-silicon modules
(**Bonn**, TU Dortmund, **Göttingen**, Siegen, HLL)

WP2.1.1 Fast timing layer
(DESY, **Hamburg**, Mainz, **Göttingen**)

WP2.1.2 A German LGAD for 4D tracking
(**Hamburg**, HLL, MPP, KIT)

WP2.2 3D sensors for fast timing (sensor & R/O Chip)
(**Freiburg**, **Bonn**, MPP, DESY)

WP2.3 CMOS sensor with gain layer
(**Freiburg**, **Heidelberg**)

WP3.1 Power management
(**Aachen**, FH Dortmund)

WP3.2 Optical data transmission
(**KIT**, Wuppertal, FH Dortmund)

WP3.6 Radiation hardness/simulation
(**Frankfurt**, Hamburg, Heidelberg, KIT, GSI)

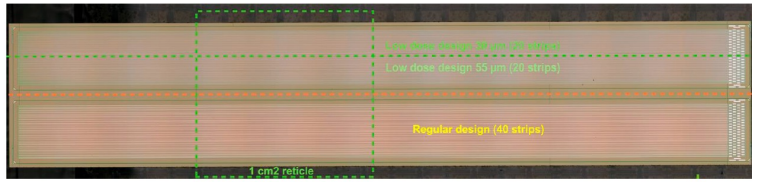
WP3.4 Al strips on pCVD carriers
(**Frankfurt**, Mainz, GSI)

Groups with BMBF R&D funding for 2024-27 in **bold face**

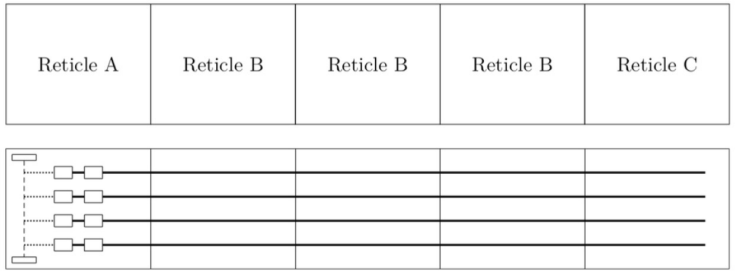
Position-sensitive monolithic detectors

Large-area silicon tracker

Freiburg, TU Dortmund, FH Dortmund, Bonn, DESY



Goal: Build cost-effective large-area silicon detectors for future experiments
Can one simply scale MAPS up in size? → may need too much power

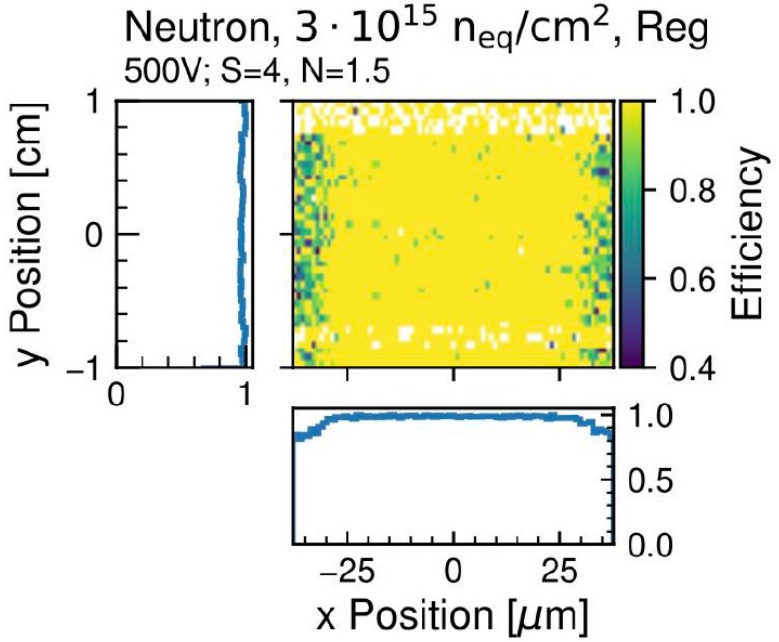


Example: CMOS strip detector

- First stitched passive strip sensors produced on 8'' wafer by commercial foundry, LFoundry 150 nm process

- **Status:**
  - Detailed simulations ongoing to understand properties
  - Very promising results from IV, CV, source and test-beam measurements, even after irradiation to 10^{15} neq cm^{-2}.
  - Stitching proven to work well before and after irradiation

- **Next step:**
  Implement FE directly in sensor → fully monolithic strip sensor



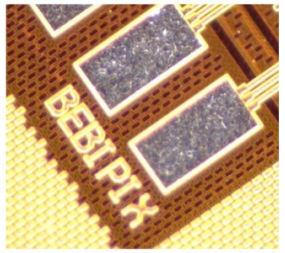
Next-generation monolithic pixel detectors for future detectors

HV-MAPS Heidelberg, KIT

VertexPix

HV-MAPS in IHP 130 nm using SiGe bipolar transistors

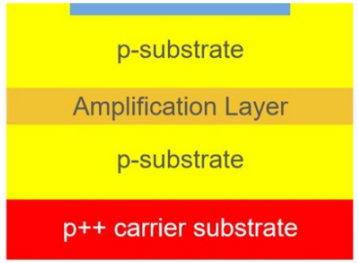
- Finish characterization of existing small-scale prototypes
- Investigate radiation tolerance
  ⇒ development of first fully monolithic small-scale sensor



Internal Gain Layer for HV-MAPS

Using epitaxial wafers with buried gain layer to further enhance HV-MAPS performance

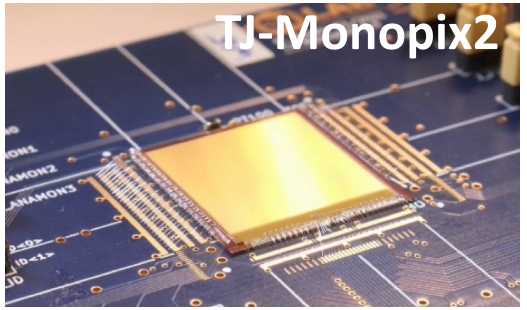
- Feasibility proven in IHP 130 nm (L. Paolozzi)
- TCAD study to find suitable epitaxial structures
- Produce a known sensor on the new wafers



DMAPS Bonn (in collaboration with CERN, CPPM, IRFU)

Monopix series: TJ-Monopix2 (180 nm), LF-Monopix (150 nm)

- Finish characterization of Monopix2
  Show very good performance also after irradiation up to 5×10^{15} neq/cm^2
- TJ-Monopix2 basis for development of OBELIX chip for Belle II VTX upgrade

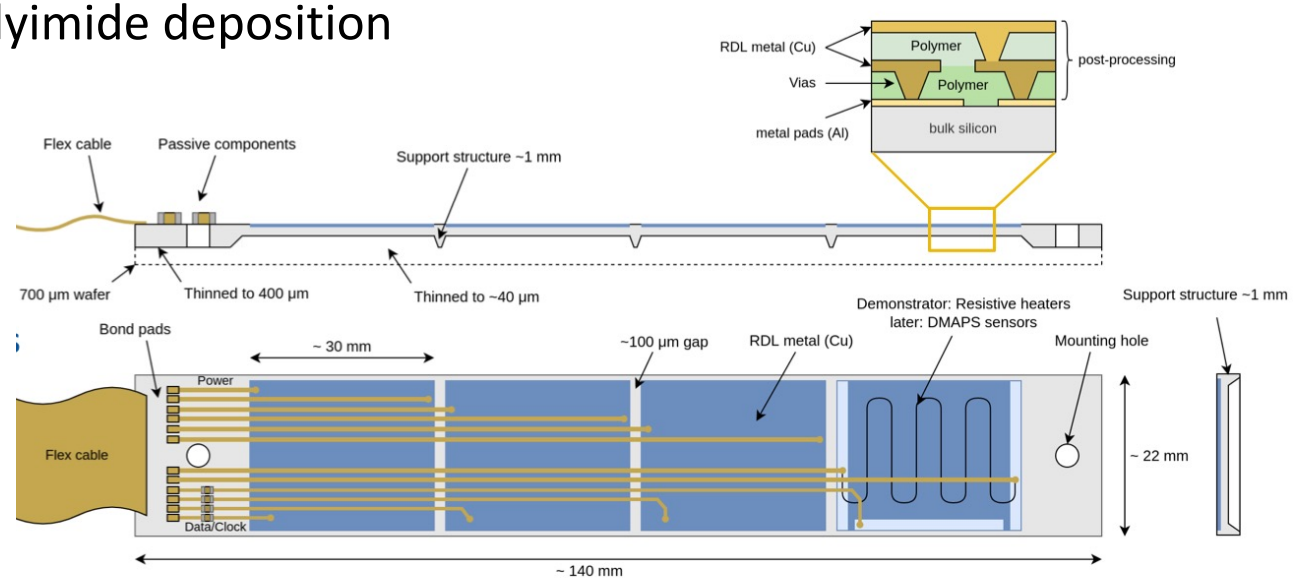


Ultra-thin all-silicon modules

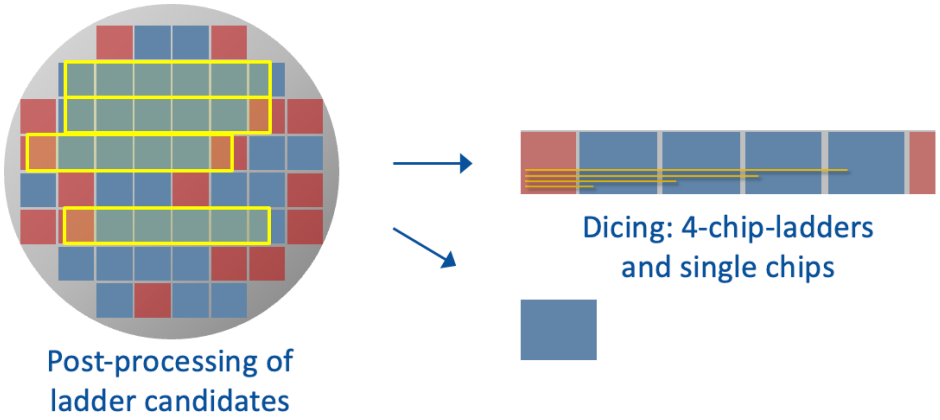
Bonn, Göttingen, TU Dortmund, Siegen, HLL

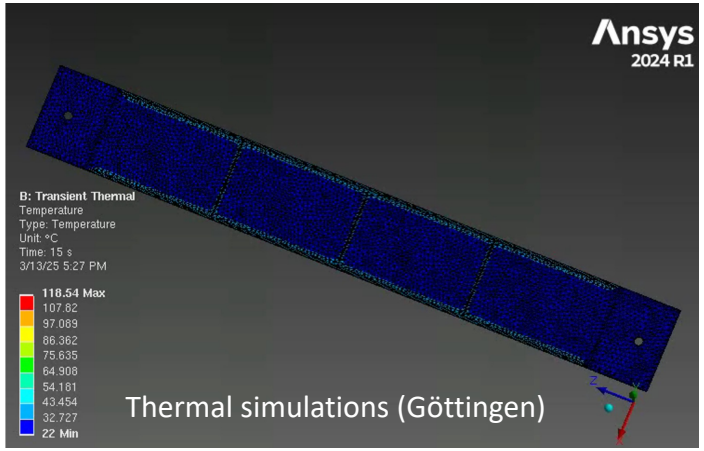
All-silicon modules for DMAPS

- Ultra-light module design
- Integration of power and readout lines directly on wafer (RDL)
  - Test measurements with RDL demonstrator module produced at IZM (thermal and electrical measurements)
  - Building all-Si modules at FTD: Al sputtering and etching, polyimide deposition



- Cooling: Is airflow sufficient?
  Therm-mechanical simulations with ANSYS ongoing at Göttingen

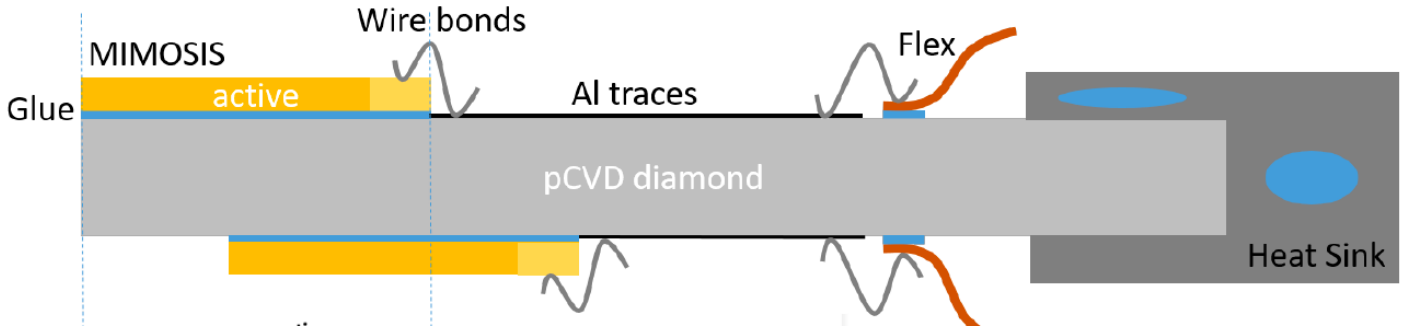




Aluminum-metallized CVD diamond sensor carrier

Frankfurt, Diamond Materials GmbH Freiburg (HSG-IMIT, Freiburg)

Demonstrator for sensor carrier made of CVD diamond with Al-metallization



Combine mechanical support, cooling, electrical connectivity in one (low-material) component

Goal:

Develop demonstrator to evaluate feasibility of carrier to provide

- support and cooling → CVD diamond
- readout and control → Al traces/structures

Technological challenges:

- Metallization of thermal-grade polycrystalline CVD diamond
- Structuring of the metallized layer via lithography
- Wire bonding of traces/pad

Fast timing

LGADs

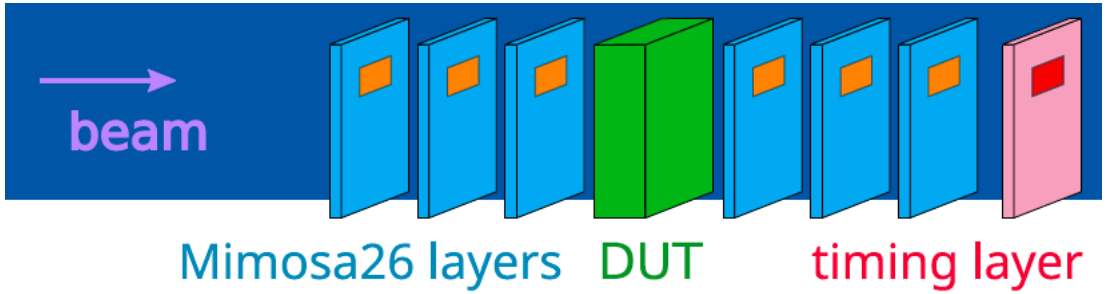
Hamburg

LGAD projects in Si-D:

- **MARTHA** (Monolithic Array of Reach-Through Avalanche photo diodes)
  Pixelated LGADs with 100% fill factor without edge breakdown (developed by HLL)
  → Analysis of first test structures ongoing

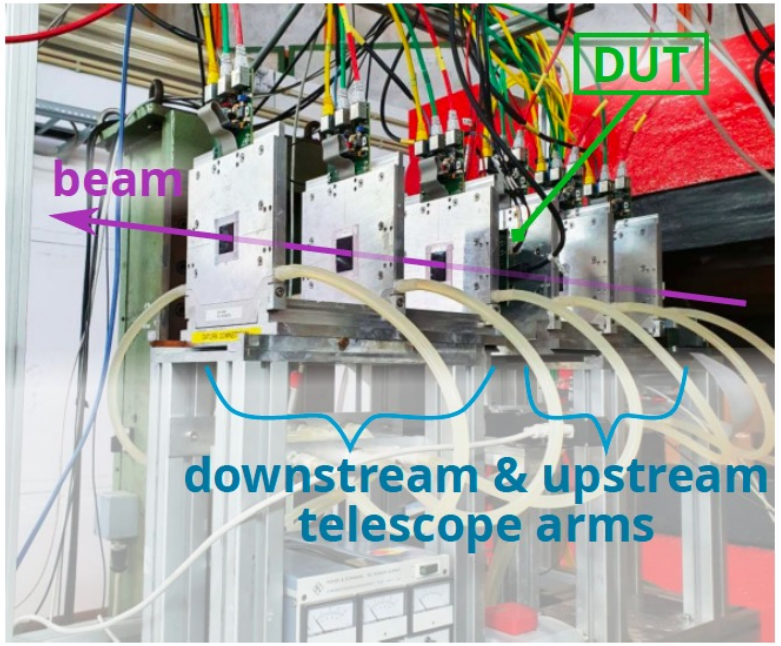
- **Radiation hardness**
  Defect-engineered diodes mimicking gain layer degradation in LGADs (continuation of RD50 project in DRD3)
  → First samples expected in April

- **LGADs for timing layers**



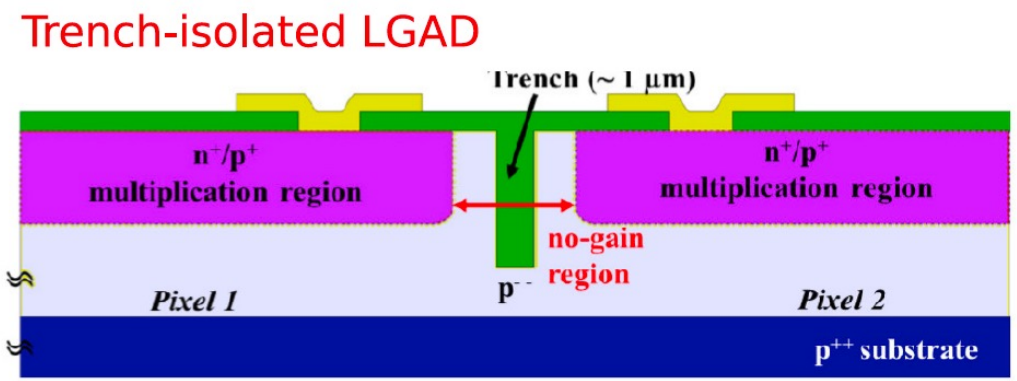
Time resolution ≪ 100 ps

LGADs with Timepix3/4 readout

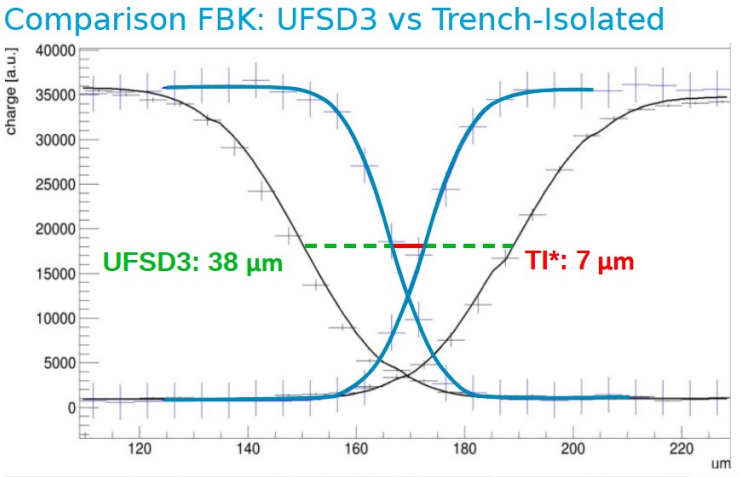


LGADs for timing layers

First prototypes: Trench-isolated LGADs (HBK)

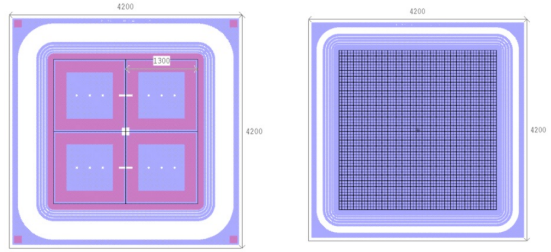


[doi: 10.1109/LED.2020.2991351]

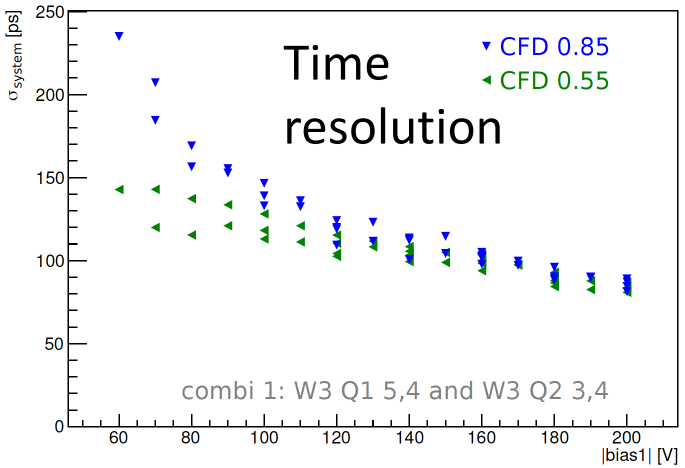


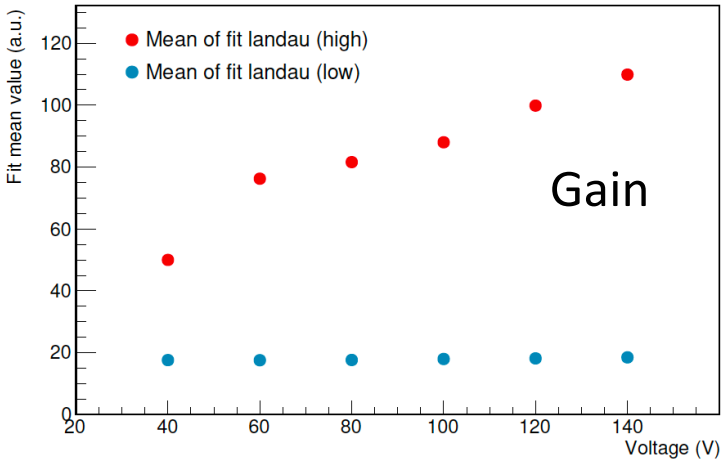
[F. Siviero, 35th RD50 workshop, Nov 2019]

- Test structures: 2 × 2 pixels, pitch: 1.3 mm → read out with oscilloscope
- Small pixel sensors: 55 × 55 µm, pitch: 55 µm → read out with Timepix3



First Testbeam measurements at DESY in Sep. 2024 (3 GeV e beams)



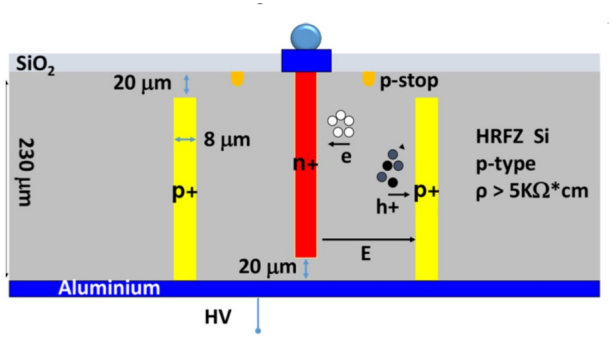


Work in progress …

Thanks to Annika Vauth

Fast timing with 3D sensors

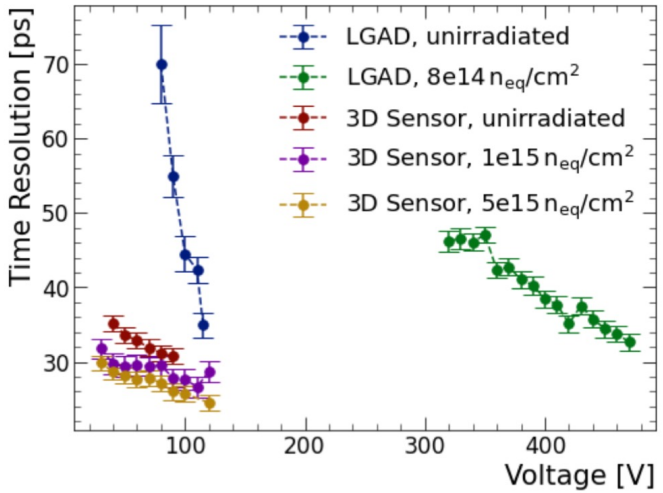
Freiburg, KIT, Bonn (in collaboration with U. Thessaloniki)

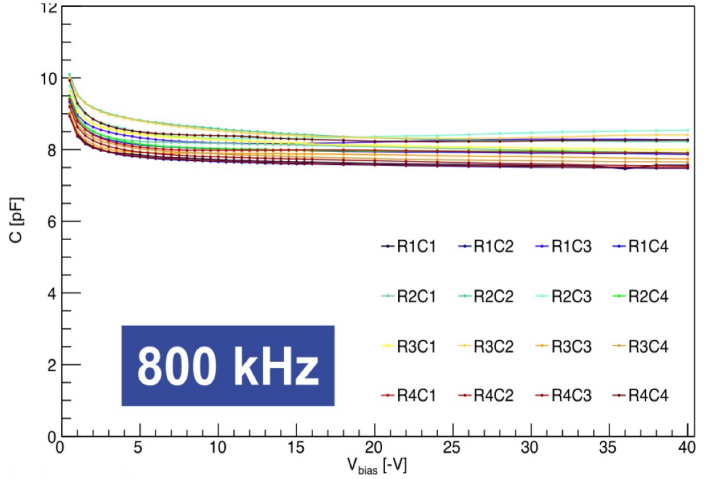


Sensors (produced by CNM)

RD50 common project sensors (+ old IBL 3D sensors)

- Hexagonal and orthogonal pixel geometries
- Initial characterizations done: I(V), C(V)
- Next steps:
  - Irradiation to high fluences (> 5 × 10^{16} neq cm^{-2})
  - Laboratory timing measurements





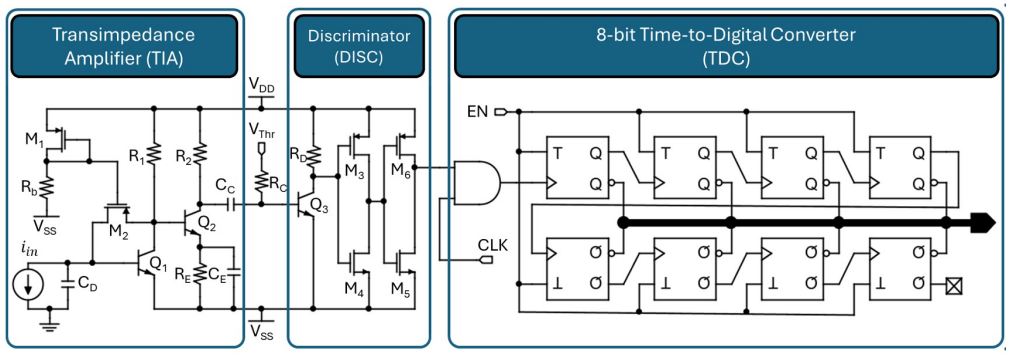
Thanks to Roland Koppenhöfer

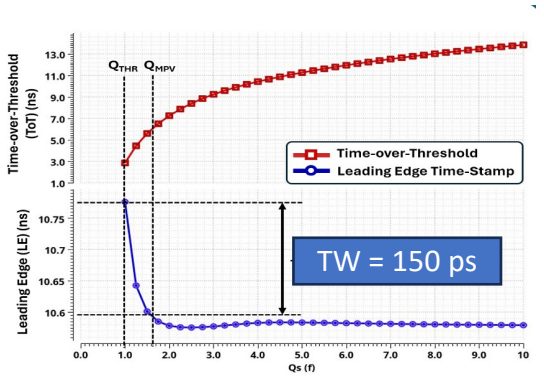
Readout chip

Design of dedicated readout ASIC with high-bandwidth analog FE adapted to large sensor capacitance

- 130 nm SiGe BiCMOS technology
- First design studies
- Tape-out of first test structures planned for summer 2025

Design/simulations by A. Michailidis





System integration and simulation

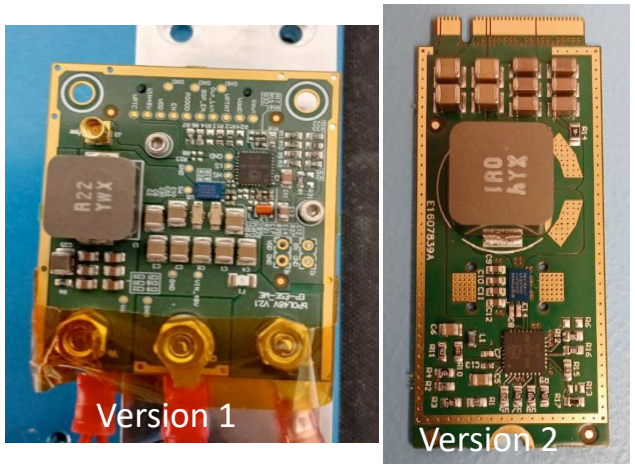
Power management: DC-DC conversion

RWTH Aachen, FH Dortmund

Explore use of DC-DC converters with a high conversion ratio in silicon modules

- Use bPOL48V by CERN, consists of a rad.-hard CMOS controller designed at CERN and a commercial Gallium Nitride power stage
- Characterization measurements: Efficiency, line and load regulation, conducted and radiated noise, thermal aspects
- Test in-system use with silicon strip modules of the CMS Phase-2 outer tracker

bPol48V prototypes



Status:

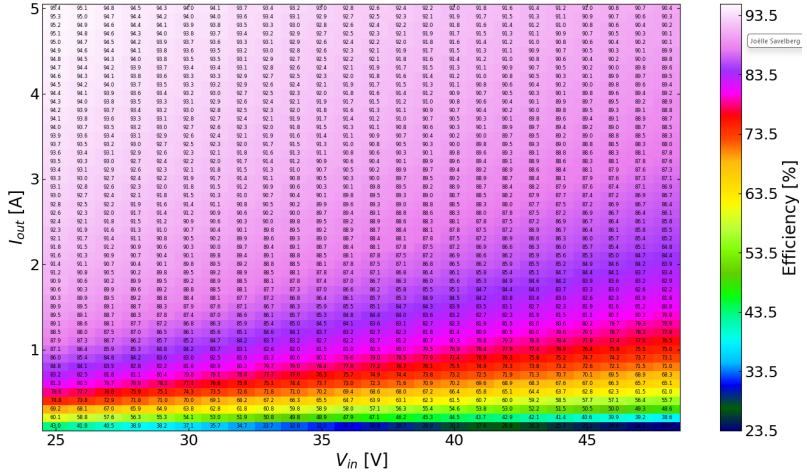
- Several setups have been installed or recommissioned
- Three different prototypes have been delivered by CERN and are being characterized
- Study of performance of different shielding options
- Investigation of PCB coils

New DC/DC converter and Shunt-LDO architectures:

- Explore new DC/DC converter architectures for next-generation power applications in HEP (hybrid converters)
- Study of new Shunt-LDO regulator architectures with higher on-chip efficiency (65 nm → 28 nm)

DC-DC conversion: Selected measurements

Efficiency as a function of V_{in} and I_{out}



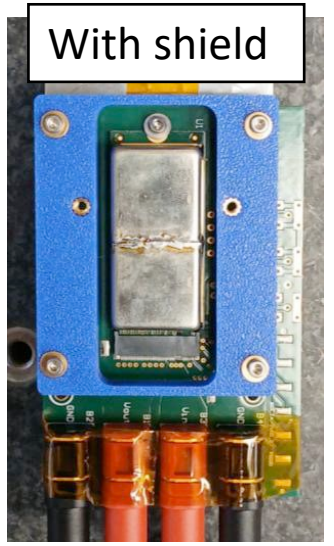
$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}}$$

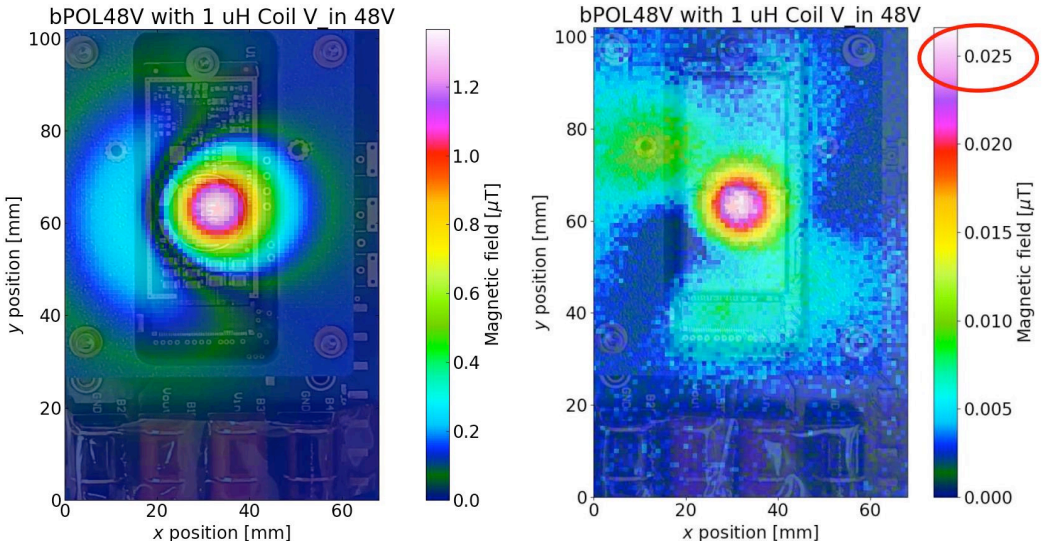
→ Efficiency well above 90 % in a large working range

Radiated noise measurement

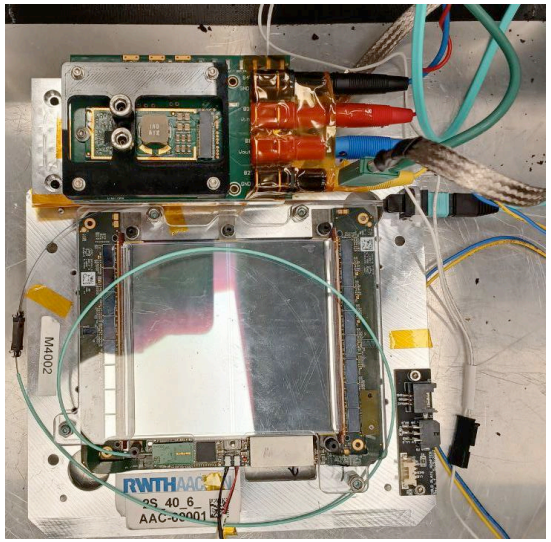
Without shield

With shield





CMS 2S-module powered by a bPol48V and read out



Powering scheme:

48V

bPol48V

bPol12V

bPol2V5

1.25V

Thanks to Katja Klein, Joelle Savelberg

Silicon photonics for tracking detectors

Vision: Develop **HV-CMOS pixel detector for high rates** featuring **high-bandwidth links** together with an **optical link** consisting of **driver chip** and **photonic ring modulator**
→ **Demonstrator chain from sensor to back-end**

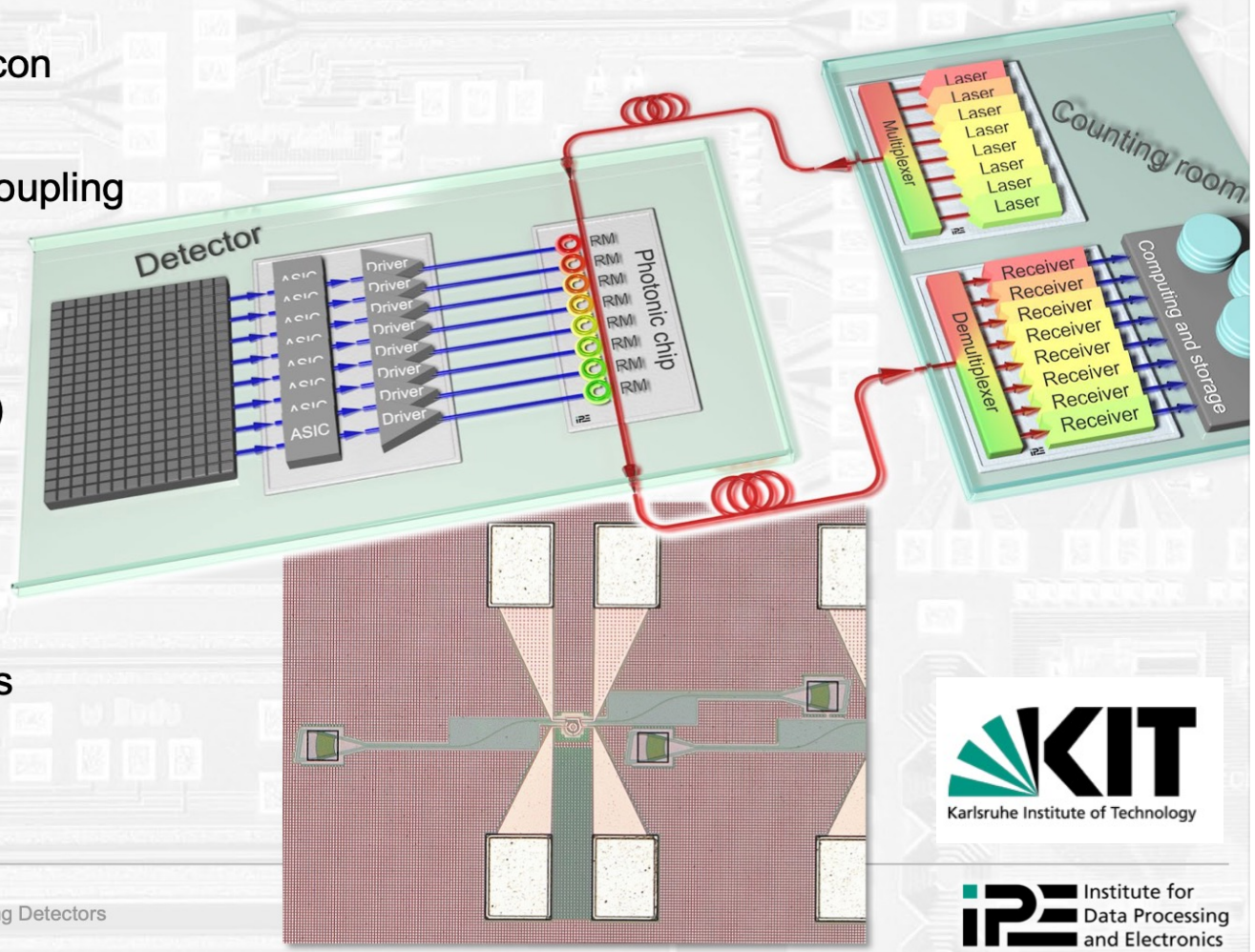
- Wavelength division multiplexing (WDM) for higher bandwidth per fiber
- Electrooptic modulators with external lasers
- Ring-resonator modulators (RM) made of silicon
- SiGe driver ASIC
- Interconnection technologies and fiber-chip coupling

WP3.2: Optical data transmission

- Development of
  - 4-channel RM-WDM system (4x25 Gb/s)
  - SiGe driver ASIC
  - Interconnection technologies (TSVs)

WP3.6: Radiation hardness and simulations

- Radiation effects on SiGe HBTs and FETs, as well as on silicon photonic RMs
  - First irradiations started



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