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Cold Electronics: Lessons from Cryogenic Neutrino Detectors

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For the DUNE Collaboration

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Why Liquid Argon?

Liquid argon calorimeters have:

- Excellent scintillation (~ 24000 photons / MeV) and good ionization (23.6 eV / electron) yields, with uniform response over a large volume
- Radiation hardness
- Relatively low cost, allowing very large detectors

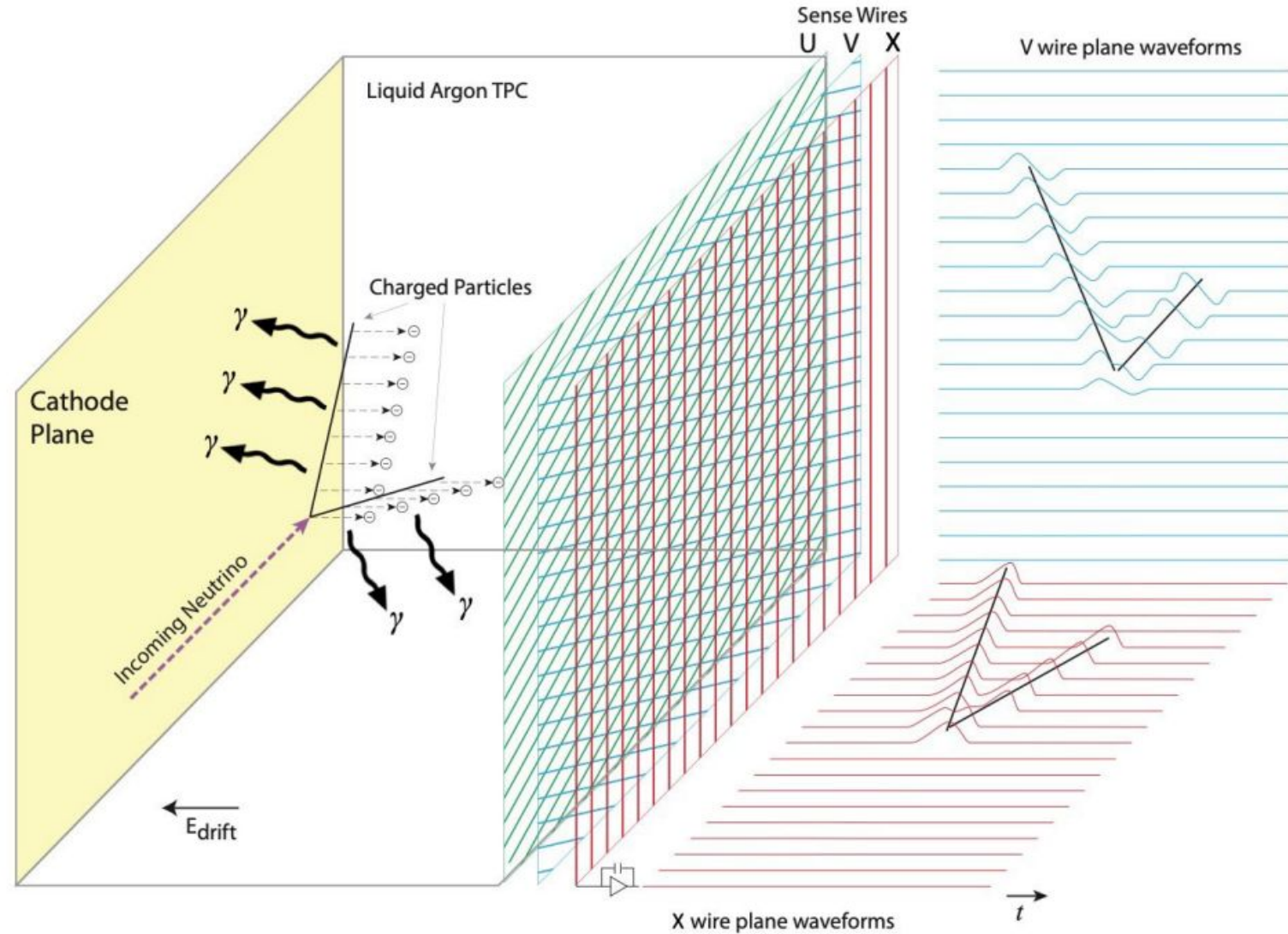
In collider experiments, these properties are exploited for use in **segmented** LAr calorimeters

These properties are similarly useful for accelerator-based neutrino experiments, but instead in the form of (mostly) **monolithic** liquid argon detectors

Liquid Argon Time Projection Chambers

Neutrino detectors use LAr TPCs for 3D event reconstruction

- A wire plane array reads a volume with drift distances up to **3-6 meters**
 - Need to sustain ~ 500 V/cm field over this distance
 - < 0.1 ppb purity requirement
 - Not good with high pileup conditions!
- Multiple plane arrays to localize the signal in 2 dimensions
 - ~ 5 mm resolution from wire spacing
- **Scintillation light** needs to be detected to provide a $t=0$, providing localization along the drift direction



Charge Readout Electronics for LArTPCs

As a **minimum requirement**, we need to be able to detect $O(\text{MeV})$ deposits per channel to resolve MIPs

- Very conservatively, this signal would be >10000 electrons (depending on wire spacing, field strength, and purity)
- Aim for noise levels of <1000 electrons equivalent noise charge (ENC) per channel

Even when other aspects of electronics design are optimized, amplifiers have a fundamental limit associated with the first transistor noise that **scales with input capacitance**

- Wire capacitance is unavoidable, but cables will contribute too

In a LArTPC large enough for neutrino measurements, charge-collecting components are $O(\text{meters})$ away from room-temperature electronics

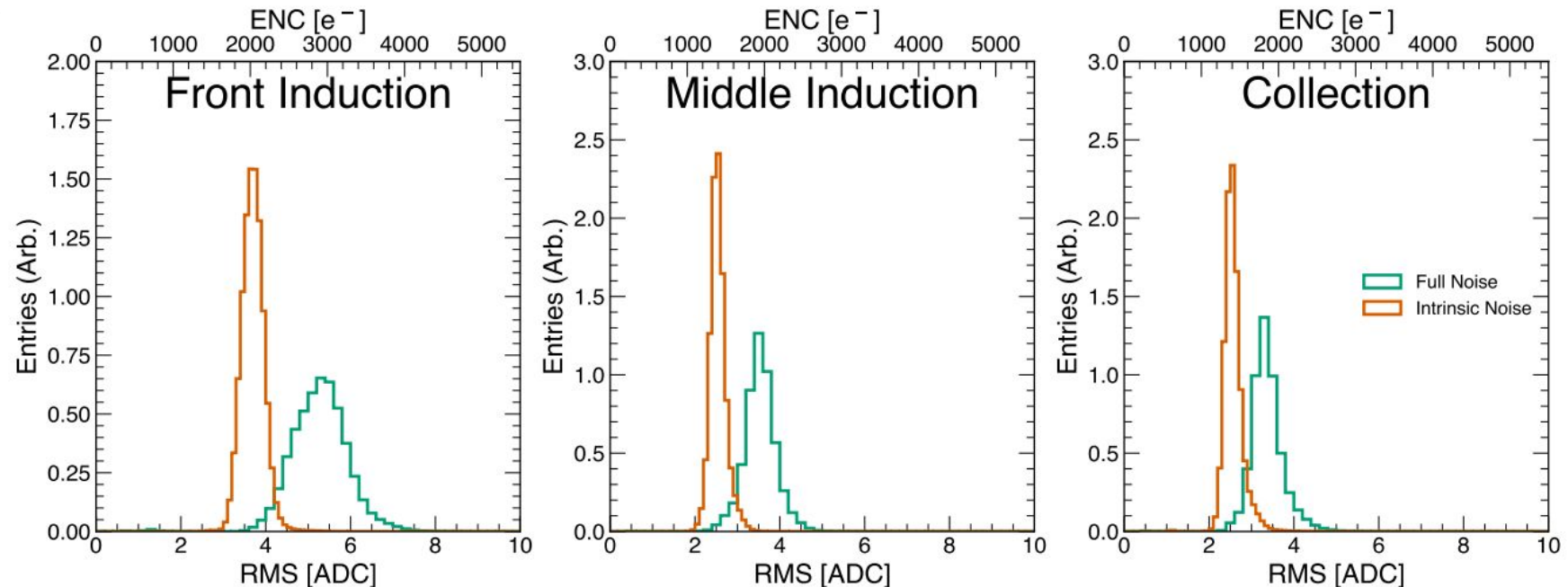
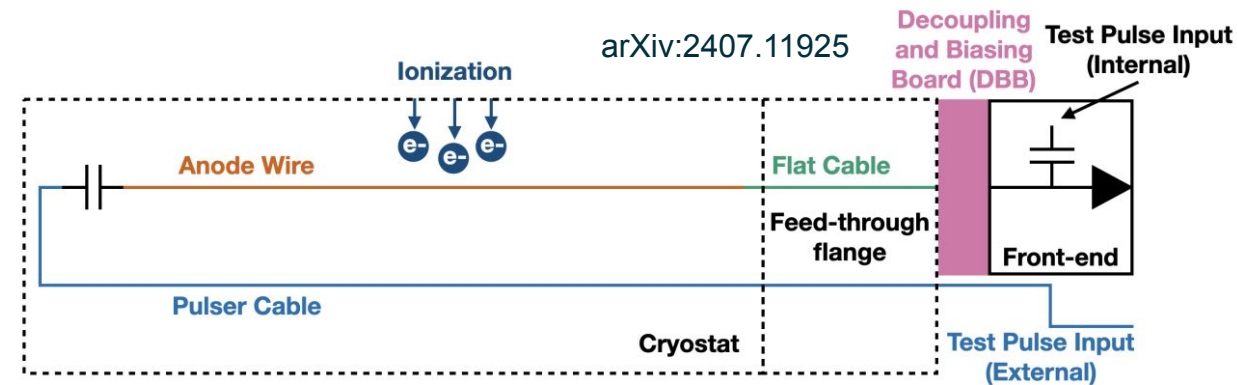
Warm Readout Electronics

The ICARUS experiment (first at LNGS and now at Fermilab) uses warm front-end electronics for LArTPC charge readout

A MIP produces ~ 15000 electrons on a collection channel, depending on purity

“Intrinsic noise” is what is left after offline filtering

- Limited by the amplifier design and input capacitance per channel



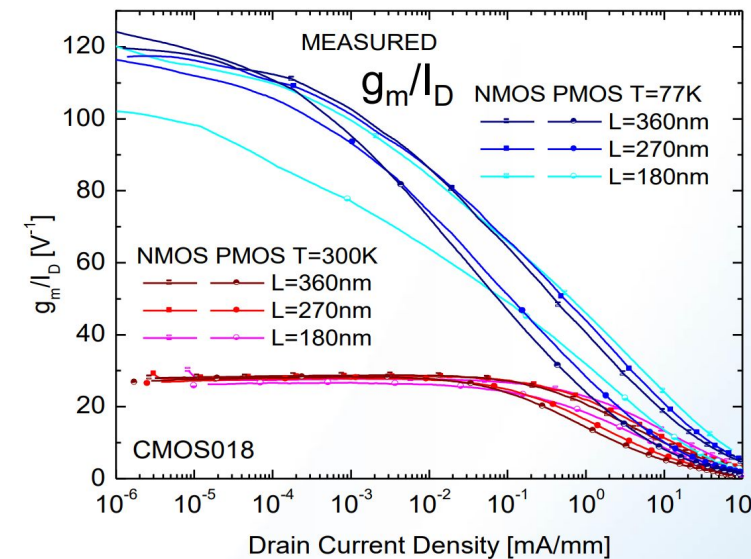
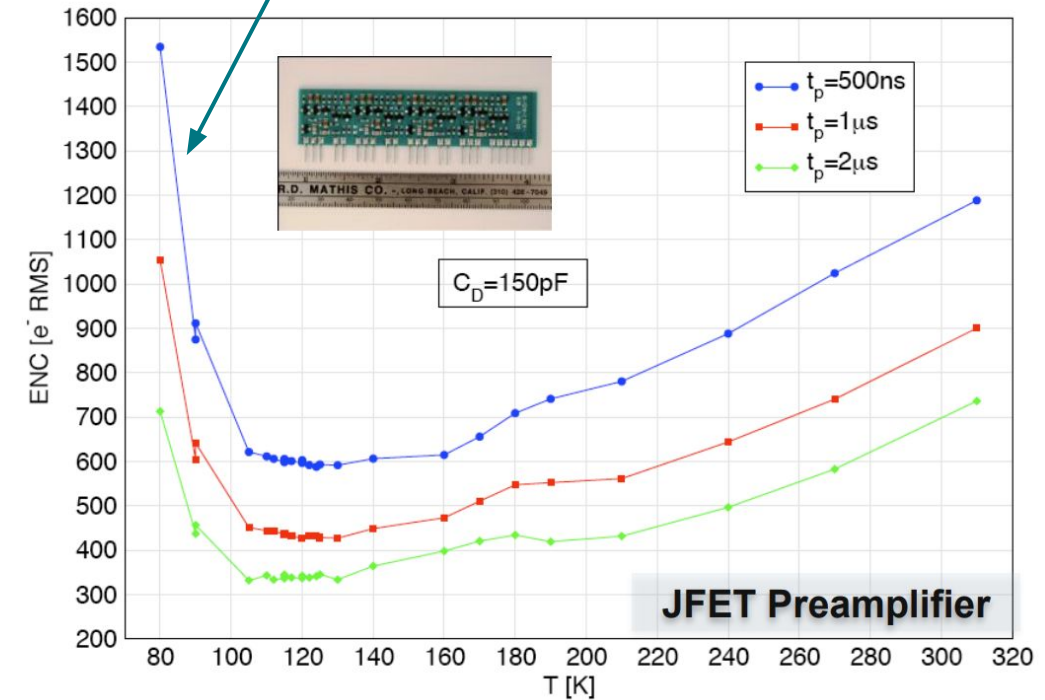
Cryogenic Charge Amplifiers

Putting the charge amplifier in the cryostat has several advantages:

- Eliminate additional input capacitance and pickup from cables
- Reduction of thermal noise
- Increase in carrier mobility and transistor transconductance

Designs have converged towards CMOS-based ASICs, which are now widely used in cryogenic regimes

JFET amplifier with rise in noise as carrier freeze-out begins



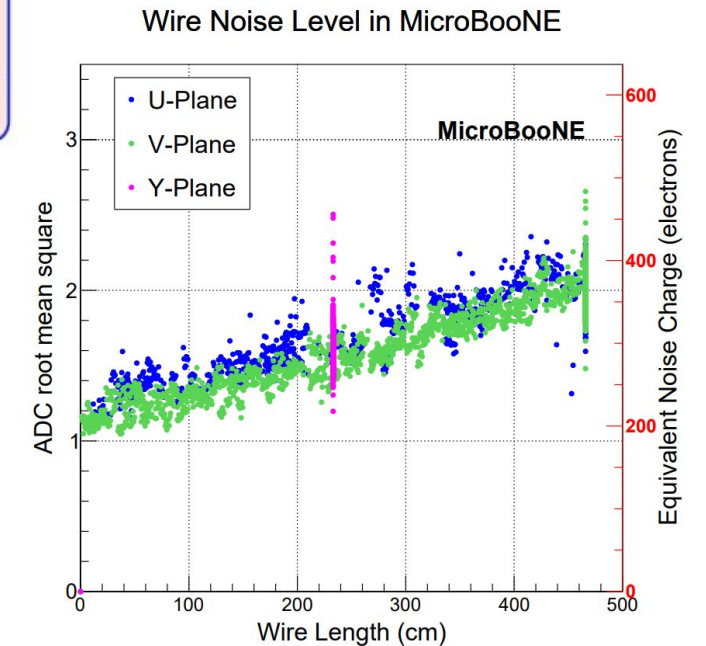
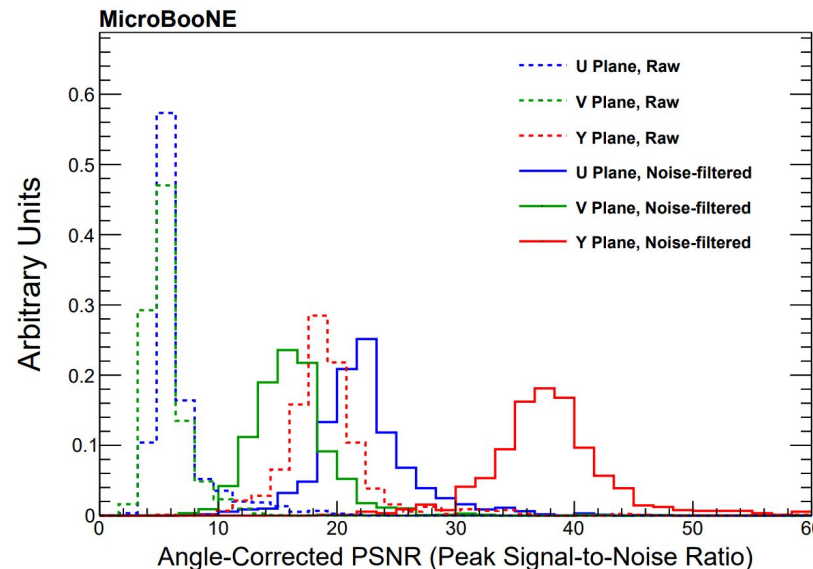
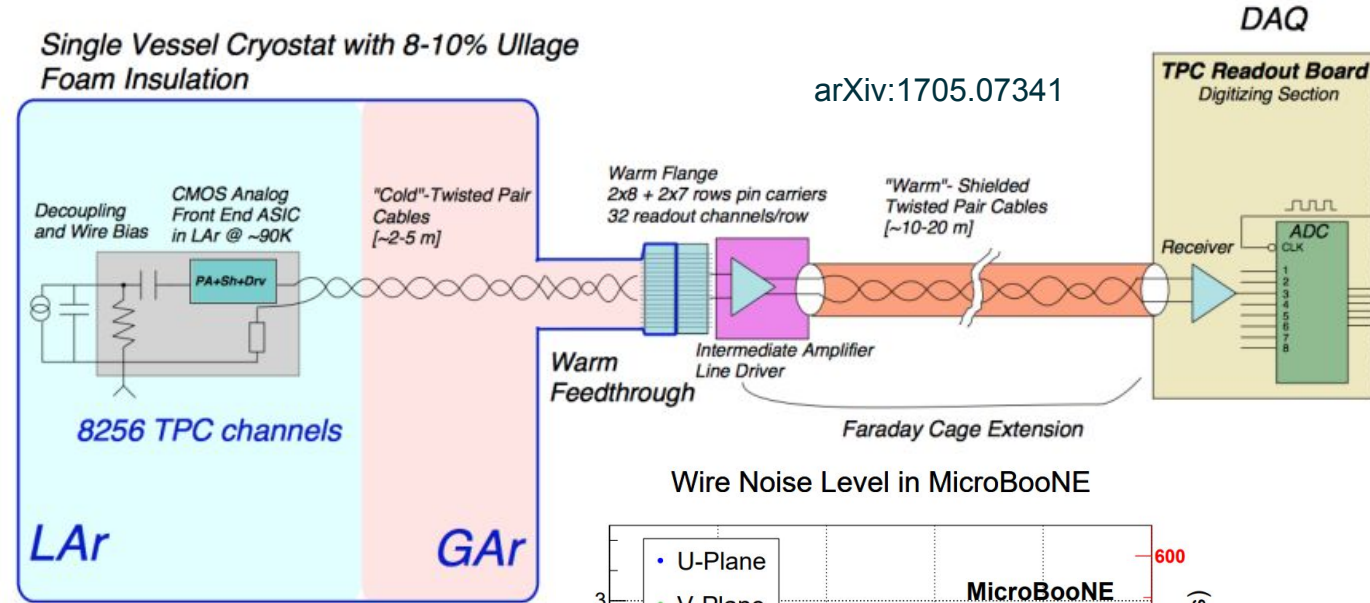
Cryogenic ASICs for Charge Amplification

MicroBooNE was a LArTPC short baseline neutrino experiment using the Booster neutrino beamline at Fermilab

For charge readout it used the **LArASIC**, a signal amplification and shaping ASIC built in 180 nm CMOS for operation in LAr

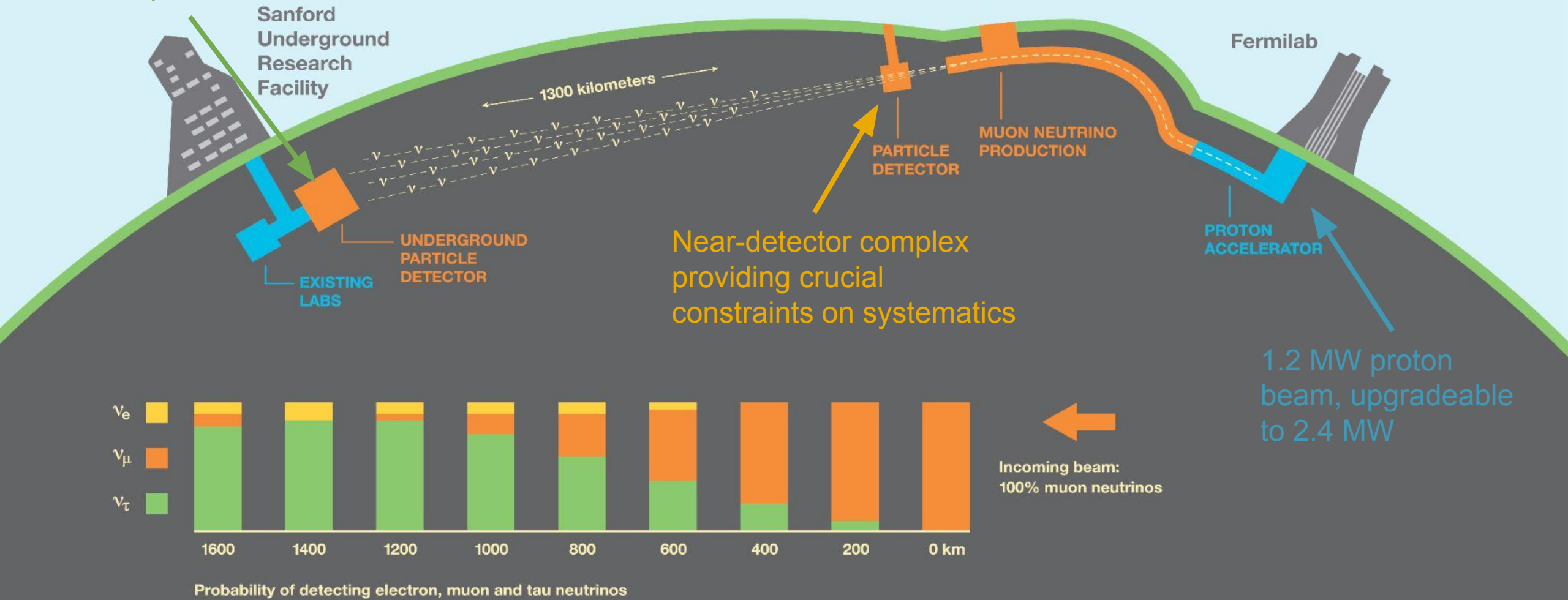
Much lower noise levels achieved!

- SNR calculated against MIPs



Up to 4x17 kilotons of liquid argon far detectors measuring the oscillated neutrino spectrum

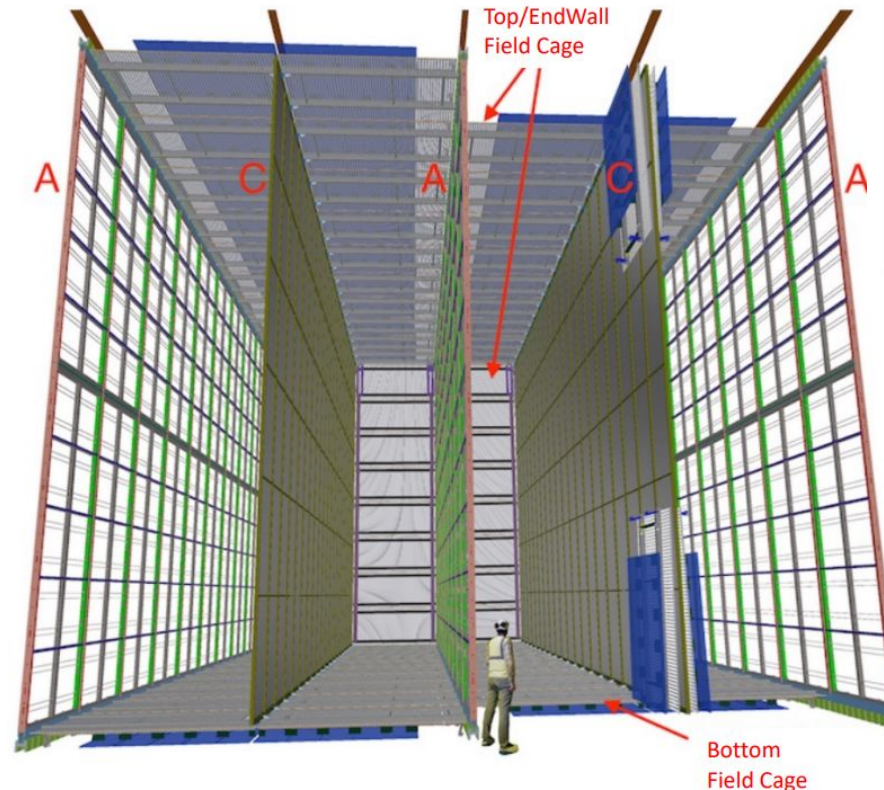
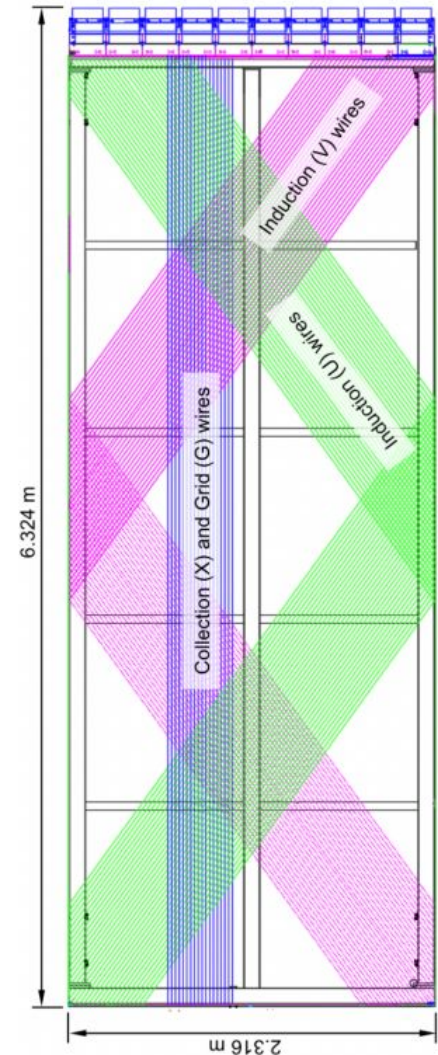
Deep Underground Neutrino Experiment



DUNE Far Detectors

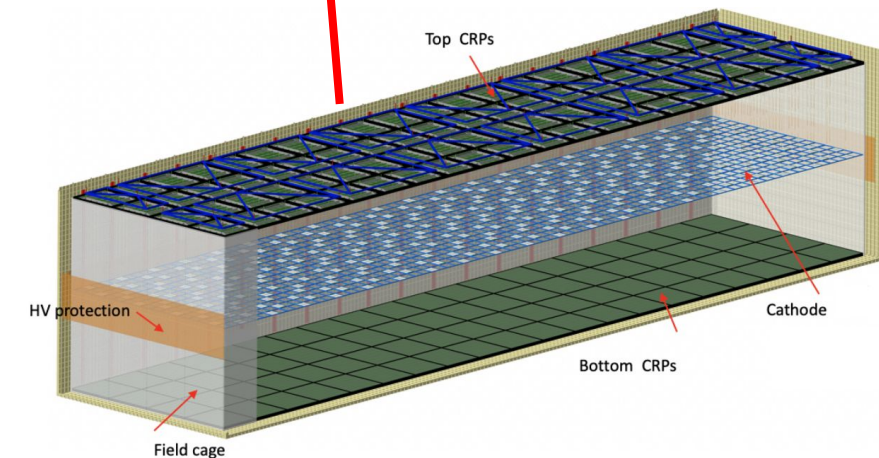
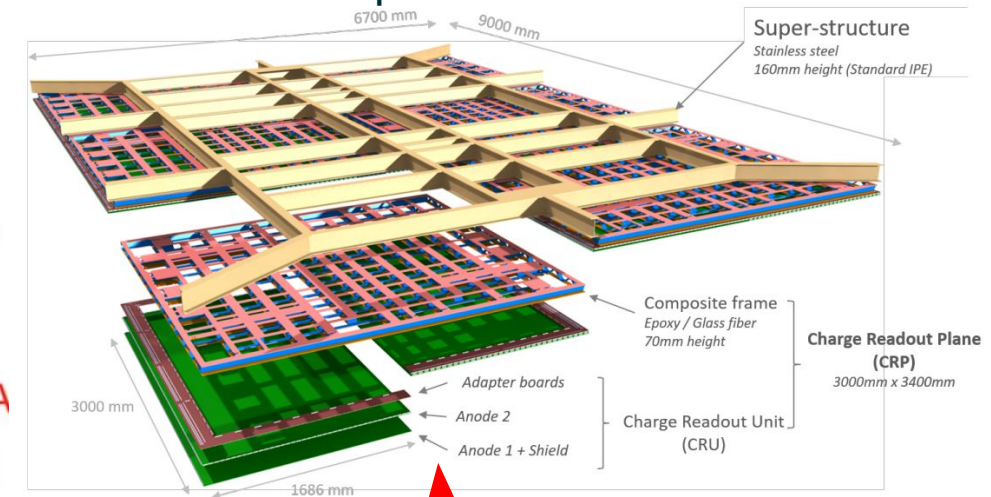
FD1 - Horizontal Drift:

- 150 wire-plane anode plane assemblies (APAs), arranged into 4 drift volumes
- 2560 channels per APA



FD2 - Vertical Drift:

- 160 charge-readout planes (CRPs), using PCB strips instead of wires for charge readout
- 3072 channels per CRP

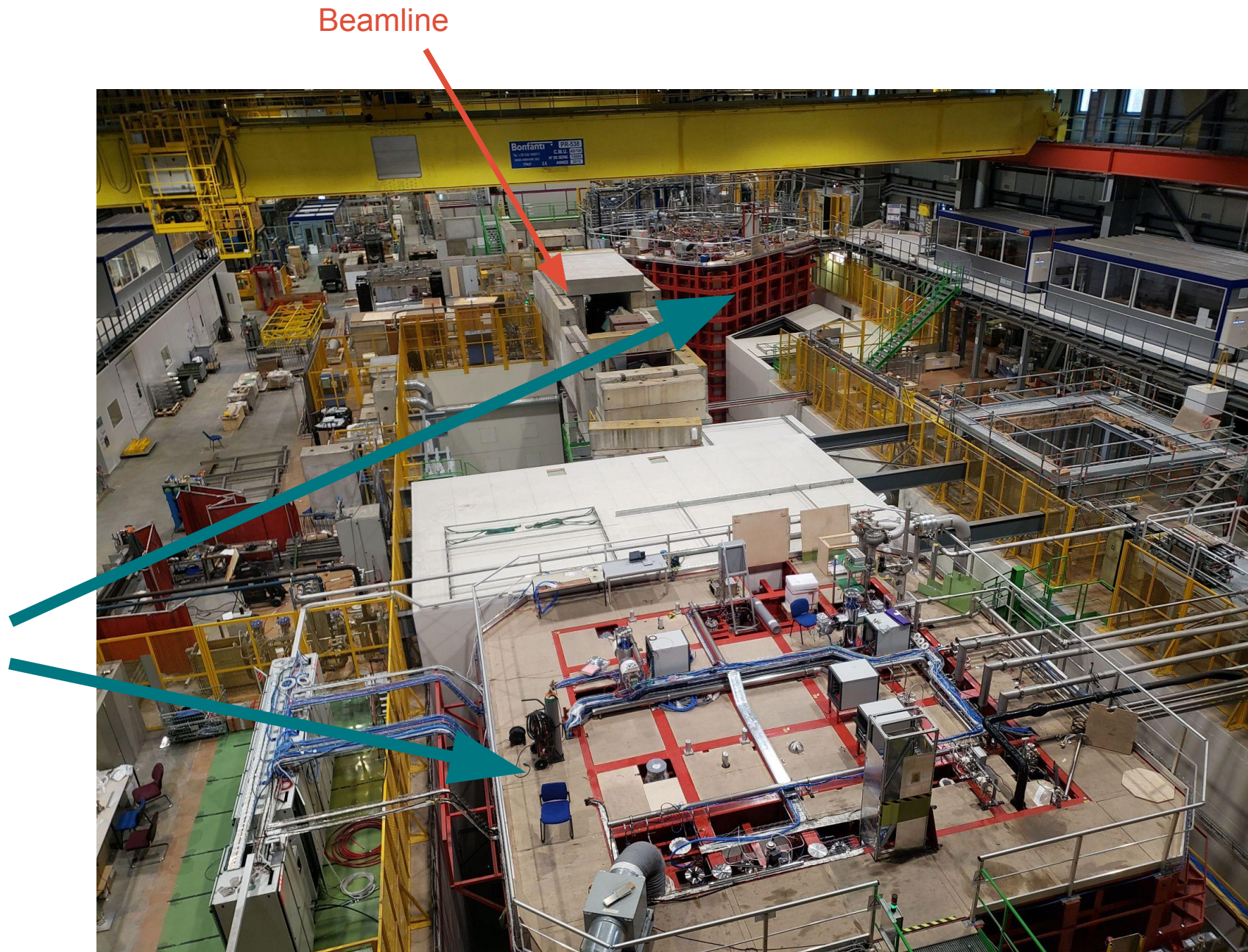


Cold TPC Readout Electronics for DUNE Far Detectors

- How do we read (14 m wide x 12 m tall x 58 m long) LArTPCs?
 - Instrumenting only the top of the LArTPC would call for 12+ meter long wires or drifts
 - But instrumentation at the bottom of the LArTPC could be more than 20 meters away from warm feedthroughs on the cryostat roof
 - How many feedthroughs do we need for this many channels?
- Solution: **charge amplification, digitization and readout electronics operating in liquid argon** (~87 K) to multiplex and bring out digital signals
 - Used for all FD1 readout, and readout of the bottom detectors in FD2
- Requirements:
 - Noise levels < 1000 electrons ENC, with the range to resolve 1000s of electrons from sub-MeV blips and up to ~500,000 electrons from O(GeV) showers
 - Low power consumption to not cause argon boiling (< **50 mW / channel**)
 - Electronics in the cryostat will never be replaced => need **~20-30 year lifetime**
 - Consistency in electronics quality in chips over hundreds of thousands of channels

The ProtoDUNE Program at CERN

- **ProtoDUNE** tested possible designs for the first two DUNE far detectors
 - Positioned to be able to collect test beam data
- **800 ton LArTPCs** at CERN's neutrino platform
- First iterations ran 2018-2020
- Second iterations running 2024 - present

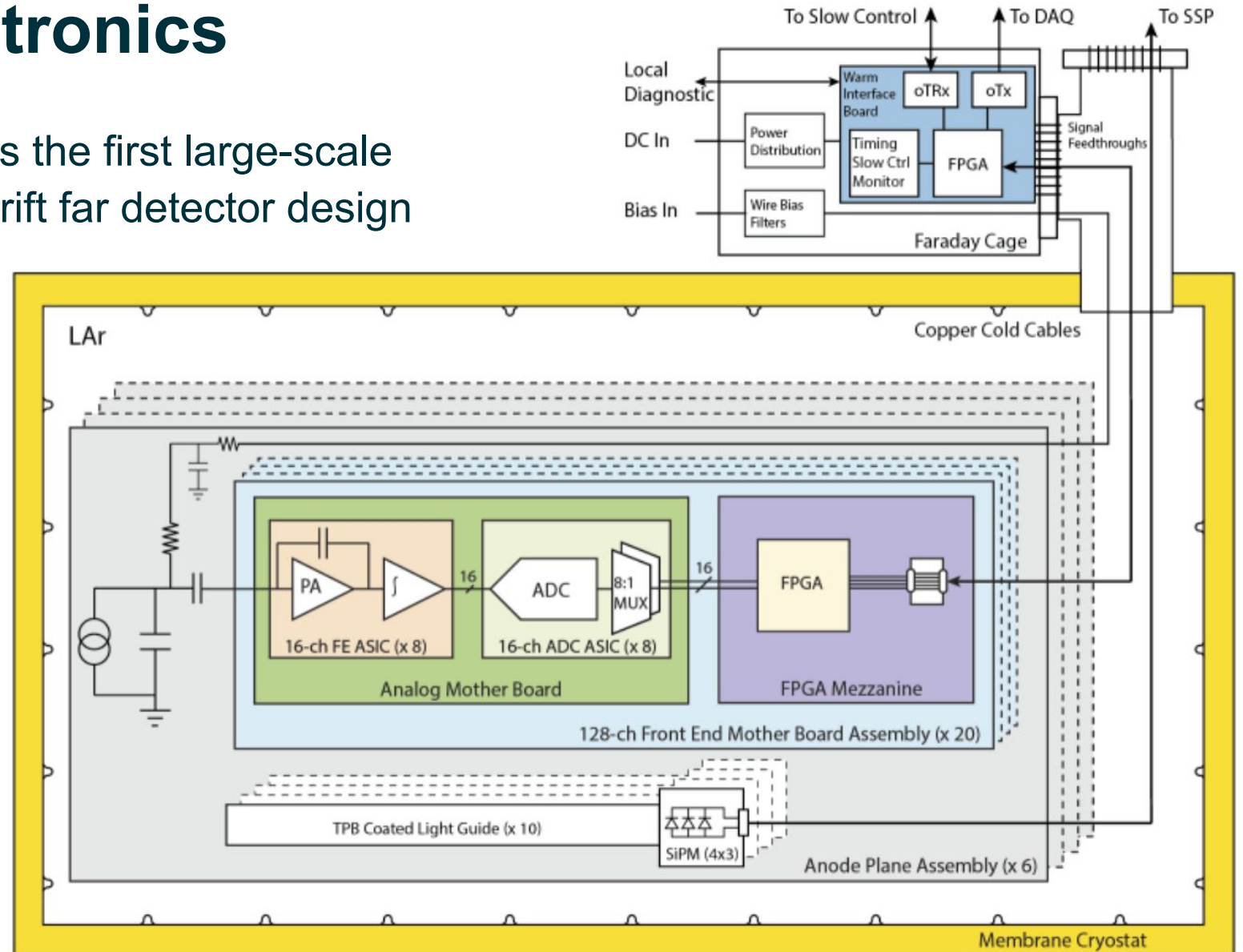


ProtoDUNE-SP Electronics

ProtoDUNE-SP (Single Phase) was the first large-scale prototype for the DUNE horizontal drift far detector design

Charge readout performed by 128-channel **front-end motherboards (FEMBs)** placed in close proximity to the sensing wires/strips*

- (Updated) LArASIC for charge amplification
- New custom ASIC for digitization
- Commercial Cyclone IV FPGA for digital communications and data transmission

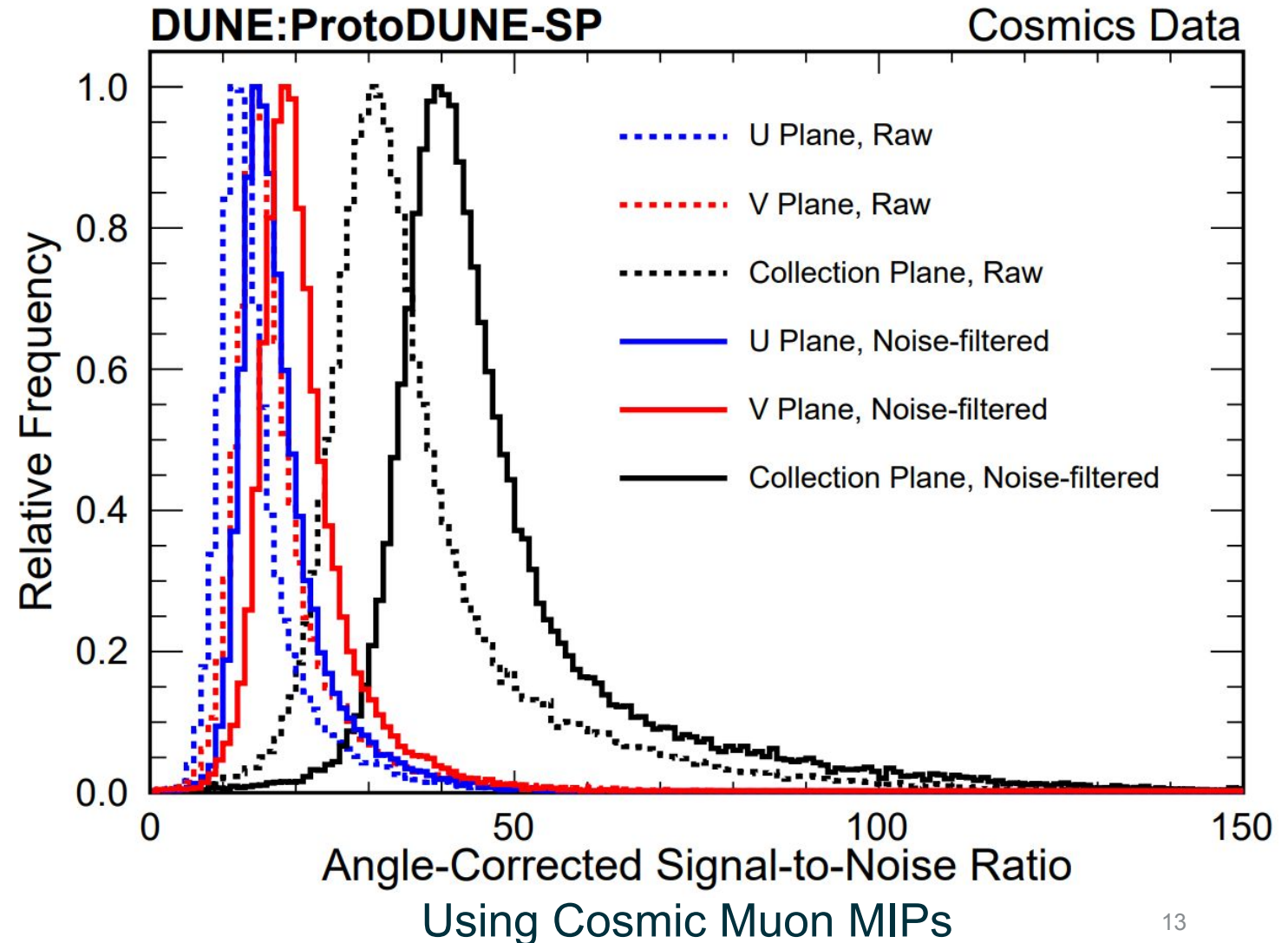
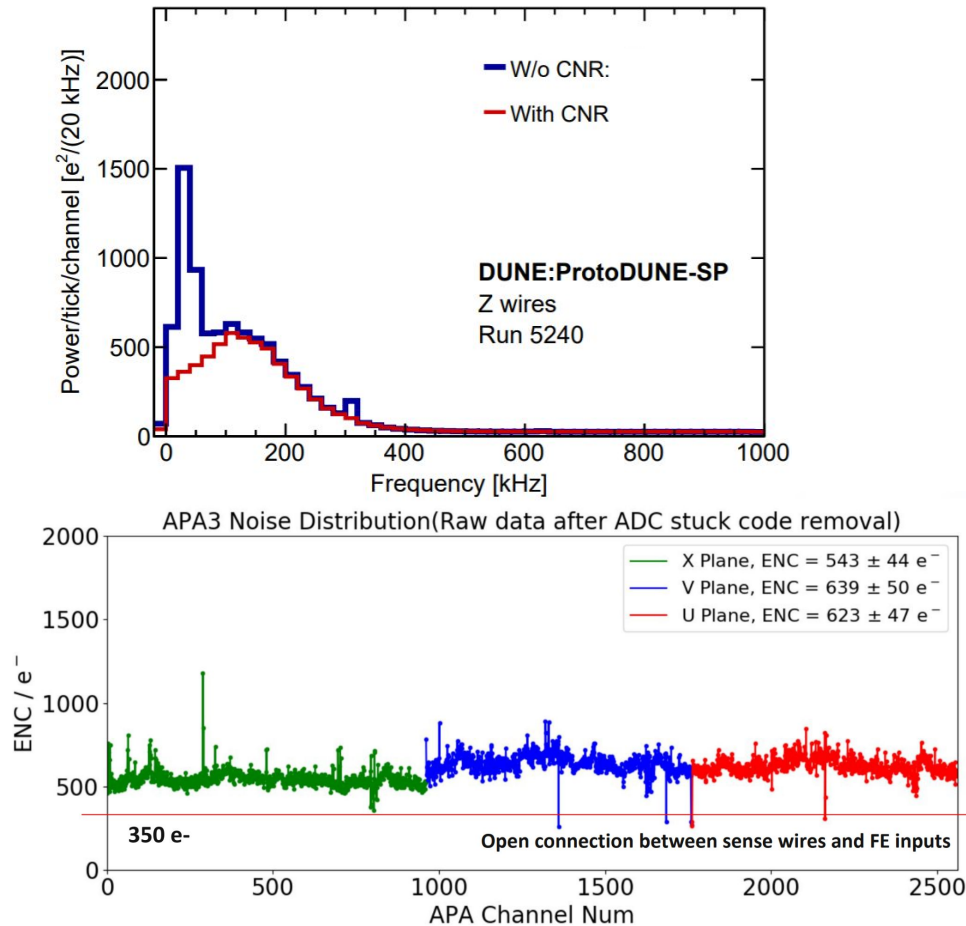


ProtoDUNE-SP Electronics Performance

Excellent noise performance

arXiv:2007.06722

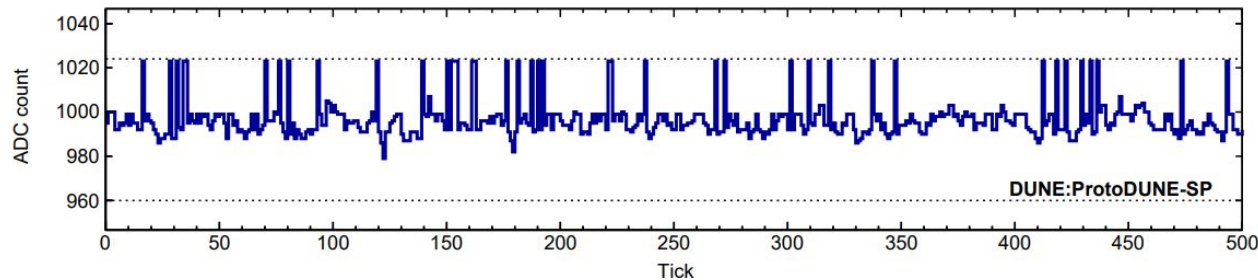
- Coherent Noise Removal (CNR) filter subtracts coherent noise from adjacent channels



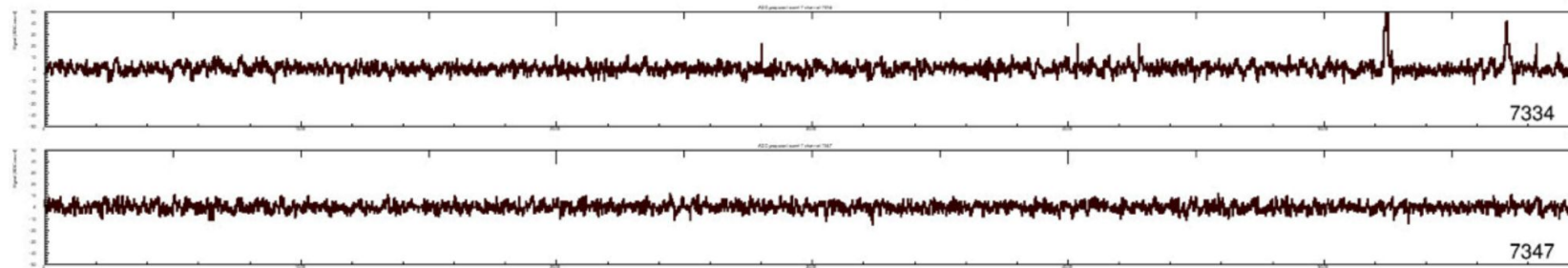
ProtoDUNE-SP ADC Issues

The ADC used a current-mode domino architecture that relied on precise transistor matching. Worked under warm conditions, but in cryogenic conditions had poor linearity, missing codes, sticky codes, and even non-monotonic response.

- Cryogenic CMOS modeling is hard!
- Use lenient designs to circumvent this



Channel with
stuck codes



Well-behaved
channels

Revising the DUNE Cold TPC Electronics

The LArASIC analog front-end satisfies all requirements, and can be used with just minor revisions

- One of the minor revisions fixed an issue with response to saturating signals

A new ADC design is needed

Commercial FPGA worked well for ProtoDUNE-SP, but for DUNE:

- Can the cryogenic lifetime be ascertained? CMOS lifetime in cryogenic conditions is understood as driven by the hot carrier effect
- Can it drive signals over even longer cables?

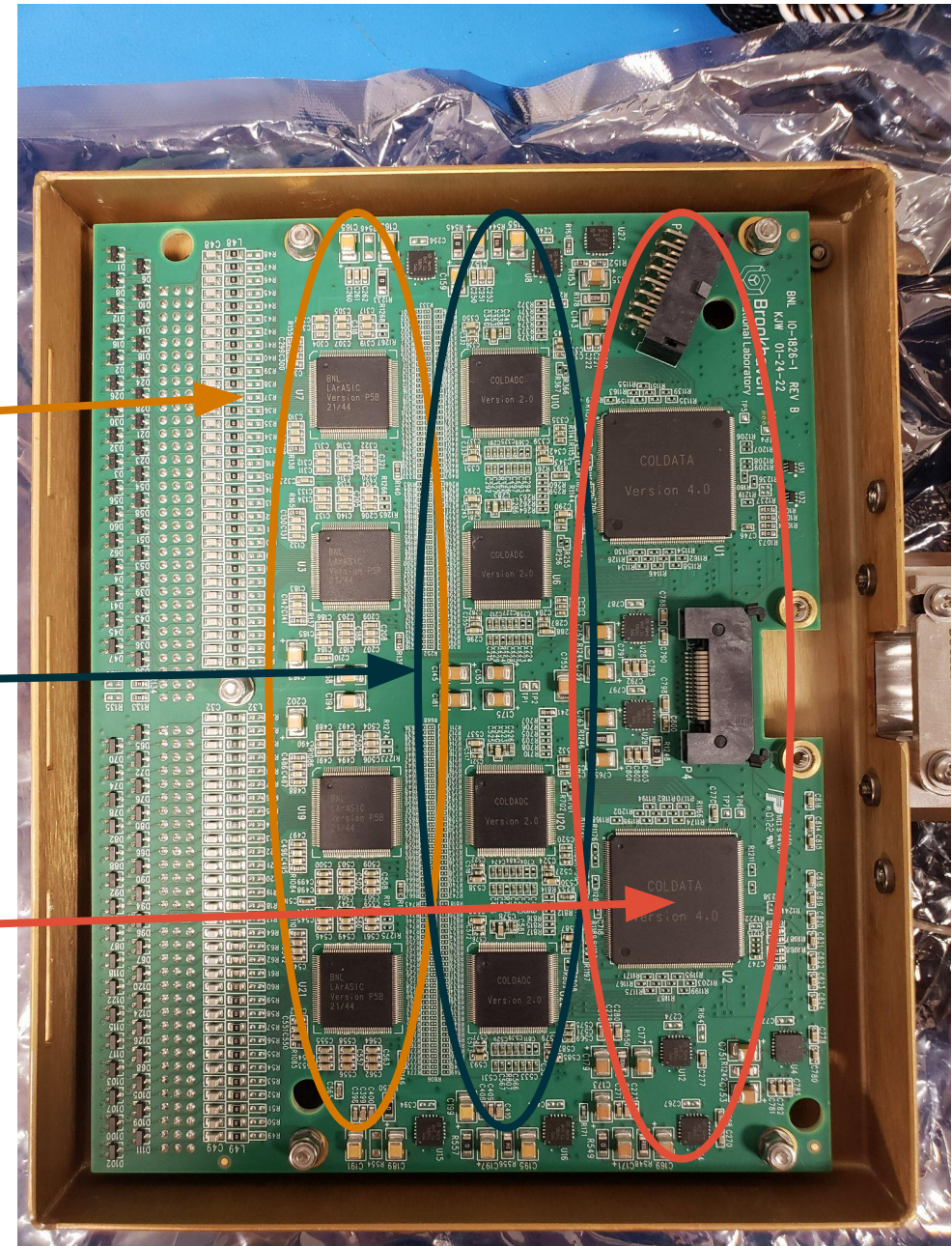
A new design can be tested in the **ProtoDUNE-II** program before far detector assembly begins

- **ProtoDUNE-II-HD** tests the horizontal drift design, which has mostly the same layout as ProtoDUNE-SP
- **ProtoDUNE-II-VD** tests the new vertical drift design

Front-end Motherboards

Each DUNE FEMB (128 channels) consists of:

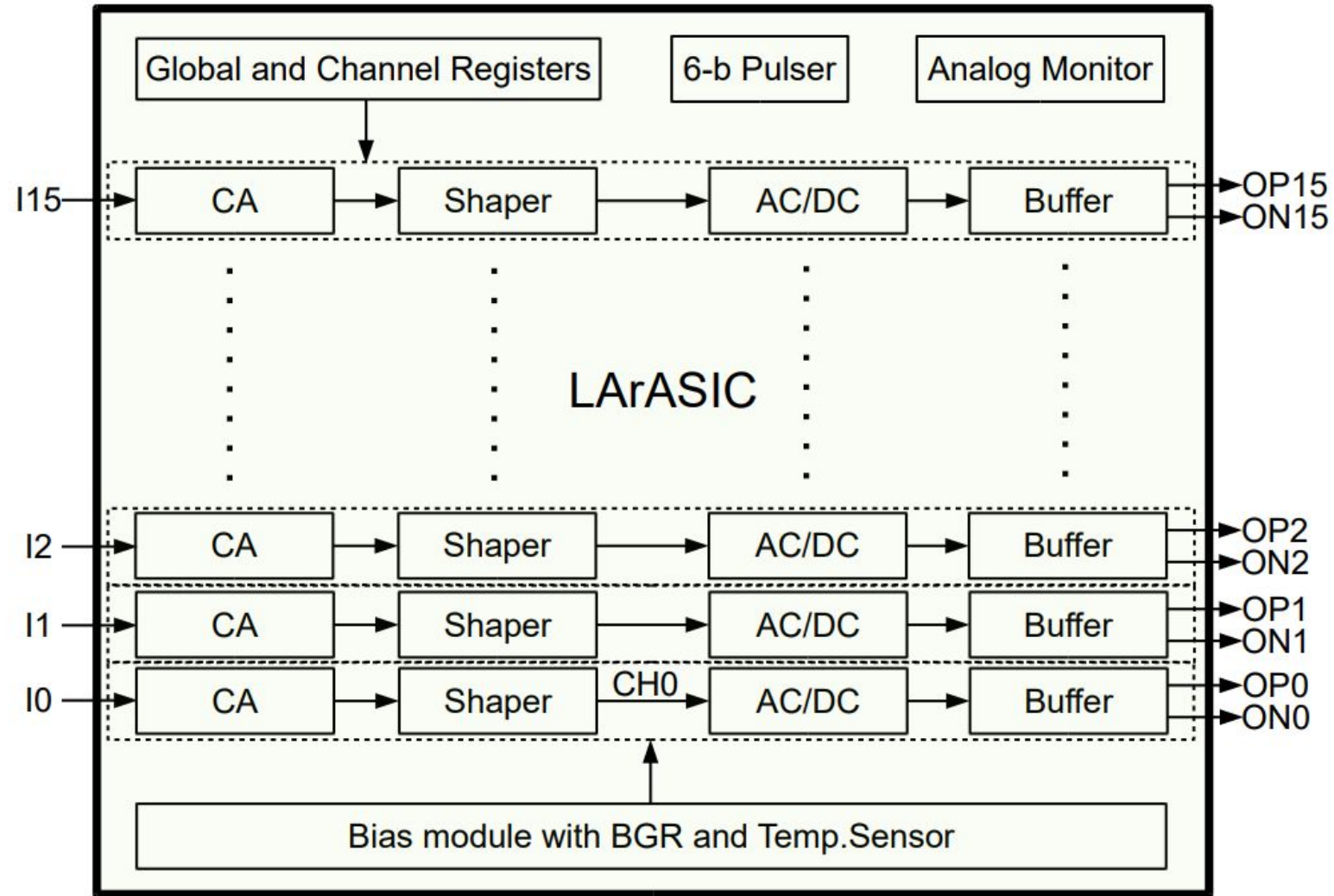
- **8 LArASIC** chips for analog charge amplification
 - Includes configurable shaper, different baseline and gain settings, and internal pulser for calibration
- **8 ColdADC** chips for digitization
 - Digitizing to 14-bit signals at ~ 2 MHz (< 1 mm spatial resolution in the TPC)
- **2 COLDATA** chips for control of and communication with LArASICs and ColdADCs
 - Receives commands from and sends serial data to the warm electronics
- Cryo-tested voltage regulators to supply power rails to each ASIC



LArASIC

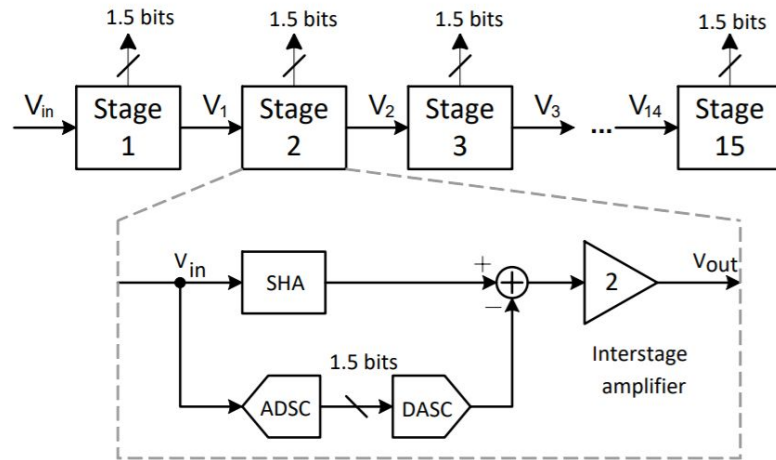
Overview

- Built in 180 nm CMOS process
- 16 channels / chip, each with SE or differential output
- Two-stage charge amplifier and 5th order shaper
- **Input charge range of 56-300 fC** (350k - 1875k electrons), depending on gain selection (320x to 60x)
- Channels configured through SPI interface
- Bias voltages generated internally with BJT bandgap reference

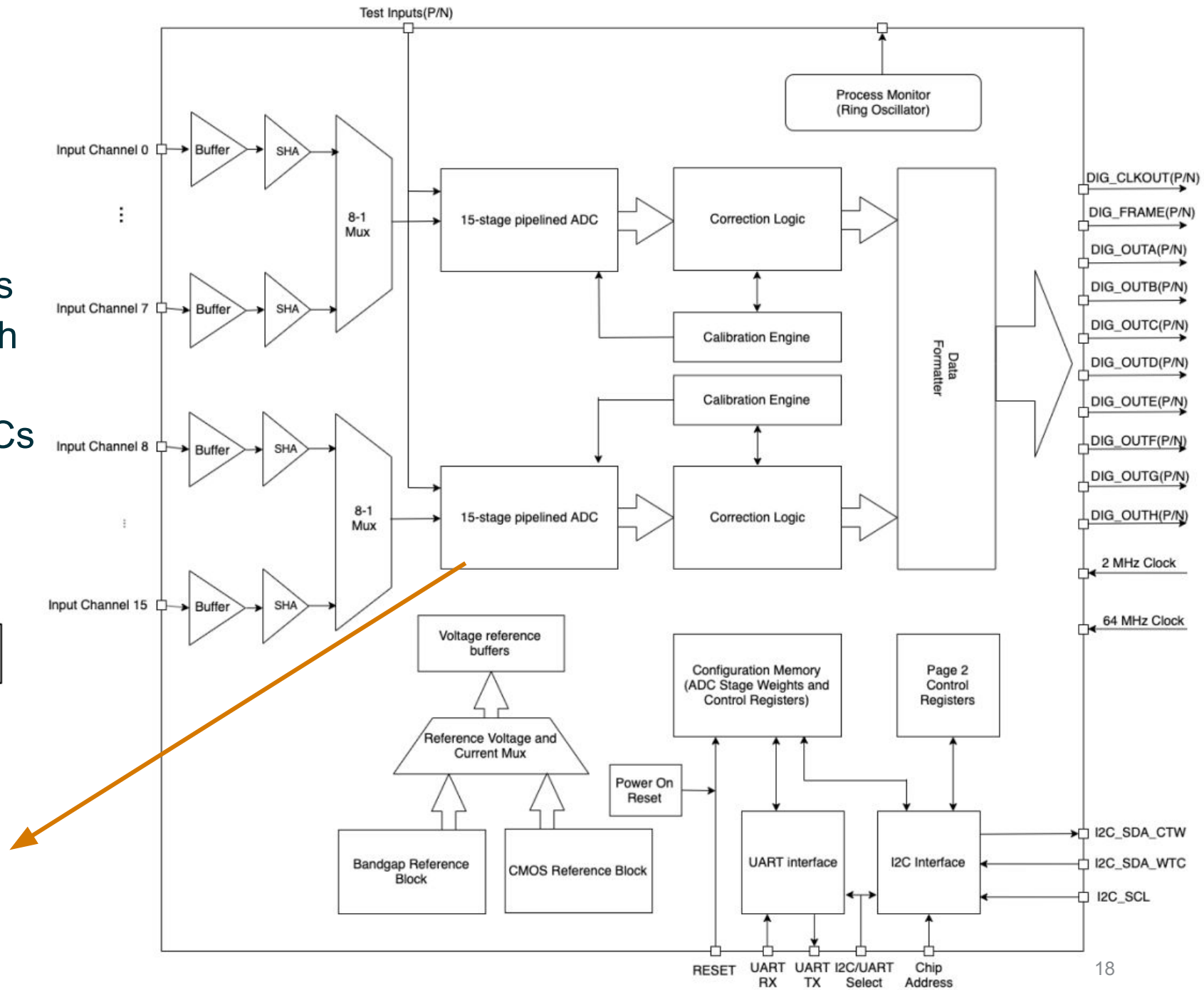


ColdADC Overview

- Built in 65 nm CMOS process
- 16 input/output channels, with 2 groups of 8 SHAs with 8:1 mux of input channels to ADCs
- 15-stage pipelined ADC with self-calibration engine



ADC block diagram



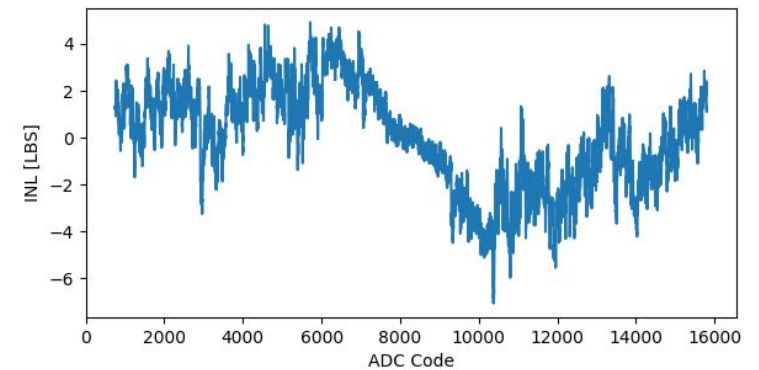
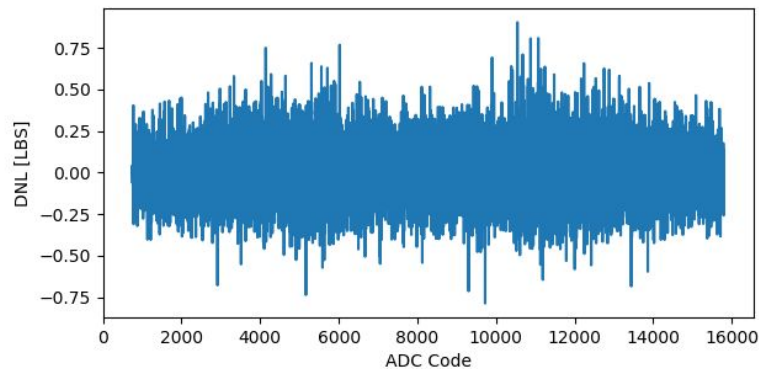
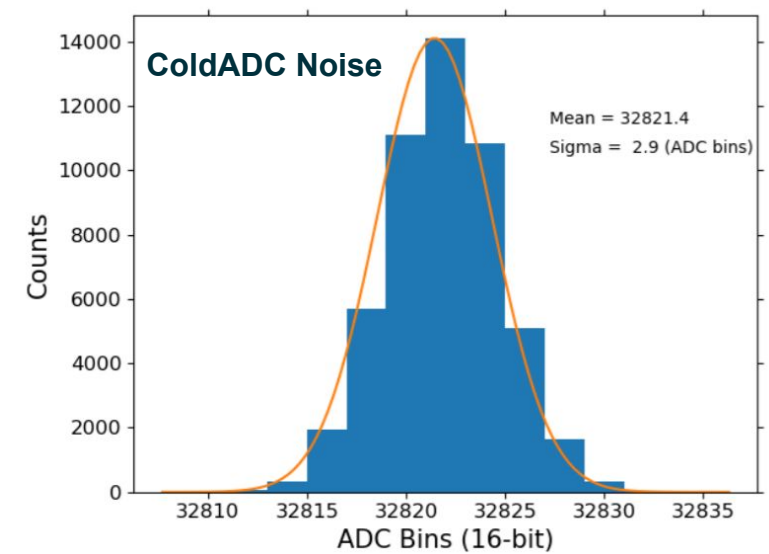
ColdADC Performance

Satisfies requirements: negligible noise, negligible cross-talk, good linearity

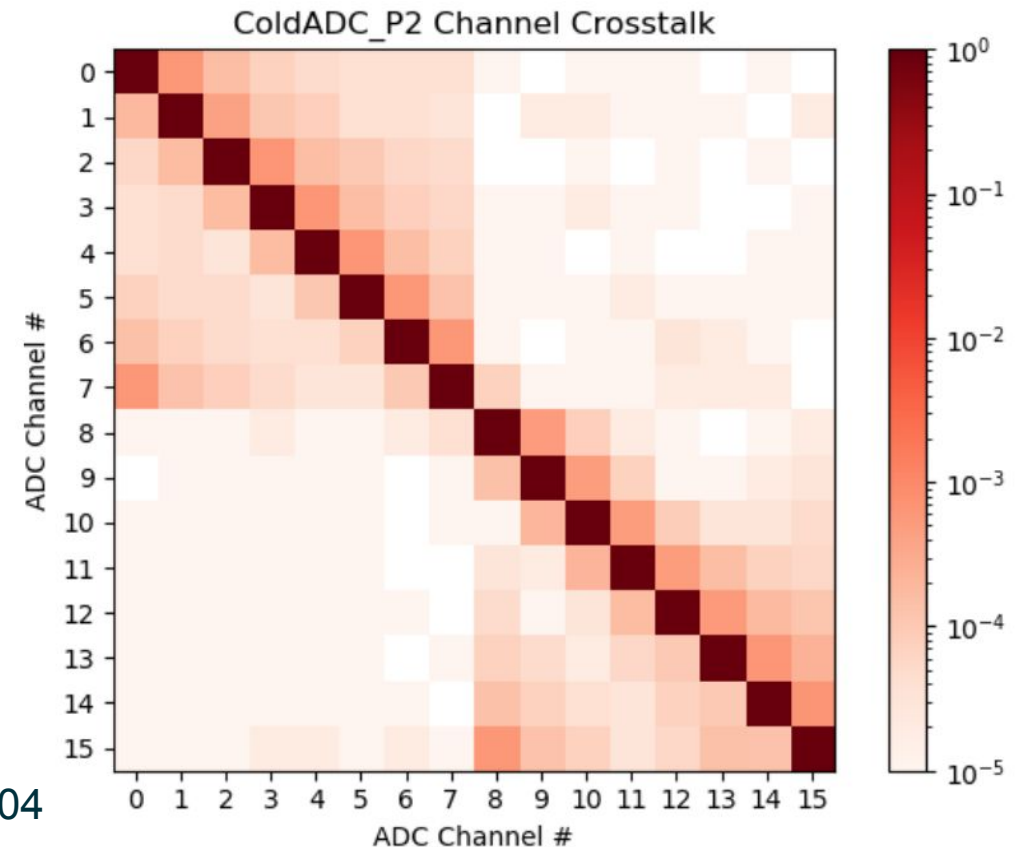
Now dominates power dissipation on FEMB:

~20 mW / channel in liquid argon

- 4x increase from previous version, but within limits

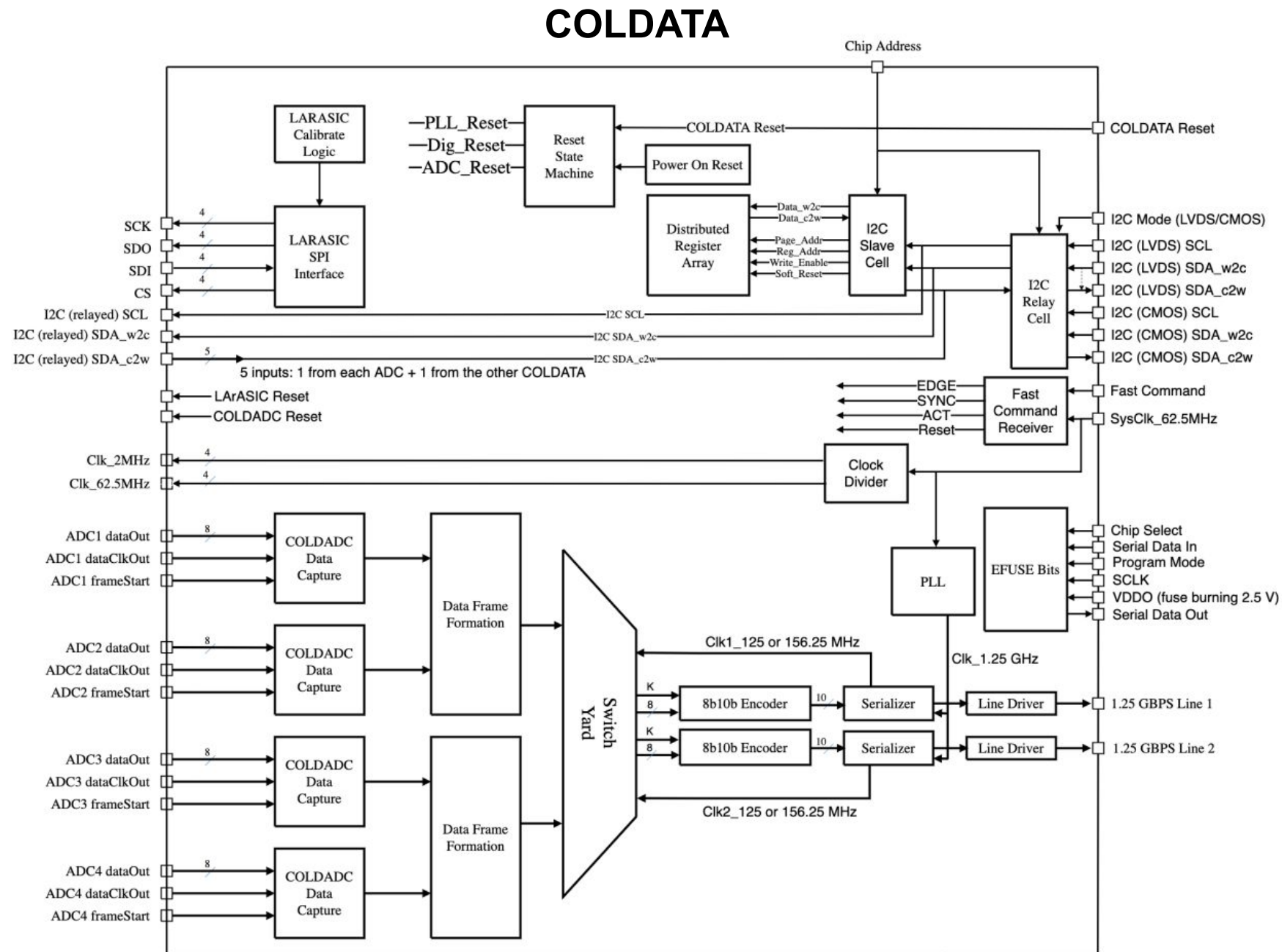


14 bit DNL (top) & INL (bottom)



COLDATA Overview

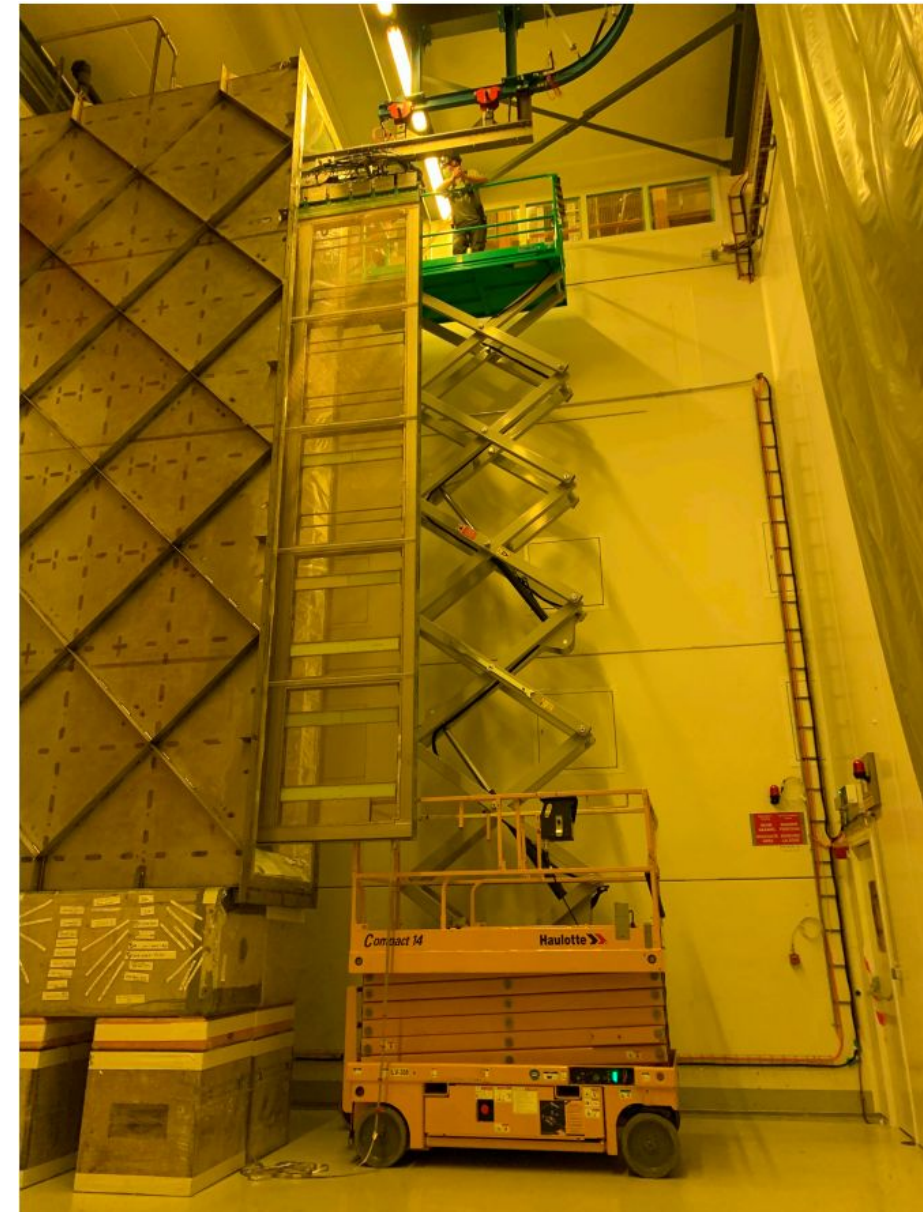
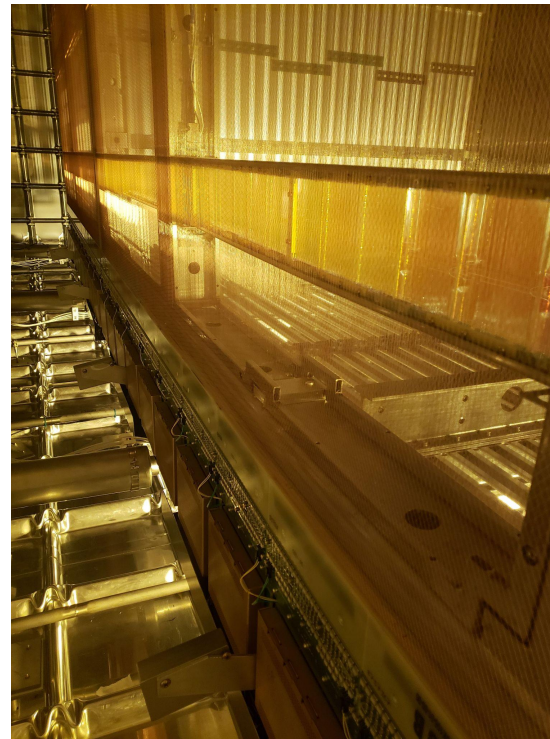
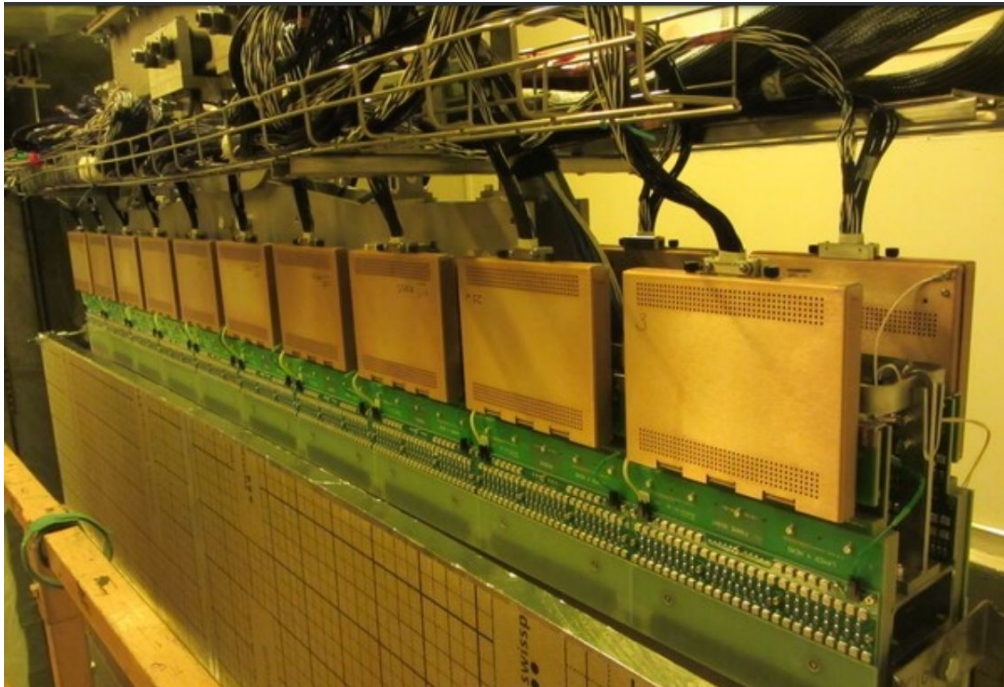
- Built in 65 nm CMOS process
- Controls and configures 4 ColdADCs and 4 LArASICs
- PLL generates 1.25 GHz clock for data serializers, multiplexing **32 channel signals onto one line**
- Configurable line driver for sending 8b10b encoded data to warm electronics



ProtoDUNE-II-HD

Each detector module tested with all readout electronics in a **nitrogen gas coldbox** (down to ~ 160 K)

Full system (4 modules) filled with LAr in 2024 and took test beam data

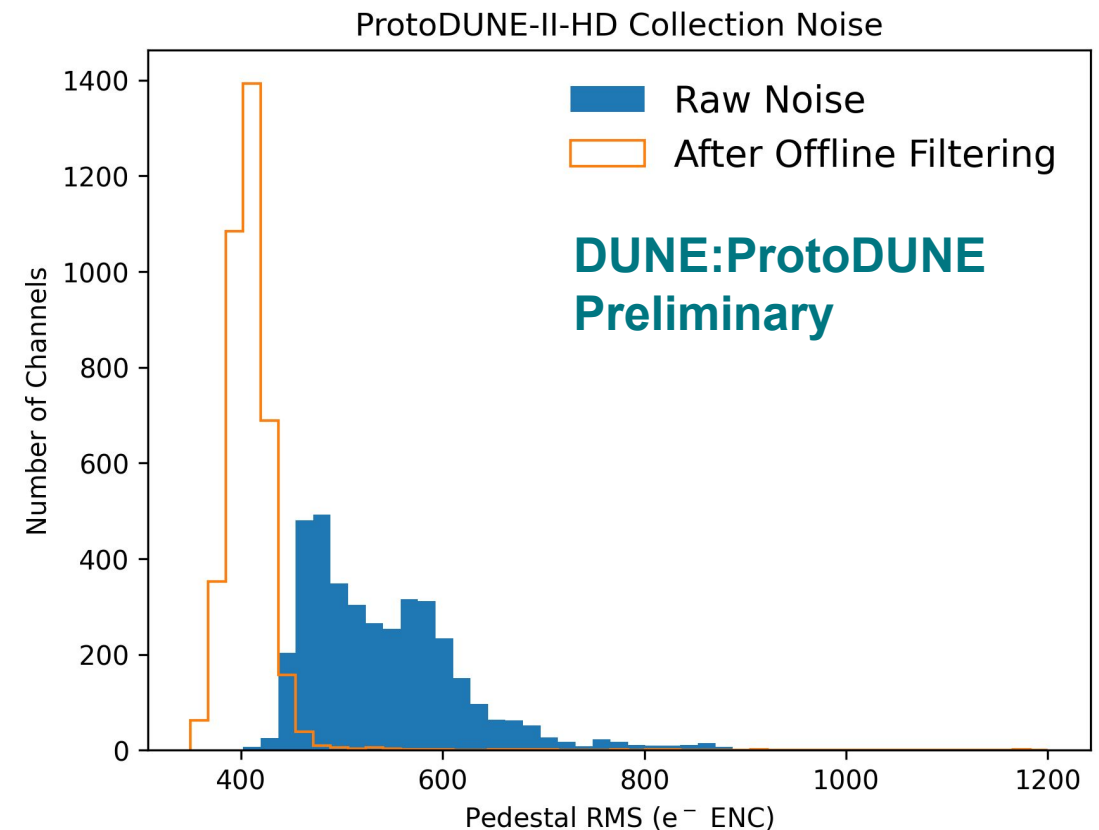
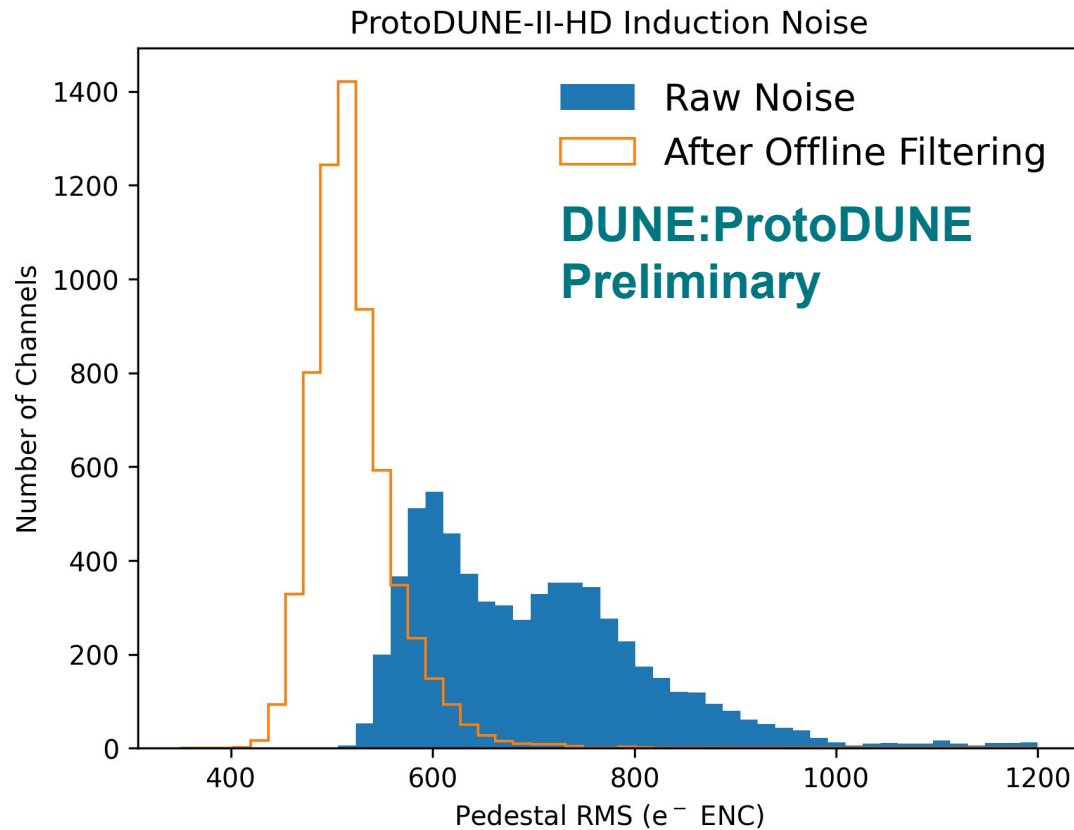
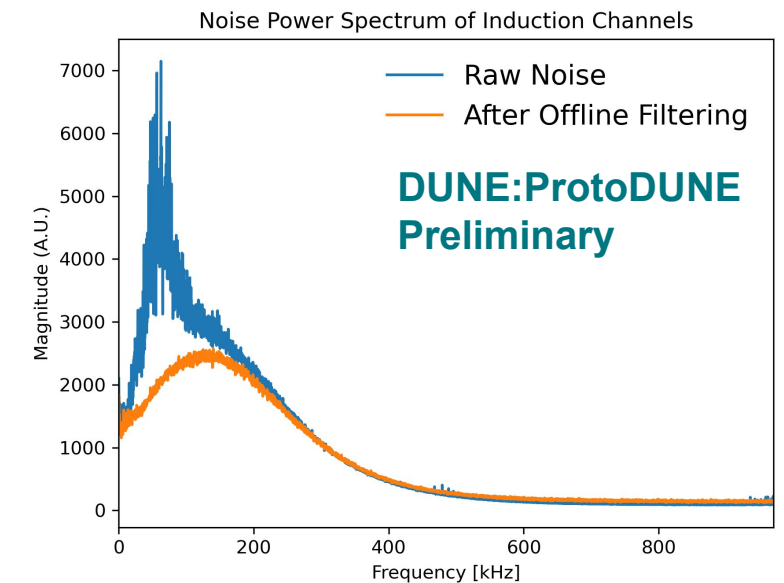


ProtoDUNE-II-HD Performance

Excellent noise levels - comparable to ProtoDUNE-SP

Some coherent noise present around lower frequencies

- Noise filter reduces this by subtracting coherent signals from adjacent channels



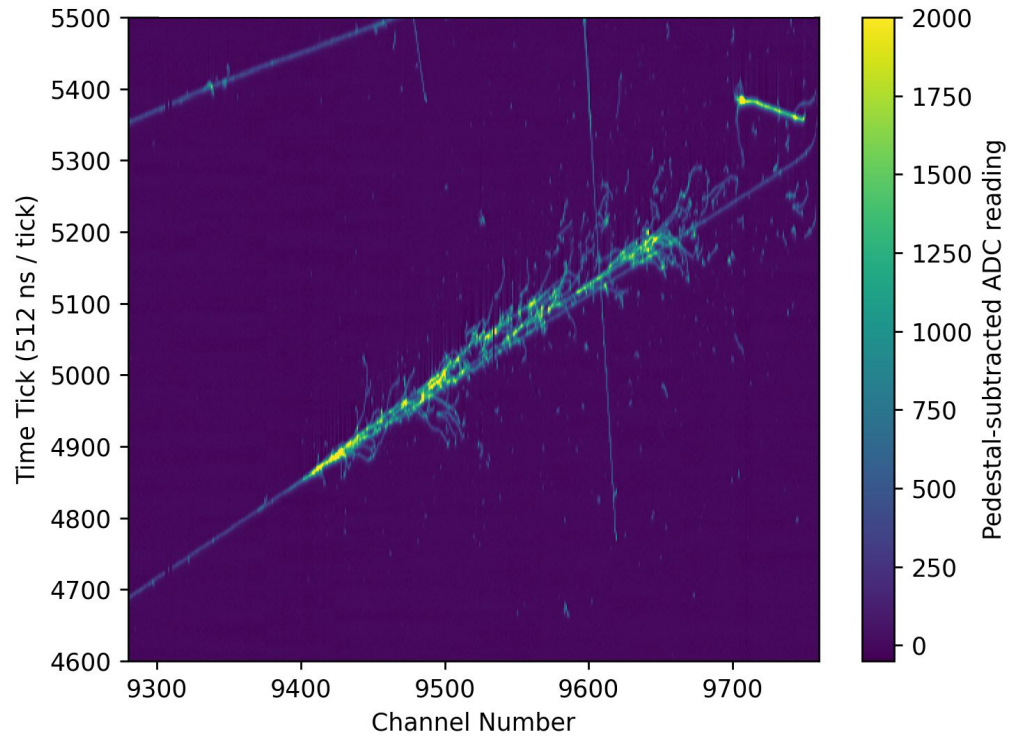
ProtoDUNE-II-HD Data

Took 8 weeks of hadron beam data last summer, and completed operations at end of 2024

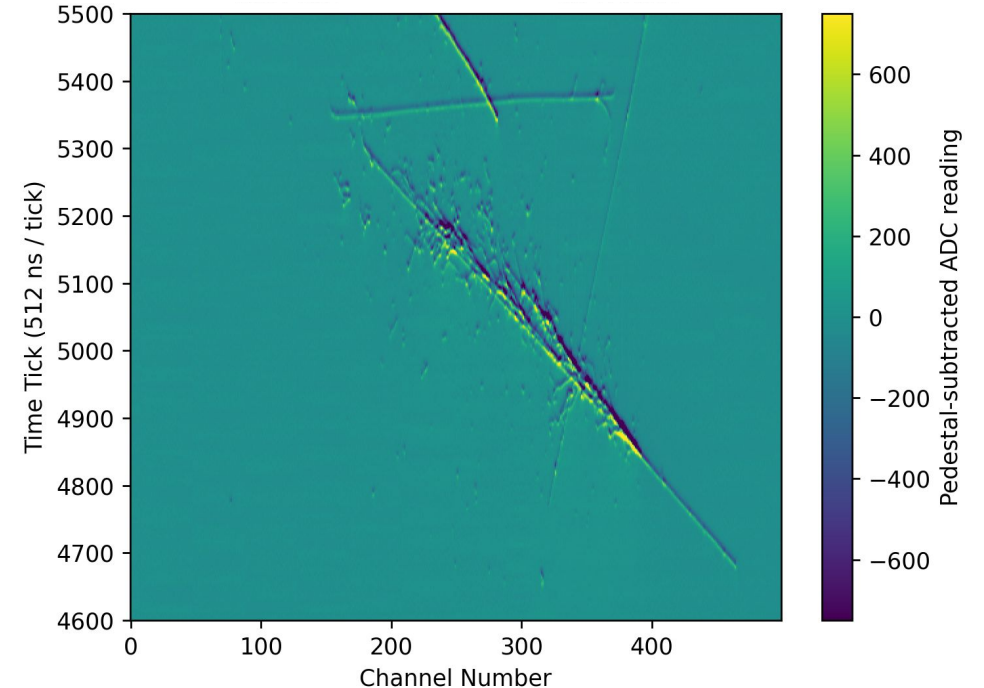
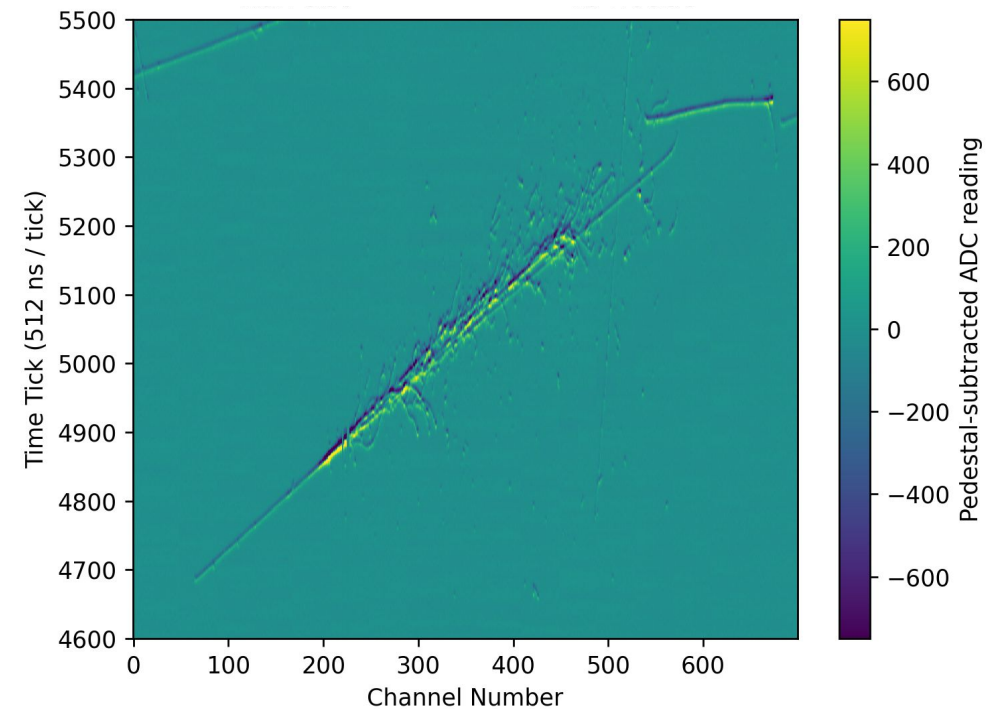
Detector performance paper later this year

Physics analyses in the pipeline

Collection View



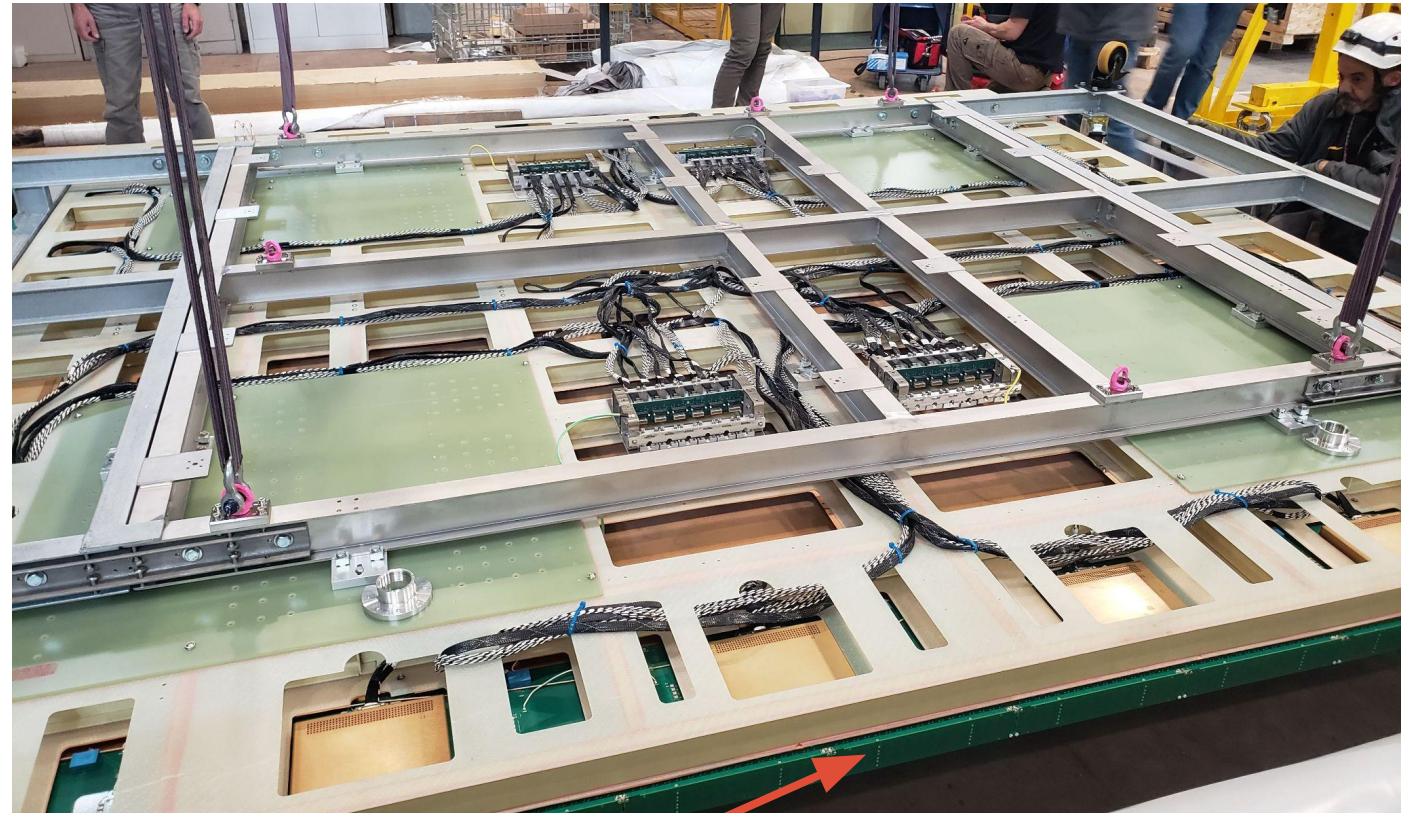
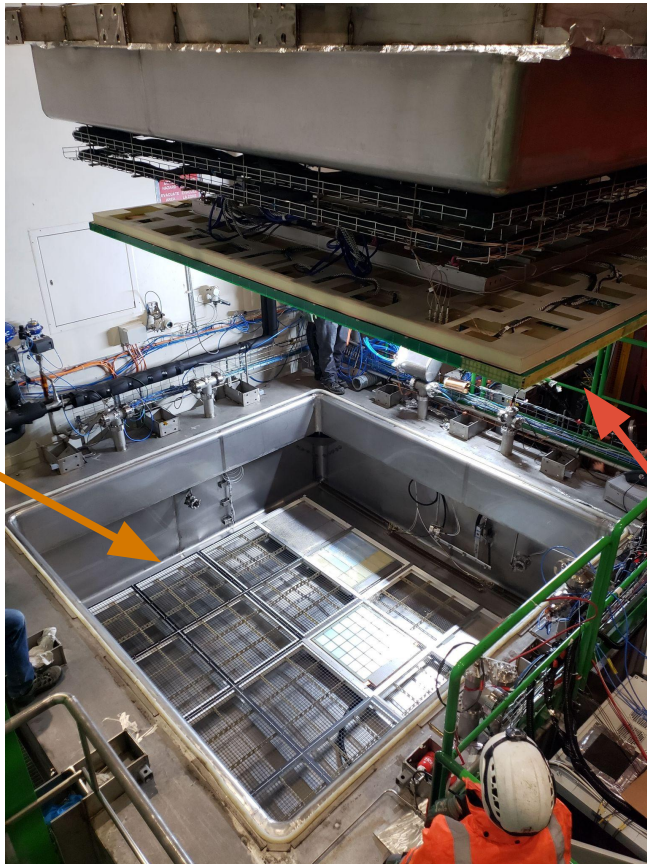
Induction Views



ProtoDUNE-II-VD

System contains 4 CRPs (3m x 3.4m each), with 2 for top-half readout and 2 for bottom-half readout

Vertical-drift detectors tested in a liquid argon coldbox, which is a fully functional mini-TPC with ~30 cm drift



Charge readout plane (CRP)

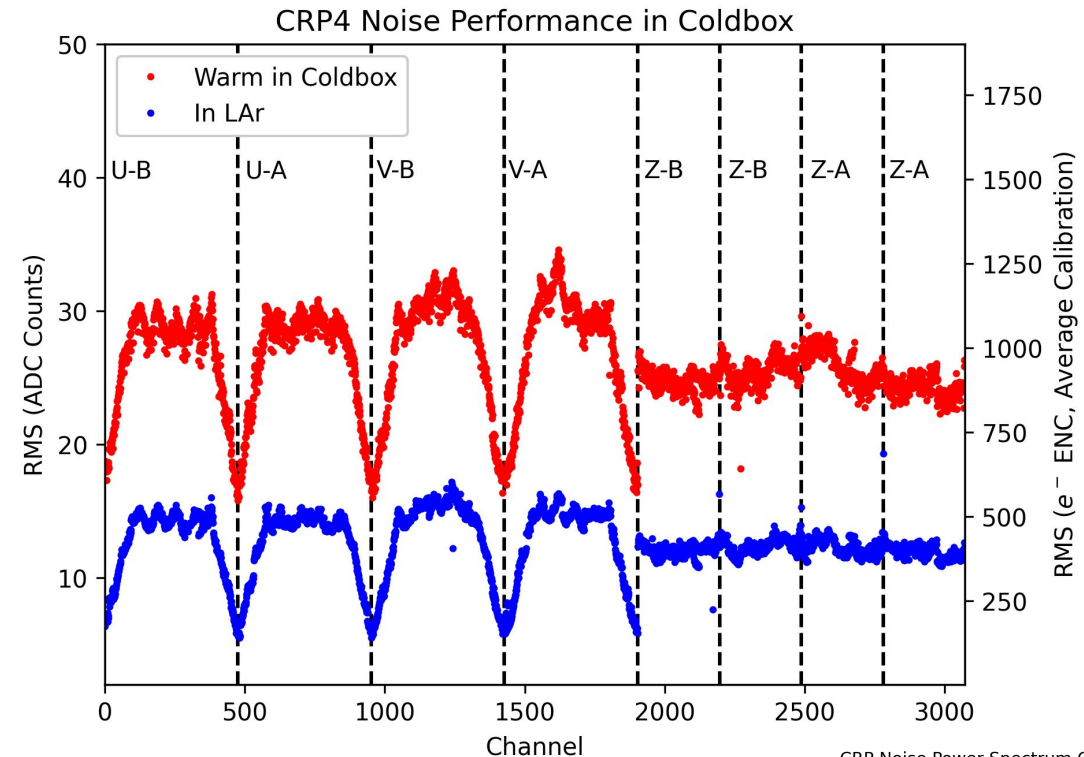
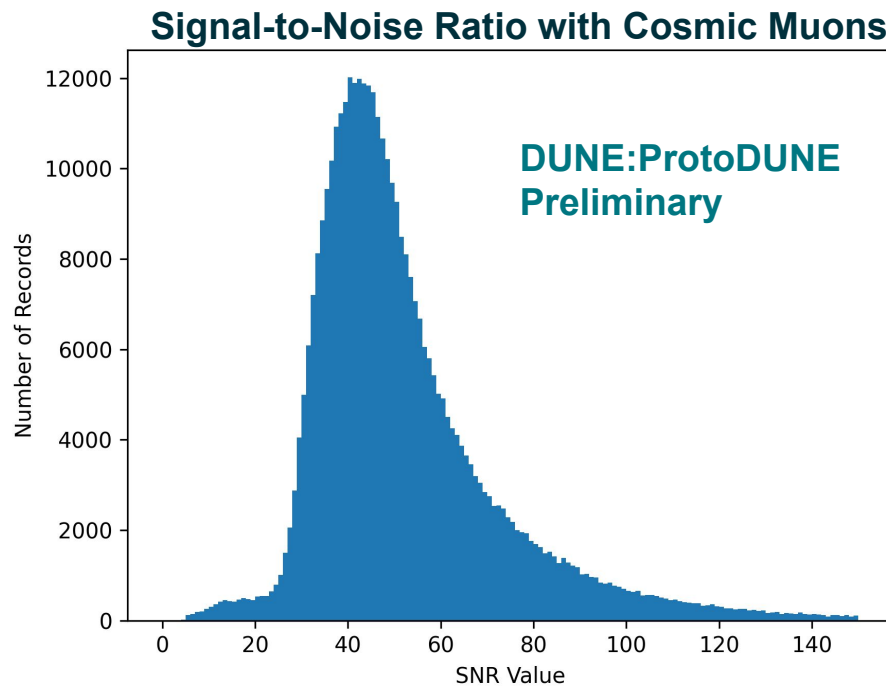
Identical FEMB/ASIC design as the APAs, other than mechanical components

Total of **~29 meters of cable** between each FEMB and the warm readout electronics

TPC Electronics Performance for ProtoDUNE-II-VD

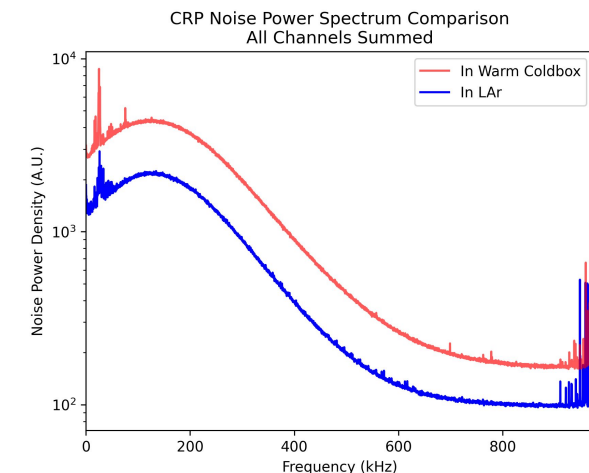
LAr coldbox tests of individual CRPs show excellent noise performance

- Minor contributions from coherent noise pickup around ~25 kHz



Simple SNR estimate of the collection channels using throughgoing muons as MIPs gives a MPV of ~45

- No noise-filtering or lifetime and geometry corrections



Inside one of the ProtoDUNE-II-VD drift volumes

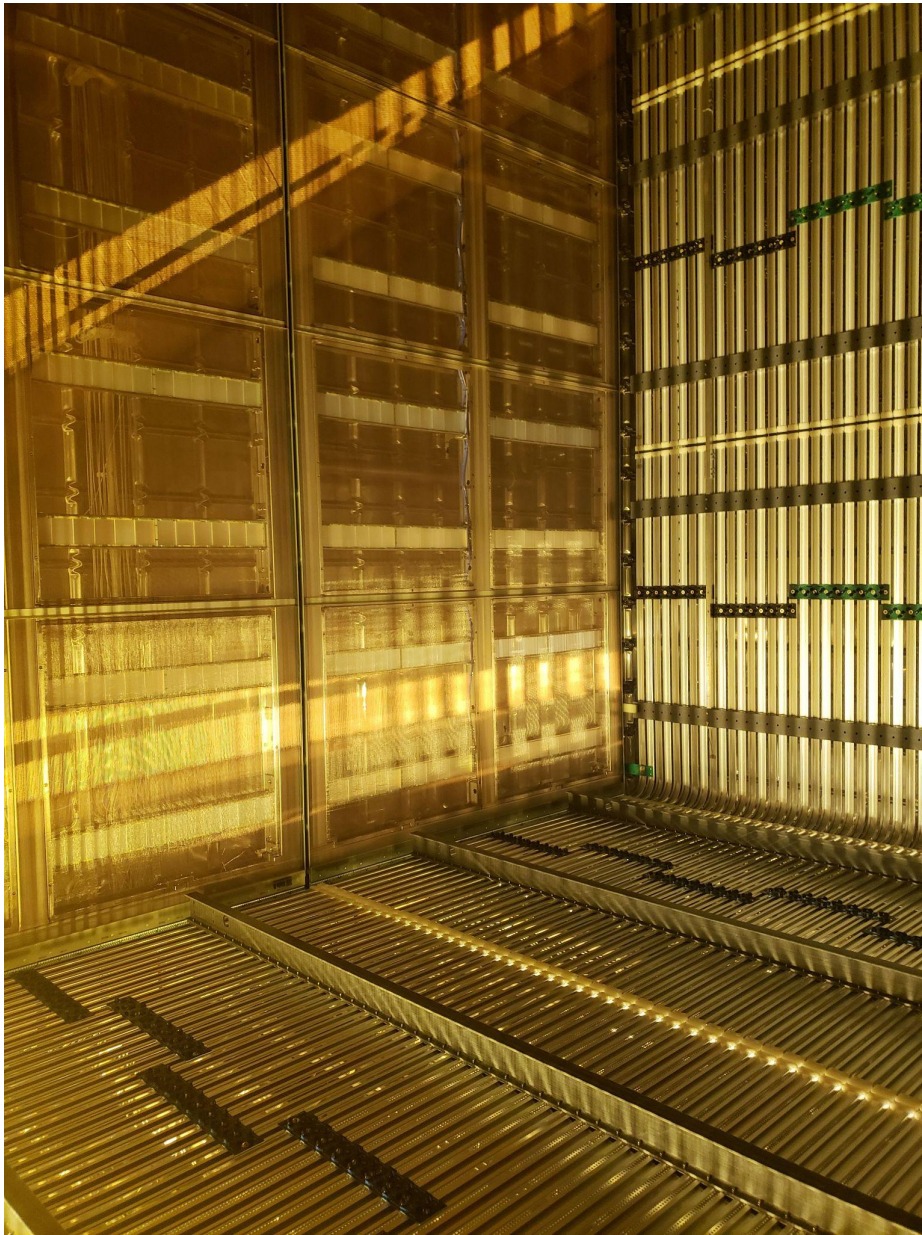


ProtoDUNE-II Status

ProtoDUNE-II-HD has completed operations, with detailed analysis of the data now in progress

ProtoDUNE-II-VD was filled with LAr at the beginning of 2025, and will take beam data this summer

The 3-ASIC charge readout cold electronics design has shown no issues for either one and foresees no more major revisions for the DUNE far detector assembly



Inside one of the ProtoDUNE-II-HD drift volumes

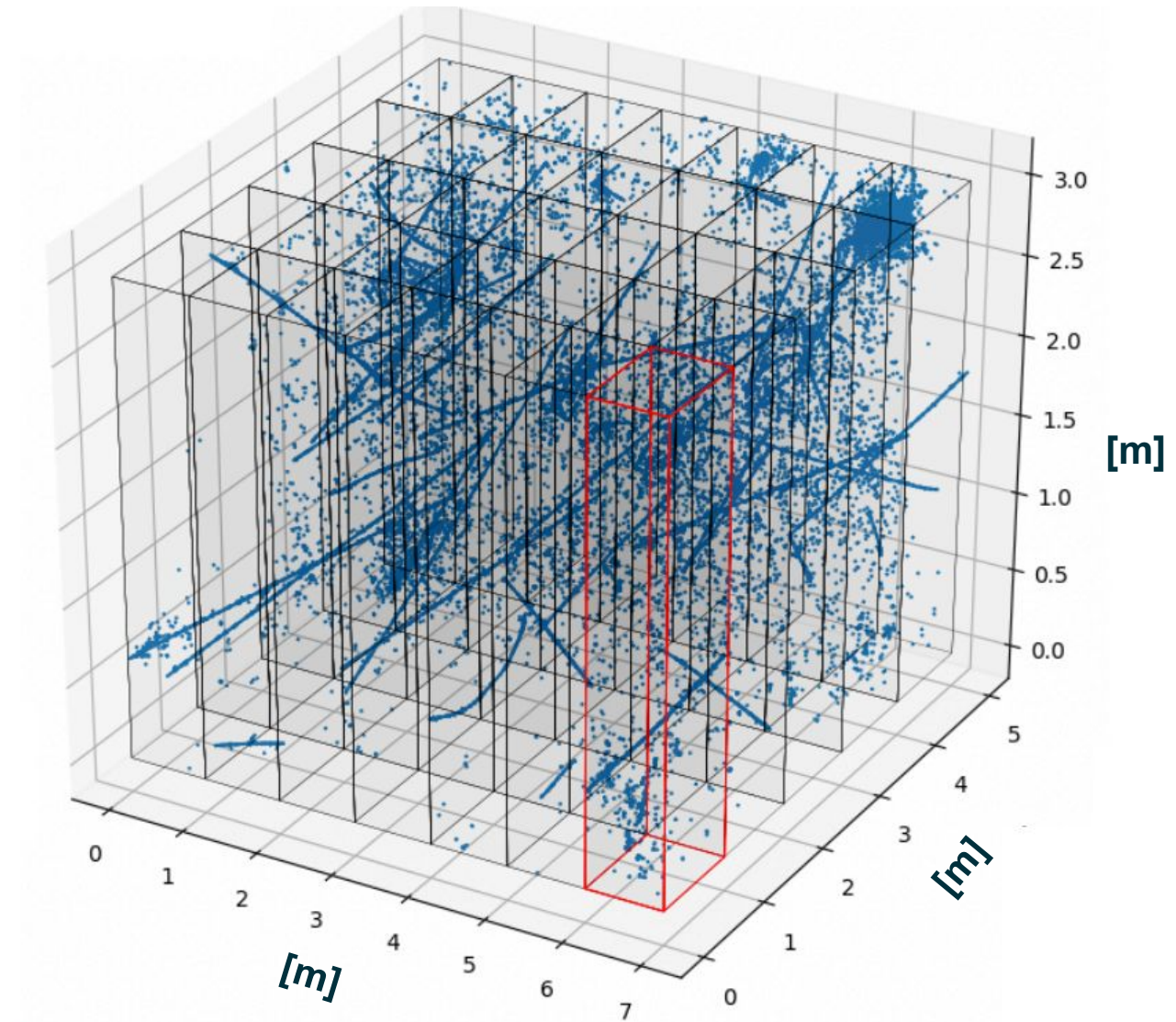
The DUNE Near Detector

DUNE needs a LArTPC near detector to constrain various systematic uncertainties for the oscillation analysis

The near detector size is “only” several meters per dimension, but faces a new problem: **neutrino pileup!**

- ~50 neutrino interactions in a 10 us beam spill

The ambiguities of wire-based readout are no problem in a sparse environment, but become unmanageable in high-rate scenarios like this



Pixelized Readout with the LArPix ASIC

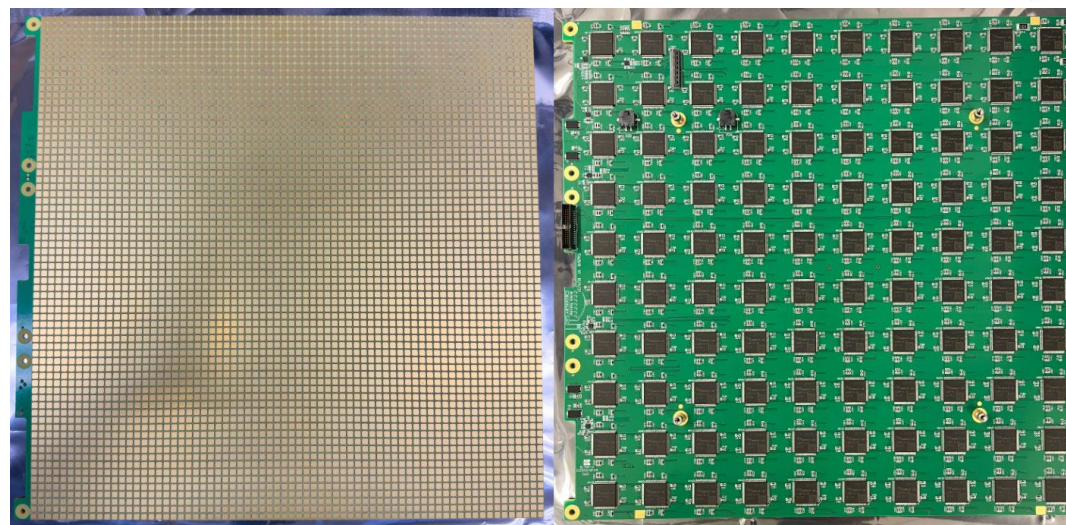
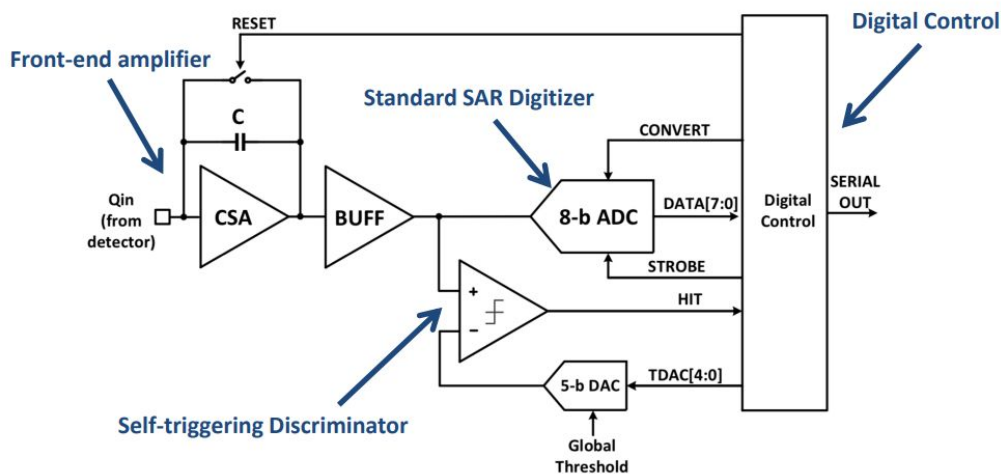
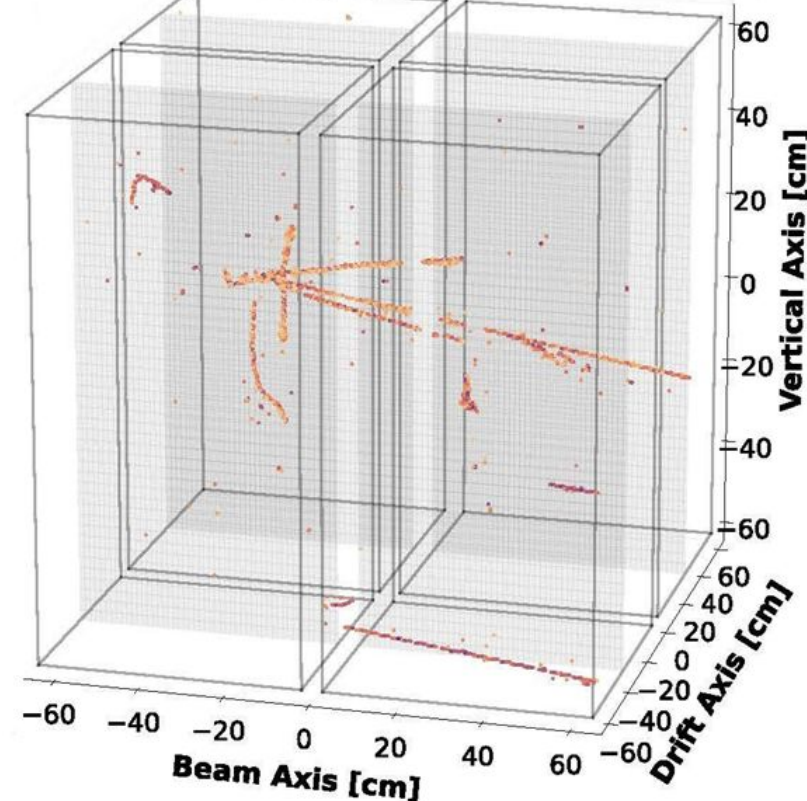
Pixelized charge readout provides true 3D reconstruction

The **LArPix ASIC** enables this with its self-triggered design: each pixel only digitizes and sends its signal once above threshold

- Lowers power consumption
- Zero-suppresses data rate at hardware level
- Combines the far detector 3-ASIC functionality into 1 chip

The LArPix approach saw neutrino beam data in 2024 with the 2x2 demonstrator at Fermilab!

2x2 Detector Neutrino Event



LArPix tile with pixel pads and ASICs

Summary

Instead of asking whether we need cold electronics, we can ask **what do cold electronics allow us to do?**

Cold electronics are **an enabling technology** for the DUNE detectors

- Frees the anode/cryostat design from constraints on where to place the readout
- Multiplexing brings the needed number of cables to a manageable level
- Plus general benefits from improved electronics properties at cold
 - Lower noise expands physics reach into lower energy regions

There are accompanying costs, but they can be managed:

- No standard cryogenic CMOS models exist, so cryo-ASIC design often needs many iterations
- Operate at low voltages to minimize power consumption and maximize lifetime
 - ~6% lower V_{ds} => 10x higher lifetime
- Long-term stability is crucial
- Accompanying passive components need to be cryo-certified too