Serenity-S1
Versatile ATCA Processing Card

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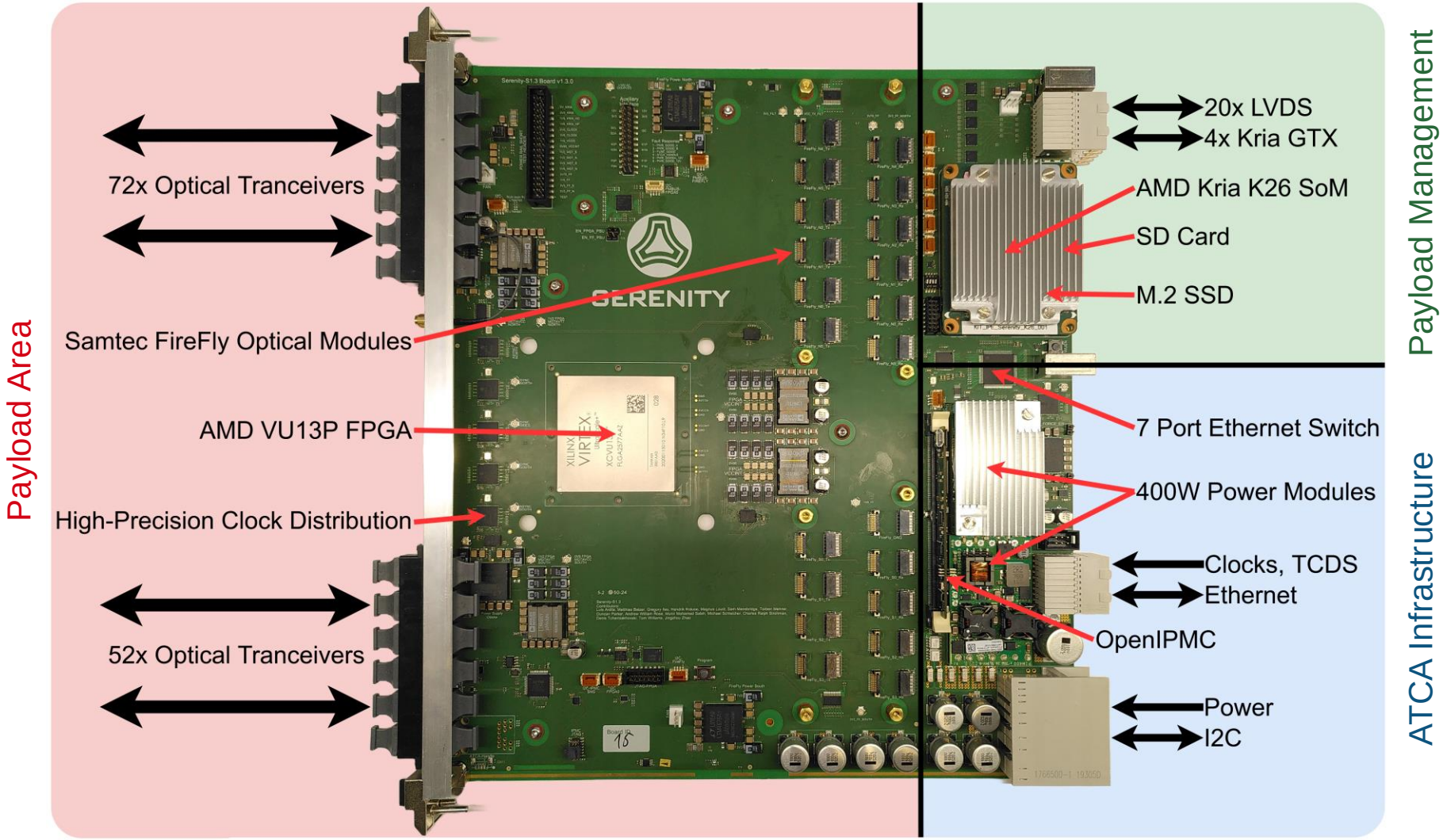
SEI-Tagung 2025

Content

1. Serenity-S1
2. Software and Firmware
3. Test Results
4. Use Cases

Serenity-S1

Section
01



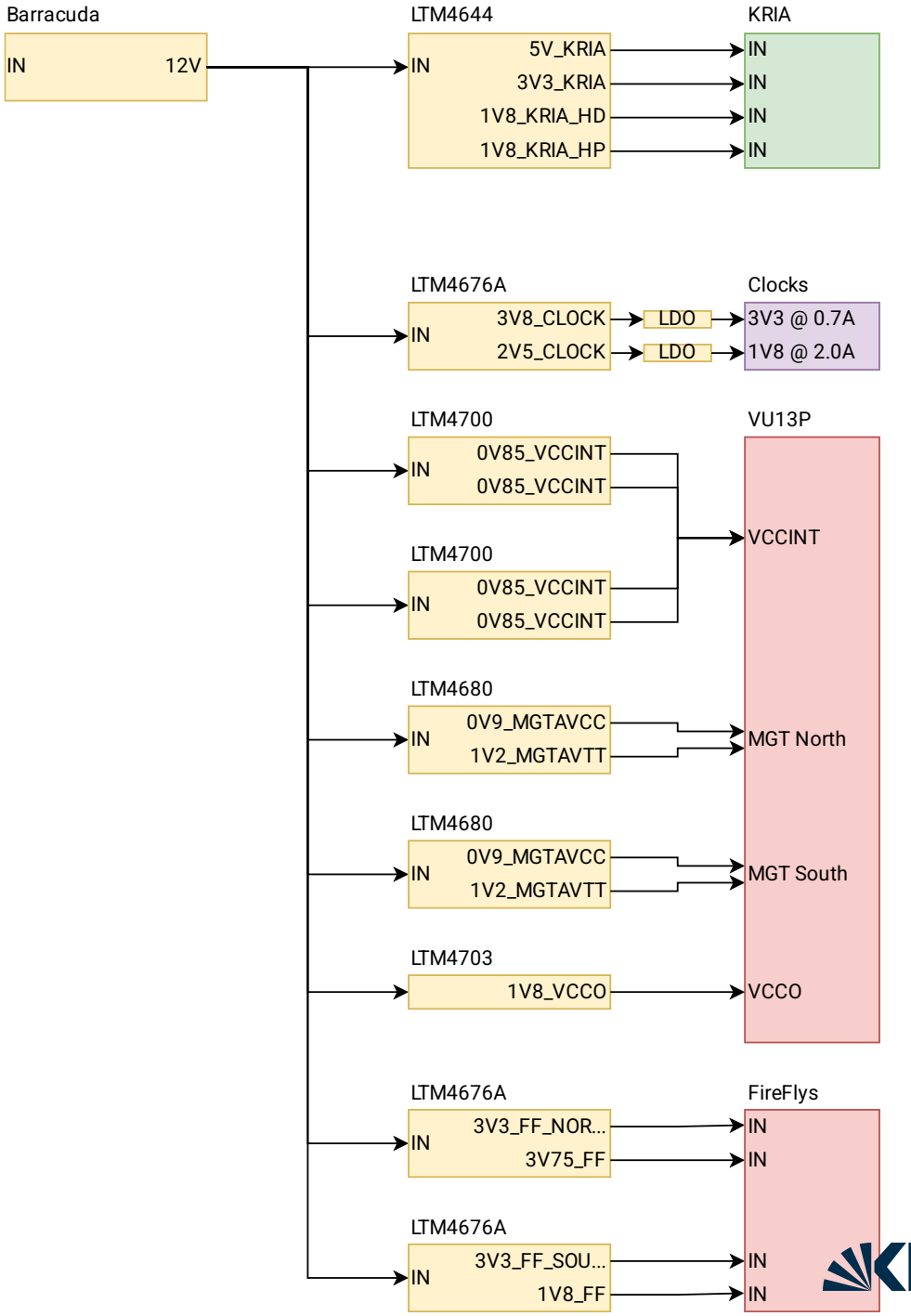
Architecture

The Serenity-S1 is a versatile data processing card with

- 3.1 Tbps digital bandwidth using FireFly optical modules
- A large VU13P processing FPGA

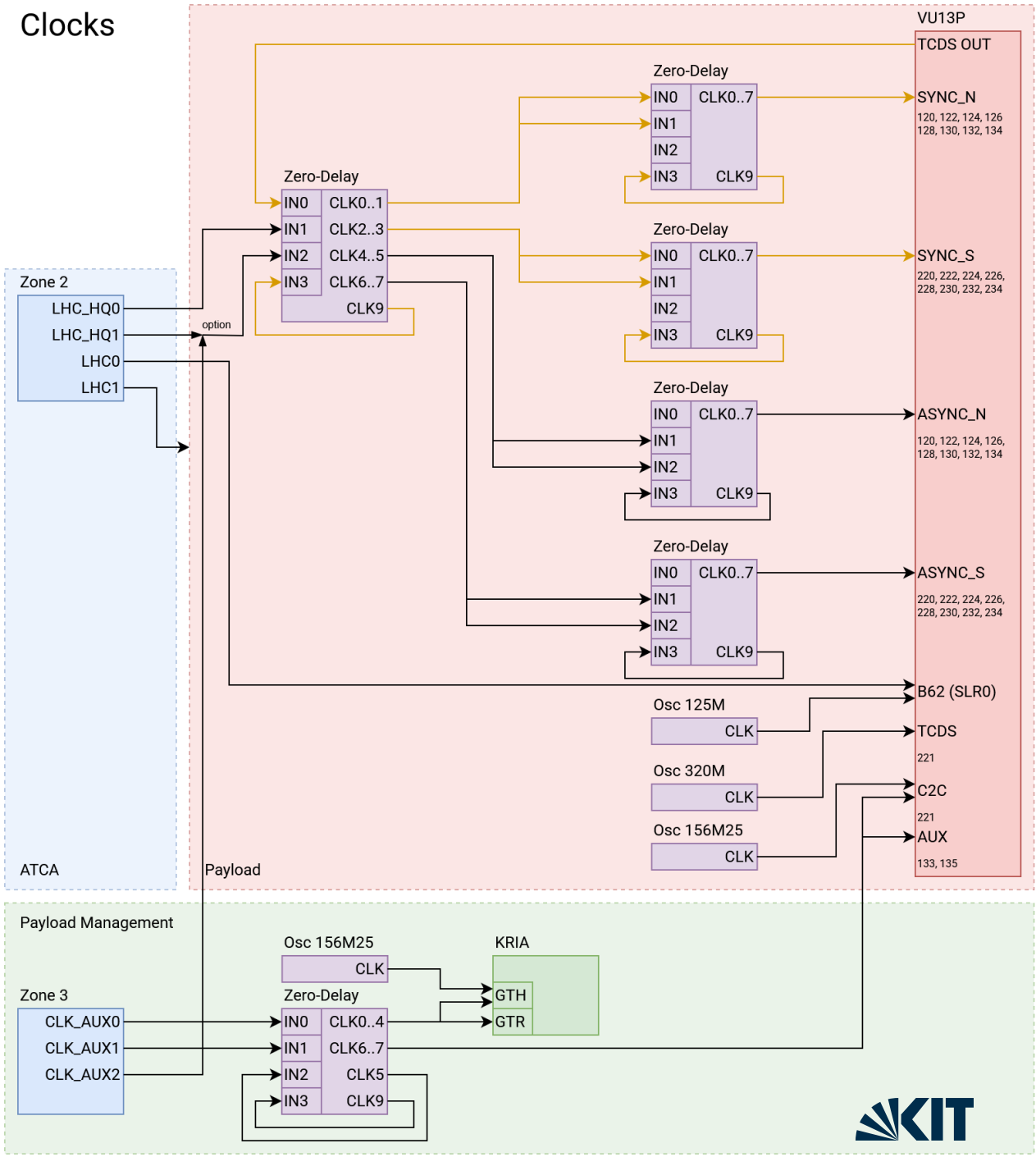
Power Architecture

- Common quarter-brick power modules are used for backplane power
  - OmniOn PIM400KZ
  - OmniOn QBDW033A0B41-HZ (Barracuda)
- Analog power modules are used for individual power supplies
  - 2x LTM4700 for FPGA VCCINT
  - 2x LTM4680 for FPGA MGTs
  - 1x LTM4703 for FPGA VCCO
  - 3x LTM4676A for FireFly supplies and clocks
  - 1x LTM4644 for Kria SoM voltages
- The 16 payload power supplies are supervised by a MAX34451 power supervisor IC
  - This also performs power sequencing of FPGA and FireFly supplies



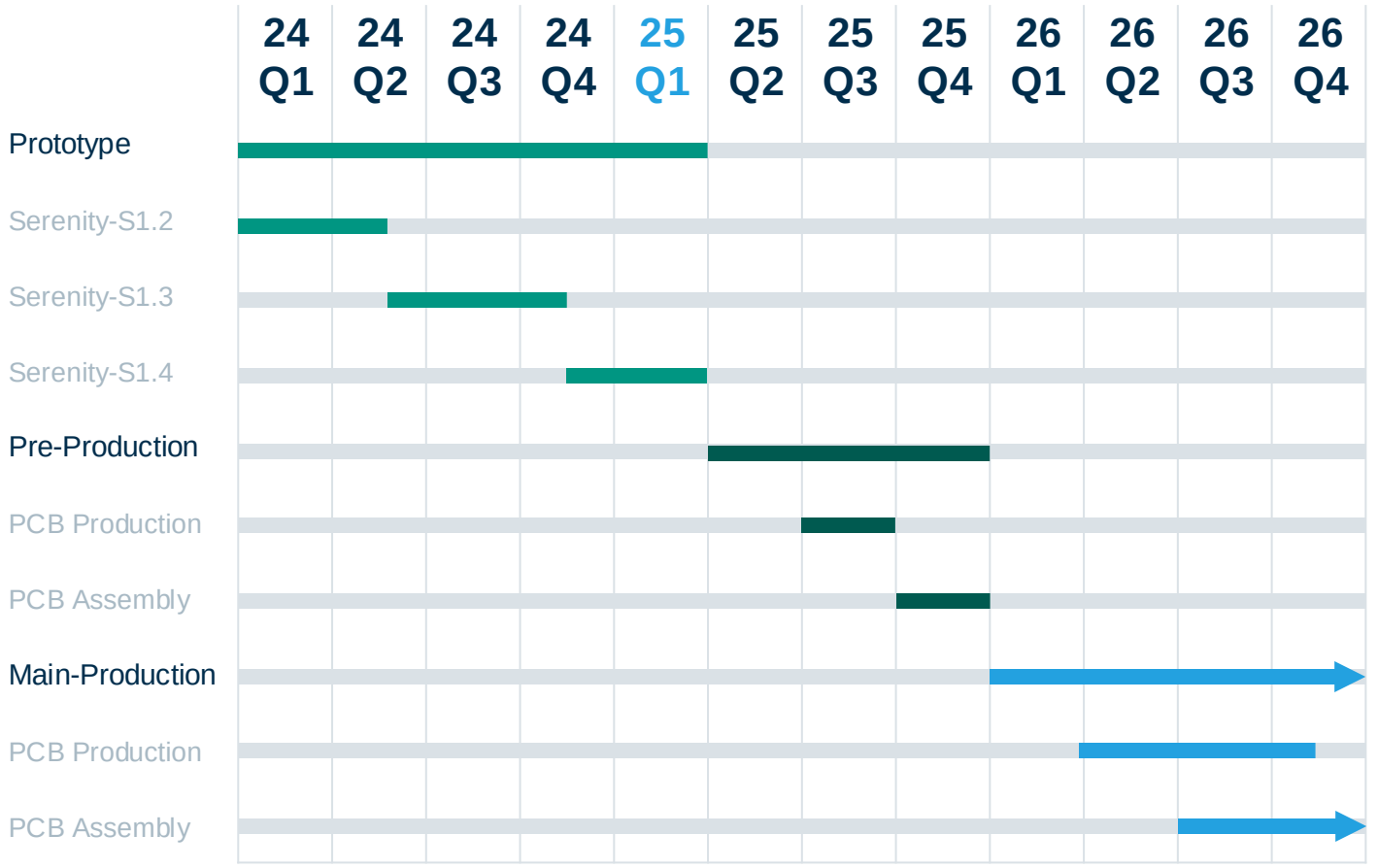
Clock Architecture

- The Serenity-S1 is using
  - ZL30274 as zero-delay buffers
  - LMK61E2 as local oscillators
- Clock sources can be
  - LHC clocks from Zone 2 (320 MHz)
  - An auxiliary clock from Zone 3
  - A clock output by the FPGA
- Any quad has access to at least 2 independent clocks
  - All clocks feature deterministic delays

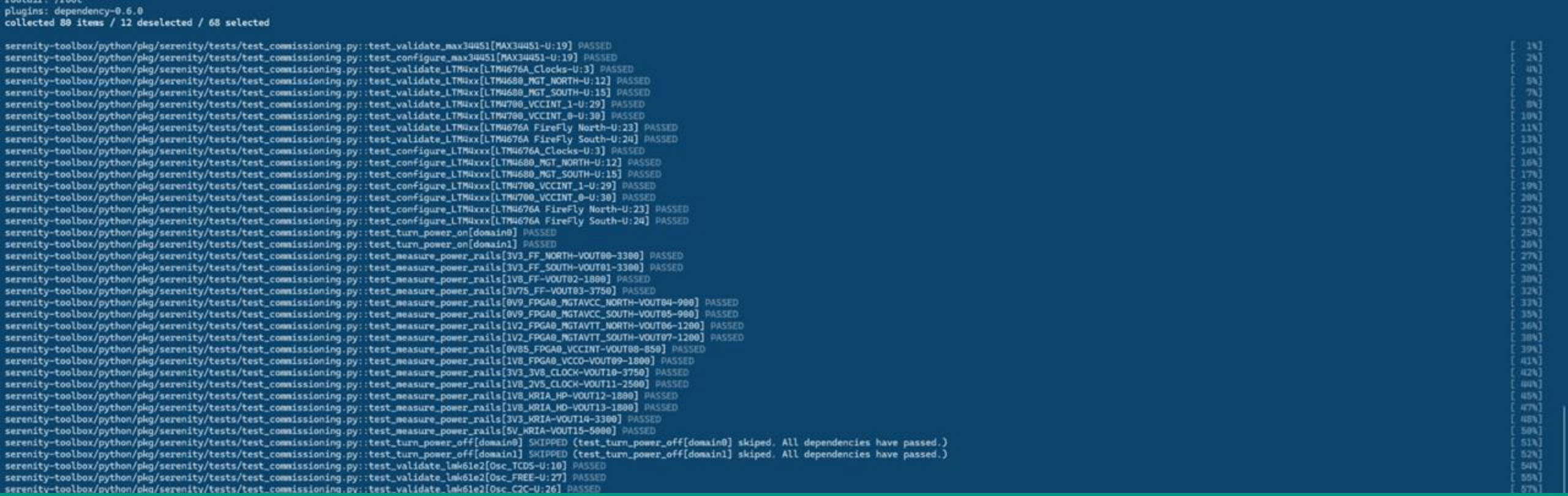


Project Timeline

- 22 cards already built (+20 ordered)
- Tender for production of 700+ cards for CMS
  - Pre-series is still planned for 2025
  - Main series in 2026
  - Commissioning in CMS in 2027-2029
- Usage in TRISTAN experiment at KIT
- Envisioned for High-D-Calo (FCC) demonstrator



Timeline for CMS production



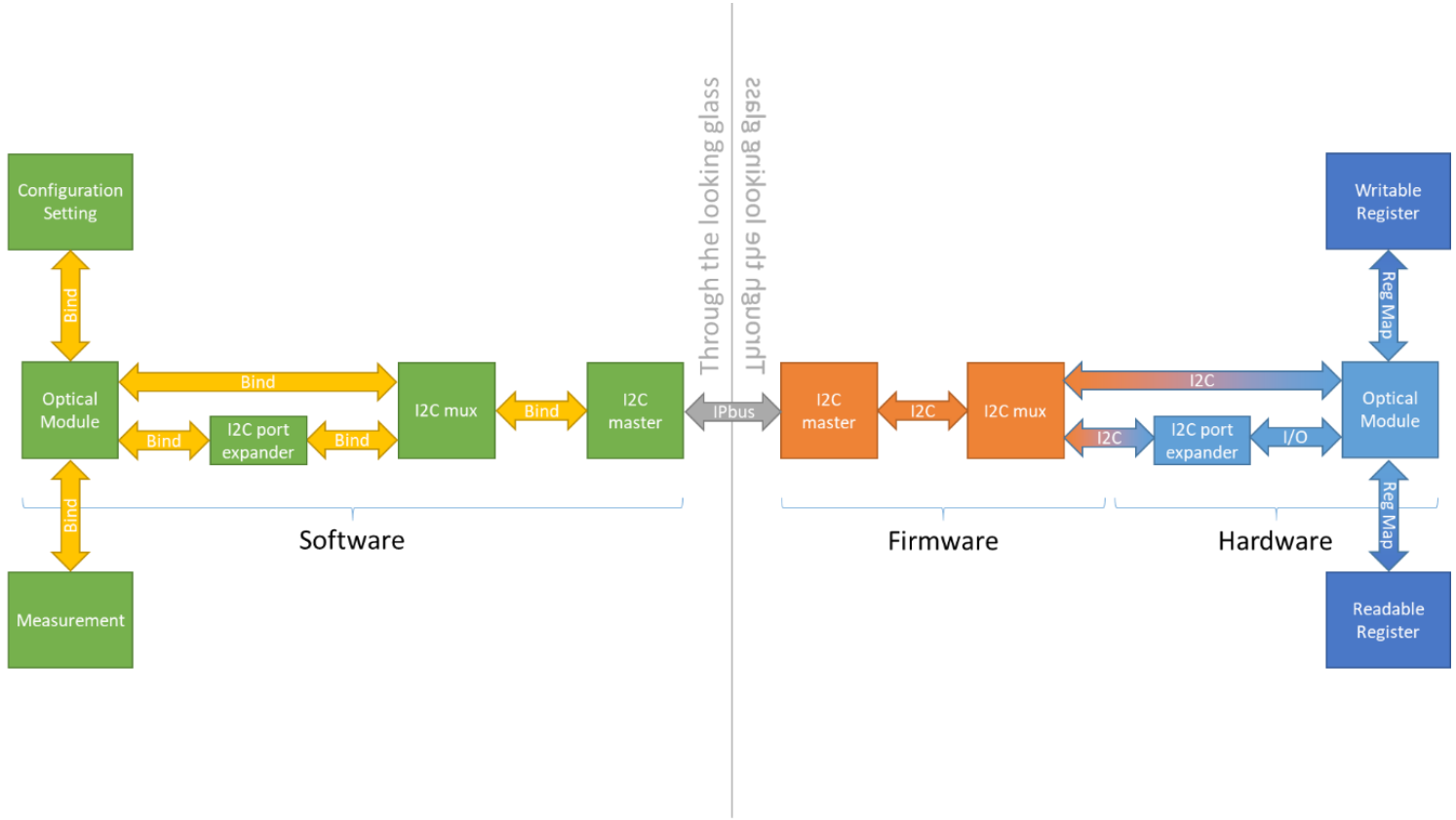
Software and Firmware

Section
02

SMASH

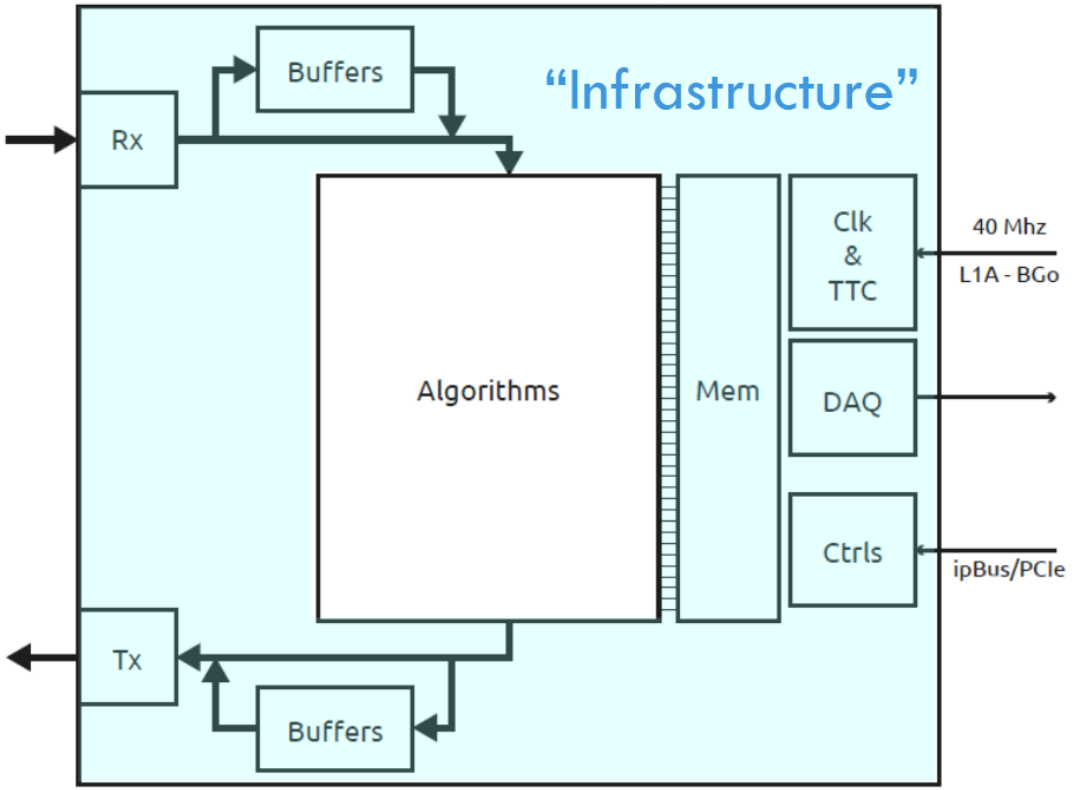
Serenity MAnagement SHell (SMASH)

- Software providing hardware abstraction for slow control
  - Comparable to Linux device tree
  - IPBus based
- Different usage options
  - Interactive shell (see below)
  - SMASH scripts
  - (Limited) Python interface




```
[root@mgmt-kki ~]# smash.exe -i
 #######  Welcome to the interactive SMASH shell.          #######
 #######  Write SMASH commands and hit <enter> to run commands  #######
 #######  Hit the 'esc' key to quit                        #######
>> Power:Sequencer Measure VOUT00
Power:Sequencer Measure VOUT00
 VOUT00 : +968.000mV
>>
```

EMP framework



Extensible, Modular data Processor (EMP)

- Framework providing hardware abstraction for the FPGA
  - Algorithm can use provided buffers for high speed access
  - Control through IPBus registers (over AXI Chip2Chip)
- EMPbutler software can access the EMP framework

Example to reset FPGA and play and receive data:

```
$ empbutler –c CONNECTIONS.xml do DEVICE_ID reset internal

$ empbutler -c CONNECTIONS_FILE.xml do DEVICE_ID buffers tx PlayOnce -c CHANNEL_LIST --inject generate://pattern

$ empbutler -c CONNECTIONS_FILE.xml do BOARD_ID buffers tx Capture -c TX_CHANNEL_LIST
$ empbutler -c CONNECTIONS_FILE.xml do BOARD_ID capture --rx RX_CHANNEL_LIST --tx TX
```

Serenity Toolbox

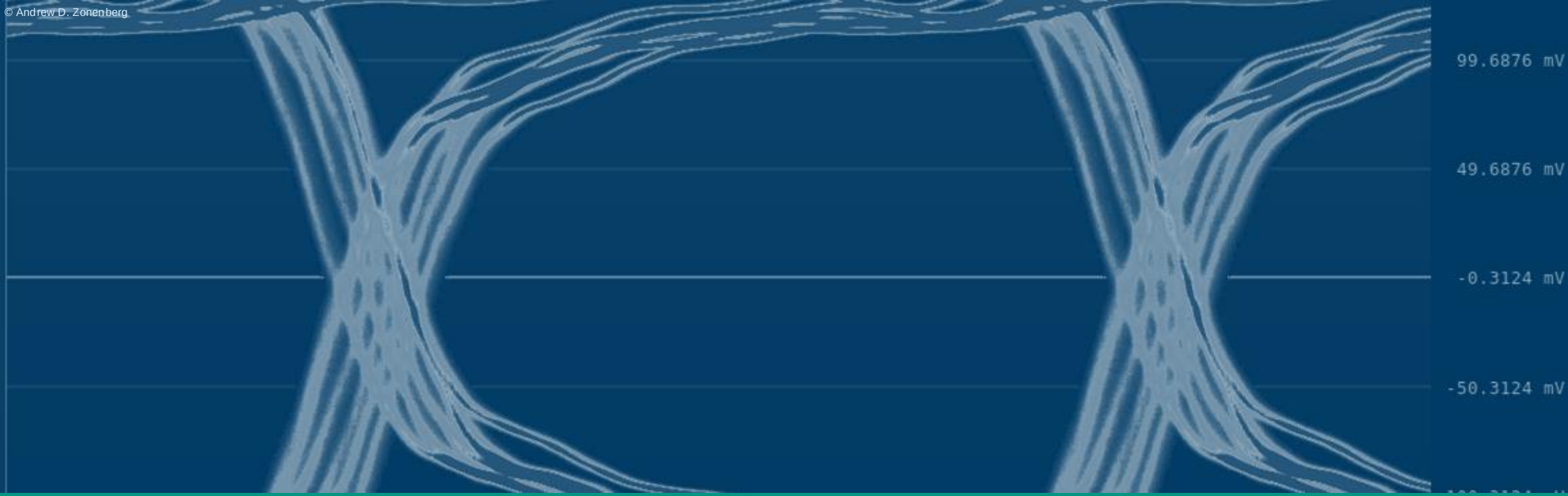
The Serenity toolbox is a wrapper for SMASH and EMPbutler

- More abstraction for end users
- Provides serenitybutler script
- Provides test suite (see Hendrik's talk)

Other even higher-level wrappers are being worked on

- HERD: common on-board application
- Shep: off-board supervisor

```
[root@mgmt-kki ~]# serenitybutler info

Using SMASH config: /etc/serenity/board.smash

Board type: S1.3

Software versions
  uHAL:       2.8.16
  EMP:        0.9.4
  SMASH:      not installed
  Serenity:   not installed
  XDMA driver: not installed

Zynq
  Firmware built from commit 3ebe425 (main) by CI job 44537806
  Filesystem built from commit 7543bda + local changes by CI job
    46068584
  Kernel built from commit 7543bda + local changes by CI job
    6068583

FPGA
  Power: Disabled

Temperatures
  Power modules: 24.4 - 25.8C
  FPGA:         Powered off
```



Test Results

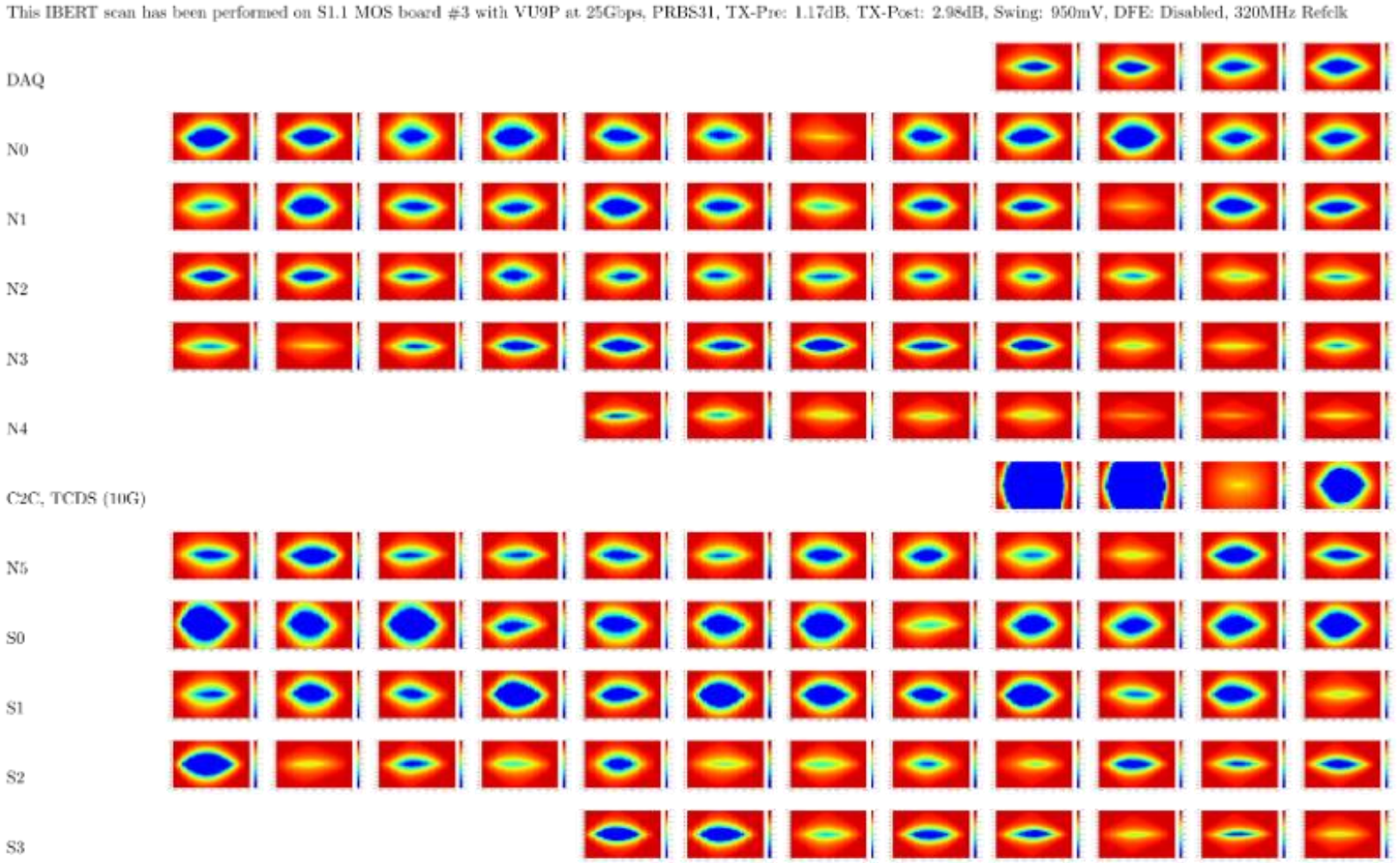
Section
03

IBERT – S1.1

Integrated Bit Error Rate Tests (IBERT) was showing bad results for first revision

Possible causes:

- Layout
  - Stubs on vias
  - Suboptimal shielding
- Socketed FPGA
  - Bad electrical connections
- Clocks
  - Noisy clocks (high jitter)
  - Wrong frequencies
- Power supplies
  - FPGA MGT power supplies
  - FireFly power supplies



IBERT – Debugging

Integrated Bit Error Rate Tests (IBERT) was showing bad results for first revision

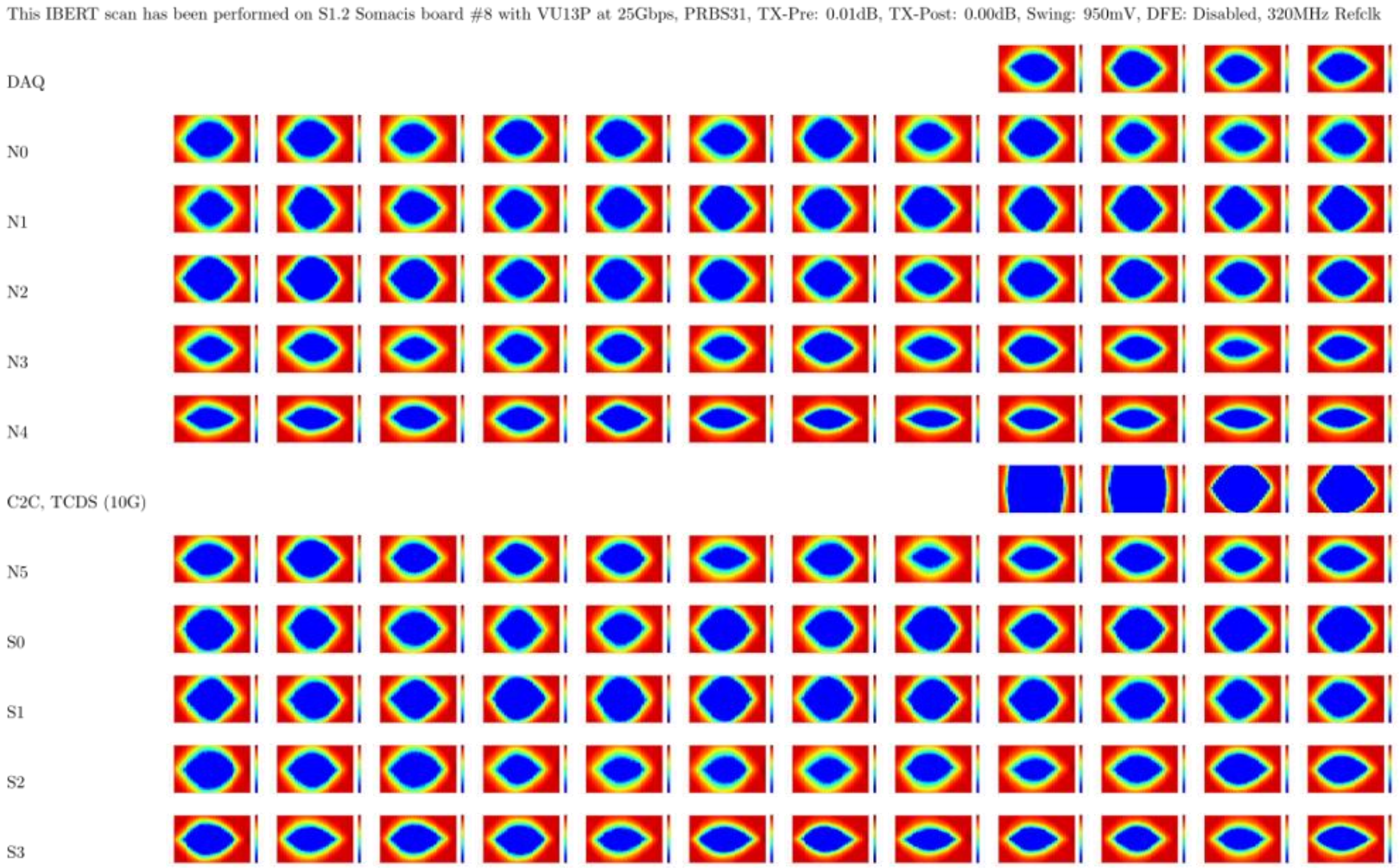
Possible causes:

- Layout
  - Stubs on vias — Stubs are avoided using microvias and backdrills.
  - Suboptimal shielding — Dedicated routing layers are shielded between 2 ground planes.
- Socketed FPGA
  - Bad electrical connections — Tests with socket on Serenity-A2577 were successful.
- Clocks
  - Noisy clocks (high jitter) — Measured low jitter on dedicated test board (with same layout).
  - Wrong frequencies — Transceiver QPLL locks successfully.
- Power supplies
  - FPGA MGT power supplies — Replaced with very low ripple supply (LTM4680, 10mVp-p).
  - FireFly power supplies — Not used for copper loopback.

IBERT – S1.2

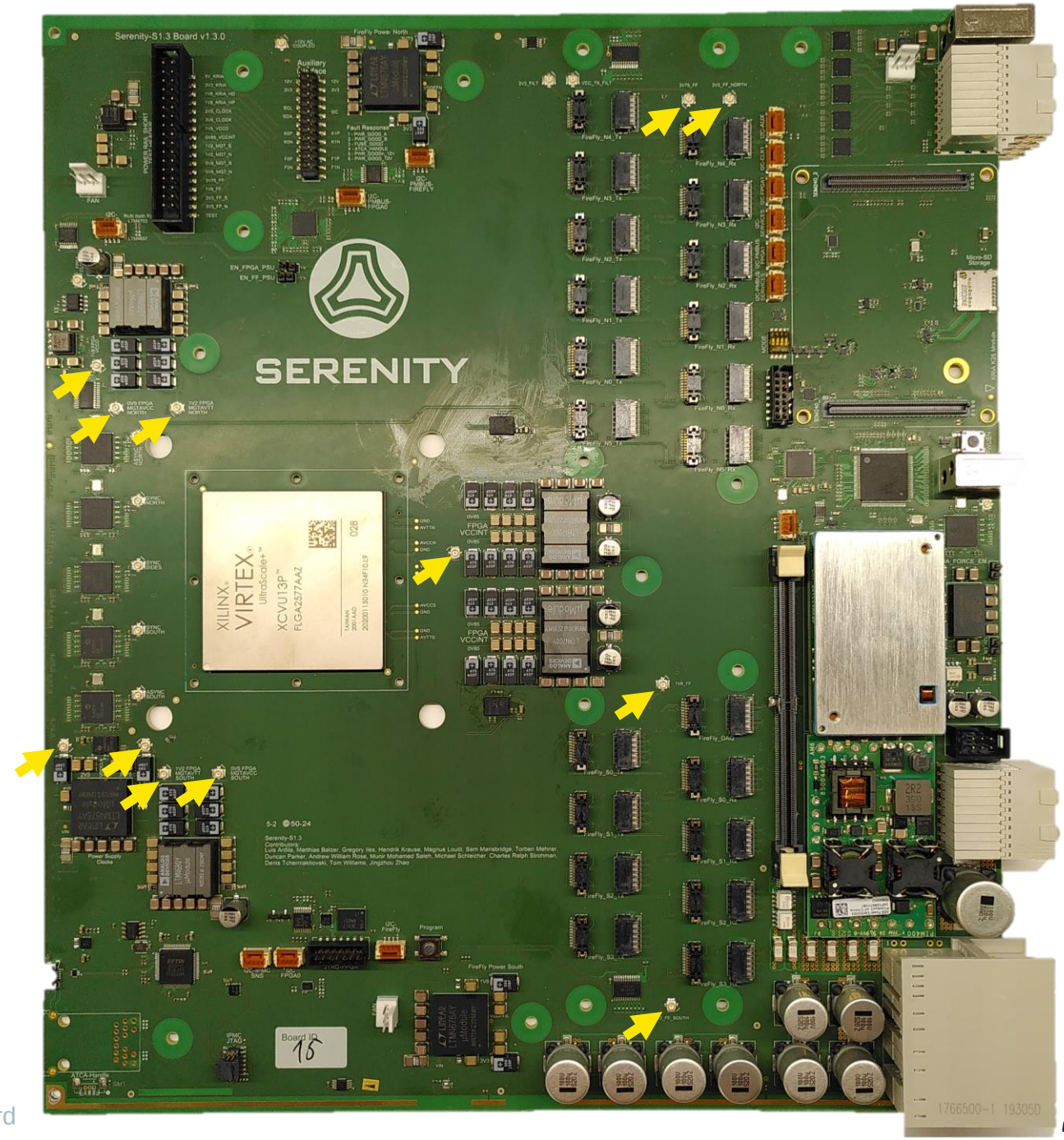
Integrated Bit Error Rate Tests (IBERT) was showing very good results from second revision

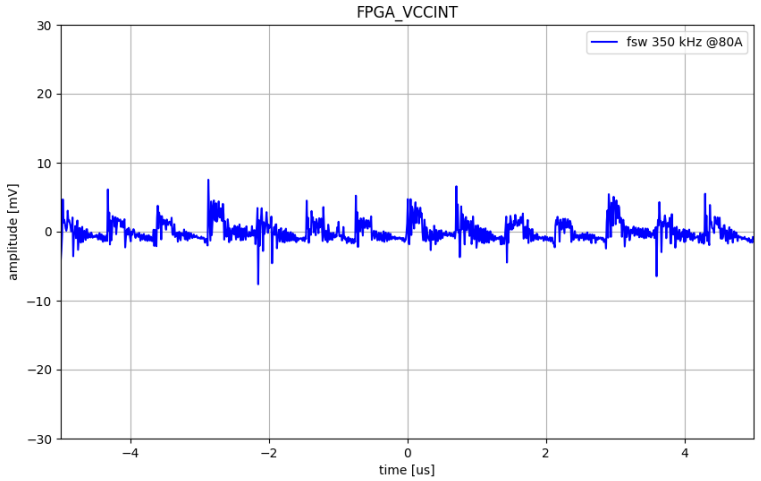
- All eyes are open.
  - No equalization is used.
- Long-term tests (14 h) show no error.
  - BER is better than 1E-15 (target for CMS: 1E-12).

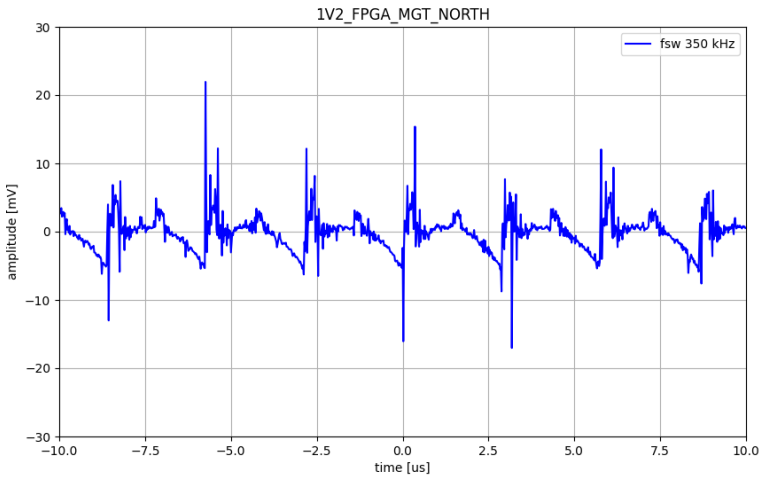


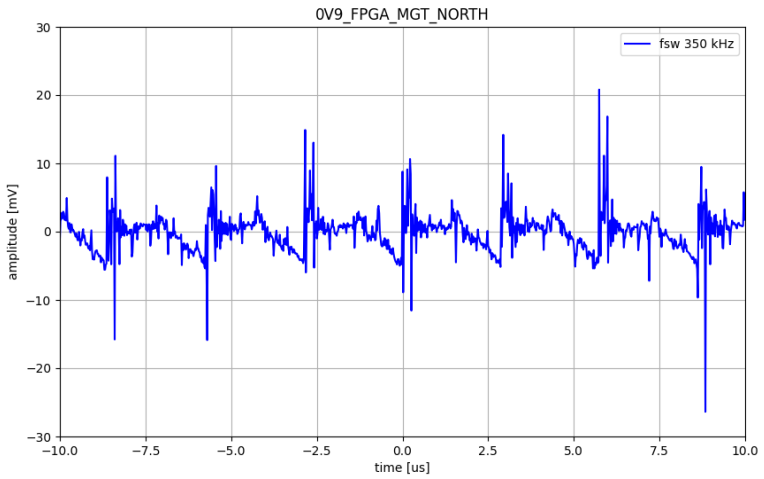
Power Supply Tests

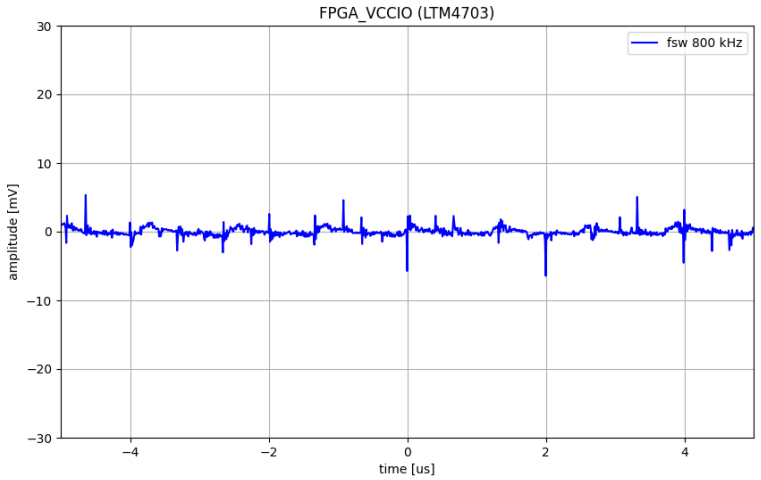
- u.FL connectors on each supply
- Noise tests were performed in steady state with high load
  - IBERT at 25Gbps for MGTs
  - Oscillation heater for VCCINT
  - Full set of 16G FireFly modules
- Step response tests were performed from off state to high load and vice versa

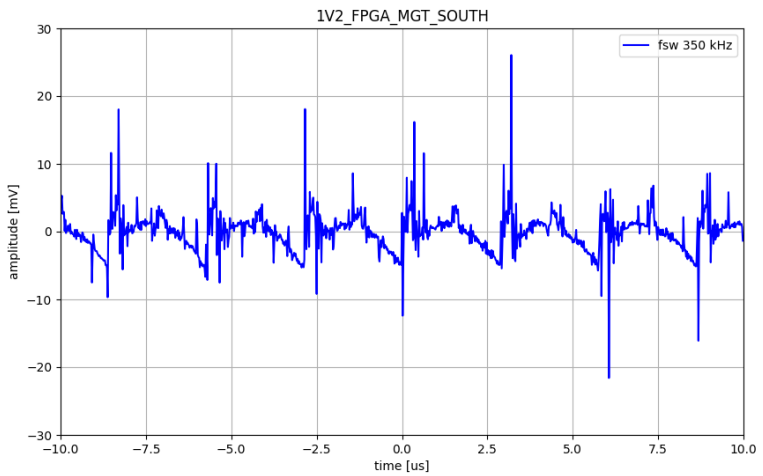


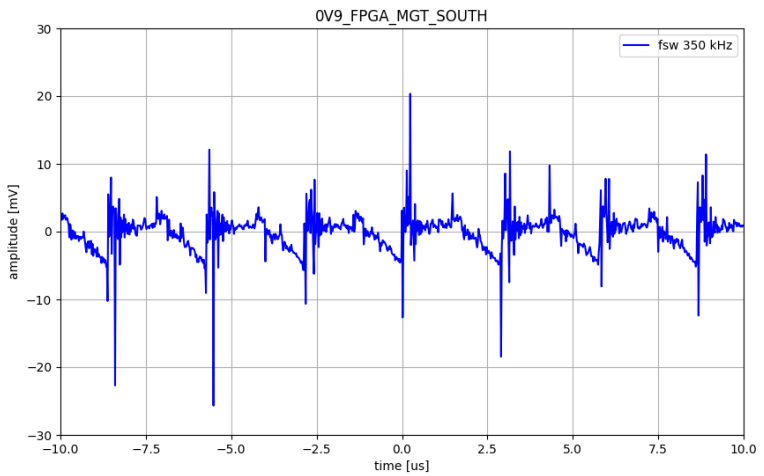






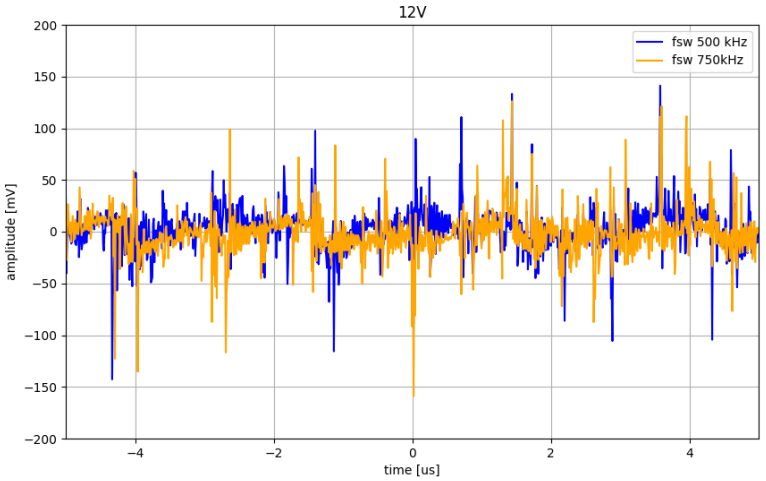


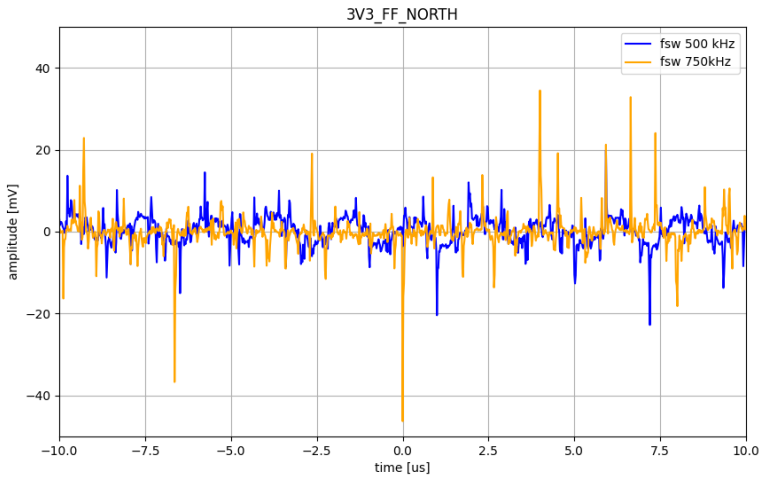


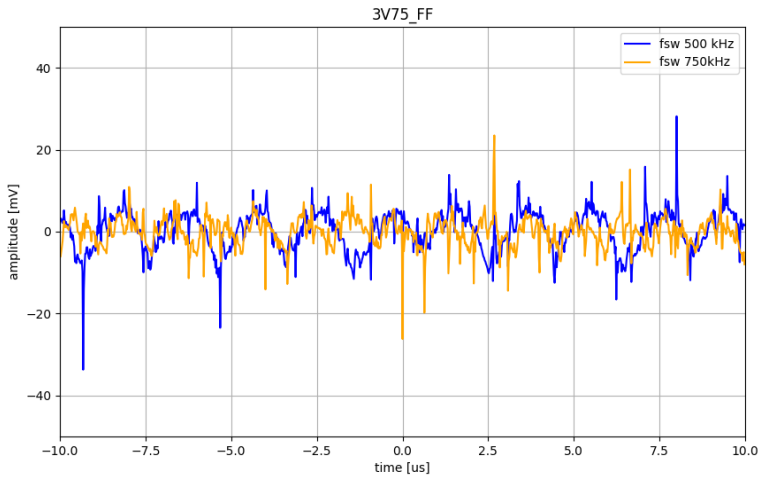


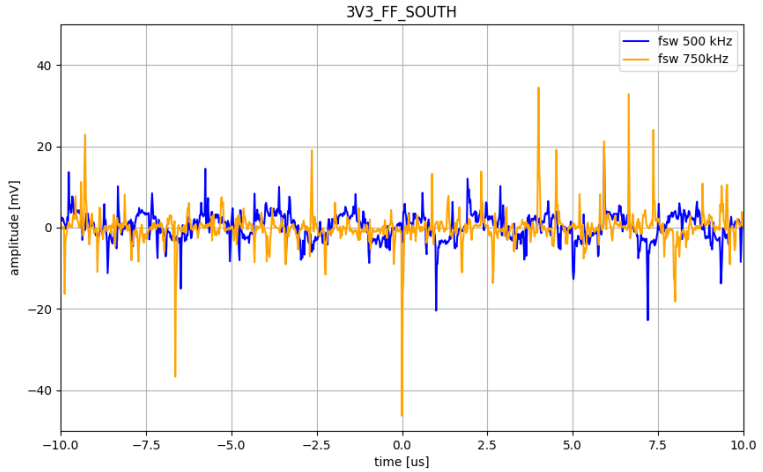
Power Supply Noise Tests
FPGA

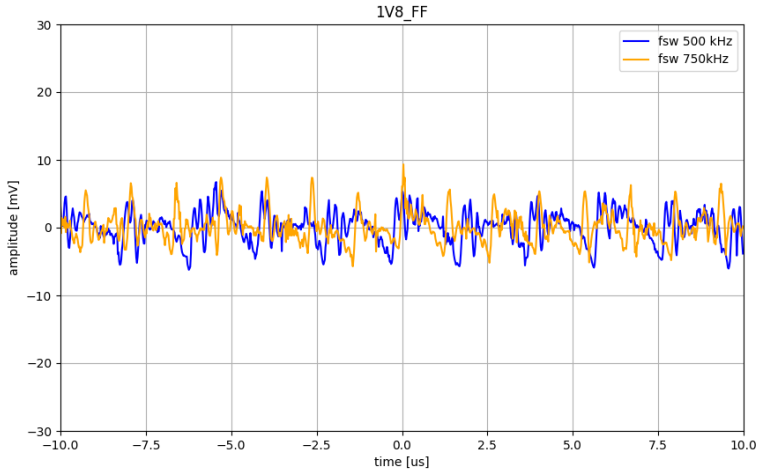
FPGA noise tests show good noise performance with only a few spikes exceeding 10mV envelope.





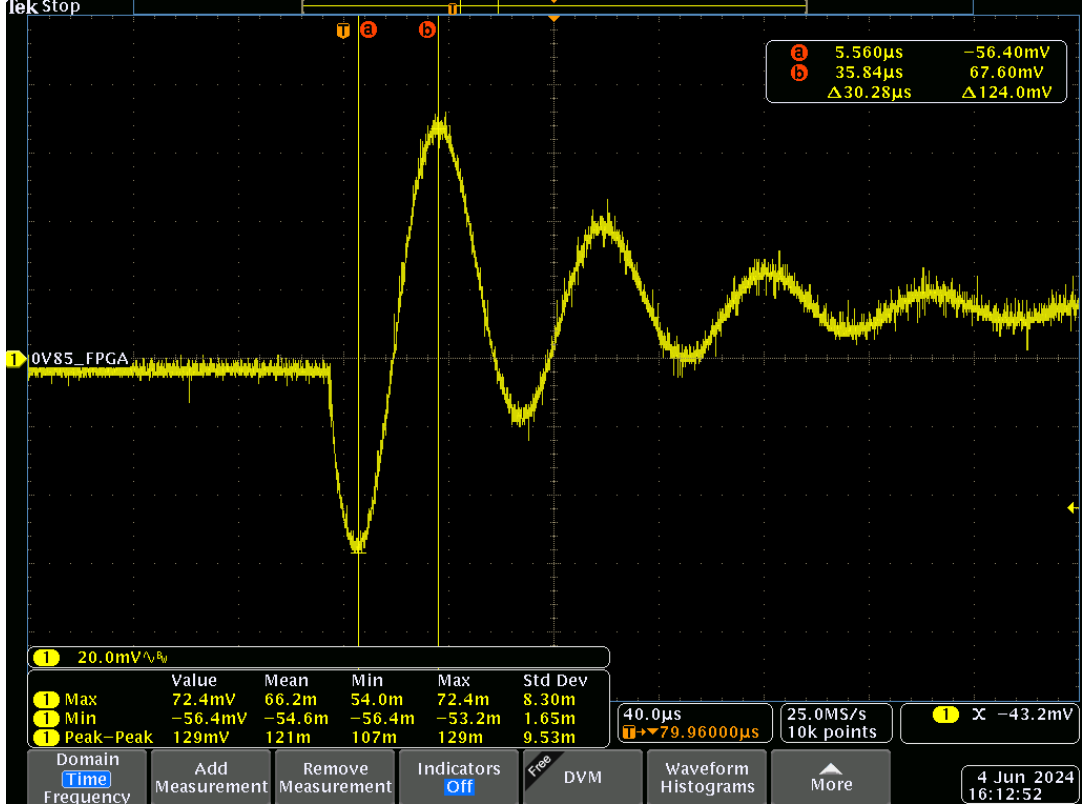


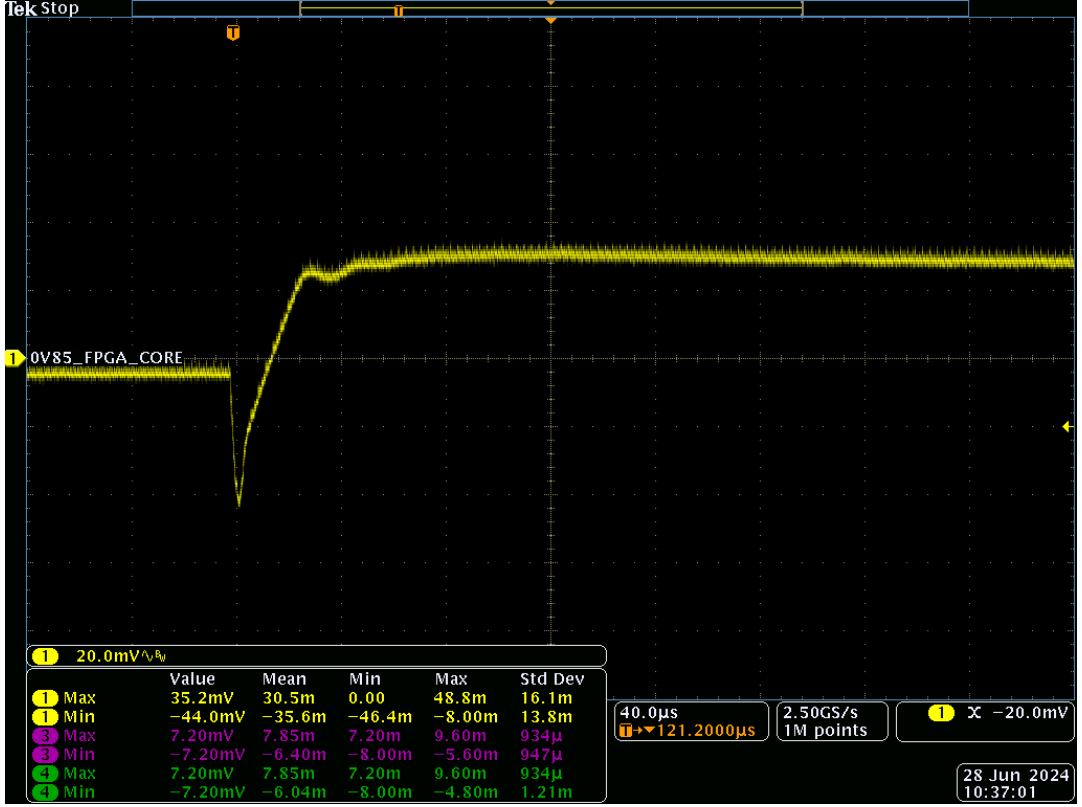




Power Supply Noise Tests
FireFlys

FireFly power supply noise at 500 kHz is lower than at recommended 750 kHz.





Power Supply Tests
Step Response

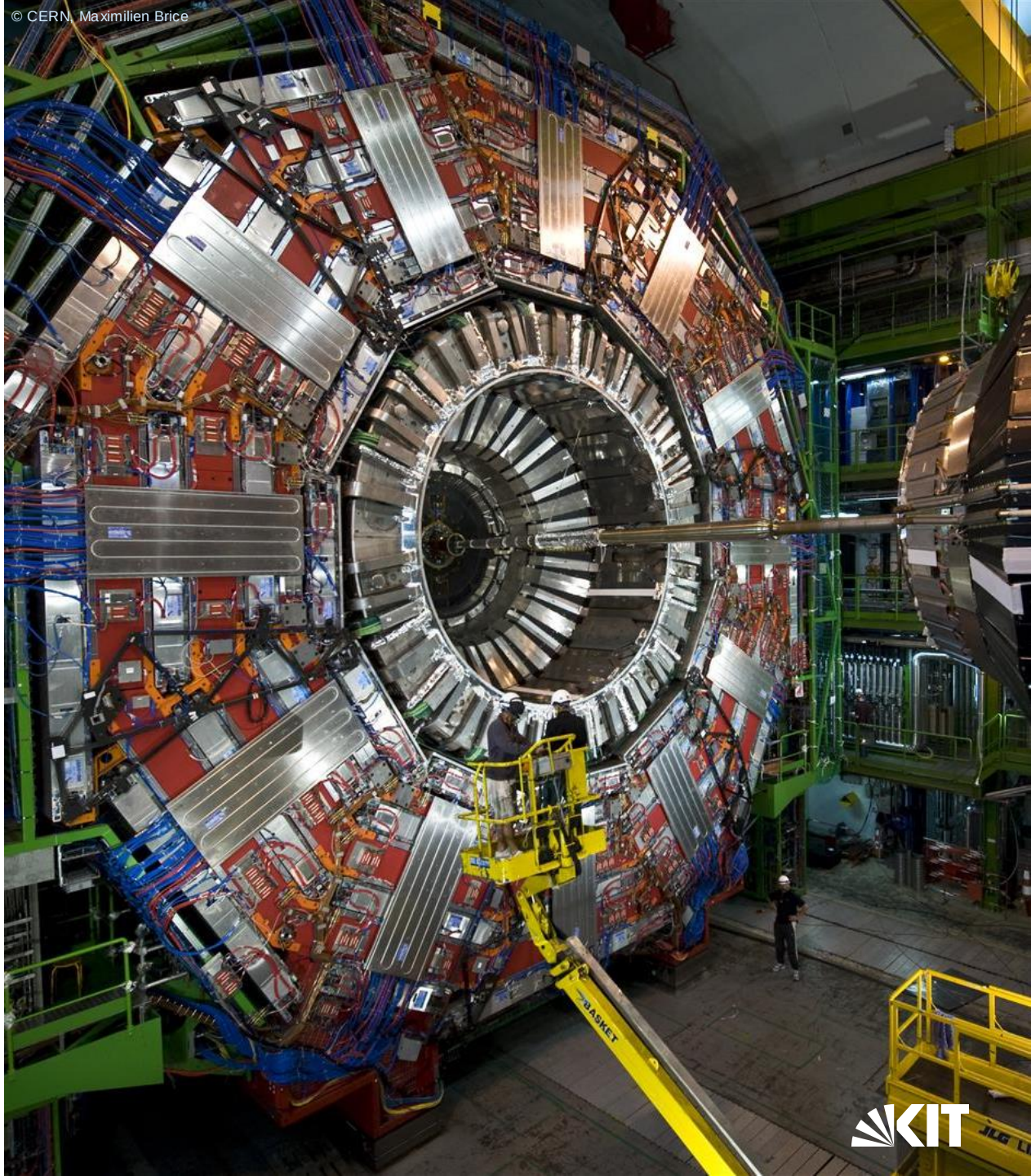
- Power supplies have been adapted to load.
  - Adapt the internal Rth for each LTM power supply.
  - Use Rth from LTPowerCAD as starting point.
- Load jumps from 10 A to 100 A were performed.
  - Undershoot from 56.4 mV to 44.0 mV
  - Overshoot from 72.4 mV to 35.2 mV

Use Cases

Section
04

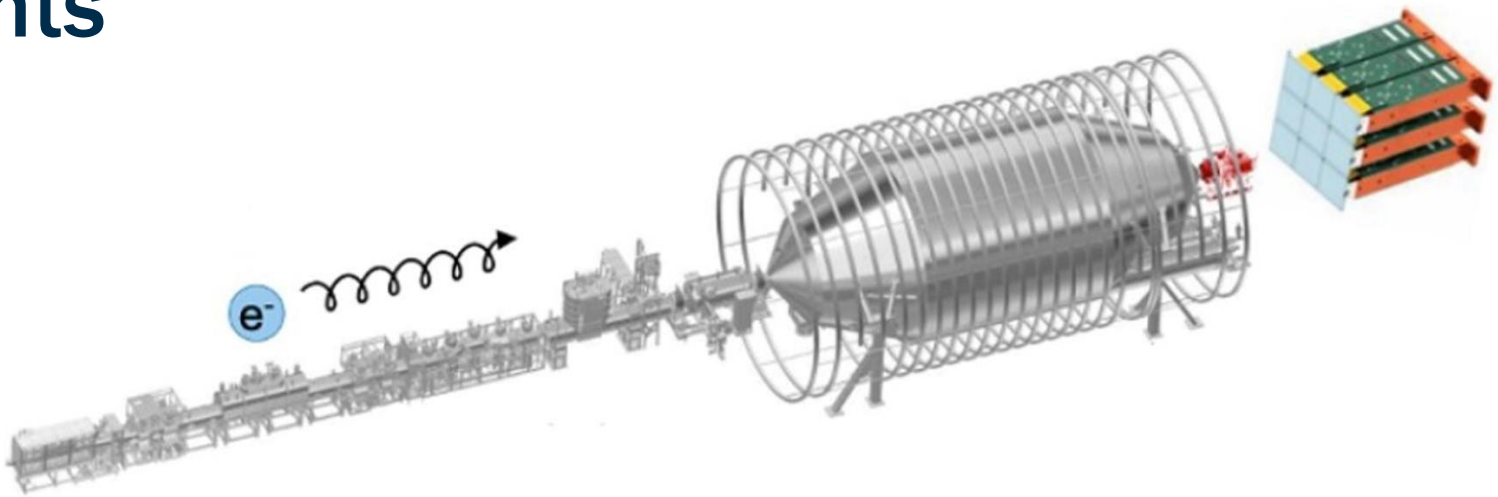
Large Scale Experiments

- CMS
  - Serenity-S1 was developed for CMS L1 Tracker.
  - Multiple subdetectors are using the Serenity-S1.
  - 725 cards are placed in a cavern 100m underground.
- Large, inaccessible deployment demands for:
  - Remote updating (M.Fuchs et. al. – Split Boot)
  - Remote access (through telnet to IPMC, ssh to Kria)
  - Remote debugging (SMASH, EMP)

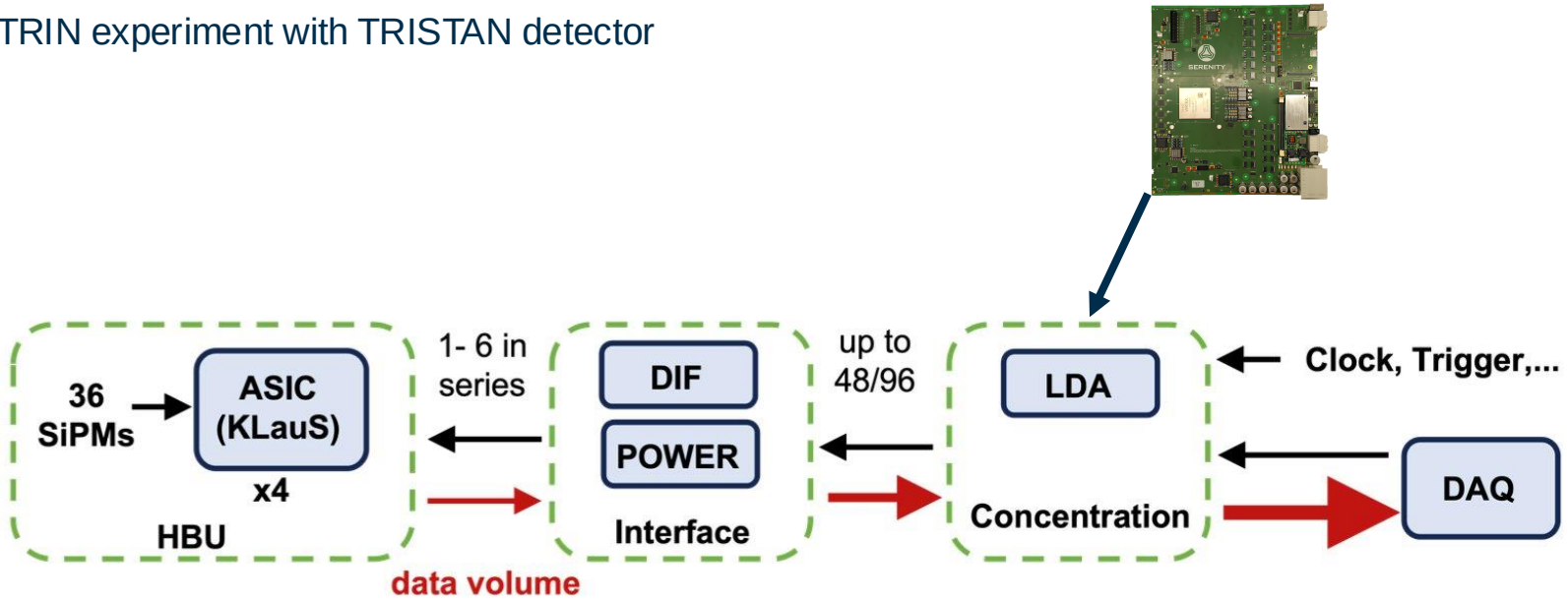


Small Scale Experiments

- TRISTAN
  - Upgrade for KATRIN
  - 3 Serenity-S1 planned
  - Single rack, easily accessible
- High-D-Calo
  - Demonstrator for future detector calorimeters
  - Serenity-S1 is a candidate for the link data aggregator (LDA)
- Small experiments require
  - Local board management
  - Quasi off-the-shelf solution



KATRIN experiment with TRISTAN detector



Current idea of High-D-Calo demonstrator

Sources

Manuals

- Serenity (old version) - serenity.web.cern.ch
- IPBus (git-firmware, git-software)
- SMASH
- EMP Framework
- Serenitybutler
- HERD
- Shep

Papers, Design Reports

- CMS-TDR-014 The Phase-2 Upgrade of the CMS Tracker
- Lessons learned while developing the Serenity-S1 ATCA card
- Split Boot – True Network-Based Booting on Heterogenous MPSoCs
- ZynqMP-based board management mezzanines for Serenity ATCA-blades
- System design and prototyping of the CMS Level-1 Trigger at the High-Luminosity LHC
- Conceptual Design Report: KATRIN with TRISTAN modules

Main contributors from the Serenity consortium: KIT, Imperial College London, STFC Rutherford Appleton Labs, IHEP Peking

Serenitybutler examples

```
[root@mgmt-kki ~]# serenitybutler power status
Using SMASH config: /etc/serenity/board.smash

Power status:
 FPGA : Disabled
 FireFlys : Disabled

LTM measurements:
                 Input          Output 1      Nominal     Output 2      Nominal    Frequency   Temperature
 ================================================================================================================
 Power:Clocks       +0.061A @ +12.000V  -0.002A @ +0.041V  +3.750V  +0.003A @ +0.042V  +2.500V  +750.000kHz      32.4C
 Power:FPGA:MgtNorth  +0.005A @ +12.031V  -0.004A @ +0.001V  +0.900V  +0.001A @ +0.041V  +1.200V  +350.000kHz      31.4C
 Power:FPGA:MgtSouth  +0.003A @ +12.016V  -0.035A @ +0.009V  +0.900V  -0.038A @ +0.240V  +1.200V  +350.000kHz      31.2C
 Power:FPGA:VCCINT0   +0.005A @ +12.016V  +0.284A @ +0.000V  +0.850V  +0.322A @ +0.000V  +0.850V  +350.000kHz      30.7C
 Power:FPGA:VCCINT1   +0.007A @ +12.016V  +0.313A @ +0.000V  +0.850V  +0.270A @ +0.000V  +0.850V  +350.000kHz      29.8C
 Power:FireFly:North  +0.061A @ +12.000V  -0.006A @ +0.966V  +3.300V  +0.004A @ +0.039V  +3.750V  +500.000kHz      32.4C
 Power:FireFly:South  +0.061A @ +11.984V  +0.000A @ +0.987V  +3.300V  -0.005A @ +0.093V  +1.800V  +500.000kHz      32.3C
 U:12             +0.007A @ +12.031V  -0.010A @ +0.001V  +0.900V  +0.020A @ +0.041V  +1.200V  +350.000kHz      31.4C
 U:15             +0.006A @ +12.016V  +0.008A @ +0.009V  +0.900V  +0.008A @ +0.240V  +1.200V  +350.000kHz      31.2C
 U:23             +0.061A @ +12.000V  -0.007A @ +0.966V  +3.300V  -0.001A @ +0.039V  +3.750V  +500.000kHz      32.4C
 U:24             +0.061A @ +11.984V  -0.002A @ +0.988V  +3.300V  +0.001A @ +0.093V  +1.800V  +500.000kHz      32.2C
 U:29             +0.005A @ +12.016V  +0.265A @ +0.000V  +0.850V  +0.293A @ +0.000V  +0.850V  +350.000kHz      29.7C
 U:3             +0.061A @ +12.000V  -0.003A @ +0.041V  +3.750V  +0.001A @ +0.042V  +2.500V  +750.000kHz      32.3C
 U:30             +0.004A @ +12.016V  +0.288A @ +0.000V  +0.850V  +0.245A @ +0.000V  +0.850V  +350.000kHz      30.8C
```