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Factory Acceptance Test for the Serenity-S1

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In the context of the CMS phase-2 upgrade, we have contributed in the Serenity collaboration to develop Serenity-S1, a versatile FPGA processing card based on Advanced Telecommunications Computing Architecture (ATCA) technology. The board has been well received and is used by many sub-detector systems for the backend data processing. This leads to the planned production of 721 Serenity-S1 boards over the next two years.

For this, an efficient and reliable Factory Acceptance Test (FAT) process is required that reduces the commissioning time that has initially taken us weeks and requires detailed expert knowledge. The goal is to commission the boards in as little as 10 minutes to allow the assembly company to perform it as an end-of-line test after the assembly. To achieve this, we minimize manual intervention, limiting it to the beginning and end of the process while maximizing automated testing coverage.

Our approach leverages Python APIs from our main board management software tools (SMASH and EMP), integrating them into Pytest environments to structure comprehensive test runs. A Jupyter notebook provides a graphical user interface (GUI), acting as a central control point for the test stand and equipment by providing an intuitive way to monitor and control the testing process.

The FAT implementation for Serenity-S1 demonstrates how automation significantly accelerates testing while maintaining quality standards. Initial results from the extended pilot production indicate a substantial reduction in commissioning time, paving the way for scalable, efficient production.

This talk will detail the implementation of the FAT for the Serenity-S1 and present the results achieved thus far.

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